**HiWire Consortium Active Electrical Cable (AEC) Specification**

**Revision 1.0**

**Nov 15, 2021**

HiWire™ Consortium

OPEN Compute Project

Abstract: This specification defines: the specific mechanical, electrical and software details inside of the existing IEEE and MSA standards that are to be used for HiWire Consortium compliance Active Electrical Cables (AECs). This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

Website : www.hiwire.org



**Notes**:

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The following were Promoter member companies of the HiWire Consortium.

| | |
|---|---|
| Credo | Broadcom |

The following were contributing participant companies of the HiWire Consortium

| | | |
|---|---|---|
| 10Gtek | Accton | Alpha Networks |
| Amphenol | Arrcus | BizLink |
| Broadex | Cameo | Canaan |
| Celestica | Centec | Chelsio Communications |
| Dell EMC | Delta | DriveNets |
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| Inventec | Juniper | Keysight |
| Kingsignal | Microsoft | Multilane |
| QCT | Senao | Spirent |
| Steligent | T&S Communications | Tencent |
| ufiSpace | UL | Volex |
| Wistron | Xena Networks | |

*Change History:*

| Revision | Date | Changes |
|---|---|---|
| 0.1 | July 27, 2020 | First Draft |
| 0.2 | April 21, 2021 | 2nd Draft with minor updates and cleanup throughout |
| 0.3 | N/A | |

| | | |
|---|---|---|
| 0.4 | Sept 14, 2021 | Incorporate all comments from comment period (July-Aug, 2021), release candidate for v1.0 |
| 1.0 | Nov 15, 2021 | Ratified version from HiWire BoD |
| 1.0_OCP | Mar 27, 2022 | Adjust license for OCP submission, HiWire Consortium and OCP Logos to cover page, added Appendix A and B, add foreward with Compliance with OCP tenants |

*Foreword*

The development work on this specification was done by the HiWire Consortium, an industry group. The membership of this group since its formation in Oct, 2019 has included a mix of companies which are leaders across the industry.

**Compliance with OCP Tenants**

**Openness**

By migrating the HiWire Consortium Specification v1.0 to the Open Compute foundation it becomes open to all to review and implement. In addition the broad membership of the OCP is able to contribute to the future development of the specification.

**Efficiency**

The purpose of the HiWire Specification to drive commonality in implementations of Active Electrical Cables (AECs) in order to reduce friction in adoption users. This directly reduces opex in the form of qualifications and software work to adapt to different AEC implementations.

**Impact**

AECs have proven an essential component of hyperscale and service provider networks in order to enable high speed, low cost, low power and highly reliable networks. Multiple companies have announced AEC products to the market; migrating this specification to OCP drives commonality in these implementations and a broader membership base to widen impact.

**Scale**

As speeds increase, beyond 28Gb/lane NRZ, the ability to use passive copper cables is challenged by copper loss, thickness and vendor interoperability. The 650 group estimates that 75% of NIC-TOR connections will be made with Active Electrical cables (AECs) by 2026; already multiple hyperscalers have deployed, or are planning to deploy AECs in both NIC to TOR and Distributed, Disaggregated Chassis (DDC) applications.

# Contents

# Introduction

Standards in the Ethernet market are developed and shared by multiple organizations including the IEEE 802.3 committees and the many multi-source agreements (MSAs) established between vendors to specific connectors and software standards. These standards define the underlying electrical and mechanical specifications, but contain many options that enable significantly different implementations of the same functions. While this may be beneficial at an early stage of an industry, it burdens the user of the cable with adapting to, testing and qualifying many different implementations of the same functionality. This creates unnecessary friction in the Ethernet Cable market.

Active Electrical Cables (AECs) are a specific implementation of high speed Ethernet cables embedded clock and data recovery (CDR) and gearboxing functionality in the AEC to provide a more robust and flexible solution than traditional direct attach copper (DAC) or optical solutions. These AECs provide a deterministic AUI to AUI interface to the hosts and manage all of the details of the line equalization using embedded CDR technology.

The purpose of the HiWire Consortium is to define specific implementations of each AEC type based on real end user input in order to enable the following capabilities:

1. Standardize the implementation of features within the existing IEEE 802.3 and MSA definitions to minimize the amount of adaptation the cable user needs to do in order to qualify different implementations of the same AEC.
2. Push end user qualification requirements upstream by defining a test specification and certified 3rd party test lab, so that users know that a HiWire qualified AEC meets their quality requirements.
3. Implement a monitoring process to ensure that HiWire AECs are manufactured and tested to a consistent level of quality that meets tier 1 end user requirements.

# HiWire AEC Cable Architecture

A HiWire AEC cable can be thought of as five blocks combined to implement a complete end to end system as shown in Fig. 1. This example applies to the 50G generation of serdes referenced in this doc.

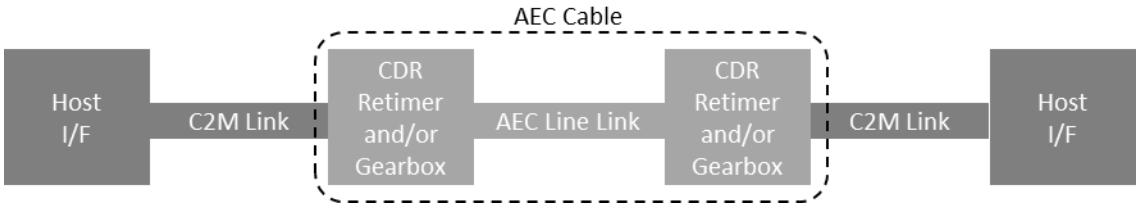


*Fig. 1 An AEC System is composed of 5 blocks: A Host on each side (Switch, NIC or other device), a chip-to-module link (max 10dB) between the Host and the AEC Paddlecard. A CDR or gearbox function in each paddle card connected via a deterministic, pre-configured Line side (unrestricted, but potentially >30dB) between the paddle cards.*

The HiWire AEC is retimed on both ends and the line link calibration is completed during production test, thus the HiWire AEC is a fully deterministic device similar to an Active Optical Cable (AOC).

HiWire AEC Cables can also implement gearboxing functions in one or both of the paddle cards to translate between different speed interfaces, initially these will enable translation between 56G PAM4 and 25G NRZ. These options are not currently available in other cable types and require L2 functionality to properly terminate and regenerate the needed forward error correction (FEC) for each link type

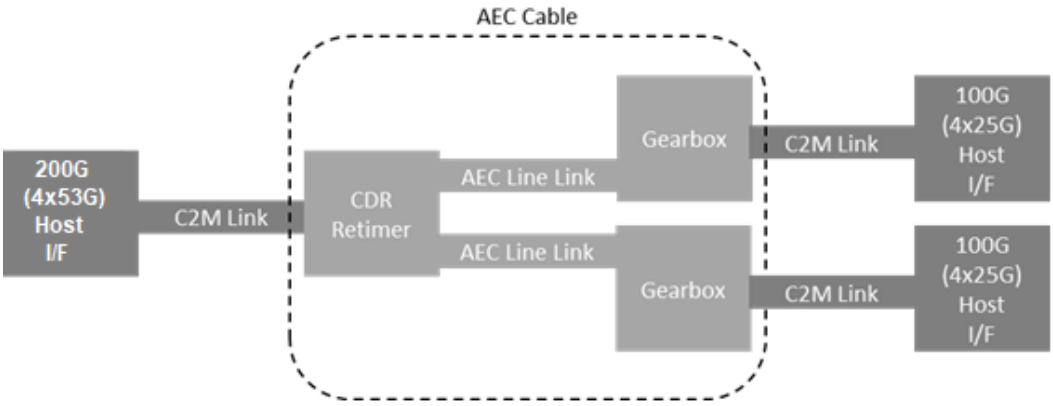


*Fig. 2 A specific 2:1 Gearbox implementation of an AEC Cable where the left Host is a 200G (4x53G) PAM4 and the right Host is each 100G (4x25G) NRZ interface. In this case, in addition gearboxing, the right side Paddlecard needs to manage forward error correction (FEC) termination and regeneration.*

In both cases the line side interface is fully self contained inside the cable system, thus the performance of the line side interface is covered by the specification but not the details of its implementation – it is most likely implemented in twin-axial copper, but this is not specified.

The HiWire AEC Specification covers the following items in explicit detail:

- C2M Interface Specifics per Cable type
    - Per cable type – which 802.3 interface(s) must be supported
    - Fixed vs. adjustable Tx/Rx parameter support
    - Forward-error correction (FEC) support
- System Level Performance Parameters
    - Maximum link time from power-on and/or reset
    - Maximum Link Latency
    - Maximum power consumption
    - Temperature and Voltage Range
    - Performance Metrics – pre-FEC and post-FEC BER requirements
- Mechanical Parameters
    - Cable shell dimensions – which version and sub-type from MSA
    - Cable diameter, bend radius and bend space
- Management Specification
    - CMIS, SFF-8636 or similar with explicit fields per cable type
- Quality and Qualification Requirements
    - Environmental Standards (RoHS, REACH, etc.)

# 400G QSFP-DD to QSFP-DD

## Description

This cable is a point to point 400G (8x56G lane, full duplex) QSFP-DD to QSFP-DD without FEC termination or gearboxing functionality.

## Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

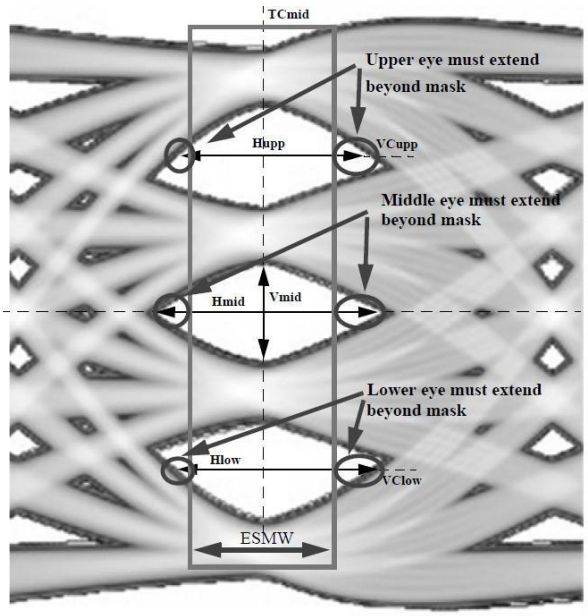


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## Performance Parameters

All QSFP-DD MSA Specifications must be met. In addition, the following items must be met which narrow the QSFP-DD MSA.

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern<br>Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with QPRBS31 pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 5W | |
| Latency | 30ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0'C – 70'C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | QSFP-DD Type 2, MSA v3.0 | |
| Cable Configuration / OD | <=3m – single conductor, <=7mm OD<br>>3m – <=7m – dual conductor, <= 6.5mm OI<br>>7m - single/dual conductor, <= 11mm | Nominal OD |
| Cable Bend Space | <=7m Max 63.5mm | Measured from end of connector to 90 degree bend in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend stress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from stated nominal length |

## Management Interface

- The device should be compliant to CMIS v4.0 protocol, see relevant MSA file for precise register set. The device must support all modes defined in this register set.

# 400G OSFP to OSFP

## Description

This cable is a point to point 400G (8x56G lane, full duplex) OSFP to OSFP without FEC termination or gearboxing functionality.

## Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

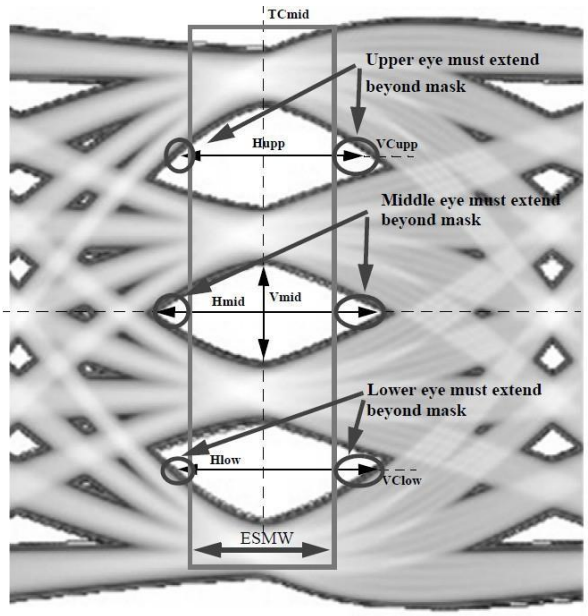


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## Performance Parameters

All OSFP Specifications must be met. In addition, the following items must be met which narrow the OSFP MSA.

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern<br>Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with PRBS31Q pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 5W | |
| Latency | 30ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0'C – 70'C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | OSFP MSA v2.0 | |
| Cable Configuration / OD | <=3m – single conductor, <=7mm OD<br>>3m – <=7m – dual conductor, <= 6.5mm OI<br>>7m - single/dual conductor, <= 11mm | Nominal OD |
| Cable Bend Space | <=7m max 63.5mm | Measured from end of connector to 90 degree bend in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend stress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from stated nominal length |

## Management Interface

- The device should be compliant to CMIS v4.0 protocol, see relevant MSA file for precise register set. The device must support all modes defined in this register set.

# 200G QSFP56 to QSFP56

## Description

This cable is a point to point 200G (4x56G lane, full duplex) QSFP56 to QSFP56 without FEC termination or gearboxing functionality.

## Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

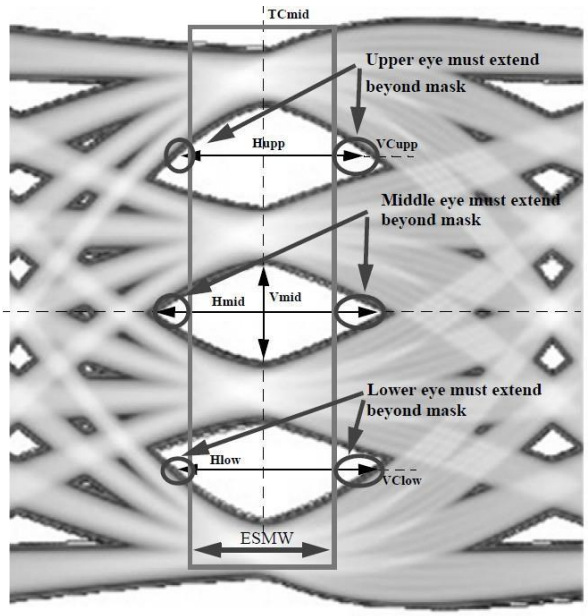


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## Performance Parameters

All SFF-8436 Specifications must be met. In addition, the following items must be met which narrow the SFF-8436 specification.

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern<br>Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with PRBS31Q pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 3W | |
| Latency | 30ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0'C – 70'C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | QSFP56, SFF8436 v4.9 compliant | |
| Cable Configuration / OD | <=7m – single conductor, <=6.8mm OD<br>>7m - single conductor, <= 9mm | Nominal OD |
| Cable Bend Space | <=7m, max 63.5mm | Measured from end of connector to 90 degree end in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend tress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from tated nominal length |

## Management Interface

- The device should be compliant to CMIS 4.0 protocol, see appendix C for precise register set. The device must support all modes defined in this register set.

# 400G QSFP-DD to 4 x QSFP28

## Description

This cable is a breakout cable connecting one 400G (8x56G lane, full duplex) QSFP-DD to 4 x QSFP28 including FEC termination or gearboxing functionality. The QSFP-DD side must operate with KP4 FEC; the QSFP28 must support software selectable KR4 FEC or CAUI-4.

## QSFP-DD Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

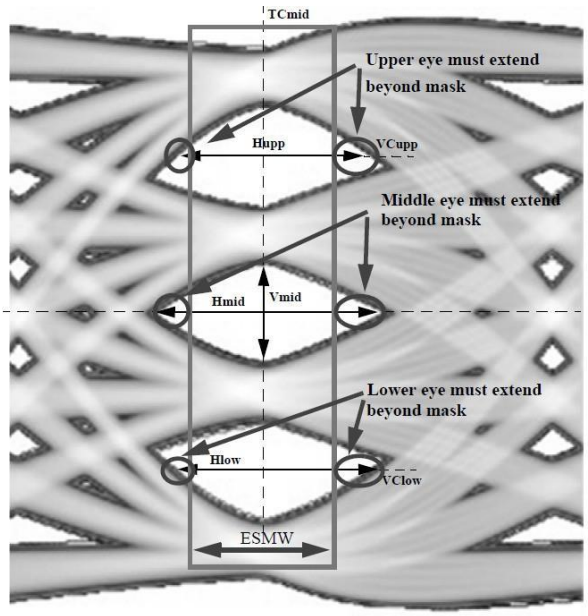


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## QSFP28 Host Side Electrical Performance

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 25.78125 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential output voltage (max) | 900 | mV |
| Eye width (min) | 0.57 | UI |
| Eye height, differential (min) | 228 | mV |
| Transition time (min, 20% to 80%) | 12 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

## Performance Parameters

All QSFP-DD MSA and SFF-8436 Specifications must be met. In addition, the following items must be met which narrow the QSFP-DD MSA.

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4 – QSFP-DD End)<br>25.78125Gbps (NRZ – QSFP28 End) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern<br>Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with PRBS31Q pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 5W QSFP-DD End<br>2.5W QSFP28 End | |
| Latency | 200ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0˚C – 70˚C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | QSFP-DD Type 2, MSA v3.0<br>QSFP28, SFF-8436 v4.9 | |
| Cable Configuration | 4 Cables emanating from QSFP-DD end | |
| Cable Outside Diameter | <=7m – maximum diameter 6mm<br>>7m – maximum diameter is 8mm | |
| Cable Bend Space | <=7m - max 63.5mm | Measured from end of connector to 90 degree bend in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend stress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from stated nominal length |

## Management Interface

- The QSFP-DD end should be compliant to CMIS v4.0 protocol, the QSFP28 End must be compliant with SFF-8636 v2.10a, see relevant MSA file precise register set. The device must support all modes defined in the attached register set.

# 400G OSFP to 4 x QSFP28

## Description

This cable is a breakout cable connecting one 400G (8x56G lane, full duplex) OSFP to 4 x QSFP28 including FEC termination or gearboxing functionality. The OSFP side must operate with KP4 FEC; the QSFP28 must support software selectable KR4 FEC or CAUI-4.

### QSFP-DD Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | -350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

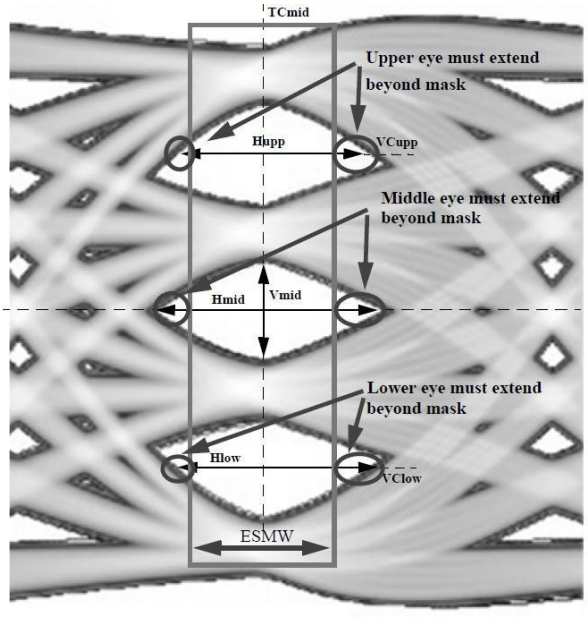


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## QSFP28 Host Side Electrical Performance

| Parameter | Value | Units |
|---|---|---|

| | | |
|---|---|---|
| Signaling rate per lane (range) | 25.78125 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential output voltage (max) | 900 | mV |
| Eye width (min) | 0.57 | UI |
| Eye height, differential (min) | 228 | mV |
| Transition time (min, 20% to 80%) | 12 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

## Performance Parameters

All OSFP MSA and SFF-8436 Specifications must be met. In addition, the following items must be met which narrow the specifications

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4 – OSFP End)<br>25.78125Gbps (NRZ – QSFP28 End) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern<br>Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with PRBS31Q pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 5W OSFP End | |
| | 2.5W QSFP28 End | |
| Latency | 200ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0'C – 70'C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | OSFP, MSA v2.0<br>QSFP28, SFF-8436 v4.9 | |
| Cable Configuration | 4 Cables emanating from OSFP side | |
| Cable Outside Diameter | <=7m – maximum diameter 6mm<br>>7m – maximum diameter is 8mm | |
| Cable Bend Space | <=7m, max 63.5mm | Measured from end of connector to 90 degree bend in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend stress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from stated nominal length |

## Management Interface

- The OSFP end should be compliant to CMIS v4.0 protocol, the QSFP28 End must be compliant with SFF-8636 v2.10a, see relevant MSA file precise register set. The device must support all modes defined in this register set.

# 200G QSFP56 to 2 x QSFP28

## Description

This cable is a breakout cable connecting one 200G (4x56G lane, full duplex) QSFP to 2 x 100G (4x28G lane, full duplex) QSFP28 including FEC termination or gearboxing functionality. The QSFP56 side must operate with KP4 FEC the QSFP28 must support software selectable KR4 FEC or CAUI-4.

## QSFP56 Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | -350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

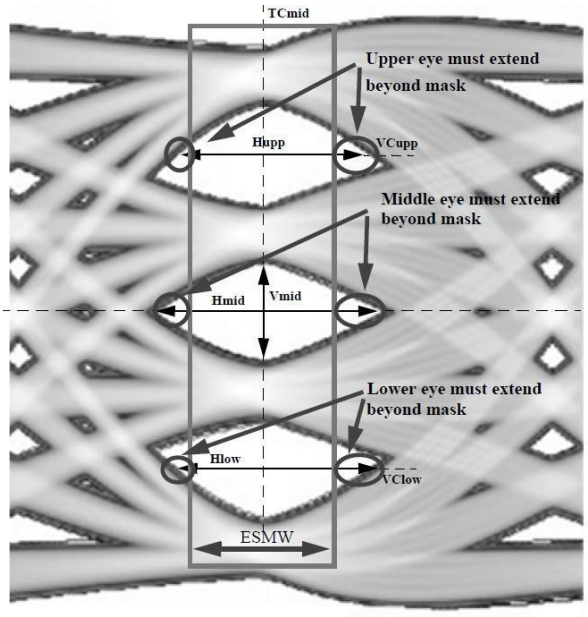


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## QSFP28 Host Side Electrical Performance

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 25.78125 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential output voltage (max) | 900 | mV |
| Eye width (min) | 0.57 | UI |
| Eye height, differential (min) | 228 | mV |
| Transition time (min, 20% to 80%) | 12 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

## Performance Parameters

All SFF-8436 Specifications must be met. In addition, the following items must be met which narrow the specifications

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4 – QSFP56 End)<br>25.78125Gbps (NRZ – QSFP28 End) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern, Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with PRBS31Q pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 3W QSFP56 End<br>2.5W QSFP28 End | |
| Latency | 200ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0˚C – 70˚C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | QSFP, SFF-8436 v4.9 | |
| Cable Configuration | 2 Cables emanating from QSFP56 side | |
| Cable Outside Diameter | <=7m – maximum diameter 6mm<br>>7m – maximum diameter is 8mm | |
| Cable Bend Space | <=7m - Max 63.5mm | Measured from end of connector to 90 degree bend in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend stress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from stated nominal length |

## Management Interface

- The Q56 end must be compliant with CMIS 4.0, the Q28 must be compliant with SFF-8636 v2.10a, see relevant MSA file precise register set. The device must support all modes defined in this register set.

# 200G QSFP56 to 2 x QSFP56

## Description

This cable is a breakout cable connecting one 200G (4x56G lane, full duplex) QSFP to 2 x 100G (2x56G lane, full duplex) QSFP56 without FEC termination or gearboxing functionality.

## QSFP56 Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

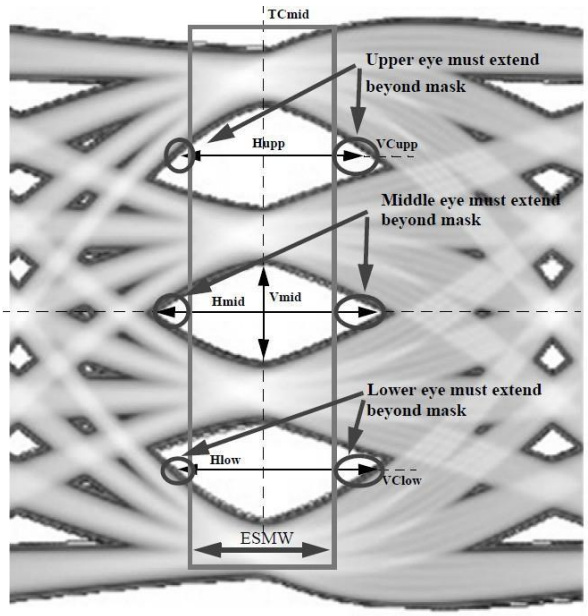


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## Performance Parameters

All SFF-8436 Specifications must be met. In addition, the following items must be met which narrow the specifications

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern, Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with PRBS31Q pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 3W QSFP56 End | |
| Latency | 30ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0'C – 70'C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | QSFP, SFF-8436 v4.9 | |
| Cable Configuration | 2 Cables emanating from QSFP56 side | |
| Cable Outside Diameter | <=7m – maximum diameter 6mm<br>>7m – maximum diameter is 8mm | |
| Cable Bend Space | <=7m - Max 63.5mm | Measured from end of connector to 90 degree bend in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend stress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from stated nominal length |

## Management Interface

- The Q56 end must be compliant with CMIS 4.0, the Q28 must be compliant with SFF-8636 v2.10a, see relevant MSA file precise register set. The device must support all modes defined in this register set.

# 100G DSFP/SFP56-DD to QSFP28

## Description

This cable is a gearboxed cable connecting one 100G (2x56G lane, full duplex) DSFP or SFP56-DD to one 100G (4x28G lane, full duplex) QSFP28 including FEC termination or gearboxing functionality. The DSFP/SFP56-DD side must operate with KP4 FEC; the QSFP28 side must support both KR4 FEC and CAUI-4 via a software switch in the QSFP28 side.

## DSFP / SFP56-DD Host side Electrical Performance

**Refer to IEEE C2M specification**

**Note:** *Please refer to IEEE802.3bs 120E for TP4 definition. Output values are fixed in cable, autonegotiation and link training are not supported.

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 26.5625 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential peak-to-peak output voltage (max) | 900 | mV |
| Near-end ESMW (Eye symmetry mask width) | 0.265 | UI |
| Near-end Eye height, differential (min) | 70 | mV |
| Far-end ESMW (Eye symmetry mask width) | 0.2 | UI |
| Far-end Eye height, differential (min) | 30 | mV |
| Transition time (min, 20% to 80%) | 9.5 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

a DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

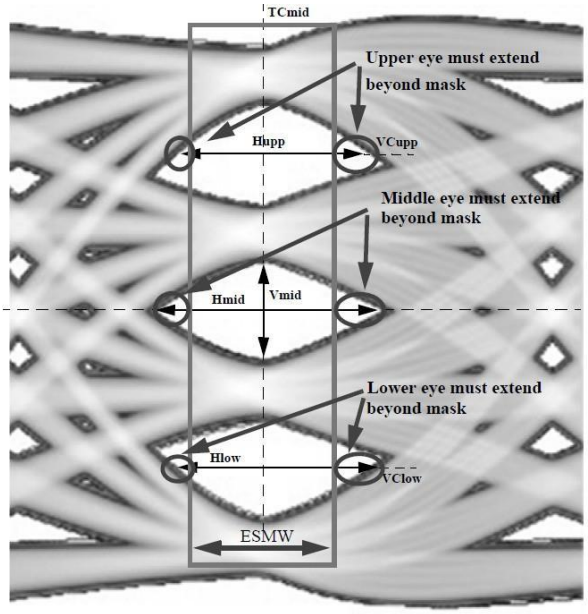


*Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask*

## QSFP28 Host Side Electrical Performance

| Parameter | Value | Units |
|---|---|---|
| Signaling rate per lane (range) | 25.78125 ± 100 ppm | GBd |
| AC common-mode output voltage (max, RMS) | 17.5 | mV |
| Differential output voltage (max) | 900 | mV |
| Eye width (min) | 0.57 | UI |
| Eye height, differential (min) | 228 | mV |
| Transition time (min, 20% to 80%) | 12 | ps |
| DC common mode voltage (min)[a] | –350 | mV |
| DC common mode voltage (max)[a] | 2850 | mV |

## Performance Parameters

All DSFP or SFP-56DD and SFF-8436 Specifications must be met. In addition, the following items must be met which narrow the specifications

| Parameter | Max Value | Comments |
|---|---|---|
| Nominal Data Rate per Lane | 53.125Gbps (PAM4 – DSFP/SFP56-DD End)<br>25.78125Gbps (NRZ – QSFP28 End) | |
| BER (Pre-FEC) | $<2x10^{-8}$ | Worst case lane, tested with PRBS31Q pattern, Room temp |
| BER (Post-FEC) | $<10^{-15}$ | Tested with PRBS31Q pattern<br>Tested at min and max operating temp |
| Power Consumption per End | 2.5W | |
| Latency | 200ns + 4.5ns/m of cable flight time | |
| Operating Case Temp | 0'C – 70'C | |
| Time to CMIS Ready | 2 seconds | Power on or reset to CMIS I2C ready to respond to commands |
| Time to link | 30 seconds | Power on or reset to link established end to end |

## Mechanical Parameters

| Parameter | Value | Comments |
|---|---|---|
| Module Form Factor | DSFP v1.0, SFP-DD v1.0, SFF-8436 v4.9 | |
| Cable Configuration | Single Cable connecting ends | |
| Cable Outside Diameter | <=7m – maximum diameter 6mm<br>>7m – maximum diameter is 8mm | |
| Cable Bend Space | Max 63.5mm | Measured from end of connector to 90 degree bend in cable |
| Cable Bend Radius | 100 cycles - 5x OD<br>10 cycles – 3x OD | Must continue to meet specifications post bend stress test |
| Length Tolerance | Nominal +/- 60mm | Connector Edge to edge length variation from stated nominal length |

## Management Interface

- SFP56-DD End must be compliant with SFP-DD Management Interface v1.0
- DSFP End must be compliant with DSFP Management Interface v1.0
- QSFP28 end must be compliant with SFF-8636
- See relevant MSA file precise register set. The device must support all modes defined in this register set.

## Appendix A - Checklist for IC approval of this Specification

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

| Item | Status or Details | Link to detailed explanation |
|---|---|---|
| Is this contribution entered into the OCP Contribution Portal? | Yes or No | If no, please state reason. |
| Was it approved in the OCP Contribution Portal? | Yes or No | If no, please state reason. |
| Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider) | Yes or No | List Supplier Name(s) |
| Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days? | Yes or No | If more time is required, please state the timeline and reason for extension request.<br><br>Please have each Supplier fill out Appendix B. |

## Appendix B-Credo - OCP Supplier Information and Hardware Product Recognition Checklist

(to be provided by each supplier seeking OCP recognition for a Hardware Product based on this specification)

Company: Credo
Contact Info: 110 Rio Robles, San Jose, CA 95134
hiwire@credosemi.com

Product Name: HiWire LP SPAN AECs
Product SKU#: CAC43X301D1D-D0-HW, CAC45X301D1D-D0-HW, CAC47X281D1D-D0-HW
Link to Product Landing Page: https://credosemi.com/products/hiwire-aec/span-lp-span/

Product Name: HiWire LP CLOS AECs
Product SKU#: CAC405321D1D-D0-HW, CAC41X321D1D-D0-HW, CAC415321D1D-D0-HW, CAC42X321D1D-D0-HW, CAC425321D1D-D0-HW
Link to Product Landing Page: https://credosemi.com/products/hiwire-aec/lp-clos/

Product Name: HiWire SHIFT AECs
Product SKU#: CAC43X301D4P-A0-HW, CAC43X301D4P-A0-HW
Link to Product Landing Page: https://credosemi.com/products/hiwire-aec/shift-lp-shift/

The following is needed for OCP hardware product recognition:

**For OCP Inspired™**

- All Suppliers must be a Silver, Gold or Platinum Member.
- Declare product is 100% compliant with specification
- Complete the OCP Inspired™ Product Recognition Checklist, which includes hardware management conformance checks and security profile.

**For OCP Accepted™**

- All Suppliers must be an OCP Member. All corporate membership levels are eligible.
- Complete the OCP Accepted™ Product Recognition Checklist, which includes hardware management conformance checks, security profile and open system firmware conformance checks.
- Submit a design package meeting OCP Hardware Design Guideline Contribution Checklist (if not already submitted by the contributor). If already submitted, declare the product is 100% compliant with the design package.
- Submit a  firmware package including a firmware image, build scripts, documentation, test results and a tool that verifies modifications
- Submit the BMC source code, if applicable to product type

Please complete the OCP Inspired™ Product Recognition Submission Checklist or OCP Accepted™ Product Recognition Checklist and the following table.

| Item | Details | Links |
|---|---|---|
| Which product recognition? | OCP Accepted™ or OCP Inspired™ | Provide link for the appropriate Product Checklist |
| If OCP Accepted™, who provided the Design Package? | | Link to OCP Contribution Database |
| Where can a potential adopter purchase the product? | | Link to OCP Marketplace |