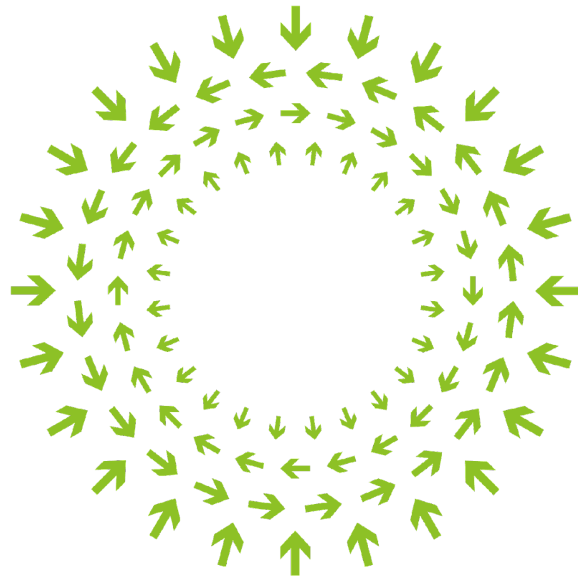




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Compute Project

Grand Teton Switch Tray Specification

Version 1.0

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2. Compliance with OCP Tenets

2.1 Openness

The Grand Teton platform design exemplifies openness by defining a platform that can support multiple use cases and workloads. This includes modular swappable trays for all system components and open-source BMC/BIC firmware, which allows users to optimize the system for their own needs.

2.2 Efficiency

Compared to past generations, the Grand Teton platform offers efficiency gains across the power and thermal systems by upgrading to the 51V ORv3 rack architecture. There are also efficiency gains through the system architecture, which utilizes trays that can be swapped to improve performance or optimize the hardware for evolving workloads.

2.3 Impact

The Grand Teton platform represents a number of firsts in large-scale AI infrastructure, including next-gen CPUs, PCIe Gen5, DDR5, and NVIDIA HGX. These technologies, along with the flexibility of the system architecture, support high-performance workloads that can scale out and utilize other OCP solutions, such as ORv3, DC-SCM, OCP NIC, OCP E1.S, Wedge400, and Minipack2.

2.4 Scale

The Grand Teton platform utilizes the latest features to support large-scale deployment, including tool-less FRUs, extensive remote management, error reporting, future upgradeability, and on-premises serviceability enhancements. Offering flexible scale capabilities, Grand Teton can be used as a single system up through hyper-scale deployment. The system also uses OpenBMC and OpenBIC open-source software.

2.5 Sustainability

The Grand Teton platform follows environmental compliance standards and best practices. The modular design allows for more targeted repairs, reducing waste and allowing the system to be used across multiple generations. The platform is fully compliant with major environmental standards, such as RoHS 2 and REACH. The system fans are optimized to sufficiently cool components while minimizing power consumption.

3. Change Log

Date	Version #	Author	Description
07AUG2023	0.1	Jeremy Baumgartner Matt Bowman	Initial draft
23AUG2023	0.9	Jeremy Baumgartner Matt Bowman	Added content to several sections
05SEPT2023	1.0	Jeremy Baumgartner Matt Bowman	Added content

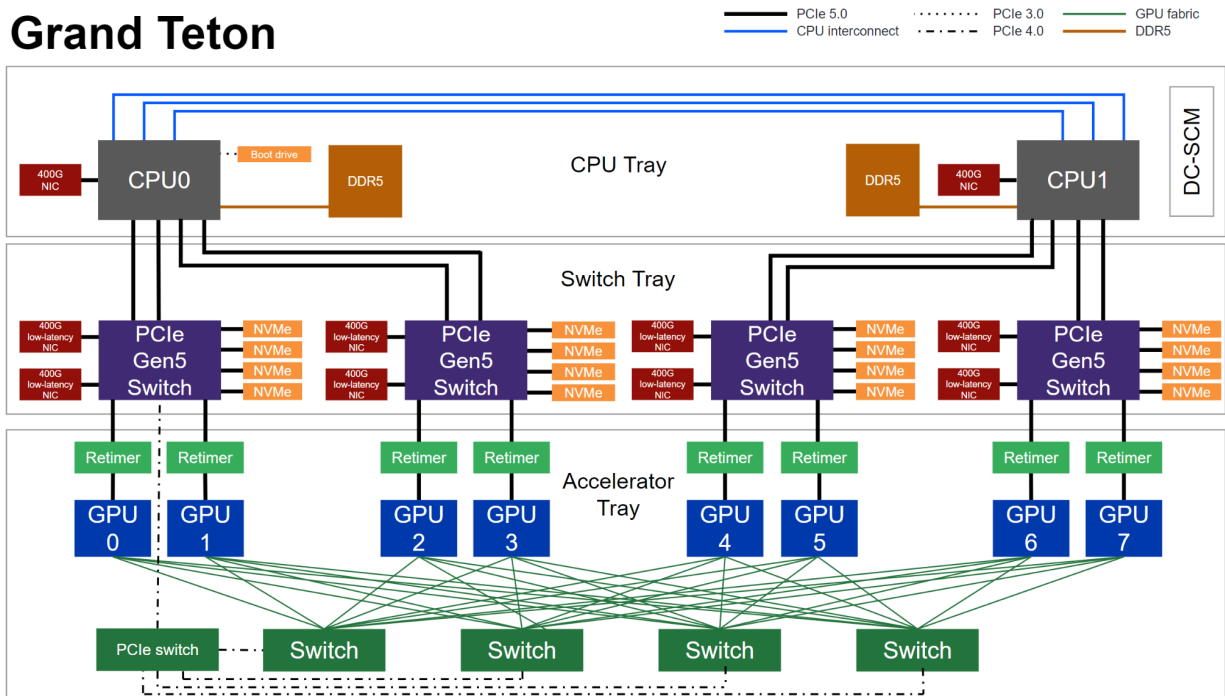
4. Scope

This document defines the Hardware Product Specification for the Grand Teton (GT) Switch Tray, which is used in the Grand Teton platform.

5. Overview

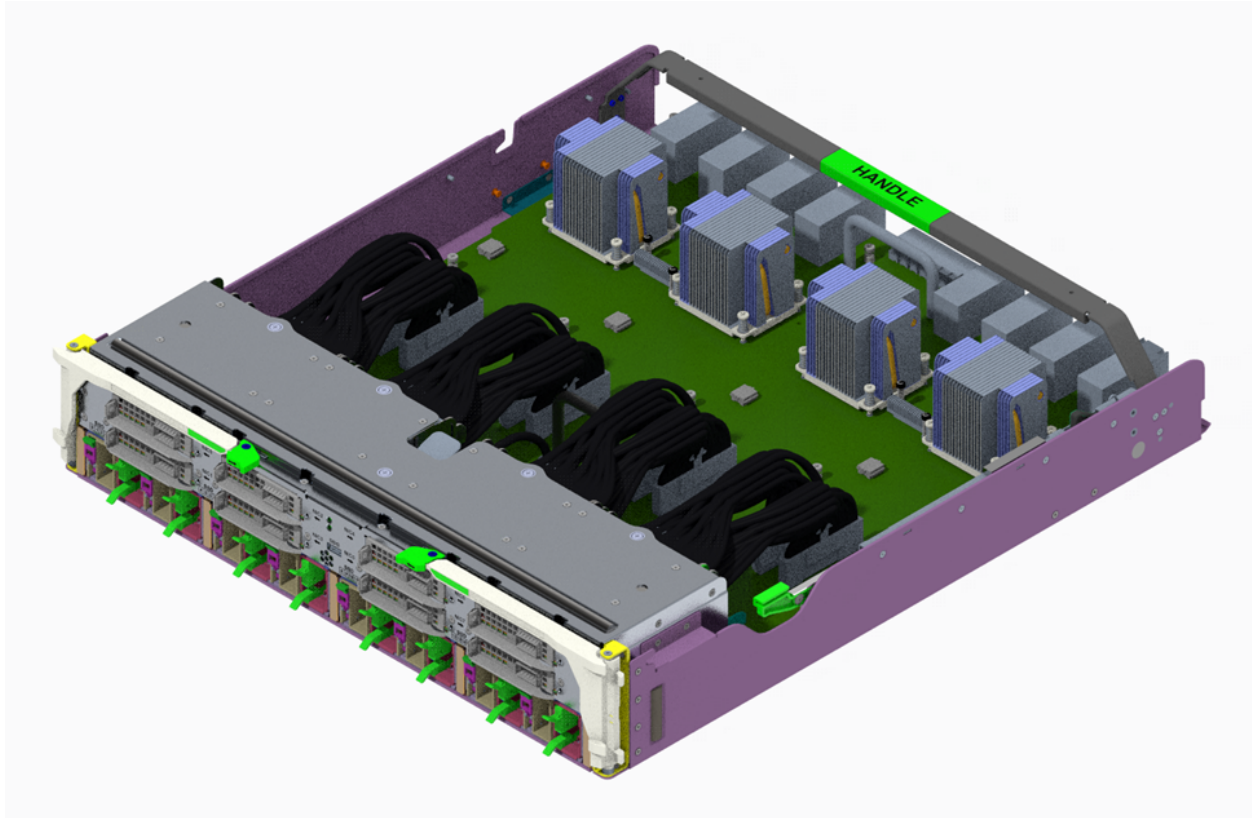
5.1 Platform Block Diagram

Grand Teton



High-level block diagram of a Grand Teton system

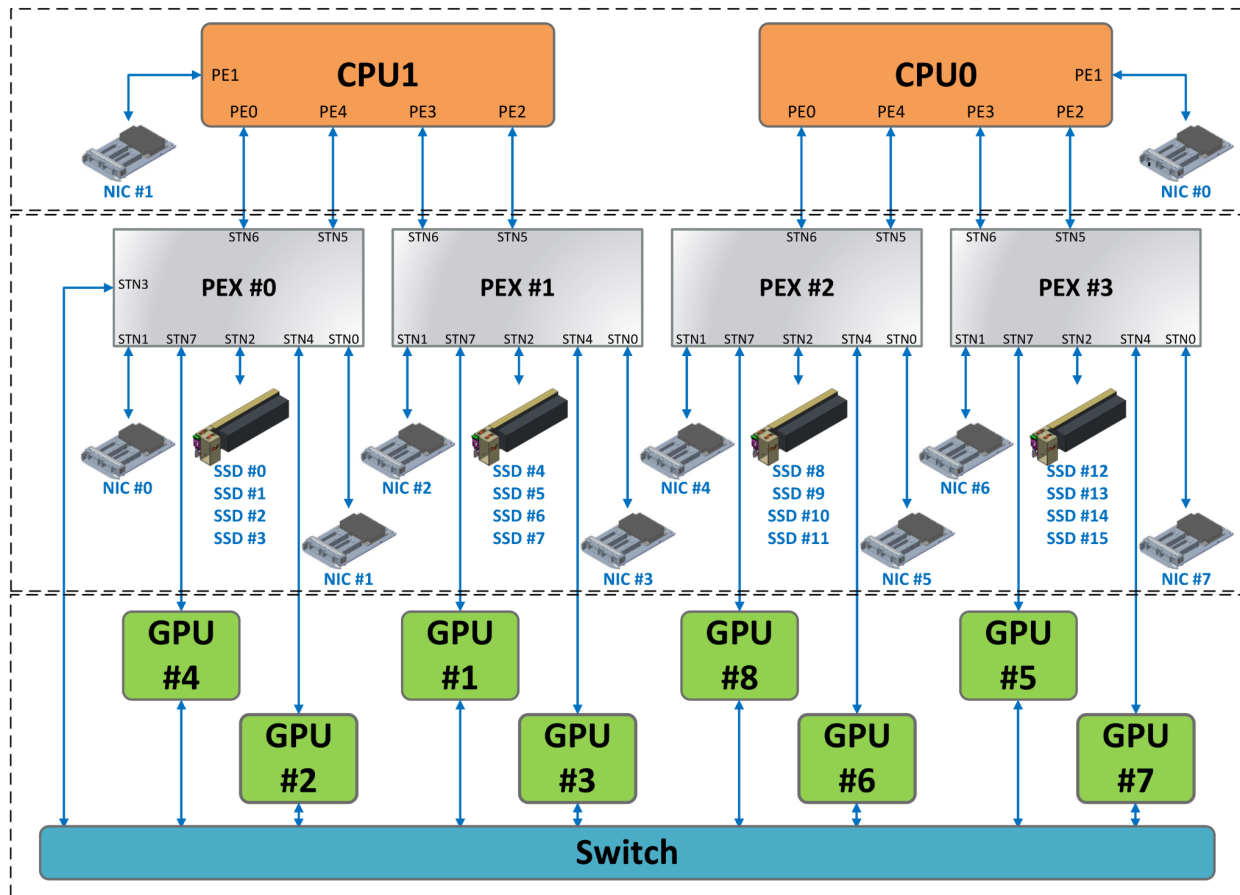
5.1 Switch Tray



Overall view of the Switch Tray

The Switch Tray contains four Broadcom PEX89144 PCIe 5.0 switches with 144 lanes each to enable the high speed interconnect between the CPUs, NICs, SSDs, and accelerators. All PCIe links are capable of operation at PCIe 5.0 speeds.

The Switch Tray supports eight (8) OCP NIC 3.0 and sixteen (16) E1.S SSDs.



Block diagram of the Switch Tray within the Grand Teton system

Each PCIe switch has the following PCIe 5.0 interfaces:

- Two x16 Upstream Ports through ExaMax high speed connectors to CPU tray
- Two x16 Downstream Ports through ExaMax high speed connectors to Accelerator tray
- Two x16 Downstream Ports through 4C+ connectors through an internal cable to front-accessible OCP NIC 3.0 TSFF
- Four x4 Downstream Ports, each to an E1.S connector to front-accessible SSDs
- One x4 Downstream Port (PEX0 only) through ExaMax high speed connector to Accelerator tray management

Each PCIe switch operates in synthetic mode, where an internal MCPU is used to create two virtual switch partitions, such that one accelerator, one NIC, and two SSDs are located under each CPU Root Port.

The front-accessible E1.S SSDs and OCP NICs are electrically safe to hot-insert and hot-remove from a powered system. The E1.S SSDs support surprise link down, error containment through DPC, and PCIe hotplug.

The Switch Tray includes a bridge IC (BIC) for board management. The BIC operates as a subsystem of the BMC, with no direct access to the outside network. The BIC is responsible for the physical connection to sensors and configuration memories on the Switch Tray, but all actions are initiated by the BMC.

The BIC supports a recovery boot mode to allow a BMC to recover a corrupt or out-of-date BIC firmware. Under normal operation, the BIC boot from an internal configuration flash.

The BIC also operates independently of all other devices on the Switch Tray and allows the BMC to recover any configuration memory located within the Switch Tray.

A programmable CPLD is used for power sequencing, sensor and status monitoring, and communication with the BMC and BIC.

The Switch Tray has a Front I/O Board that has a USB 3.0 debug port.

5.3 Base Specification

This specification is a subset of the *Grand Teton Platform Specification*.

6. Environmental Regulatory Compliance And Requirements

6.1 Environmental

- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: +5°C to +35°C
- Operating and Storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-ratings: 6000 feet

6.2 Regulatory Compliance

- CE and NRTL (UL listed) marks in accordance with the listing and surveillance requirements of the NRTL
- EU Low Voltage Directive (2014/35/EC)
- EU EMC Directive (2014/30/EC)
- EN55032/CISPR32, Class A criteria
- EN55035/CISPR35
- CISPR16
- ANSI C63.4
- EN61000-4-2
- EN61000-4-3
- EN61000-4-4
- EN61000-4-5
- EN61000-4-6
- EN61000-4-11
- FCC CFR47 Part 15, Subpart B, Class A criteria
- RoHS Directive (2015/863/EU)
- WEEE Directive (2012/19/EU)
- REACH regulation (EC 1097/2006)
- US EPA 40 CFR751
- IEC/EN 62368-1, hazard-based performance standard for audio video, and ITE

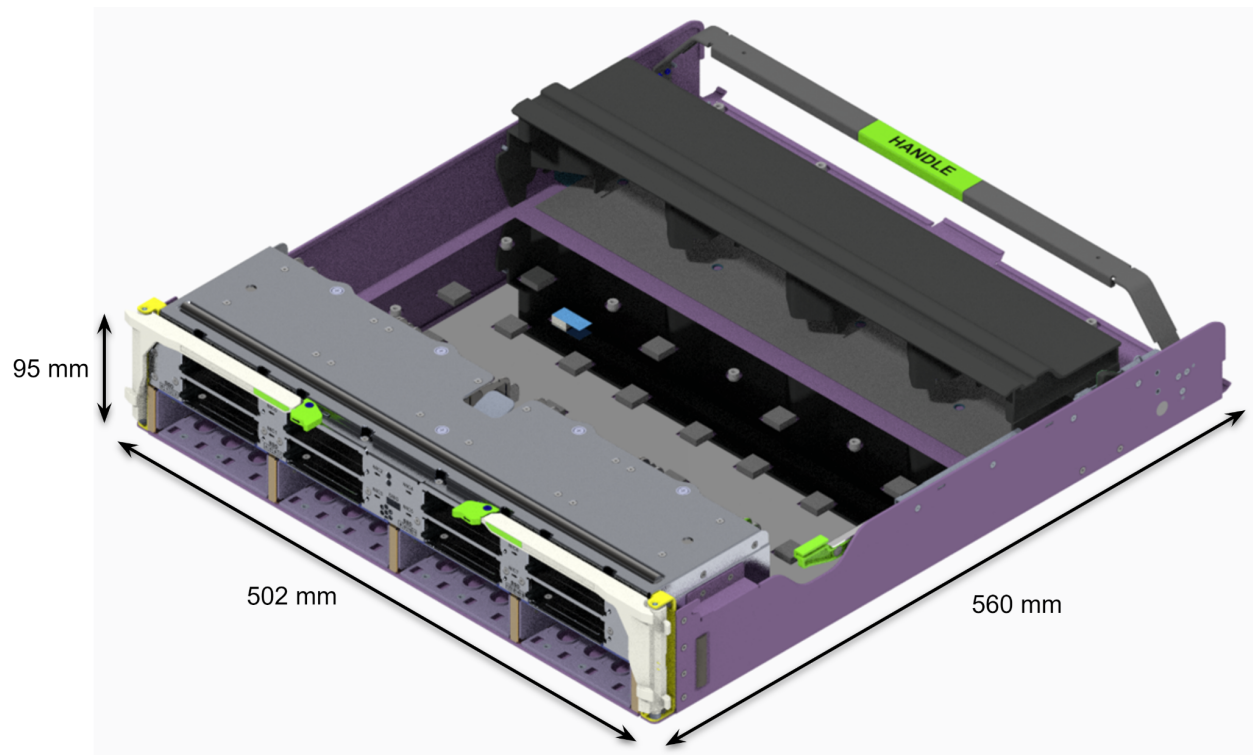
7.2 PCB Stackup

Layer#	Material	Description	Copper Weight (oz)	Thickness (mil)	Tolerance (mil)	Glass Fabric	Er
		Soldermask		0.60			3.8
1		TOP	0.5+plating	1.95			
	EM-890K	PP		2.70	±0.709	1078x1	2.92
2		GND	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
3		VCC	1 (VL411)	1.30			
	EM-890K	PP		8.00	±1.5	3313x2	2.97
4		VCC1	2 (RTF)	2.60			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
5		GND1	1 (VL411)	1.30			
	EM-890K	PP		8.00	±1.5	3313x2	2.97
6		IN1	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
7		GND2	1 (VL411)	1.30			
	EM-890K	PP		8.00	±1.5	3313x2	2.97
8		IN2	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
9		GND3	1 (VL411)	1.30			
	EM-890K	PP		7.80	±1.5	3313x2	2.97
10		IN3	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
11		GND4	1 (VL411)	1.30			
	EM-890K	PP		8.00	±1.5	3313x2	2.97
12		IN4	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
13		GND5	1 (VL411)	1.30			
	EM-890K	PP		8.00	±1.5	3313x2	2.97
14		IN5	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
15		GND6	2 (RTF)	2.60			
	EM-890K	PP		8.00	±1.5	3313x2	2.97
16		IN6	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
17		GND7	1 (VL411)	1.30			
	EM-890K	PP		2.70	±0.709	1078x1	2.92
18		BOTTOM	0.5+plating	1.95			
		Soldermask		0.60			3.8
			Total	121.70	±10%		

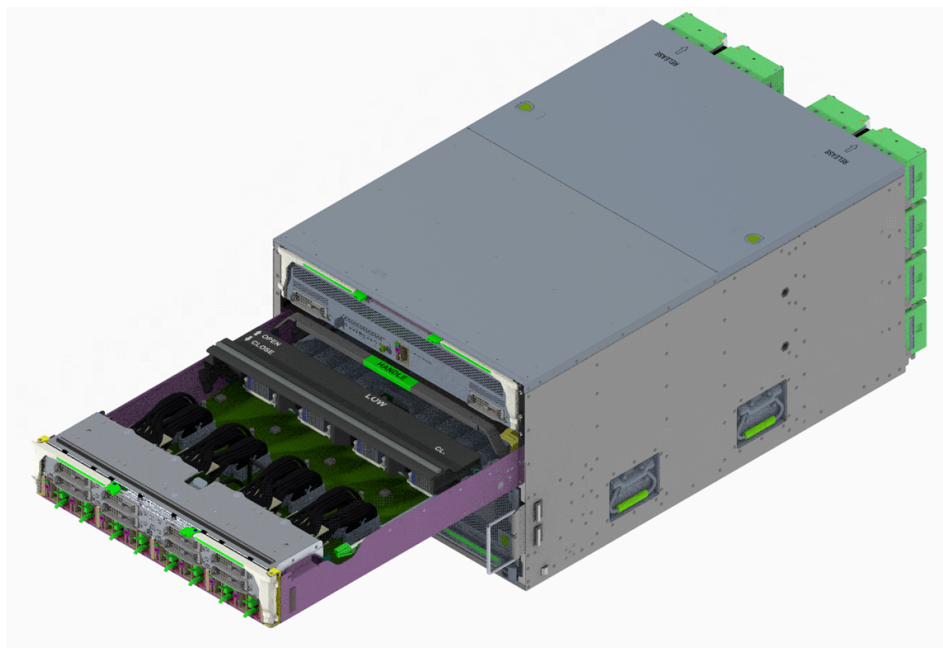
7.3 Mechanical

The Switch Tray includes two lever arms at the front top of the tray for installation and removal leverage. The tray also includes a stop latch that prevents inadvertent removal of the entire tray until the technician is ready.

The tray and included FRUs all feature tool-less removable and green touchpoints.



Overall dimensions of the Switch Tray with air baffles installed



Switch Tray partially removed from the chassis

The Switch Tray weighs approximately 12.1 kg (26.6 lb) overall.

7.4 Rack Compatibility

The Switch Tray is intended to be used in a Grand Teton platform chassis installed in an Open Rack V3 (ORv3) compatible rack.

8. Electrical Requirements

The Switch Tray uses the 12VDC rail from the Vertical Power Distribution Board (VPDB). The VPDB converts 51VDC from the ORv3 bus bar down to 12VDC and is capable of powering 6kW. The 12V provided to the Switch Tray should have a tolerance of +/- 10%.

9. Thermal Design Requirements

9.1 Thermal Architecture

Grand Teton is an 8OU system with 3 trays in parallel: CPU Tray, Switch Tray and Accelerator Tray. Airflow to all 3 trays is delivered by a fan array at the rear side of the chassis, with a shared plenum. All components are air-cooled, using passive heatsinks where applicable.

9.2 System Thermal Specification

	Normal Operation	Corner Case	Remain Power on
Inlet Temperature	Up to 30°C	Up to 35°C	Up to 45°C
Altitude (no inlet temp deration)	Up to 6000 ft	Up to 6000 ft	Up to 6000 ft
Cold/Hot Aisle Δp	Within +/- 0.005 InH ₂ O	Within +/- 0.1 InH ₂ O	Within +/- 0.1 InH ₂ O
Relative Humidity	10% ~ 90%	10% ~ 90%	10% ~ 90%
Fan Status	All Healthy	Single fan/rotor failure	Single fan/rotor failure
Air side ΔT (CFM/W)	More than 12.5°C (22°F) Less than 0.145 CFM/W at sea level [Max loading condition only]	NA	NA
Thermal Throttling	Not allowed	Not allowed	Allowed
Minimum Thermal Margin	7% of component temperature spec	NA	NA
Fan Power Ratio	Below 5% of system total power	NA	NA

	[Max loading condition only]		
--	------------------------------	--	--

9.3 Fan Configuration

Grand Teton uses sixteen (16) 80x56mm counter rotating fan modules. A shared fan wall is used for all trays, sharing the same PWM control algorithm. Single rotor failure is supported in corner cases.

9.4 Fan Control Target

Under normal operation conditions, minimum margin (critical component) shall be at least 7% of component temperature spec, while fan power consumption shall be less than 5% of system total power (account for max loading power only).

9.5 Thermal Sensors

The BMC monitors all applicable temperature, power, and fan speed sensors, and adopts selective temperature readings for fan speed control algorithms when applicable. The maximum allowable tolerance of the inlet temperature sensor is $\pm 2^{\circ}\text{C}$. The maximum allowable tolerance of other thermal sensors is $\pm 5^{\circ}\text{C}$.

9.6 Fan Control Algorithm

Look up tables are applied to the inlet temperature sensor, and temperature sensors of all components with thermal risk under all possible operation conditions, if the fans operate at the minimum duty specified (20%). PID control tables should be applied to temperature sensors of all components that may be thermally critical under all possible operation conditions.

9.7 Special Conditions

For devices/components/parts that do not have built-in temperature sensors or cannot be included in fan speed control, their thermal solution design should enable the inlet-temperature based FSC to ensure their cooling at idling/low loading conditions. The PID control FSCs should ensure their cooling at heavy load conditions.

Special fan modes shall be designed for the following scenarios:

- AC Cycle
- DC Power Off/Cycle
- Single rotor Failure
- Fan Board Failure
- Sensor failure or exceed LCR/UCR limits

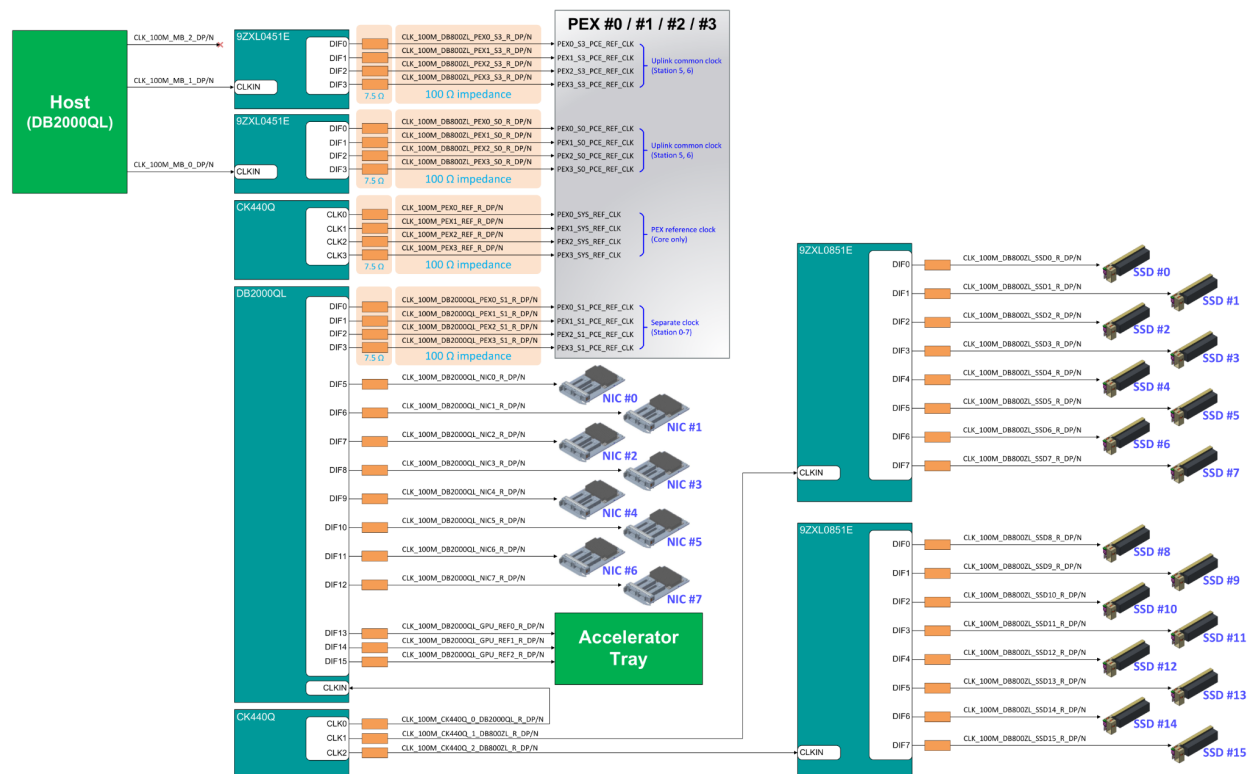
10. Interfaces

10.1 Signal List

The Switch Tray includes the following signals:

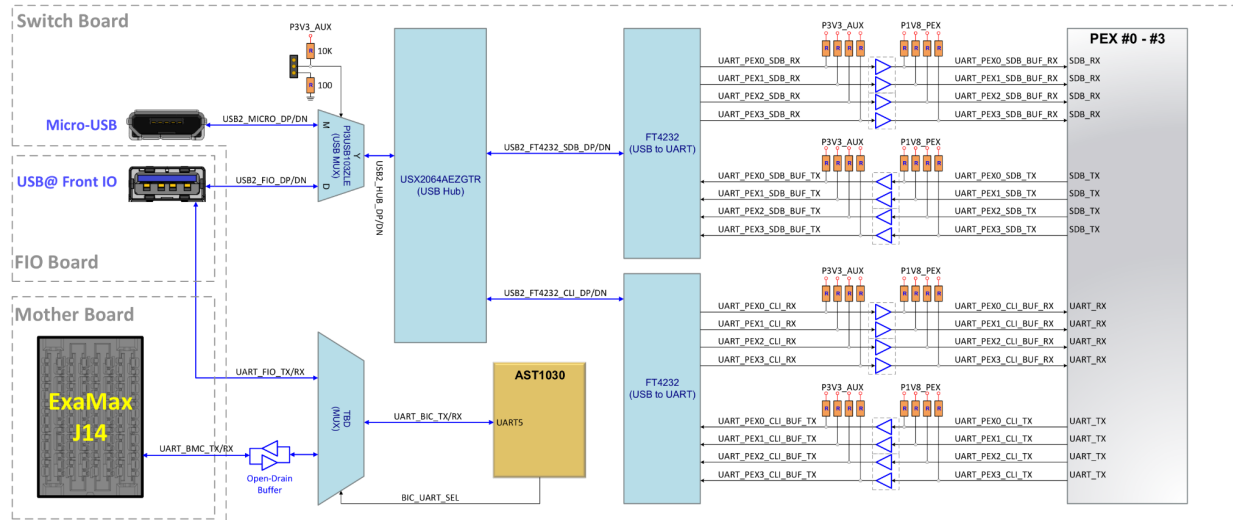
- High-speed signals
 - PCIe 5.0 between the switches, NICs, SSDs, and backplane connectors
 - Clocks (see diagram below)
- Low-speed signals
 - I2C/I3C/SPI for management, sensors, I/O expanders, and other components
 - USB 3.0 for debug connections
 - GPIO
 - JTAG
 - UART for debug access

Below are diagrams of Switch Tray signals:

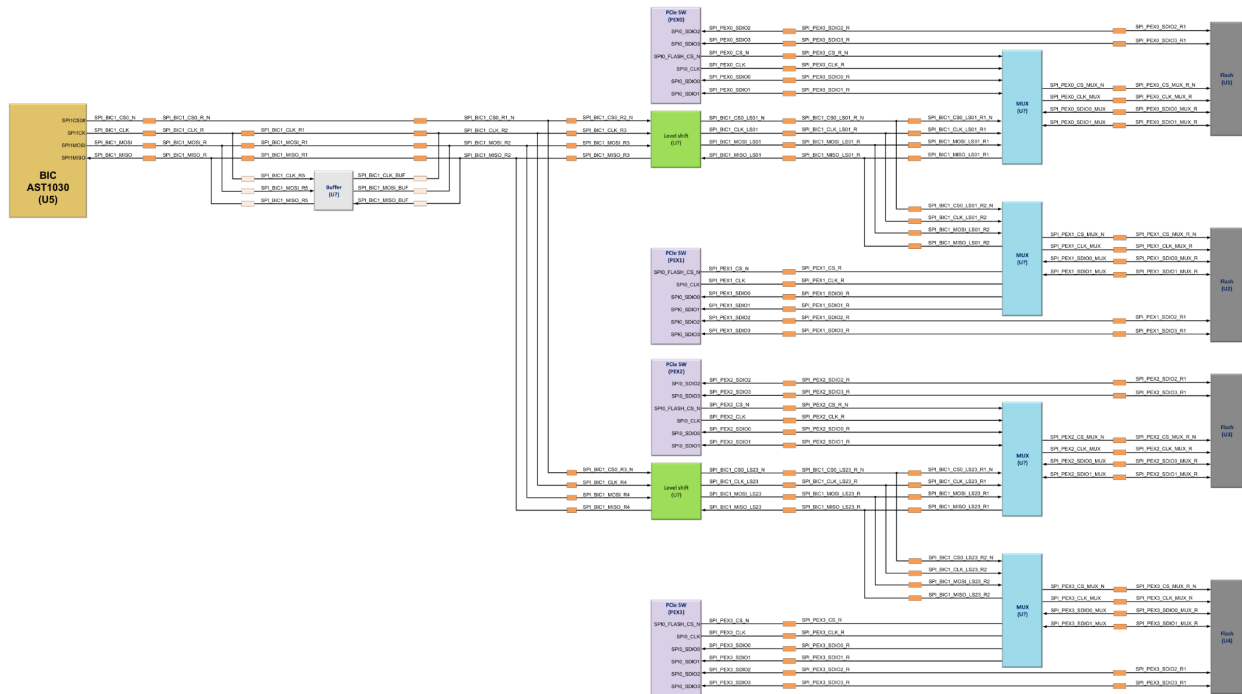


Block diagram of Switch Tray clock signals

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Block diagram of Switch Tray UART signals



Block diagram of Switch Tray SPI signals

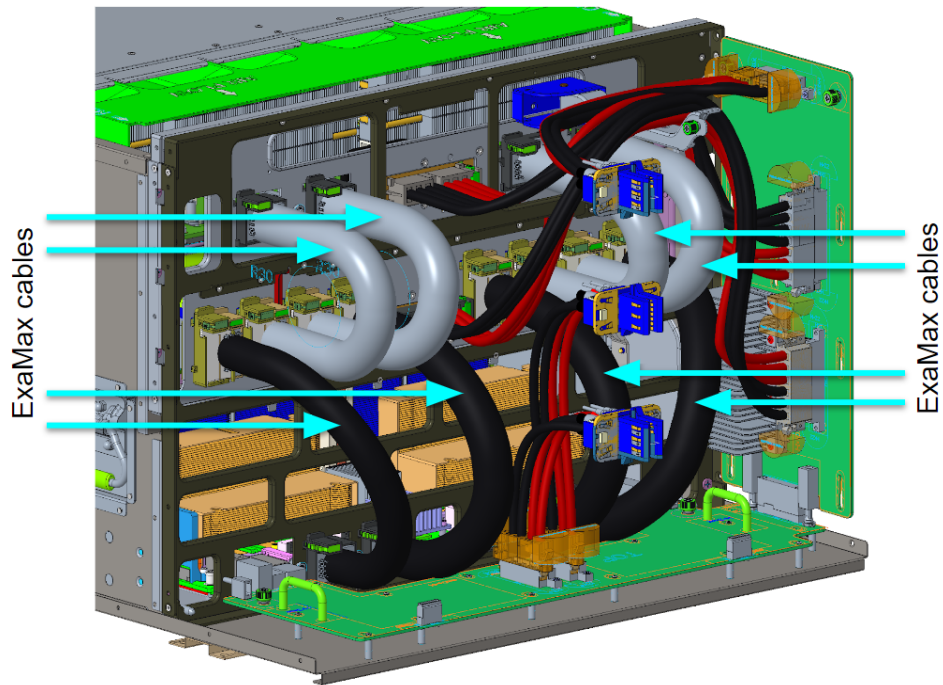
The Switch Tray has the following control and status interfaces:

Signal name	Direction	PU/PD	CPU tray device	Switch Tray Device	Description
3V3IO_RSVD [1,3,4]	IN	none	CPLD	CPLD	Reserved pins for future use
BIC_MON	OUT	none	CPLD	BIC	Output heartbeat signal from BIC to indicate that BIC is operating as expected.
BIC_RDY	OUT	none	CPLD	BIC	Output signal from BIC to indicate that AUX power is present, and BIC/CPLD configuration is complete.
BIC_UART_RX	IN	PD	BMC	BIC	Debug UART interface
BIC_UART_TX	OUT	none	BMC	BIC	Debug UART interface
BMC_MON	IN	PD	CPLD	BIC	Input heartbeat signal from BMC to indicate that BMC is operating as expected
HSC_EN	IN	PD	CPLD	HSC	HSC Enable controlling 12V to tray. Must only be asserted if PRSNT_N.
HSC_GD	OUT (OD)	PU	CPLD	HSC	HSC Power Good signal indicating 12V is present on the board. Must be asserted before checking BIC_RDY or enabling Main Power
I2C_SCL/SDA	IN/OUT (OD)	none	BMC	CPLD	I2C interface to CPLD
I3C_SCL/SDA	IN/OUT (OD)	PU	BMC	BIC	I3C interface to BIC
PERST_N[0:2]	IN	PD	CPLD	CPLD	PCIe Reset signal input to CPLD. CPLD uses this input to generate reset signals for downstream peripherals
PRSNT_N	OUT	GND	CPLD	GND	Passive present detect. Connected to GND when tray is seated in rear connector

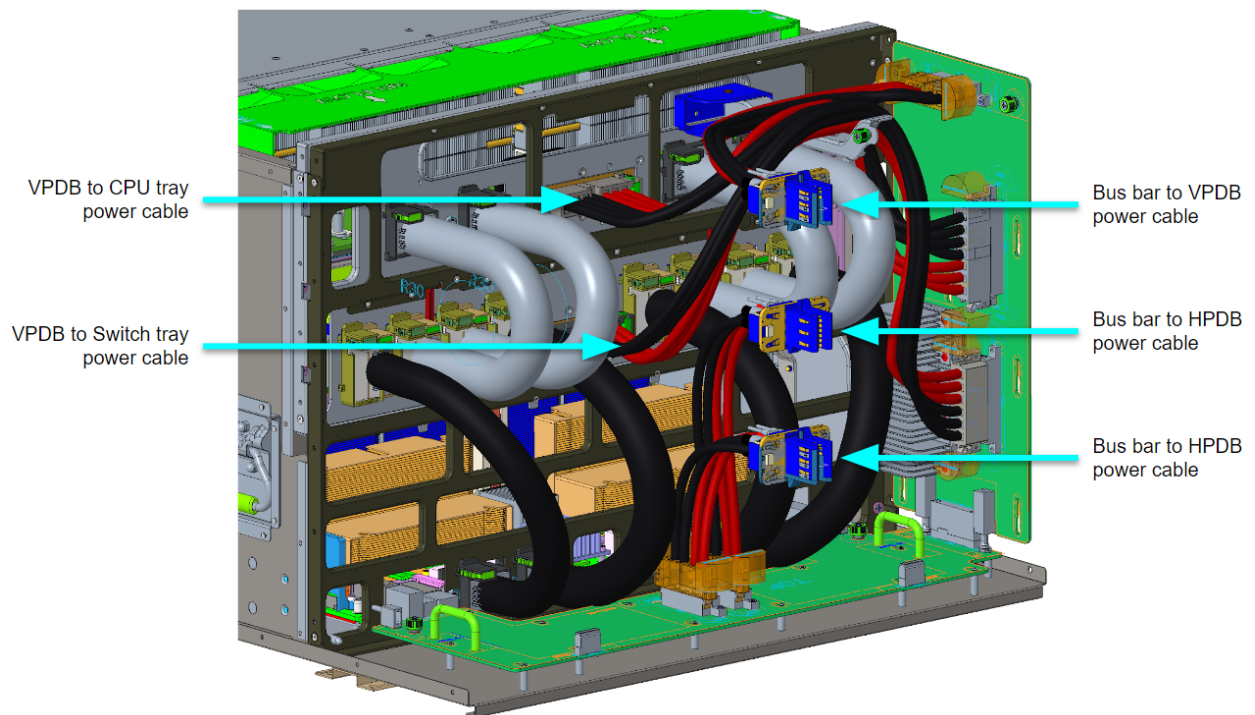
					indicating board is ready. HSC_EN must not be asserted until PRSNT_N
PWR_EN	IN	PD	CPLD	CPLD	Main Power enable. May only be asserted after HSC_EN, HSC_GD and BIC_RDY signals have been asserted.
PWR_GD	OUT	PU	CPLD	CPLD	Main Power good. Asserted when all VR are operating within required tolerances.
RST_BIC_N	IN	PU	CPLD	BIC	Input signal to reset BIC. Signal can be asserted at power up to delay BIC configure or left to float.
RST_BMC_N	OUT	none	CPLD	BIC	Output signal to reset system BMC. Signal must remain deasserted and free of glitches throughout power up and down sequence.
USB_DP/DM	IN/OUT	none	BMC	USB Hub	USB Hub Upstream Port. Downstream ports are connected to BIC and GPU tray.

10.2 Cable Backplane

The Switch Tray slides into the chassis to blind mate into the ExaMax data cable and power cable backplane at the rear interior of the chassis. These connections include 12VDC power from the VPDB, PCIe 5.0 to the CPU tray and Accelerator tray, and management signals routed throughout the chassis. All ExaMax cables include a presence detect signal.



Overall diagram of the ExaMax cable backplane



Overall diagram of the power cables backplane

10.3 Front I/O Board

The Switch Tray contains a Front I/O (FIO) Board, which is a cabled extension board from the Switch board to the front panel that provides a USB 3.0 debug for OCP Debug card access to the system. This includes I2C access to the BIC and OCP Debug card-defined I/O expander, as well as UART access to the BIC.

11. Onboard Power System

The VPDB supplies the Switch Tray with 12VDC. The Switch board has a 12V hot swap controller to support tray insertion and removal from a live system. Voltage regulators on the board step down the 12V to all necessary voltages.

12. System Firmware

The Grand Teton system uses the following open source firmware:

- OpenBMC, an open-source firmware stack for the BMC on the SCM:
<https://github.com/facebook/openbmc/tree/helium/meta-facebook/meta-grandteton>
- OpenBIC, an open-source firmware for the BIC in the Switch Tray
<https://github.com/facebook/OpenBIC/tree/main/meta-facebook/gt-cc>

The Switch Tray includes the following programmable parts:

- Main 12V hotswap controller
- Voltage regulators
- BIC
- Management CPLD
- FRU EEPROM

13. Hardware Management

13.1 Out-Of-Band Management

The CPU tray has a dedicated 400G NIC for out-of-band (OOB) management of the system. OOB access is always online as long as standby power is provided. The NIC attaches to the CPU tray at slot NIC0 and is OCP NIC 3.0 compliant.

The BMC can update NIC firmware through OOB to ensure NIC update is available in case the OS is not accessible and in-band update fails.

The BIC supports a recovery boot mode to allow a BMC to recover a corrupt or out-of-date BIC firmware. Under normal operation, the BIC boot from an internal configuration flash.

13.2 BMC

This system uses an ASPEED AST2600 BMC with one 8Gb x16 DDR4 SDRAM and 65MB flash for various platform management services. The BMC interfaces with hardware, BIOS, and host firmware.

The BMC resides on the SCM board, which attaches to the CPU tray and follows the DC-SCM v1.0 specification (with board pinout exceptions, see the *Grand Teton Platform Specification*).

The BMC is a standalone system in parallel to the host. The health status of the host system does not affect the normal operation and network connectivity of BMC.

The BMC is remote upgradeable either by in-band across the network or out-of-band through the NIC.

13.3 BIC

This Switch Tray uses an ASPEED AST1030 BIC with 1MB internal flash and 768KB internal SRAM for Switch Tray hardware management services.

13.3 Remote Upgradeability

The system is capable of remotely upgrading the VRs, CPLDs, BIC, switches, and FRU EEPROMs. The BMC can access each device, update code from BMC to the device, and verify the code.

The BMC is capable of recovering all CPLD and BIC in the system from image corruption or an accidental erase. The BMC does not rely on proper operation of the BIC or CPLD for booting or to be accessible remotely.

13.4 Sensors

BMC has access to all Switch Tray analog sensors directly or through host management:

```
GT_SWB_NIC0_TEMP_C
GT_SWB_NIC0_VOLT_V
GT_SWB_NIC0_CURR_A
GT_SWB_NIC0_PWR_W
GT_SWB_NIC1_TEMP_C
GT_SWB_NIC1_VOLT_V
GT_SWB_NIC1_CURR_A
GT_SWB_NIC1_PWR_W
GT_SWB_NIC2_TEMP_C
GT_SWB_NIC2_VOLT_V
GT_SWB_NIC2_CURR_A
```

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GT_SWB_NIC2_PWR_W
GT_SWB_NIC3_TEMP_C
GT_SWB_NIC3_VOLT_V
GT_SWB_NIC3_CURR_A
GT_SWB_NIC3_PWR_W
GT_SWB_NIC4_TEMP_C
GT_SWB_NIC4_VOLT_V
GT_SWB_NIC4_CURR_A
GT_SWB_NIC4_PWR_W
GT_SWB_NIC5_TEMP_C
GT_SWB_NIC5_VOLT_V
GT_SWB_NIC5_CURR_A
GT_SWB_NIC5_PWR_W
GT_SWB_NIC6_TEMP_C
GT_SWB_NIC6_VOLT_V
GT_SWB_NIC6_CURR_A
GT_SWB_NIC6_PWR_W
GT_SWB_NIC7_TEMP_C
GT_SWB_NIC7_VOLT_V
GT_SWB_NIC7_CURR_A
GT_SWB_NIC7_PWR_W
GT_SWB_HSC_TEMP_C
GT_SWB_HSC_VOUT_V
GT_SWB_HSC_CURR_A
GT_SWB_HSC_PWR_W
GT_SWB_P12V_AUX_V
GT_SWB_P5V_AUX_V
GT_SWB_P3V3_AUX_V
GT_SWB_P1V2_AUX_V
GT_SWB_P3V3_V
GT_SWB_P1V8_PEX0_V
GT_SWB_P1V8_PEX1_V
GT_SWB_P1V8_PEX2_V
GT_SWB_P1V8_PEX3_V
GT_SWB_PEX0_VR_TEMP_C
GT_SWB_PEX0_P0V8_VOLT_V
GT_SWB_PEX0_P0V8_CURR_A
GT_SWB_PEX0_P0V8_PWR_W
GT_SWB_PEX0_P1V25_VOLT_V
GT_SWB_PEX0_P1V25_CURR_A
GT_SWB_PEX0_P1V25_PWR_W
GT_SWB_PEX1_VR_TEMP_C
GT_SWB_PEX1_P0V8_VOLT_V
GT_SWB_PEX1_P0V8_CURR_A
GT_SWB_PEX1_P0V8_PWR_W
GT_SWB_PEX1_P1V25_VOLT_V
GT_SWB_PEX1_P1V25_CURR_A
GT_SWB_PEX1_P1V25_PWR_W
GT_SWB_PEX2_VR_TEMP_C

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GT_SWB_PEX2_P0V8_VOLT_V
GT_SWB_PEX2_P0V8_CURR_A
GT_SWB_PEX2_P0V8_PWR_W
GT_SWB_PEX2_P1V25_VOLT_V
GT_SWB_PEX2_P1V25_CURR_A
GT_SWB_PEX2_P1V25_PWR_W
GT_SWB_PEX3_VR_TEMP_C
GT_SWB_PEX3_P0V8_VOLT_V
GT_SWB_PEX3_P0V8_CURR_A
GT_SWB_PEX3_P0V8_PWR_W
GT_SWB_PEX3_P1V25_VOLT_V
GT_SWB_PEX3_P1V25_CURR_A
GT_SWB_PEX3_P1V25_PWR_W
GT_SWB_PEX_P1V8_VOLT_V
GT_SWB_PEX_P1V8_CURR_A
GT_SWB_PEX_P1V8_PWR_W
GT_SWB_PEX0_TEMP_C
GT_SWB_PEX1_TEMP_C
GT_SWB_PEX2_TEMP_C
GT_SWB_PEX3_TEMP_C
GT_SWB_SYSTEM_INLET_TEMP_C
GT_SWB_OUTLET_TEMP_L1_C
GT_SWB_OUTLET_TEMP_L2_C
GT_SWB_OUTLET_TEMP_R1_C
GT_SWB_OUTLET_TEMP_R2_C
GT_SWB_E1S_0_TEMP_C
GT_SWB_E1S_0_VOLT_V
GT_SWB_E1S_0_CURR_A
GT_SWB_E1S_0_PWR_W
GT_SWB_E1S_1_TEMP_C
GT_SWB_E1S_1_VOLT_V
GT_SWB_E1S_1_CURR_A
GT_SWB_E1S_1_PWR_W
GT_SWB_E1S_2_TEMP_C
GT_SWB_E1S_2_VOLT_V
GT_SWB_E1S_2_CURR_A
GT_SWB_E1S_2_PWR_W
GT_SWB_E1S_3_TEMP_C
GT_SWB_E1S_3_VOLT_V
GT_SWB_E1S_3_CURR_A
GT_SWB_E1S_3_PWR_W
GT_SWB_E1S_4_TEMP_C
GT_SWB_E1S_4_VOLT_V
GT_SWB_E1S_4_CURR_A
GT_SWB_E1S_4_PWR_W
GT_SWB_E1S_5_TEMP_C
GT_SWB_E1S_5_VOLT_V
GT_SWB_E1S_5_CURR_A
GT_SWB_E1S_5_PWR_W

GT_SWB_E1S_6_TEMP_C
GT_SWB_E1S_6_VOLT_V
GT_SWB_E1S_6_CURR_A
GT_SWB_E1S_6_PWR_W
GT_SWB_E1S_7_TEMP_C
GT_SWB_E1S_7_VOLT_V
GT_SWB_E1S_7_CURR_A
GT_SWB_E1S_7_PWR_W
GT_SWB_E1S_8_TEMP_C
GT_SWB_E1S_8_VOLT_V
GT_SWB_E1S_8_CURR_A
GT_SWB_E1S_8_PWR_W
GT_SWB_E1S_9_TEMP_C
GT_SWB_E1S_9_VOLT_V
GT_SWB_E1S_9_CURR_A
GT_SWB_E1S_9_PWR_W
GT_SWB_E1S_10_TEMP_C
GT_SWB_E1S_10_VOLT_V
GT_SWB_E1S_10_CURR_A
GT_SWB_E1S_10_PWR_W
GT_SWB_E1S_11_TEMP_C
GT_SWB_E1S_11_VOLT_V
GT_SWB_E1S_11_CURR_A
GT_SWB_E1S_11_PWR_W
GT_SWB_E1S_12_TEMP_C
GT_SWB_E1S_12_VOLT_V
GT_SWB_E1S_12_CURR_A
GT_SWB_E1S_12_PWR_W
GT_SWB_E1S_13_TEMP_C
GT_SWB_E1S_13_VOLT_V
GT_SWB_E1S_13_CURR_A
GT_SWB_E1S_13_PWR_W
GT_SWB_E1S_14_TEMP_C
GT_SWB_E1S_14_VOLT_V
GT_SWB_E1S_14_CURR_A
GT_SWB_E1S_14_PWR_W
GT_SWB_E1S_15_TEMP_C
GT_SWB_E1S_15_VOLT_V
GT_SWB_E1S_15_CURR_A
GT_SWB_E1S_15_PWR_W

14. Security

The Switch Tray uses secure boot and signed firmware on all PEX switches.

Appendix A - Checklist for IC approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

Item	Status	Link to detailed explanation
Has this contribution been presented to an OCP Project group during a project call or engineering workshop?	Yes or No	If “No”, please state the reason.
Approval by Project Leads	Yes or No	If “No”, please state the reason.
Is this contribution entered into the OCP Contribution Portal?	Yes or No	If “No”, please state the reason.
Was it approved in the OCP Contribution Portal?	Yes or No	If “No”, please state the reason.