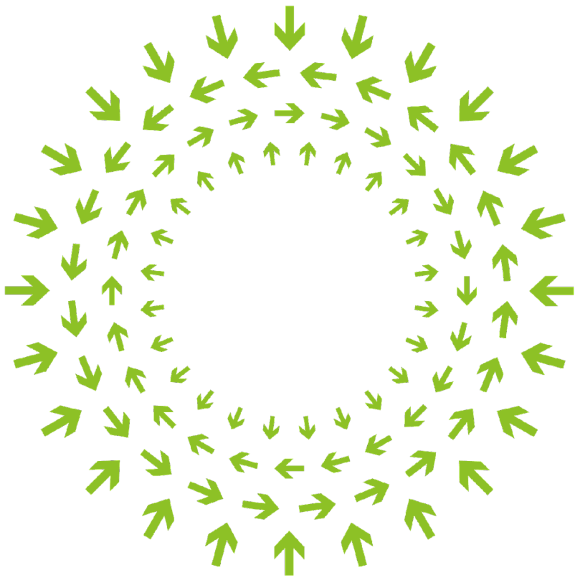

OPEN Compute Project

Grand Teton Intel-Based CPU Tray Specification

Version 1.0

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2. Compliance with OCP Tenets

2.1 Openness

The Grand Teton platform design exemplifies openness by defining a platform that can support multiple use cases and workloads. This includes modular swappable trays for all system components and open-source BMC/BIC firmware, which allows users to optimize the system for their own needs.

2.2 Efficiency

Compared to past generations, the Grand Teton platform offers efficiency gains across the power and thermal systems by upgrading to the 51V ORv3 rack architecture. There are also efficiency gains through the system architecture, which utilizes trays that can be swapped to improve performance or optimize the hardware for evolving workloads.

2.3 Impact

The Grand Teton platform represents a number of firsts in large-scale AI infrastructure, including next-gen CPUs, PCIe Gen5, DDR5, and NVIDIA HGX. These technologies, along with the flexibility of the system architecture, support high-performance workloads that can scale out and utilize other OCP solutions, such as ORv3, DC-SCM, OCP NIC, OCP E1.S, Wedge400, and Minipack2.

2.4 Scale

The Grand Teton platform utilizes the latest features to support large-scale deployment, including tool-less FRUs, extensive remote management, error reporting, future upgradeability, and on-premises serviceability enhancements. Offering flexible scale capabilities, Grand Teton can be used as a single system up through hyper-scale deployment. The system also uses OpenBMC and OpenBIC open-source software.

2.5 Sustainability

The Grand Teton platform follows environmental compliance standards and best practices. The modular design allows for more targeted repairs, reducing waste and allowing the system to be used across multiple generations. The platform is fully compliant with major environmental standards, such as RoHS 2 and REACH. The system fans are optimized to sufficiently cool components while minimizing power consumption.

3. Change Log

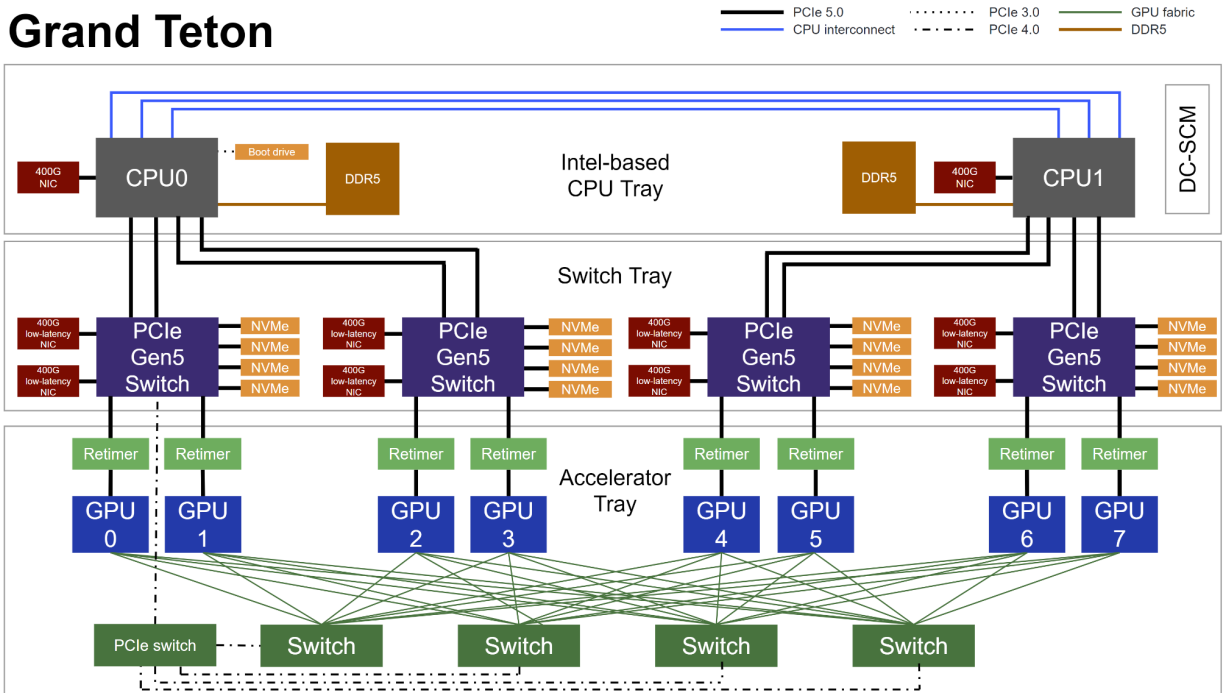
Date	Version #	Author	Description
07AUG2023	0.1	Jeremy Baumgartner Matt Bowman	Initial draft
23AUG2023	0.9	Jeremy Baumgartner Matt Bowman	Added content to several sections
05SEPT2023	1.0	Jeremy Baumgartner Matt Bowman	Added content

4. Scope

This document defines the Hardware Product Specification for the Grand Teton (GT) Intel-based CPU Tray, which is used in the Grand Teton platform.

5. Overview

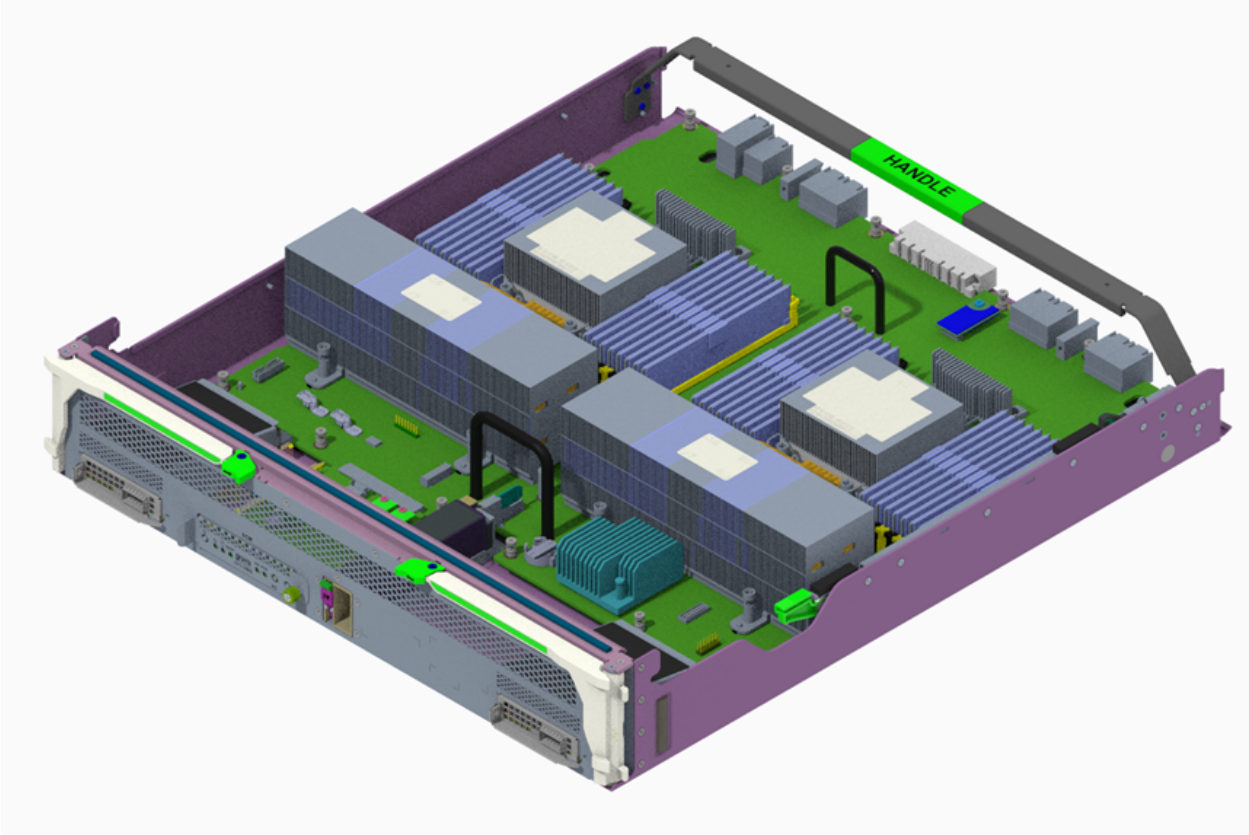
5.1 Platform Block Diagram



High-level block diagram of an Intel-based Grand Teton system

5.2 Intel-based CPU Tray

The Grand Teton Intel-based CPU Tray is a 2-socket CPU motherboard that supports 4th Generation Intel Xeon Scalable Processors, code named “Sapphire Rapids”, with a TDP up to 350W.



Overall view of the Intel-based CPU Tray

The CPU Tray is designed to be installed in a Grand Teton platform chassis, along with a Switch Tray, Accelerator Tray, and other components such as power distribution boards, fans, and cables.

The CPU Tray contains multiple field-removable units (FRUs), including two OCP NICs, two boot drives, and one SCM with BMC.

The boot drive could either be an internal M.2 SSD or a front-accessible E1.S SSD. The E1.S drive and NICs are electrically safe to hot insert and remove from a powered system.

Power to the CPU Tray comes from the Vertical Power Distribution Board (VPDB) via power cables.

High-speed data cables handle interconnection between the CPU Tray and the Switch tray.

5.3 Base Specification

This specification is a subset of the *Grand Teton Platform Specification*.

6. Environmental Regulatory Compliance And Requirements

6.1 Environmental

- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: +5°C to +35°C
- Operating and Storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-ratings: 6000 feet

6.2 Regulatory Compliance

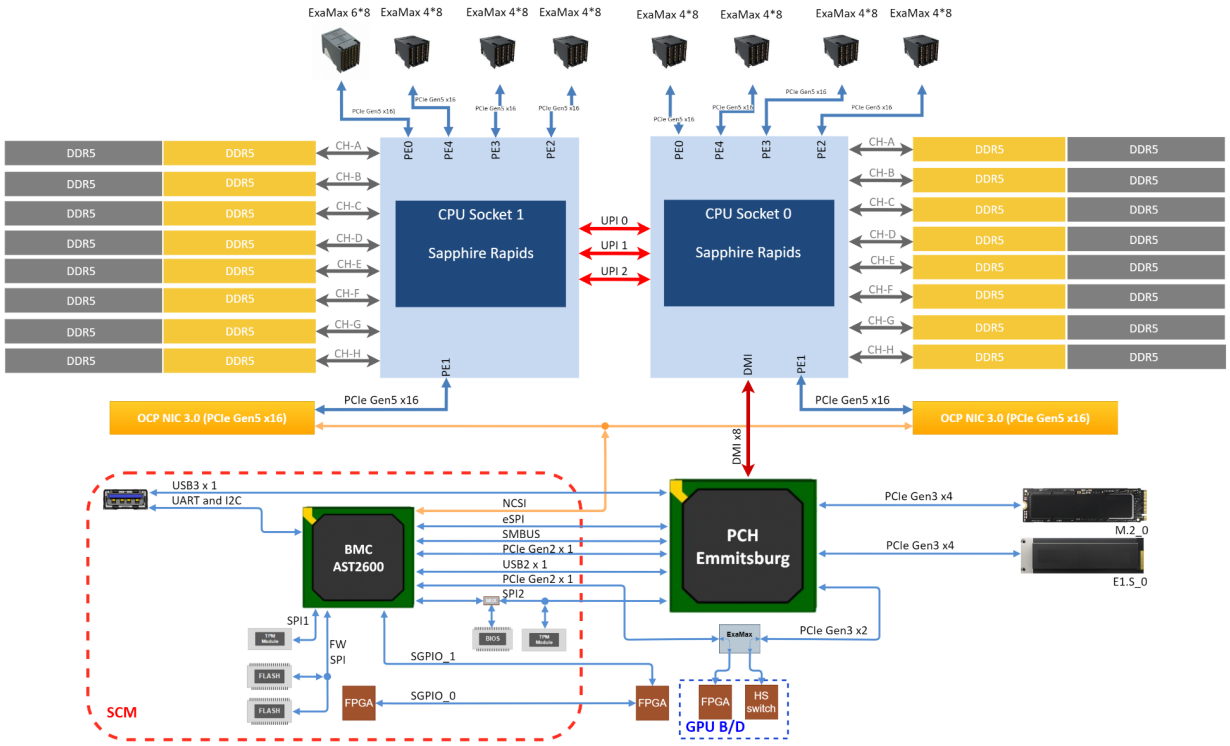
- CE and NRTL (UL listed) marks in accordance with the listing and surveillance requirements of the NRTL
- EU Low Voltage Directive (2014/35/EC)
- EU EMC Directive (2014/30/EC)
- EN55032/CISPR32, Class A criteria
- EN55035/CISPR35
- CISPR16
- ANSI C63.4
- EN61000-4-2
- EN61000-4-3
- EN61000-4-4
- EN61000-4-5
- EN61000-4-6
- EN61000-4-11
- FCC CFR47 Part 15, Subpart B, Class A criteria
- RoHS Directive (2015/863/EU)
- WEEE Directive (2012/19/EU)
- REACH regulation (EC 1097/2006)
- US EPA 40 CFR751
- IEC/EN 62368-1, hazard-based performance standard for audio video, and ITE

7. Physical Specifications

7.1 CPU Board

The Grand Teton Intel-based CPU motherboard includes the following features:

- 2 sockets for 4th Generation Intel Xeon Scalable Processors, code named “Sapphire Rapids”, with a TDP up to 350W
- 56 cores per CPU (up to 112 threads per CPU with Intel Hyper-Threading Technology)
- 3 full-width 24-lane Intel UPI links up to 16 GT/s/lane (UPI0/1/2)
- 2TB DDR5 memory (8 channels per CPU, 2DPC, 32 DIMMs total, 64GB per DIMM)



Overall block diagram of the Intel CPU Tray

The PCIe 5.0 interfaces are mapped as follows:

- Each CPU has one PCIe 5.0 x16 channel supporting one OCP NIC 3.0 (PE1)
- Each CPU has four PCIe 5.0 x16 channels routed to ExaMax high speed connectors (PE0/2/3/4)

Connectivity to the system is provided through eight ExaMax blind mate connectors at the interior cable backplane at the rear of the chassis. ExaMax connectors are arranged in pairs such that eight connectors mate with four cables.

- Seven (7) ExaMax 4x8 connectors
    - 32 high speed pairs for one PCIe 5.0 x16 interface
    - 8 GPIO for status, control and OOB management
- One (1) ExaMax 6x8 connector includes all ExaMax 4x8 signals plus:
    - BMC USB 2.0 Interface
        - 1 high speed pair for USB 2.0
    - BMC RC PCIe interface
        - 2 high speed pairs for one PCIe 2.0 x1 interface
        - 1 high speed pair for reference clock
        - Independent PERST is contained within GPIO
    - PCH RC PCIe interface
        - 4 high speeds pairs for one PCIe 3.0 x2 interface
        - Uses primary clock and reset domains
    - Primary PCIe reference clocks
        - 3 high speed pairs for PCIe reference clocking
        - Clocks are copies from the same fanout buffer
    - I2C management
        - 2 high speed pairs for two I2C interfaces to BMC
- One (1) power cable to the platform Vertical Power Distribution Board (VPDB)
    - 12V for main power rails
    - Status and control signals

A secure control module (SCM) is used on the CPU Tray to enable out-of-band (OOB) access through a BMC. For details on the SCM, refer to the *Grand Teton Platform Specification*.

The SCM, OCP NICs, E1.S, and CPU Tray are hot-insertable and hot-removable.

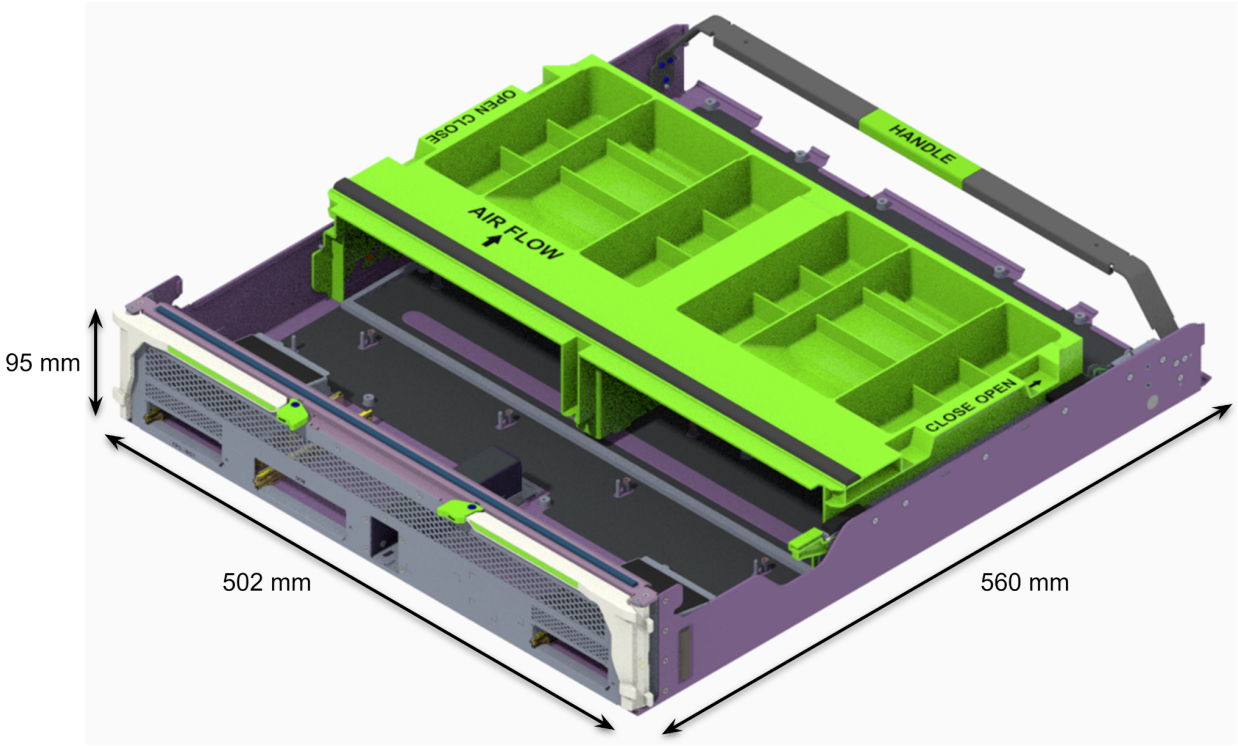
7.2 PCB Stackup

Layer#	Material	Description	Copper Weight (oz)	Thickness (mil)	Tolerance (mil)	Glass Fabric	Er
		Soldermask		0.60			3.8
1		TOP	0.5+plating	1.95			
	EM-890K	PP		2.70	±0.709	1078x1	2.92
2		GND	0.5 (VL411)	0.65			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
3		IN1	1 (VL411)	1.30			
	EM-890K	PP		5.00	±0.984	1078x2	2.94
4		GND1	0.5 (VL411)	0.65			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
5		IN2	1 (VL411)	1.30			
	EM-890K	PP		5.00	±0.984	1078x2	2.94
6		GND2	0.5 (VL411)	0.65			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
7		IN3	1 (VL411)	1.30			
	EM-890K	PP		5.00	±0.984	1078x2	2.94
8		GND3	1 (VL411)	1.30			
	EM-890K	CORE		3.50	±0.709	1078x1	2.93
9		VCC	2 (RTF)	2.60			
	EM-890K	PP		4.00	±0.709	1080x2	2.93
10		VCC1	2 (RTF)	2.60			
	EM-890K	CORE		3.50	±0.709	1078x1	2.93
11		GND4	1 (VL411)	1.30			
	EM-890K	PP		5.00	±0.984	1078x2	2.94
12		IN4	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
13		GND5	0.5 (VL411)	0.65			
	EM-890K	PP		5.00	±0.984	1078x2	2.94
14		IN5	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
15		GND6	0.5 (VL411)	0.65			
	EM-890K	PP		5.00	±0.984	1078x2	2.94
16		IN6	1 (VL411)	1.30			
	EM-890K	CORE		4.00	±0.709	1078x1	2.93
17		GND7	0.5 (VL411)	0.65			
	EM-890K	PP		2.70	±0.709	1078x1	2.92
18		BOTTOM	0.5+plating	1.95			
		Soldermask		0.60			3.8
			Total	**95.00**	**±10%**		

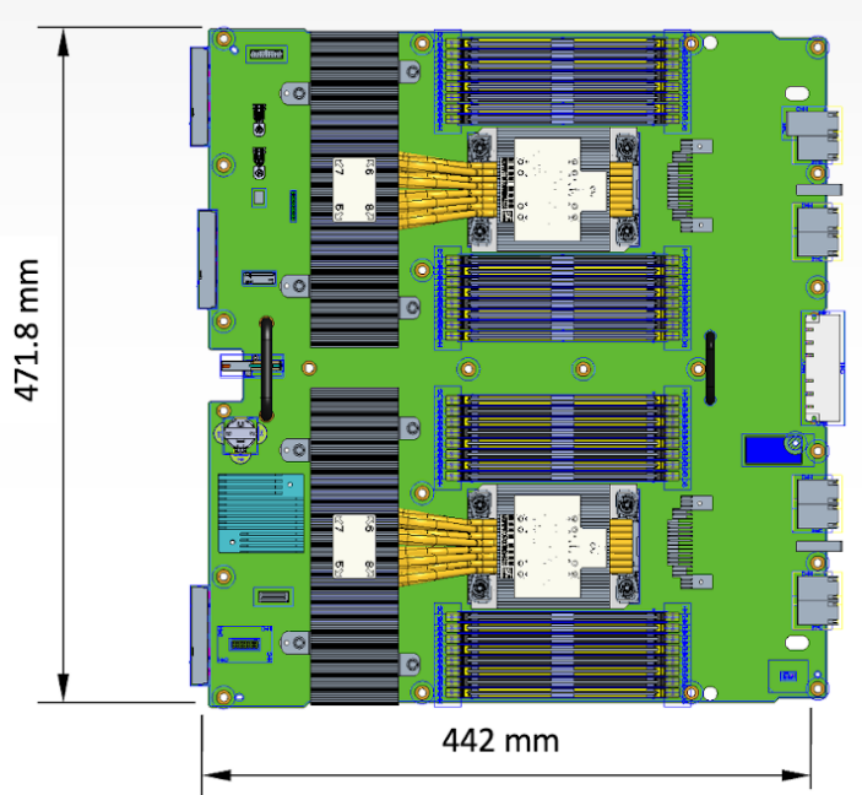
7.3 Mechanical

The CPU Tray includes two lever arms at the front top of the tray for installation and removal leverage. The tray also includes a stop latch that prevents inadvertent removal of the entire tray until the technician is ready.

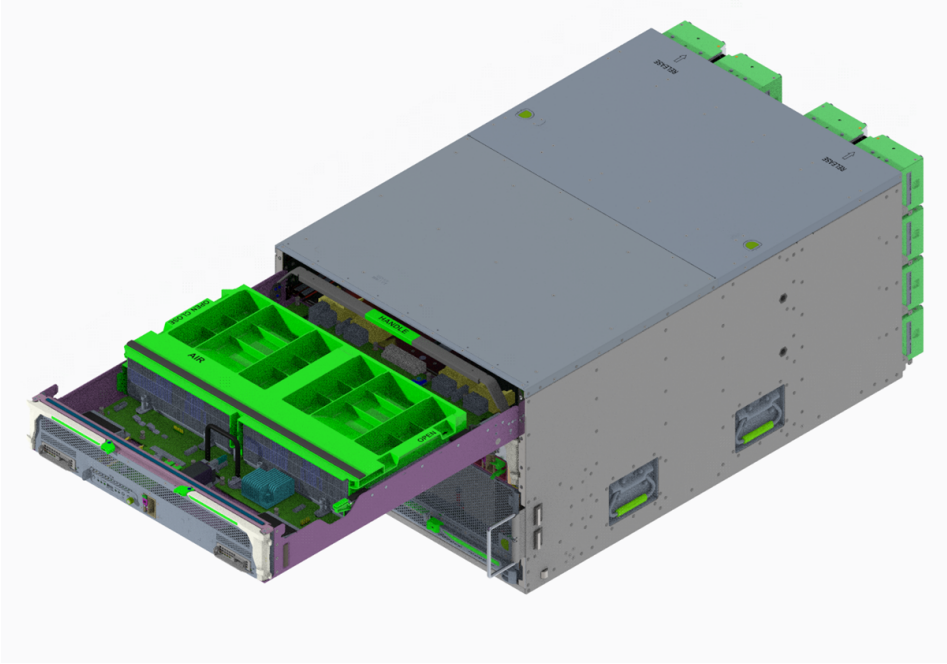
The tray and included FRUs all feature tool-less removable and green touchpoints.



Overall dimensions of the CPU Tray with air baffles installed



Overall dimensions of the Intel-based CPU board



CPU Tray partially removed from the chassis

The CPU Tray weighs approximately 12.1 kg (26.6 lb) overall.

7.4 Rack Compatibility

The CPU Tray is intended to be used in a Grand Teton platform chassis installed in an Open Rack V3 (ORv3) compatible rack.

8. Electrical Requirements

The CPU Tray uses the 12VDC rail from the Vertical Power Distribution Board (VPDB). The VPDB converts 51VDC from the ORv3 bus bar down to 12VDC and is capable of powering 6kW. The 12V provided to the CPU Tray should have a tolerance of +/- 10%.

9. Thermal Design Requirements

9.1 Thermal Architecture

Grand Teton is an 8OU system with 3 trays in parallel: CPU Tray, Switch Tray and Accelerator Tray. Airflow to all 3 trays is delivered by a fan array at the rear side of the chassis, with a shared plenum. All components are air-cooled, using passive heatsinks where applicable.

9.2 System Thermal Specification

	Normal Operation	**Corner Case**	**Remain Power on**
Inlet Temperature	Up to 30°C	Up to 35°C	Up to 45°C
Altitude (no inlet temp deration)	Up to 6000 ft	Up to 6000 ft	Up to 6000 ft
Cold/Hot Aisle Δp	Within +/- 0.005 InH2O	Within +/- 0.1 InH2O	Within +/- 0.1 InH2O
Relative Humidity	10% ~ 90%	10% ~ 90%	10% ~ 90%
Fan Status	All Healthy	Single fan/rotor failure	Single fan/rotor failure
Air side ΔT (CFM/W)	More than 12.5°C (22°F) Less than 0.145 CFM/W at sea level [Max loading condition only]	NA	NA
Thermal Throttling	Not allowed	Not allowed	Allowed

Minimum Thermal Margin	7% of component temperature spec	NA	NA
Fan Power Ratio	Below 5% of system total power [Max loading condition only]	NA	NA

9.3 Fan Configuration

Grand Teton uses sixteen (16) 80x56mm counter rotating fan modules. A shared fan wall is used for all trays, sharing the same PWM control algorithm. Single rotor failure is supported in corner cases.

9.4 Fan Control Target

Under normal operation conditions, minimum margin (critical component) shall be at least 7% of component temperature spec, while fan power consumption shall be less than 5% of system total power (account for max loading power only).

9.5 Thermal Sensors

The BMC monitors all applicable temperature, power, and fan speed sensors, and adopts selective temperature readings for fan speed control algorithms when applicable. The maximum allowable tolerance of the inlet temperature sensor is ±2°C. The maximum allowable tolerance of other thermal sensors is ±5°C.

9.6 Fan Control Algorithm

Look up tables are applied to the inlet temperature sensor, and temperature sensors of all components with thermal risk under all possible operation conditions, if the fans operate at the minimum duty specified (20%). PID control tables should be applied to temperature sensors of all components that may be thermally critical under all possible operation conditions.

9.7 Special Conditions

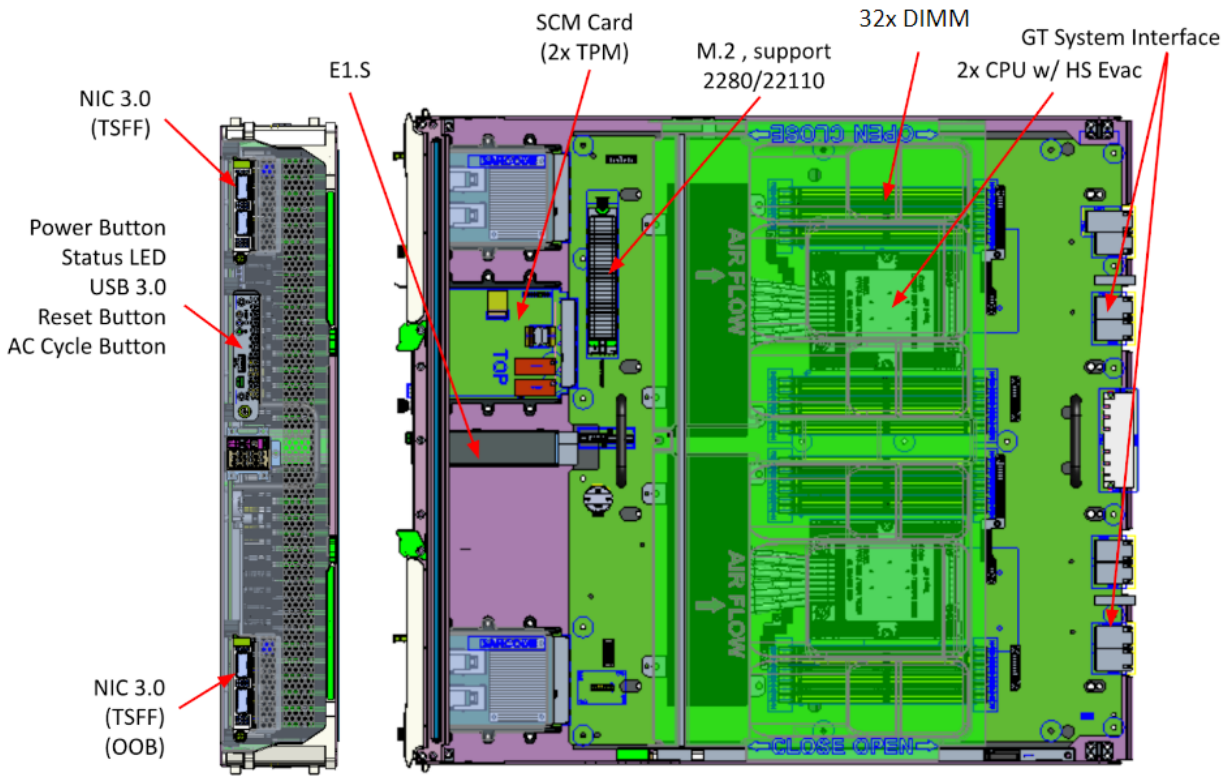
For devices/components/parts that do not have built-in temperature sensors or cannot be included in fan speed control, their thermal solution design should enable the inlet-temperature based FSC to ensure their cooling at idling/low loading conditions. The PID control FSCs should ensure their cooling at heavy load conditions.

Special fan modes shall be designed for the following scenarios:

- AC Cycle
- DC Power Off/Cycle
- Single rotor Failure

- Fan Board Failure
- Sensor failure or exceed LCR/UCR limits

10. Interfaces

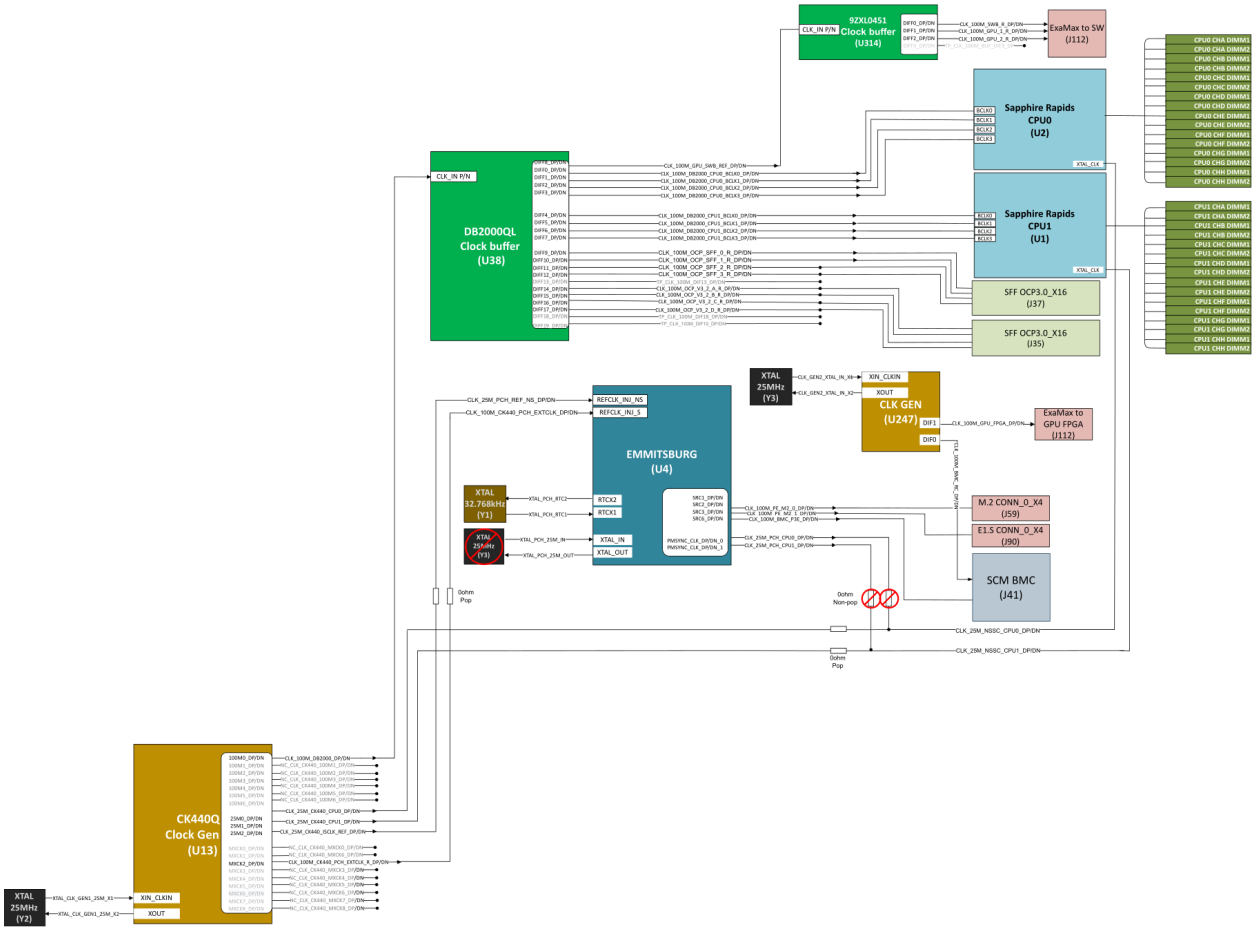


Overview of Intel CPU Tray interfaces and components

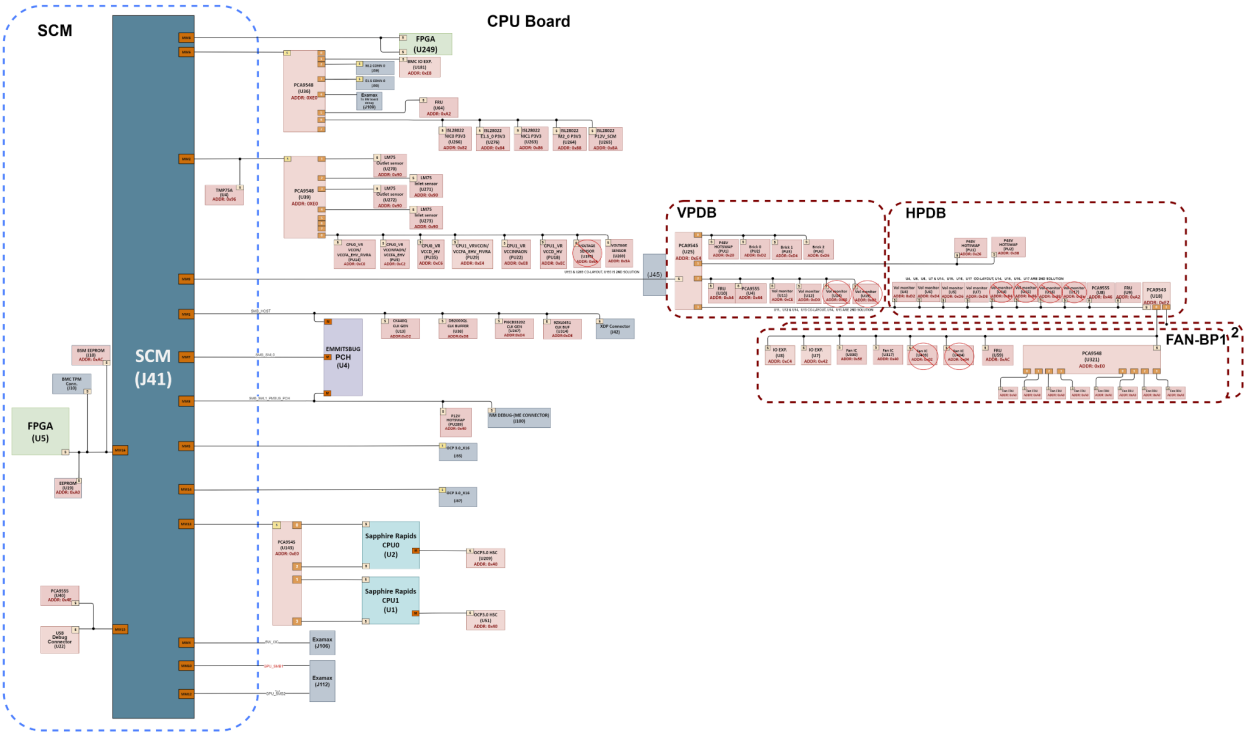
10.1 Signal List

The CPU Tray includes the following signals:

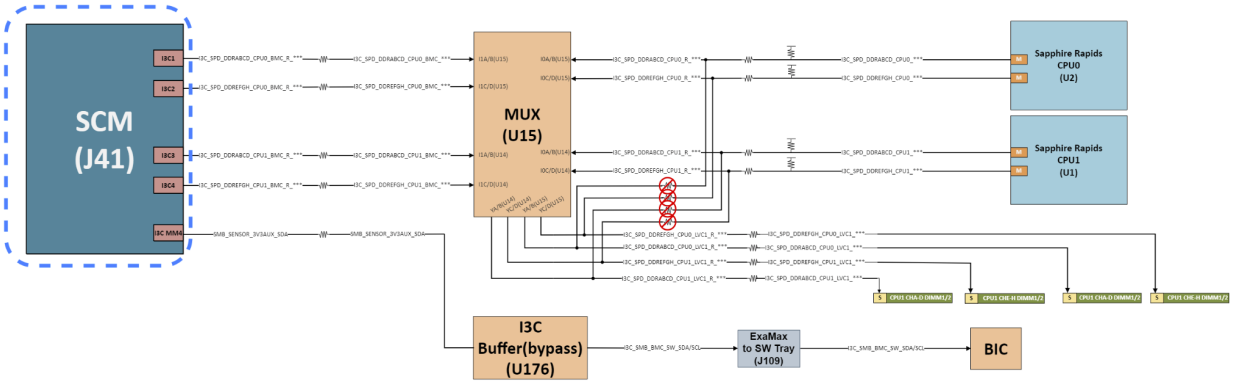
- High-speed signals
  - PCIe 5.0 between the CPU, NIC, SCM, SSD, and backplane connectors
  - Intel UPI between the CPUs
  - Clocks
- Low-speed signals
  - I2C/I3C/SPI for management, sensors, I/O expanders, and other components
  - USB for debug interface
  - GPIO
  - JTAG



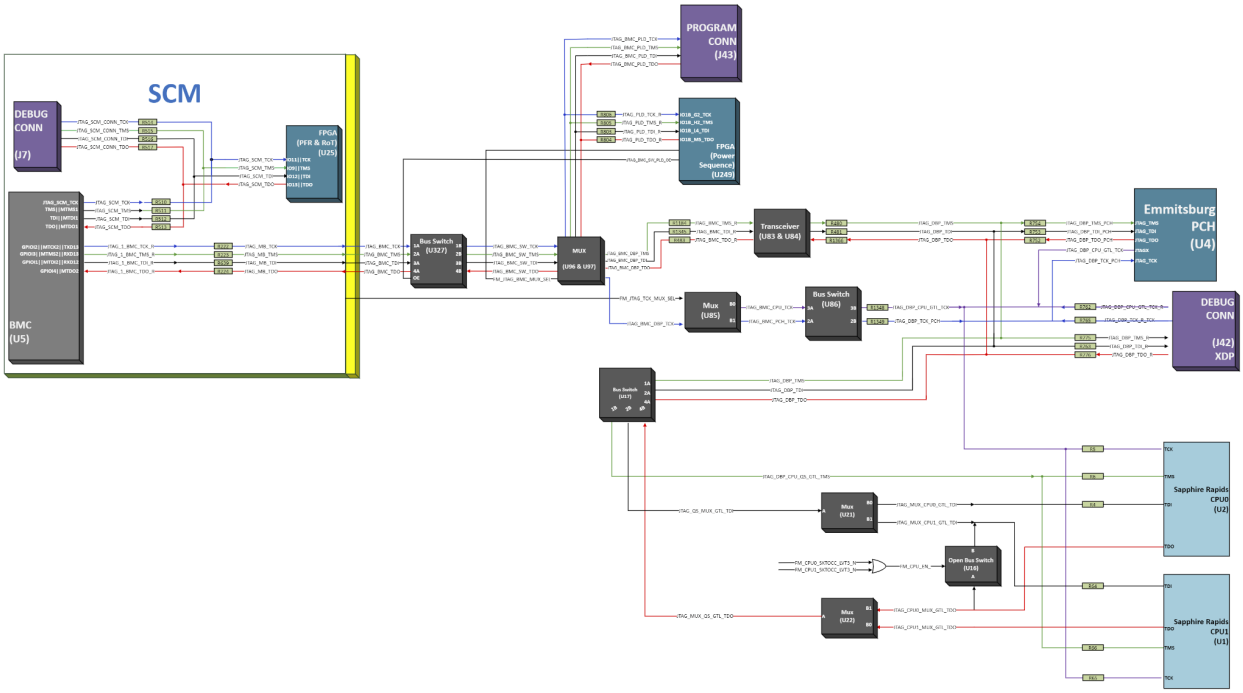
Block diagram of CPU Tray clock signals



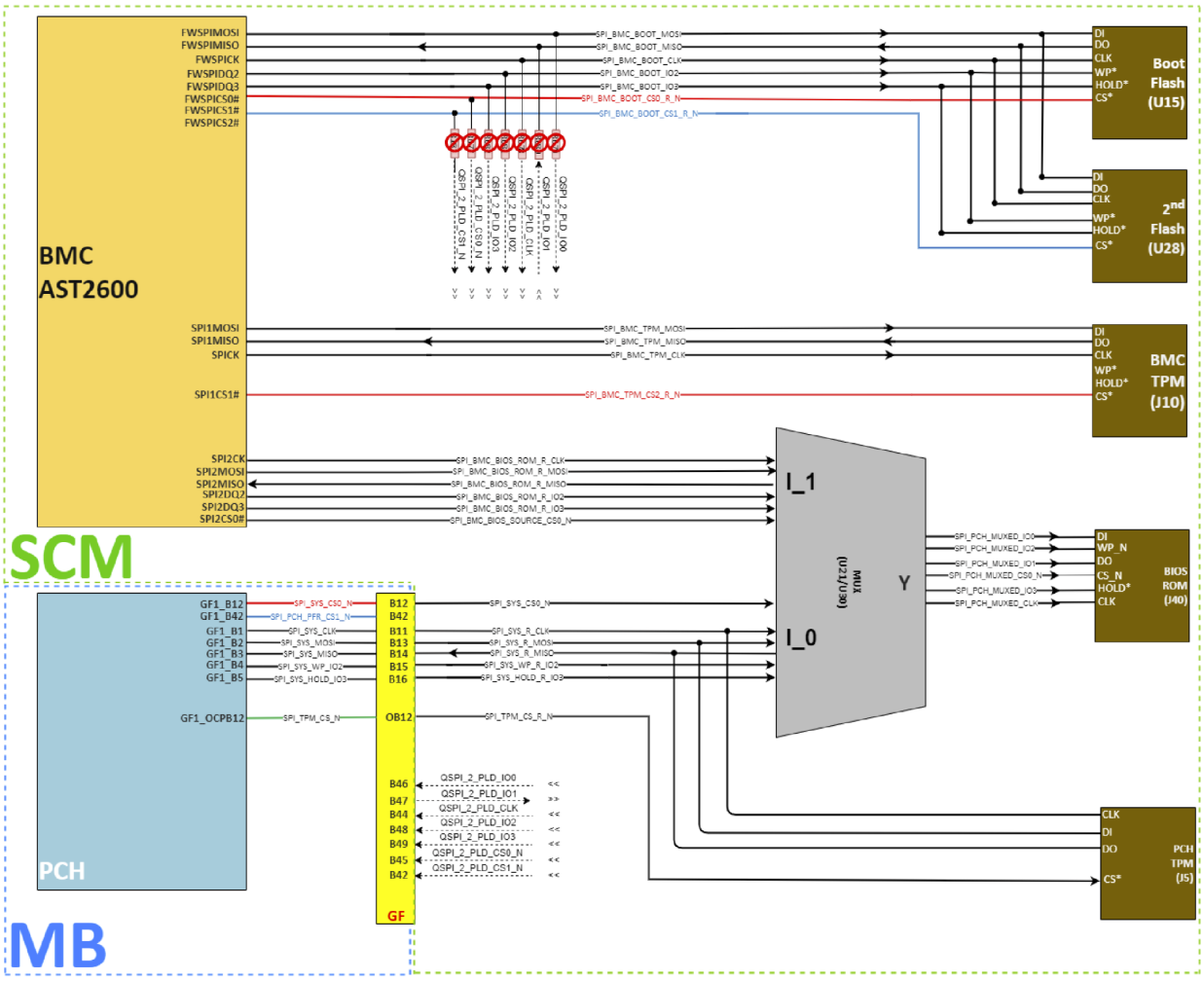
Block diagram of CPU Tray I2C signals



Block diagram of CPU Tray I3C signals



Block diagram of CPU Tray JTAG signals

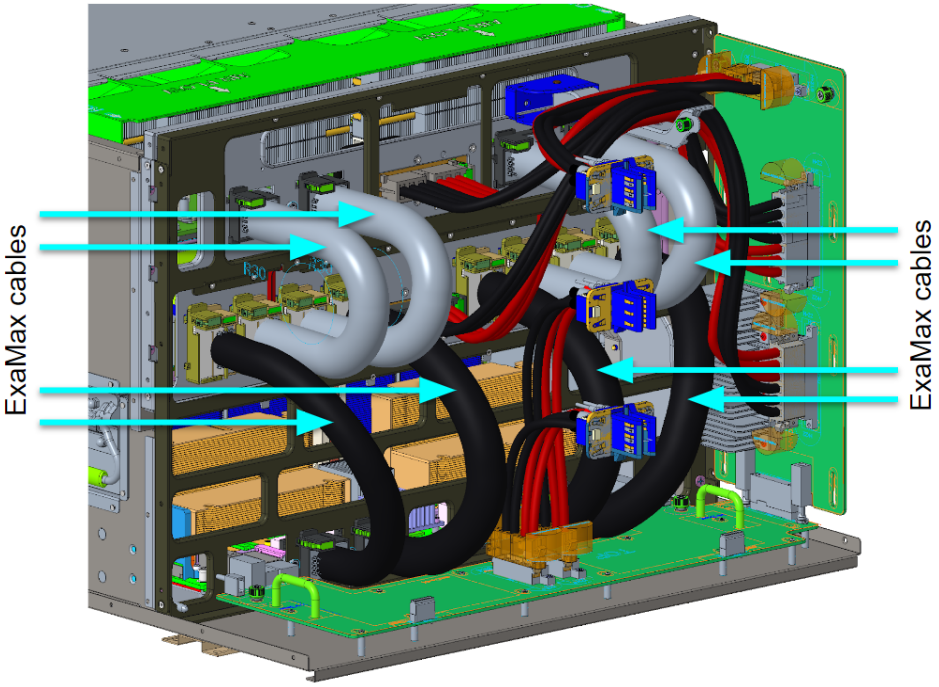


Block diagram of CPU Tray JTAG signals

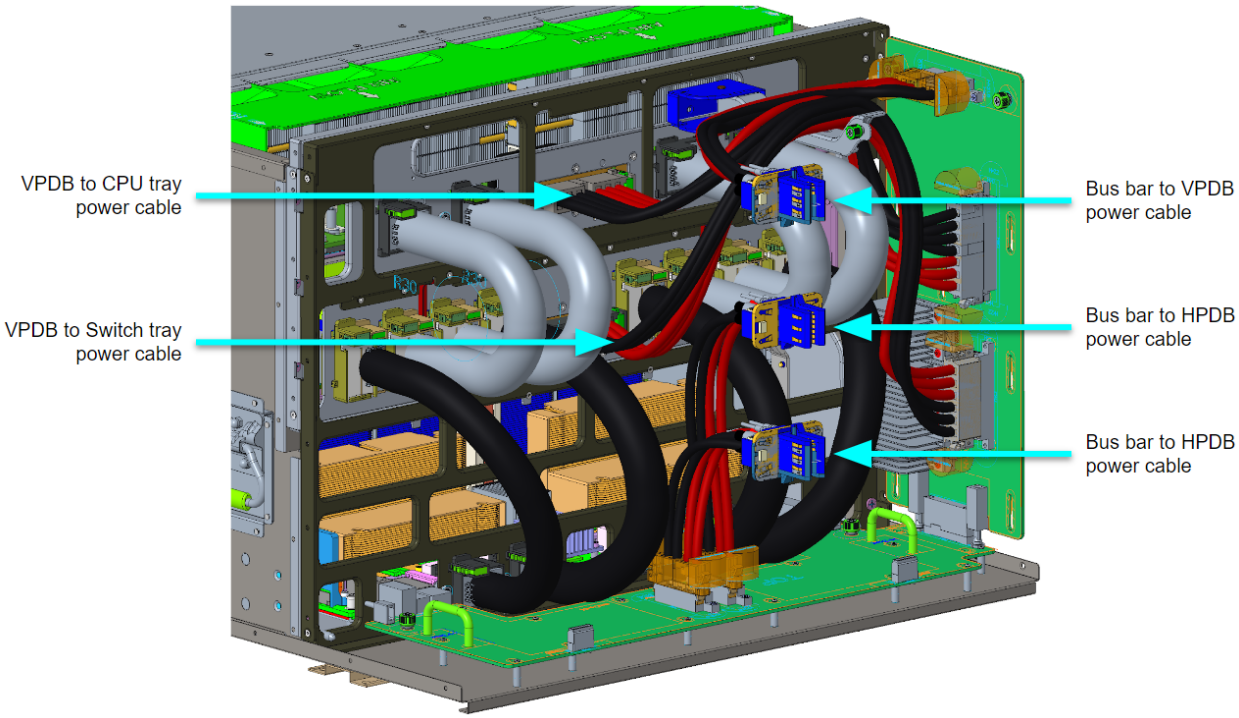
10.2 Cable Backplane

The CPU Tray slides into the chassis to blind mate into the ExaMax and power cable backplane at the rear interior of the chassis. These connections include 12VDC power from the VPDB, PCIe 5.0 to the Switch tray, and management signals routed throughout the chassis. All ExaMax cables include a presence detect signal, which is read by an I/O expander under SCM control.

As part of system-level power sequencing, power good signals from the Switch Tray and Accelerator Tray are required for the CPU Tray to fully boot. However, as a debug feature, the CPU Tray has a control switch to enable boot without these other system components.

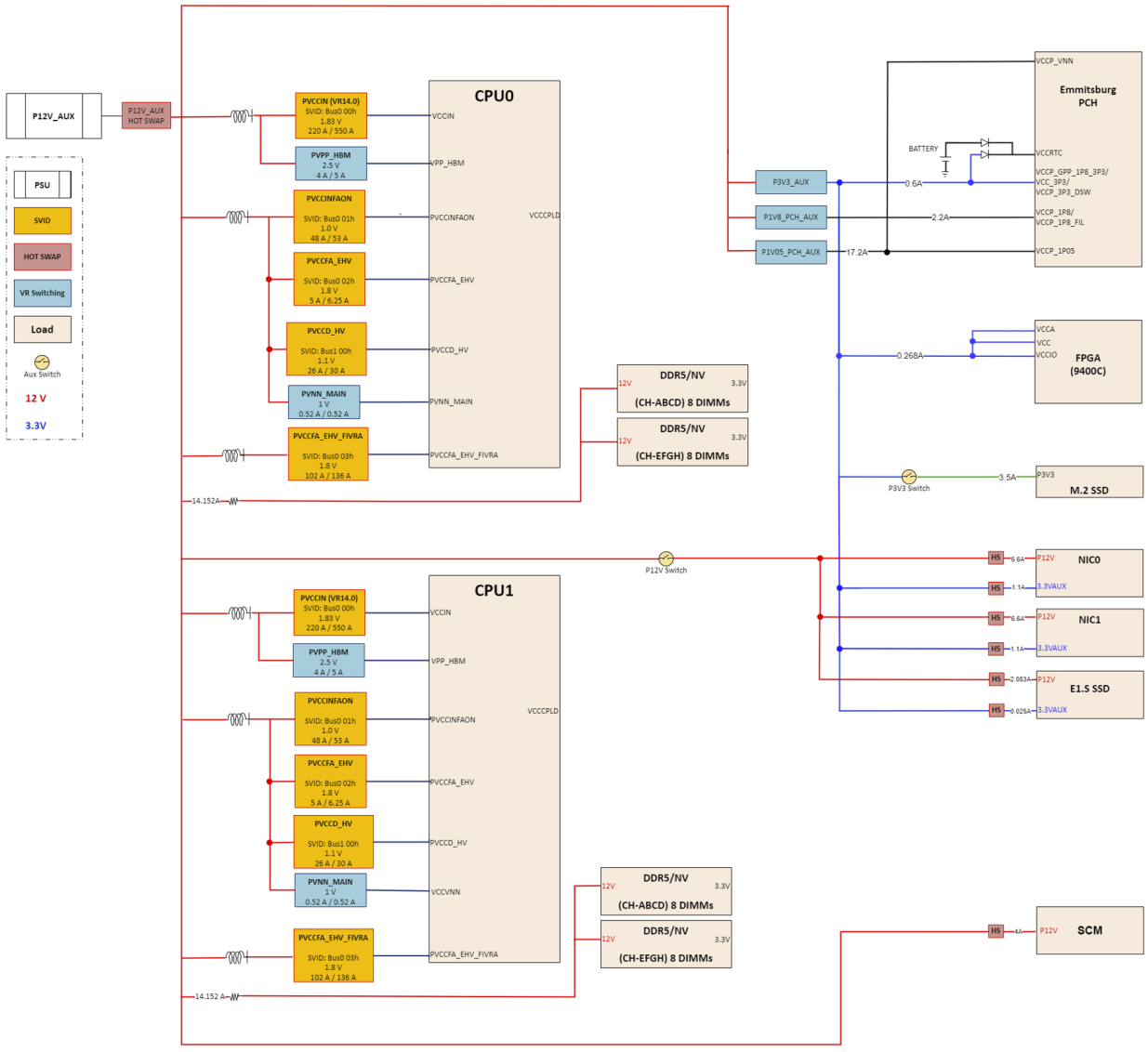


Overall diagram of the ExaMax cable backplane



Overall diagram of the power cables backplane

11. Onboard Power System



Block diagram of the CPU board power system

The VPDB supplies the CPU Tray with 12VDC. The CPU board has a 12V hot swap controller to support tray insertion and removal from a live system. Details of all of the hotswap circuits are below. NIC0 and NIC1 have the same hotswap configuration details.

- 12V hotswap
    - Overcurrent trip: 240A
    - Overvoltage trip: 14.33V

    - Undervoltage trip: 10.09V
- OCP NIC 12V hotswap
    - Overcurrent trip point: 8.58A
    - Overvoltage trip: 14.91V
    - Undervoltage trip: 10.17V
- OCP NIC 3.3V hotswap
    - Overcurrent trip point: 1.43A
    - Overvoltage trip: 3.89V
    - Undervoltage trip: 2.63V
- E1.S 12V hotswap
    - Overcurrent trip point: 2.71A
    - Overvoltage trip: 14.91V
    - Undervoltage trip: 10.17V
- E1.S 3.3V hotswap
    - Overcurrent trip point: 0.75A
    - Overvoltage trip: 3.89V
    - Undervoltage trip: 2.63V

12. System Firmware

The Grand Teton system uses the following open source firmware:

- OpenBMC, an open-source firmware stack for the BMC on the SCM: https://github.com/facebook/openbmc/tree/helium/meta-facebook/meta-grandteton
- OpenBIC, an open-source firmware for the BIC in the Switch tray https://github.com/facebook/OpenBIC/tree/main/meta-facebook/gt-cc

The CPU Tray includes the following programmable parts:

- CPU core voltage regulators
- Main 12V hotswap controller
- Management CPLD
- CPU board FRU EEPROM
- BIOS (physically on the SCM)
- Expansion CPLD (physically on the SCM)
- SCM FRU EEPROM

13. Hardware Management

13.1 Out-Of-Band Management

The CPU Tray has a dedicated 400G NIC for out-of-band (OOB) management of the system. OOB access is always online as long as standby power is provided. The NIC attaches to the CPU Tray at slot NIC0 and is OCP NIC 3.0 compliant.

The BMC can update NIC firmware through OOB to ensure NIC update is available in case the OS is not accessible and in-band update fails.

13.2 BMC

This system uses an ASPEED AST2600 BMC with one 8Gb x16 DDR4 SDRAM and 65MB flash for various platform management services. The BMC interfaces with hardware, BIOS, and host firmware.

The BMC resides on the SCM board, which attaches to the CPU Tray and follows the DC-SCM v1.0 specification (with board pinout exceptions, see the *Grand Teton Platform Specification*).

The BMC is a standalone system in parallel to the host. The health status of the host system does not affect the normal operation and network connectivity of BMC.

The BMC is remote upgradeable either by in-band across the network or out-of-band through the NIC.

13.3 Remote Upgradeability

The system is capable of remotely upgrading the VRs, CPLDs, BIC, switches, and FRU EEPROMs. The BMC can access each device, update code from BMC to the device, and verify the code.

The BMC is capable of recovering all CPLD and BIC in the system from image corruption or an accidental erase. The BMC does not rely on proper operation of the BIC or CPLD for booting or to be accessible remotely.

13.4 Sensors

BMC has access to all analog sensors directly or through host management. Below is a table of all sensors:

Sensor Name	Sensor Name
GT_MB_E1S_P3V3_VOLT_V	GT_MB_CPU1_DIMM_B3_PWR_W
GT_MB_E1S_P12V_VOLT_V	GT_MB_CPU1_DIMM_D3_PWR_W

GT_MB_E1S_P12V_CURR_A	GT_MB_CPU1_DIMM_B4_PWR_W
GT_MB_E1S_P12V_PWR_W	GT_MB_CPU1_DIMM_D4_PWR_W
GT_MB_E1S_TEMP_C	GT_MB_CPU1_DIMM_B5_PWR_W
GT_MB_POWER_FAIL	GT_MB_CPU1_DIMM_D5_PWR_W
GT_MB_PROCESSOR_FAIL	GT_MB_CPU1_DIMM_B6_PWR_W
GT_MB_HSC_VOLT_V	GT_MB_CPU1_DIMM_D6_PWR_W
GT_MB_HSC_CURR_A	GT_MB_CPU1_DIMM_B7_PWR_W
GT_MB_HSC_PWR_W	GT_NIC0_P3V3_VOLT_V
GT_MB_HSC_TEMP_C	GT_NIC0_P12V_VOLT_V
GT_MB_HSC_PEAK_PIN_W	GT_NIC0_P12V_CURR_A
GT_MB_INLET_R_TEMP_C	GT_NIC0_P12V_PWR_W
GT_MB_INLET_L_TEMP_C	GT_NIC0_TEMP_C
GT_MB_OUTLET_R_TEMP_C	GT_NIC1_P3V3_VOLT_V
GT_MB_OUTLET_L_TEMP_C	GT_NIC1_P12_VOLT_V
GT_MB_CPU0_TEMP_C	GT_NIC1_P12_CURR_A
GT_MB_CPU1_TEMP_C	GT_NIC1_P12_PWR_W
GT_MB_CPU0_THERM_MARGIN	GT_NIC1_TEMP_C
GT_MB_CPU1_THERM_MARGIN	GT_PDBV_HSC0_VIN
GT_MB_CPU0_TJMAX	GT_PDBV_HSC0_CURR_A
GT_MB_CPU1_TJMAX	GT_PDBV_HSC0_PWR_W
GT_MB_CPU0_PKG_PWR_W	GT_PDBV_HSC0_TEMP_C
GT_MB_CPU1_PKG_PWR_W	GT_PDBV_HSC0_PEAK_PIN_W
GT_MB_CPU0_DIMM_GRPA_TEMP_C	GT_PDBV_BRICK0_VOLT_V
GT_MB_CPU0_DIMM_GRPB_TEMP_C	GT_PDBV_BRICK0_CURR_A
GT_MB_CPU0_DIMM_GRPC_TEMP_C	GT_PDBV_BRICK0_TEMP_C
GT_MB_CPU0_DIMM_GRPD_TEMP_C	GT_PDBV_BRICK0_PWR_W
GT_MB_CPU0_DIMM_GRPE_TEMP_C	GT_PDBV_BRICK1_VOLT_V
GT_MB_CPU0_DIMM_GRPF_TEMP_C	GT_PDBV_BRICK1_CURR_A
GT_MB_CPU0_DIMM_GRPG_TEMP_C	GT_PDBV_BRICK1_TEMP_C
GT_MB_CPU0_DIMM_GRPH_TEMP_C	GT_PDBV_BRICK1_PWR_W
GT_MB_CPU1_DIMM_GRPA_TEMP_C	GT_PDBV_BRICK2_VOLT_V
GT_MB_CPU1_DIMM_GRPB_TEMP_C	GT_PDBV_BRICK2_CURR_A
GT_MB_CPU1_DIMM_GRPC_TEMP_C	GT_PDBV_BRICK2_TEMP_C
GT_MB_CPU1_DIMM_GRPD_TEMP_C	GT_PDBV_BRICK2_PWR_W
GT_MB_CPU1_DIMM_GRPE_TEMP_C	GT_PDBV_P3V3_AUX_IN6_VOLT_V
GT_MB_CPU1_DIMM_GRPF_TEMP_C	GT_PDBH_HSC1_VOLT_V
GT_MB_CPU1_DIMM_GRPG_TEMP_C	GT_PDBH_HSC1_CURR_A

GT_MB_CPU1_DIMM_GRPH_TEMP_C	GT_PDBH_HSC1_PWR_W
GT_MB_VR_CPU0_VCCIN_VOLT_V	GT_PDBH_HSC1_TEMP_C
GT_MB_VR_CPU0_VCCIN_TEMP_C	GT_PDBH_HSC1_PEAK_PIN_W
GT_MB_VR_CPU0_VCCIN_CURR_A	GT_PDBH_HSC2_VOLT_V
GT_MB_VR_CPU0_VCCIN_PWR_W	GT_PDBH_HSC2_CURR_A
GT_MB_VR_CPU0_VCCFA_FIVRA_VOLT_V	GT_PDBH_HSC2_PWR_W
GT_MB_VR_CPU0_VCCFA_FIVRA_TEMP_C	GT_PDBH_HSC2_TEMP_C
GT_MB_VR_CPU0_VCCFA_FIVRA_CURR_A	GT_PDBH_HSC2_PEAK_PIN_W
GT_MB_VR_CPU0_VCCFA_FIVRA_PWR_W	GT_BP0_FAN0_INLET_SPEED_RPM
GT_MB_VR_CPU0_VCCIN_FAON_VOLT_V	GT_BP0_FAN0_OUTLET_SPEED_RPM
GT_MB_VR_CPU0_VCCIN_FAON_TEMP_C	GT_BP0_FAN1_INLET_SPEED_RPM
GT_MB_VR_CPU0_VCCIN_FAON_CURR_A	GT_BP0_FAN1_OUTLET_SPEED_RPM
GT_MB_VR_CPU0_VCCIN_FAON_PWR_W	GT_BP0_FAN4_INLET_SPEED_RPM
GT_MB_VR_CPU0_VCCFA_VOLT_V	GT_BP0_FAN4_OUTLET_SPEED_RPM
GT_MB_VR_CPU0_VCCFA_TEMP_C	GT_BP0_FAN5_INLET_SPEED_RPM
GT_MB_VR_CPU0_VCCFA_CURR_A	GT_BP0_FAN5_OUTLET_SPEED_RPM
GT_MB_VR_CPU0_VCCFA_PWR_W	GT_BP0_FAN8_INLET_SPEED_RPM
GT_MB_VR_CPU0_VCCD_HV_VOLT_V	GT_BP0_FAN8_OUTLET_SPEED_RPM
GT_MB_VR_CPU0_VCCD_HV_TEMP_C	GT_BP0_FAN9_INLET_SPEED_RPM
GT_MB_VR_CPU0_VCCD_HV_CURR_A	GT_BP0_FAN9_OUTLET_SPEED_RPM
GT_MB_VR_CPU0_VCCD_HV_PWR_W	GT_BP0_FAN12_INLET_SPEED_RPM
GT_MB_P12V_AUX_IN0_VOLT_V	GT_BP0_FAN12_OUTLET_SPEED_RPM
GT_MB_P5V_IN3_VOLT_V	GT_BP0_FAN13_INLET_SPEED_RPM
GT_MB_P3V3_IN4_VOLT_V	GT_BP0_FAN13_OUTLET_SPEED_RPM
GT_MB_P3V3_AUX_IN5_VOLT_V	GT_BP1_FAN2_INLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_VOLT_V	GT_BP1_FAN2_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_TEMP_C	GT_BP1_FAN3_INLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_CURR_A	GT_BP1_FAN3_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_PWR_W	GT_BP1_FAN6_INLET_SPEED_RPM
GT_MB_VR_CPU1_VCCFA_FIVRA_VOLT_V	GT_BP1_FAN6_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCFA_FIVRA_TEMP_C	GT_BP1_FAN7_INLET_SPEED_RPM
GT_MB_VR_CPU1_VCCFA_FIVRA_CURR_A	GT_BP1_FAN7_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCFA_FIVRA_PWR_W	GT_BP1_FAN10_INLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_FAON_VOLT_V	GT_BP1_FAN10_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_FAON_TEMP_C	GT_BP1_FAN11_INLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_FAON_CURR_A	GT_BP1_FAN11_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCIN_FAON_PWR_W	GT_BP1_FAN14_INLET_SPEED_RPM

GT_MB_VR_CPU1_VCCFA_VOLT_V	GT_BP1_FAN14_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCFA_TEMP_C	GT_BP1_FAN15_INLET_SPEED_RPM
GT_MB_VR_CPU1_VCCFA_CURR_A	GT_BP1_FAN15_OUTLET_SPEED_RPM
GT_MB_VR_CPU1_VCCFA_PWR_W	GT_SCM_P12V_V
GT_MB_VR_CPU1_VCCD_HV_VOLT_V	GT_SCM_P5V_V
GT_MB_VR_CPU1_VCCD_HV_TEMP_C	GT_SCM_P3V3_V
GT_MB_VR_CPU1_VCCD_HV_CURR_A	GT_SCM_P2V5_V
GT_MB_VR_CPU1_VCCD_HV_PWR_W	GT_SCM_P1V8_V
GT_MB_P3V_BAT_V	GT_SCM_PGPPA_V
GT_MB_PCH_TEMP_C	GT_SCM_P1V2_V
GT_MB_CPU0_DIMM_A0_PWR_W	GT_SCM_P1V0_V
GT_MB_CPU0_DIMM_C0_PWR_W	GT_SCM_P12V_VOLT_V
GT_MB_CPU0_DIMM_A1_PWR_W	GT_SCM_P12V_CURR_A
GT_MB_CPU0_DIMM_C1_PWR_W	GT_SCM_P12V_PWR_W
GT_MB_CPU0_DIMM_A2_PWR_W	GT_SCM_TEMP_C
GT_MB_CPU0_DIMM_C2_PWR_W	
GT_MB_CPU0_DIMM_A3_PWR_W	
GT_MB_CPU0_DIMM_C3_PWR_W	
GT_MB_CPU0_DIMM_A4_PWR_W	
GT_MB_CPU0_DIMM_C4_PWR_W	
GT_MB_CPU0_DIMM_A5_PWR_W	
GT_MB_CPU0_DIMM_C5_PWR_W	
GT_MB_CPU0_DIMM_A6_PWR_W	
GT_MB_CPU0_DIMM_C6_PWR_W	
GT_MB_CPU0_DIMM_A7_PWR_W	
GT_MB_CPU0_DIMM_C7_PWR_W	
GT_MB_CPU1_DIMM_B0_PWR_W	
GT_MB_CPU1_DIMM_D0_PWR_W	
GT_MB_CPU1_DIMM_B1_PWR_W	
GT_MB_CPU1_DIMM_D1_PWR_W	
GT_MB_CPU1_DIMM_B2_PWR_W	
GT_MB_CPU1_DIMM_D2_PWR_W	

14. Security

The Intel-based CPU Tray uses Platform Secure Boot. The SCM with OpenBMC uses verified boot with signed firmware and contains 2 trusted platform modules (TPM), one for BMC and one for the host.

Appendix A - Checklist for IC approval of this Specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document .

Item	Status	Link to detailed explanation
Has this contribution been presented to an OCP Project group during a project call or engineering workshop?	Yes or No	If “No”, please state the reason.
Approval by Project Leads	Yes or No	If “No”, please state the reason.
Is this contribution entered into the OCP Contribution Portal?	Yes or No	If “No”, please state the reason.
Was it approved in the OCP Contribution Portal?	Yes or No	If “No”, please state the reason.