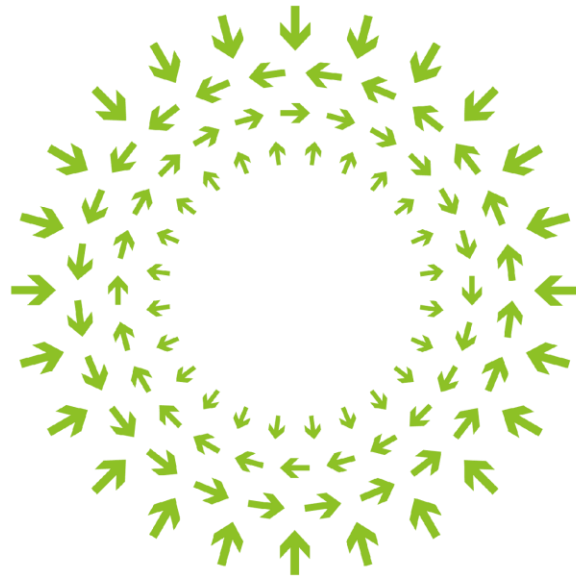




OPEN

Compute Project

Composable Memory Appliance (CMA) Base Specification

V1.1

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Author: Seagate Technology Team Member(s)

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1. License

OCP CLA

1.1 OCP CLA

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Notes:

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1.2 Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their design contributions:

- Intel Corp. / Altera Corp. for their Agilex-I FPGA and CXL Hard and Soft IP.
- Astera-Labs Corp. for their PCIe-5.0 x16 Retimer device and their PHY compatibility and tuning efforts.
- SerialCable Corp. for their PCIe 5.0 x16 QSFP-DD CXL Retimer HBA design, compatibility, and tuning. [OBJ]

2. Compliance with OCP Tenets

The Seagate Composable Memory Appliance (CMA) Base-Specification contribution effort and the creation of the CMA and Composability Fabric Manager (CFM) Sub-Projects within the Composable Memory System (CMS) workstream that is under the Server Project is a step towards creating an industry collaborative effort that aims to achieve openness, efficiency and optimized TCO for scaling external pooled memory capacity with non-bandwidth while maintaining ~2x Non-Unified-Memory-Access (NUMA) hop latency, which can improve sustainability through DDR4 recycling with reduced cost and overall power per GB for memory capacity scaling.

2.1 Openness

The OCP CMA specification and prototype solution POC were developed in dialogue with the potential OCP customer. The CMA Sub-Project under the CMS Workstream and the Server Project will enable open discussions around the current contributed architecture and will be open for suggestions and concepts that could enhance its capability to better serve the OCP community. The initial Base specification contribution will act as a catalyst that will encourage more innovation and result in the creation of the ideal OCP solution/platform that will best serve the community. This ecosystem is nascent, so we are confident that this CMA architecture will evolve over time, and that the future CMA specifications will represent the wisdom of the collective ecosystem on the scenarios and requirements for creating the optimal Computer Express Link (CXL) Pooled Memory solutions serving the near future datacenter and enterprise applications.

2.2 Efficiency

The efficiency goals of this Base specification as well as the future CMA and CFM Sub-Projects are to seed the OCP ecosystem with a base solution and then together identify the key scenarios and requirements for the most efficient final solution that is fully vetted by vendors and customers. Additionally, it is our goal to help solve the various existing datacenter and enterprise memory wall efficiency challenges and explore optimal intersecting solutions along with the pros and cons of such possible industry unified solutions.

2.3 Impact

Architecturally, the OCP CMA Pooled Memory solution base specification shall enable datacenter and enterprise infrastructure designers to take advantage of using similar pooled memory connectivity infrastructure and drive the most efficient economy of scale TCO benefits using CXL memory pooling in the industry.

2.4 Scale

The OCP CMA/CFM solution base specification shall act as an example and a proof of concept to the future CMA/CFM sub-project final specification that will aim at enabling best in class rack-level memory disaggregation and allow for close to ideal compute cloud and AI solutions scalability soon datacenter with optimal scalability efficiency.

2.5 Sustainability

This OCP CMA Base-Specification initiative will enable the physical disaggregation of memory components and allow for superior scale-out architectures that are composable in nature, thus the minimization of stranded resources and overprovisioning (eliminating unreachable and underutilized memory resources) in the modern datacenter, by starting small and expanding on a temporal basis depending on the datacenter requirements. This architecture also enables reuse and re-deployment of prior generation DRAM memory standard modular hardware infrastructure across multiple platforms and multiple hardware generations, thus enabling:

- Reuse of our natural resources that are consumed to make memory solutions.
- Allow us to create more optimal computer solutions with less datacenter power and cost.
- Creating the most efficient forms of AI (Artificial Intelligence) and cloud compute solutions while mindful of the environmental impact. [OBI]

3. Change Log

Date	Version #	Author	Description
7/25/2024	0.1	Mohammad El-Batal	Updated the content for Acknowledgements, Compliance and Openness
7/26/2024	0.2	Mohammad El-Batal	Updated the content for Efficiency, Impact, Scale and Sustainability
7/26/2024	0.3	Mohammad El-Batal	Updated the content for scope and overview
7/26/2024	0.4	Kanika Arya	Updated the content for mechanical, electrical, and thermal requirements
8/10/2024	0.5	Mohammad El-Batal	Added the interface ports information and provided the OCP required introductory sections
8/30/2024	1.0	Mohamad El-Batal Kanika Arya	Final Thermal Analysis added Completed BMC tables General formatting changes
9/23/2024	1.1	Mohamad El-Batal Kanika Arya	Removed "Seagate Confidential" and "Not Released" notes from mechanical figures Fixed timing diagrams to complete the signal names Added CMA Blade Physical Block Diagram to section-8.3 Various minor corrections Removed cutoff SPI protocol timing block diagrams

Table 1. Change Log Table

4. Scope

The CMA Base Hardware and Software Specification is an architectural and mechanical framework example of a disaggregated pooled memory solution alignment. This specification is for a Proof-of-Concept solution that will act as a catalyst to the OCP Market and drive more general customer requirements into the final specifications. Together Customer and Vendors will get together within the CMA/CFM Sub-Project to discuss the future specification with collaboration between competitors and partners that shall contribute equally towards the benefit of the industry through Open Hardware architectures that will drive a healthy execution excellence amongst the pool of solution engineering providers.

5. Overview

The OCP CMA/CFM solution base specification is contributed by Seagate as a complete TCO-optimized disaggregated pooled memory solution aiming to address the datacenter computational Memory-wall and Stranded-resource challenges.

Furthermore, this solution is a Non-blocking CXL pooled memory bandwidth performance while reducing the remote memory pool cache-line access latency to be as close as possible to approximately ~2x Non-Unified-Memory-Access (NUMA) hops in order to avoid negatively impacting as many cloud applications as possible and providing them with composable memory resources and enable all the positives of such solution in terms of temporal access to memory capacity on an as needed basis and avoid started memory resources behind a single compute device.

The Seagate contribution effort and the creation of the CMA and CFM Sub-Projects within the Composable Memory System (CMS) workstream that is under the Server Project is a step towards creating an industry collaborative effort that aims to achieve openness, efficiency, and optimized TCO for scaling external pooled memory capacity with non-bandwidth while maintaining ~2x NUMA latency, which can improve sustainability through DDR4 recycling with reduced cost and overall power per GB for memory capacity scaling.

6. Physical Specifications

6.1 Mechanical

6.2 Enclosure

The following pictures illustrate the CMA 3U chassis that fits in an EIA 19-inch rack.

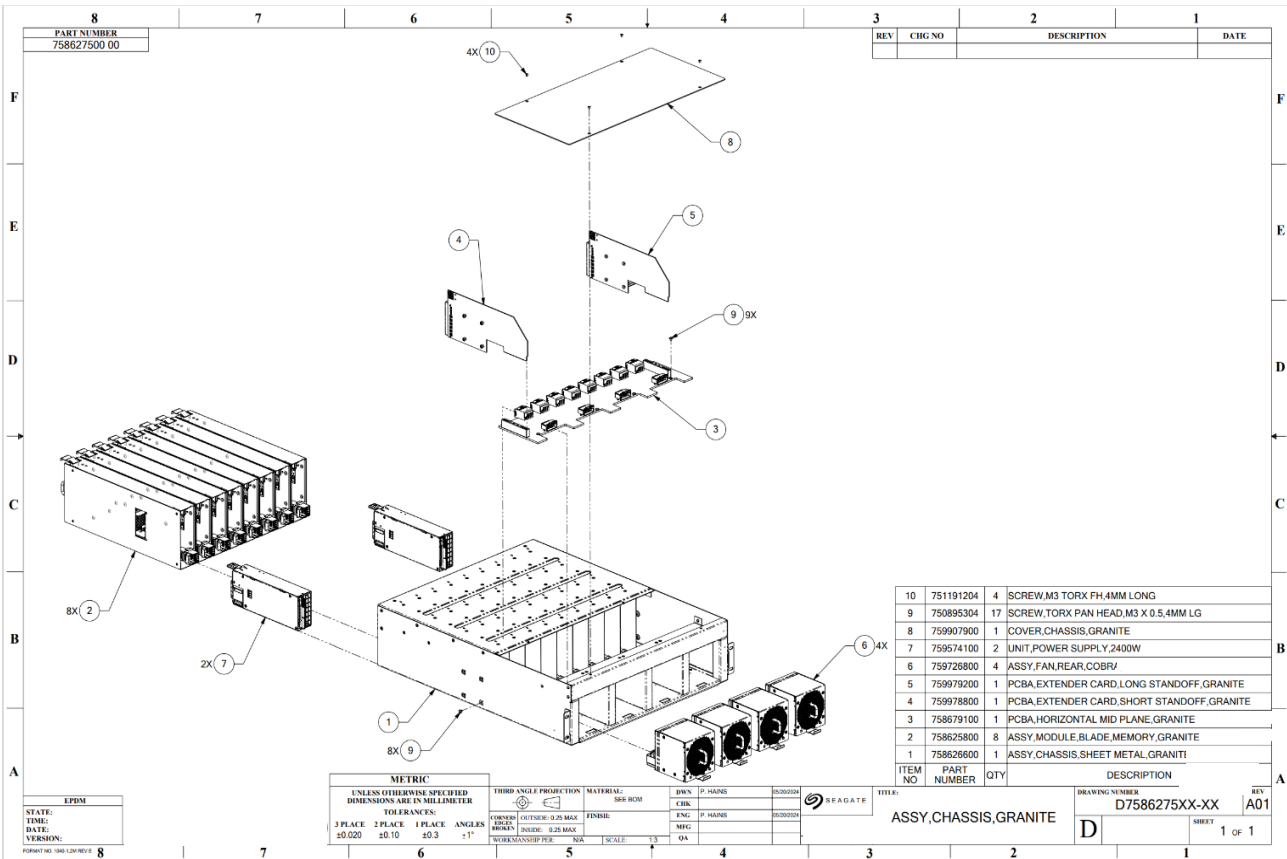


Figure 1. Exploded Enclosure Drawing with Components

6.3 Front of Chassis

The Fan FRUs are hot swappable accessible from the front of the chassis. Fan FRU 0-3 are logically mapped right to left looking from the chassis front view.

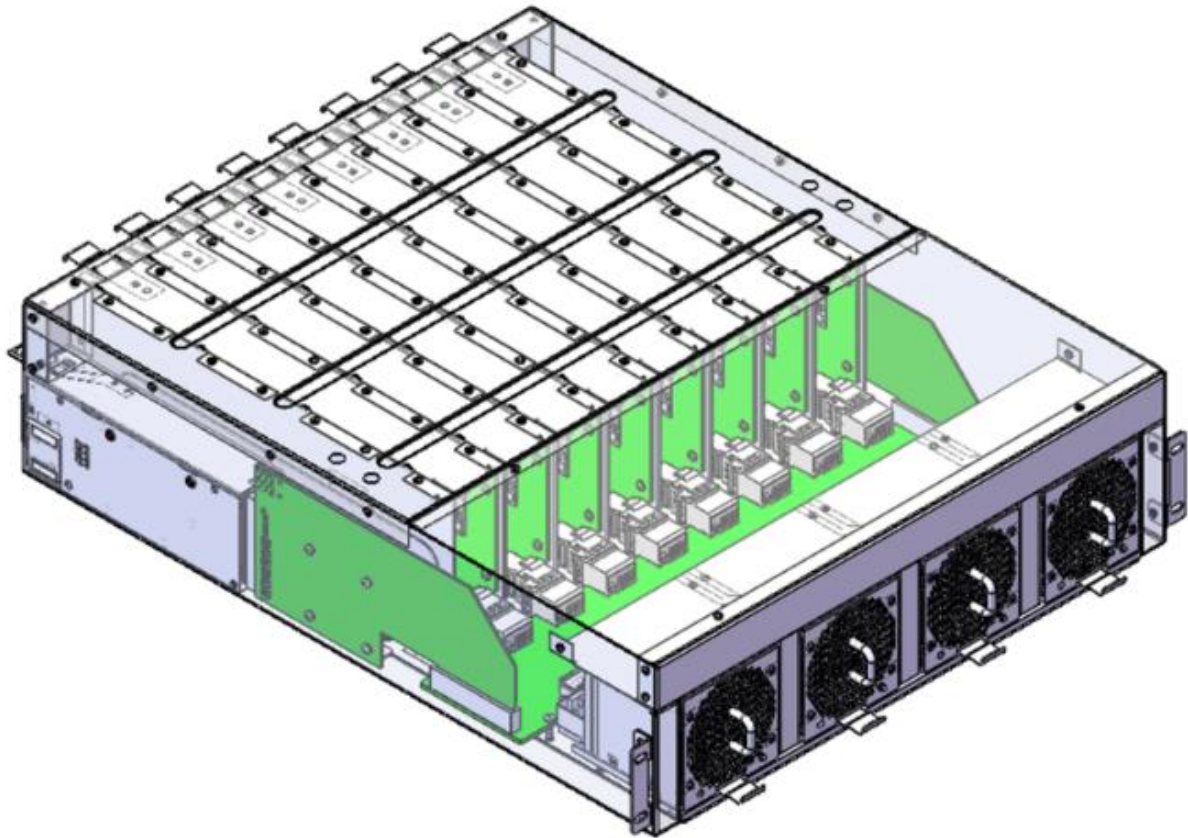


Figure 3. Enclosure Rendering - Front

6.4 Rear of Chassis

The CMA Blade FRUs and CRPS power supplies are hot swap accessible from the rear of the chassis. Controller blade FRU 0-7 and PSU's 0-1 are logically mapped left to right looking from the chassis rear view.

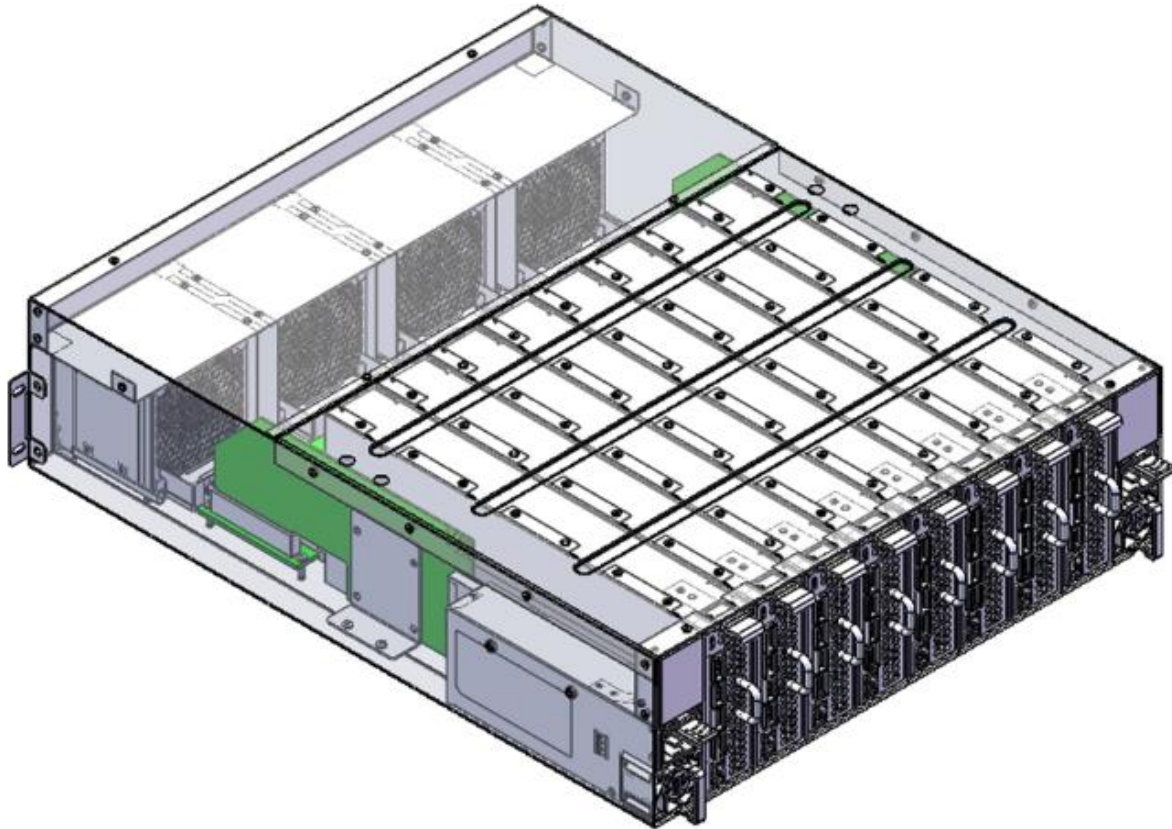


Figure 4. Enclosure Rendering - Rear

6.5 Controller Canister

The CMA blades are housed in a mechanical sheet metal canister. They are hot swappable and latch into chassis slots.

- Base Plane Connector
 - A single orthogonal right angle connector combining power and I/O is used to minimize board area and air flow impedance.
 - Molex 171574-7807 (CONN, 100 OHM, 4 PAIR, RIGHT ANGLE ORTHOGONAL DIRECT HEADER, TOP GUIDE, TH-96P)
- QSFP-DD sockets
 - Looking from right to left, the UP0 and UP1 ports are PCIe Gen5 16-lane per pair of adjacent sockets. Each socket has a green status and yellow fault LED passed through a light pipe above the socket cage assembly.
- USB2.0 Micro-B
 - This connector brings out the FPGA Teccan processor CLI, the BMC (Board Management Controller) serial Linux port and the MSP430 user interface. The USB controller on-board is a 5V VBus powered from the host.
- FRU LEDs
 - There are two externally visible LEDs located on each side under the USB connector:
 - Green status
 - Yellow fault

The DDR4 DIMMs and BMC module socket mounts to the controller board. The rear orthogonal connector blind mate hot swappable to/from the enclosure base plane.

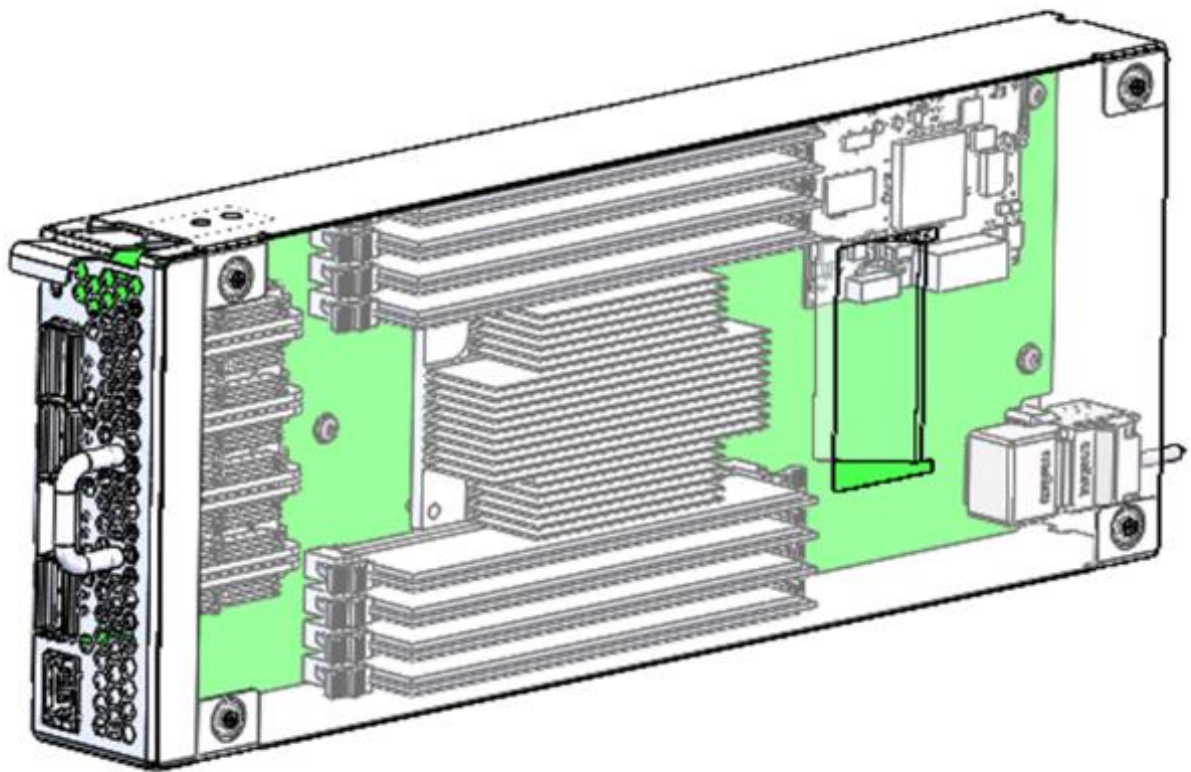


Figure 5. Blade Rendering with Sled - Data Side

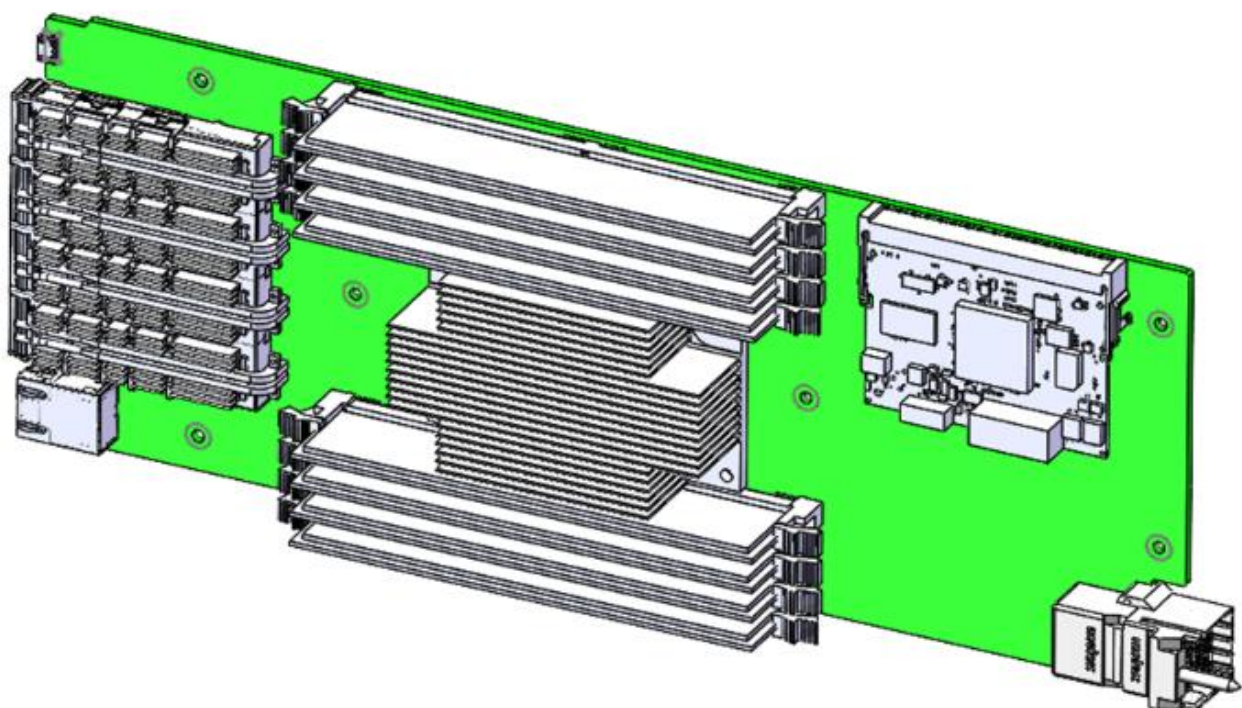


Figure 6. Blade Rendering without Sled - Data Side

6.6 Power Supplies

The Common Redundant Power Supplies (CRPS) hot swappable to/from the chassis and current share 12V DC power on the base plane. Each controller FRU slot has an independent hot swap over-current protection circuit integrated on the base plane. The CRPS has a C19 110/220 VAC compatible input power connector, integrated fan, and external fault LED.

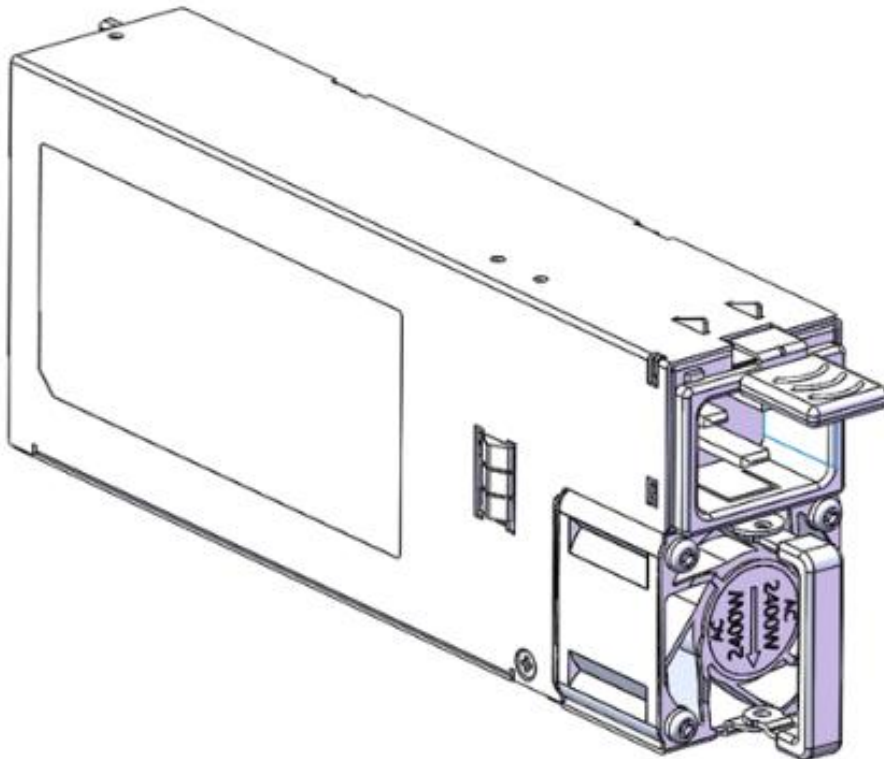


Figure 7. Power Supply Rendering

6.7 Fan Modules

The hot swappable Fan FRUs are leveraged from the common 4U106 enclosures. The base plane CPLD (Complex Programmable Logic Device) controls the fan PWM via registers accessed by the controller slot 0 BMC. Each fan module has an external yellow fault LED.

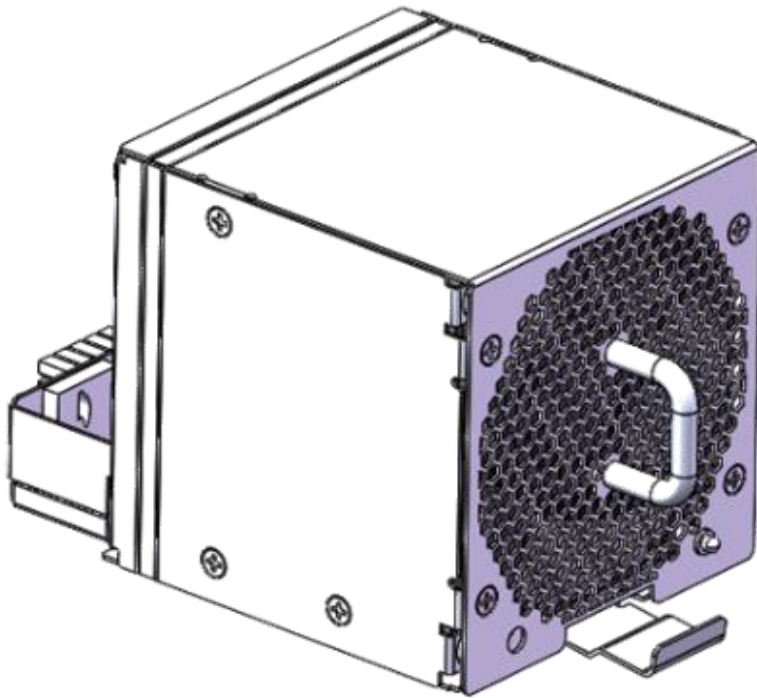


Figure 8. Fan Module Rendering

7. Environmental / Regulatory Requirements

The enclosure must be able to perform properly during and/or after the following requirements:

- Operating temperature and altitude range – ASHRAE A2 (35°C)
- Storage temperature range - -40 to 70°C, 5% to 100% relative humidity, 29°C max wet bulb
- Transportation temperature range – same as storage
- Shock and Vibration requirements:
 - Non-Op Vibration:
 - Z-axis: 0.78gRMS random vibration, 10-200Hz, 30 mins
 - X, Y-axes: 0.25 gRMS random vibration, 10-200Hz, 30 mins
 - Op Vibration:
 - 0.18gRMS, Random vibration 10-500Hz, 30 min per axis
 - Will also evaluate at 0.4g swept sine, 10 sweeps, 5-500Hz, 1 octave/min (EVT only – P1)
 - Non-Op Shock:
 - Z axis: +20g half sine, 7ms, 2 shocks in positive Z
 - X, Y-axes: +/-12g half sine, 11ms, 6 shocks in both directions
 - Op Shock:
 - Z-axis: +5G half sine 11ms, 10 shocks in positive Z
 - X, Y axes: +/-5G half sine 11ms, 10 shocks in both directions

8. Platform Hardware Design

These sections describe CMA hardware platform. The platform enclosure fits in a 3U 19-inch rack mount form factor. The enclosure has the following fixed boards integrated:

- Active base plane PCBA 60-00000616
- Passive redundant power supply adapter PCBAs 60-00000617

The following Field Replaceable Units (FRUs) plug into the CMA chassis:

- CMA Blade PCBA 60-00000629 housed in a mechanical sheet metal canister.
- 4x redundant Cobra 4U modified dual-rotor fan modules.
- 2x redundant 2400W CRPS (Common Redundant Power Supplies) with C19 receptacles

8.1 CMA Blade

The CMA Blade PCBA assembly 60-00000629 integrates:

- The PCIe Gen5 CXL to DDR4 memory aggregator FPGA
 - Intel Agilex-7 I-Series pn AGIB027R29A1E2VR3
- RunBMC compatible SoDIMM 260-pin right angle socket
 - Supports Seagate BMC module 60-00000588.
- Mixed Signal Microcontroller
 - TI part number TI MSP430FR2155TRSMR
- Scalable DC Power Modules
 - MPS part number MPM82504GBH-0000
- 4x QSFP-DD external sockets
 - PCIe Gen5 8-lane
- 8x DDR4 RDIMM 288-pin vertical sockets
 - Support for up to 128GB DDR4 RDIMM modules, 1TB memory total.
- External User Interfaces
 - 1GbaseT Ethernet (RJ45)
 - USB2.0 (Micro-B)
 - Status (Green) and Fault (Yellow) LEDs

8.2 CMA Blade Block Diagram

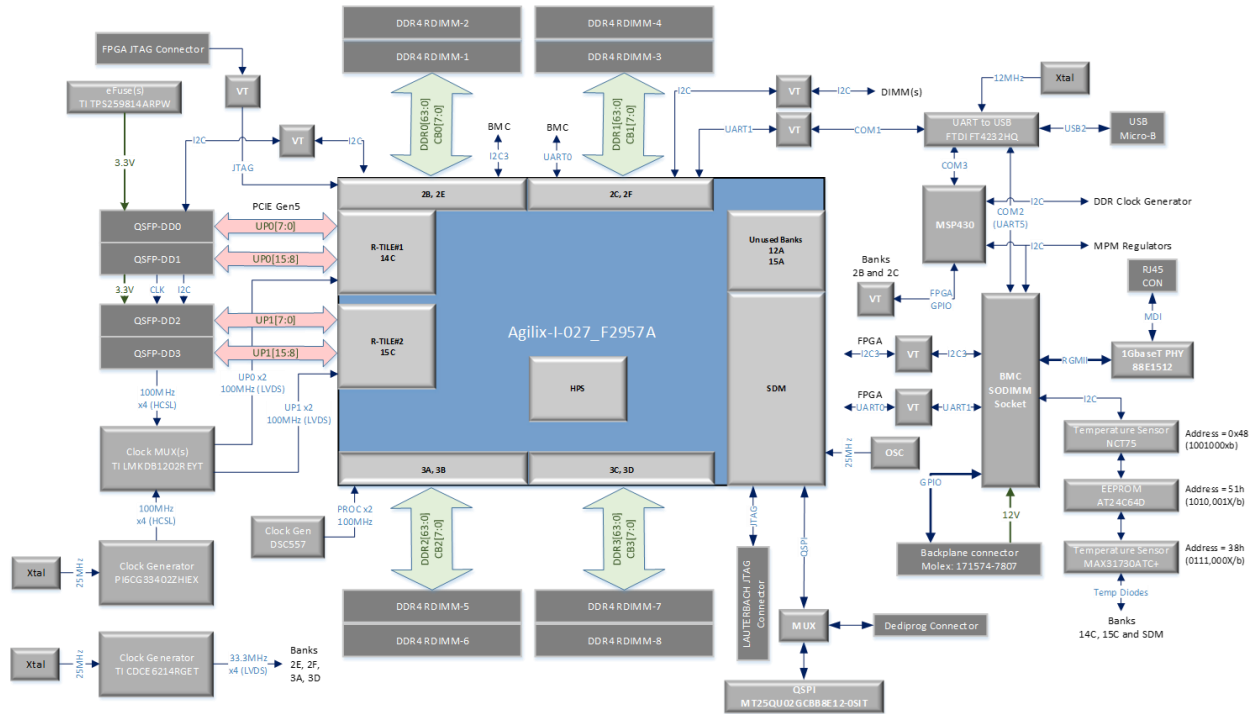


Figure 9. Drawing of the General Block Diagram

8.3 CMA Blade PCB Design

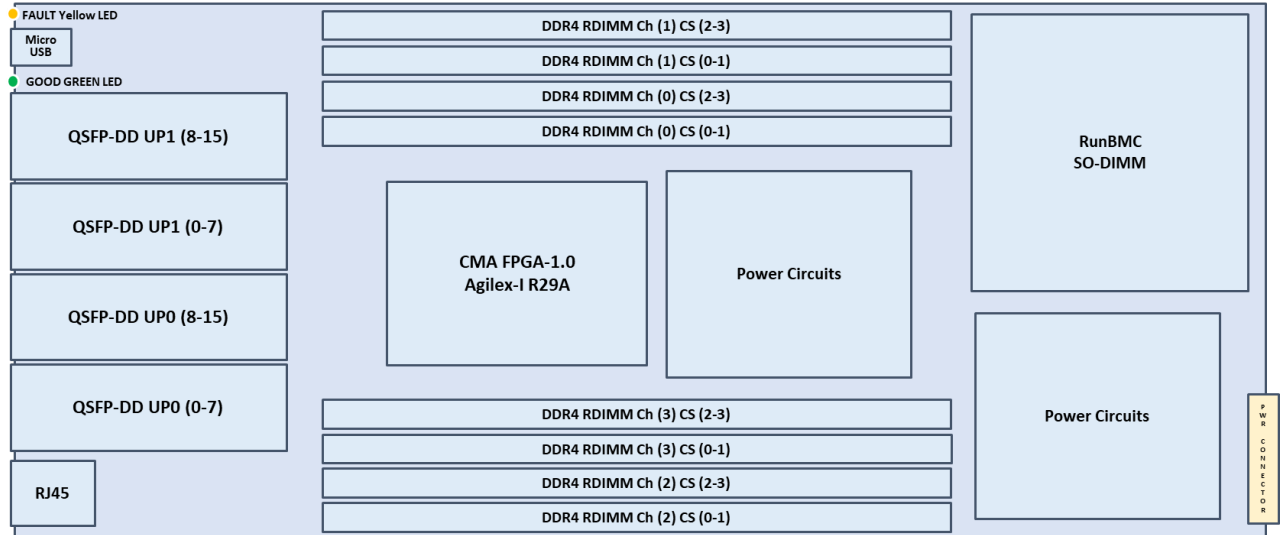


Figure 10. CMA Blade Physical Block Diagram

8.4 Assembly Drawing

The diagram below is a macro view of the PCB and highlights the debug interface connectors and LEDs on the 60-00000629 PCB.

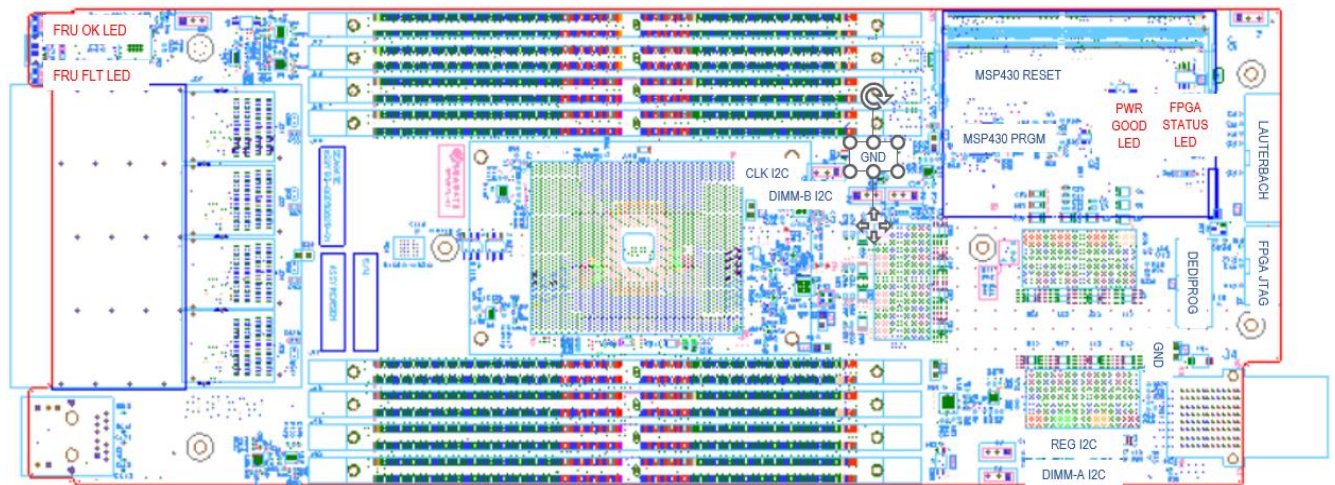


Figure 11. Micro View PCB Top

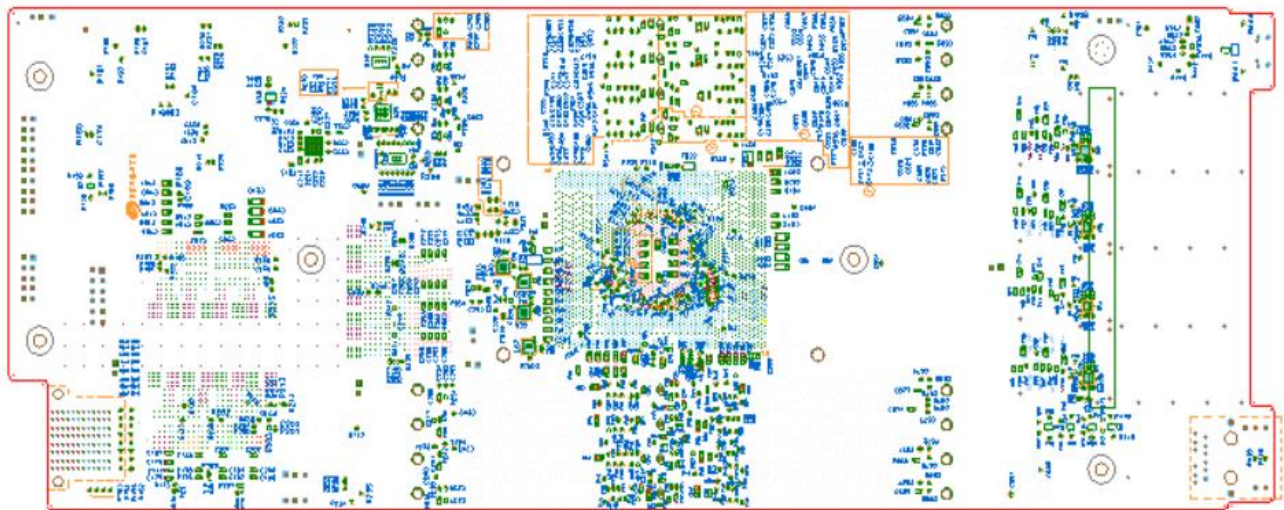


Figure 12. Micro View PCB Back

8.5 Outline and Stack Up

The diagrams below are taken from the 61-00000629-01 fab drawing. The PCB outline is 4.858 x 12.992 inches. The PCB is fabricated with a low loss tangent material, EM-528. PCIe Gen5 differential impedance is nominal 90 ohm.

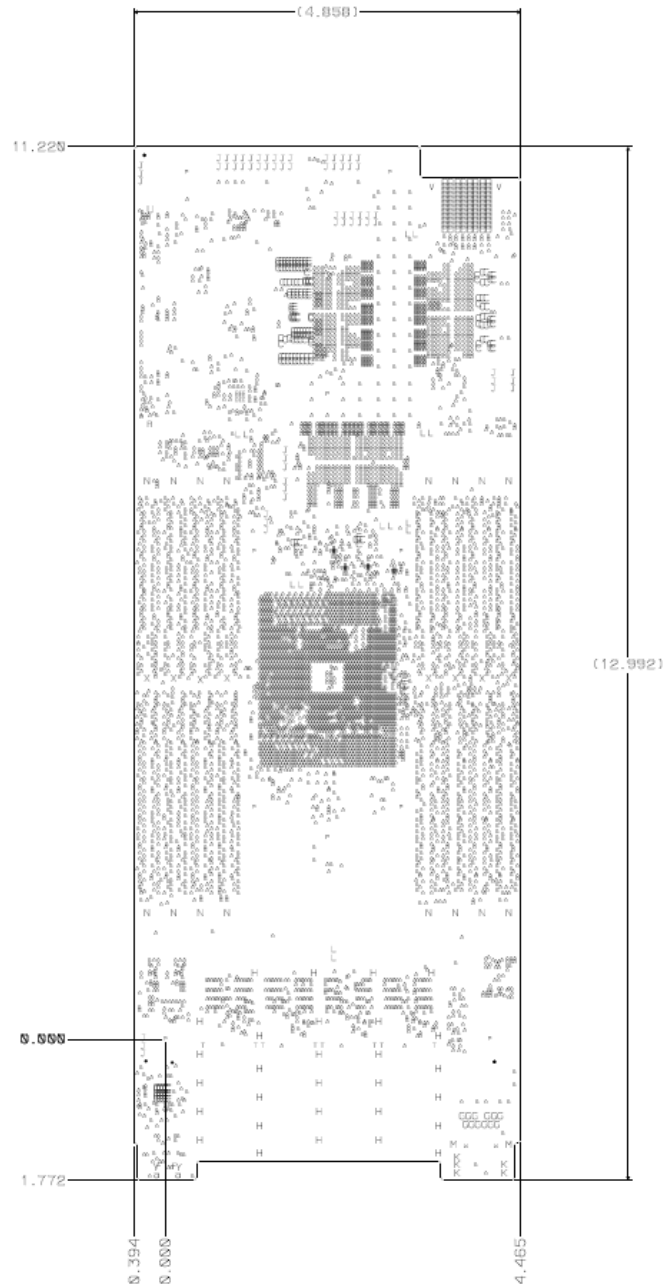


Figure 13. Base Plane Dimensions

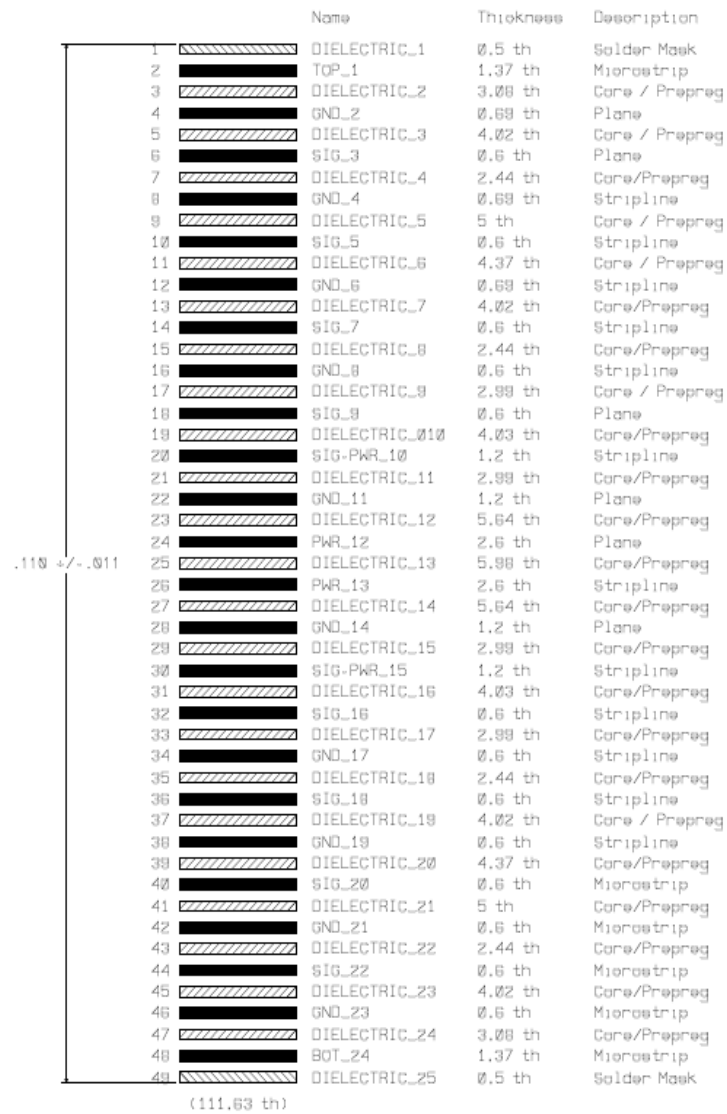


Figure 14. Base Plane Stack Up

IMPEDANCE CHART

IMPEDANCE TOLERANCE = +/- 10%

90 OHM DIFFERENTIAL		100 OHM DIFFERENTIAL	50 OHM SINGLE ENDED
LAYER	TR/SP/TR (MILS)	TR/SP/TR (MILS)	TRACE WIDTH (MILS)
5,7,9, 16,18,20, 22	3.5 / 4.0 / 3.5		
1,24		3.5 / 5.0 / 3.5	5.2
3,5,7, 18,20, 22		2.75 / 5.8 / 2.75	3.0
9,16		2.75 / 6.0 / 2.75	

Figure 15. Base Plane Impedance

8.6 CMA Blade to Base-Plane Connector Pin-Out

ACE PCBA
Pin Number

Midplane PCBA
Pin Number

ORTHO PIN MAPPING							
POSITION 270° (OD RAM - RAF)							
A1-A1	A2-B1	A3-D1	A4-E1	A5-G1	A6-H1	A7-K1	A8-L1
B1-A2	B2-C1	B3-D2	B4-F1	B5-G2	B6-J1	B7-K2	B8-M1
C1-B2	C2-C2	C3-E2	C4-F2	C5-H2	C6-J2	C7-L2	C8-M2
D1-A3	D2-B3	D3-D3	D4-E3	D5-G3	D6-H3	D7-K3	D8-L3
E1-A4	E2-C3	E3-D4	E4-F3	E5-G4	E6-J3	E7-K4	E8-M3
F1-B4	F2-C4	F3-E4	F4-F4	F5-H4	F6-J4	F7-L4	F8-M4
G1-A5	G2-B5	G3-D5	G4-E5	G5-G5	G6-H5	G7-K5	G8-L5
H1-A6	H2-C5	H3-D6	H4-F5	H5-G6	H6-J5	H7-K6	H8-M5
J1-B6	J2-C6	J3-E6	J4-F6	J5-H6	J6-J6	J7-L6	J8-M6
K1-A7	K2-B7	K3-D7	K4-E7	K5-G7	K6-H7	K7-K7	K8-L7
L1-A8	L2-C7	L3-D8	L4-F7	L5-G8	L6-J7	L7-K8	L8-M7
M1-B8	M2-C8	M3-E8	M4-F8	M5-H8	M6-J8	M7-L8	M8-M8

NOTE: PINOUTS SHOWN IN BALLOONS ARE GROUNDS.
GROUND PATHS ARE NOT DISCRETE CIRCUITS.

Figure 16. Blade to Base-Plane Connectors Pin-Out

8.7 CMA Blade Host Interfaces

Four CXL1.1 x8 PCIe-5.0 endpoint Host/Client QSFP-DD sockets connections providing either:

- UP0 – One x16 CXL1.1 PCIe-5.0 Endpoint Upstream Port-0 that combines the two QSFP-DD x8 connections on J24 upper 8-bits and J25 lower 8-bits.
- UP1 – One x16 CXL1.1 PCIe-5.0 Endpoint Upstream Port-1 that combines the two QSFP-DD x8 connections on J21 upper 8-bits and J22 lower 8-bits.

SC Proposed QSFP-DD DAC/AEC/AOC Cable Connectors					Seagate CMA QSFP-DD Blade Connector	
P1 QSFP-DD			P2 QSFP-DD		QSFP-DD	
GND	1		20	GND	GND	1
TX2N	2		21	RX2N	TX2N	2
TX2P	3		22	RX2P	TX2P	3
GND	4		23	GND	GND	4
TX4N	5		24	RX4N	TX4N	5
TX4P	6		25	RX4P	TX4P	6
GND	7		26	GND	GND	7
MODSELL	8		8	MODSELL	MODSELL	8
PERST#0	9		9	PERST#0	PERST#0	9
VCCRX-3.3V	10		10	VCCRX-3.3V	VCCRX-3.3V	10
SCL0	11		11	SCL0	EEPROM-SCL0	11
SDA0	12		12	SDA0	EEPROM-SDA0	12
GND	13		32	GND	GND	13
RX3P	14		33	TX3P	RX3P	14
RX3N	15		34	TX3N	RX3N	15
GND	16		35	GND	GND	16
RX1P	17		36	TX1P	RX1P	17
RX1N	18		37	TX1N	RX1N	18
GND	19		38	GND	GND	19
GND	20		1	GND	GND	20
RX2P	21		2	TX2P	RX2P	21
RX2N	22		3	TX2N	RX2N	22
GND	23		4	GND	GND	23
RX4P	24		5	TX4P	RX4P	24
RX4N	25		6	TX4N	RX4N	25
GND	26		7	GND	GND	26
MODPRSL	27		27	MODPRSL	PRPE/MODPRSL	27
INTL	28		28	INTL	INTL-NC	28

VCCTX-3.3V	29	29	VCCTX-3.3V		VCCTX-3.3V	29
VCC1-3.3V	30	30	VCC1-3.3V		VCC1-3.3V	30
INITMODE-NC	31	31	INITMODE-NC		INITMODE-NC	31
GND	32	13	GND		GND	32
TX3N	33	14	RX3N		TX3N	33
TX3P	34	15	RX3P		TX3P	34
GND	35	16	GND		GND	35
TX1N	36	17	TX1N		TX1N	36
TX1P	37	18	TX1P		TX1P	37
GND	38	19	GND		GND	38
GND	39	58	GND		GND	39
TX6N	40	59	RX6N		TX6N	40
TX6P	41	60	RX6P		TX6P	41
GND	42	61	GND		GND	42
TX8N	43	62	RX8N		TX8N	43
TX8P	44	63	RX8P		TX8P	44
GND	45	64	GND		GND	45
CLKP0	46	46	CLKP0		FLEXIO2/CLKP0	46
CLKN0	47	47	CLKN0		FLEXIO1/CLKN0	47
VCCR1-3.3V	48	48	VCCR1-3.3V		VCCR1-3.3V	48
VS2-NC	49	49	VS2-NC		FLEXIO3-NC	49
VS3-NC	50	50	VS3-NC		FLEXIO4-NC	50
GND	51	70	GND		GND	51
RX7P	52	71	TX7P		RX7P	52
RX7N	53	72	TX7N		RX7N	53
GND	54	73	GND		GND	54
RX5P	55	74	TX5P		RX5P	55
RX5N	56	75	TX5N		RX5N	56
GND	57	76	GND		GND	57
GND	58	39	GND		GND	58
RX6P	59	40	TX6P		RX6P	59
RX6N	60	41	TX6N		RX6N	60
GND	61	42	GND		GND	61
RX8P	62	43	TX8P		RX8P	62
RX8N	63	44	TX8N		RX8N	63
GND	64	45	GND		GND	64
NC	65	65	NC		NC	65
RESV2-NC	66	66	RESV2-NC		RESV2-NC	66

VCCTX1-3.3V	67		67	VCCTX1-3.3V		VCCTX1-3.3V	67
VCC2-3.3V	68		68	VCC2-3.3V		VCC2-3.3V	68
RESV3-NC	69		69	RESV3-NC		RESV3-NC	69
GND	70		51	GND		GND	70
TX7N	71		52	RX7N		TX7N	71
TX7P	72		53	RX7P		TX7P	72
GND	73		54	GND		GND	73
TX5N	74		55	RX5N		TX5N	74
TX5P	75		56	RX5P		TX5P	75
GND	76		57	GND		GND	76

Table 2. QSFPDD Socket and Cable Pin-Out and Signal Names

The 60-00000629 DC power diagram below highlights the load currents, power on sequencing for the FPGA and I2C addresses used by the MSP430 to monitor and manage power telemetry.

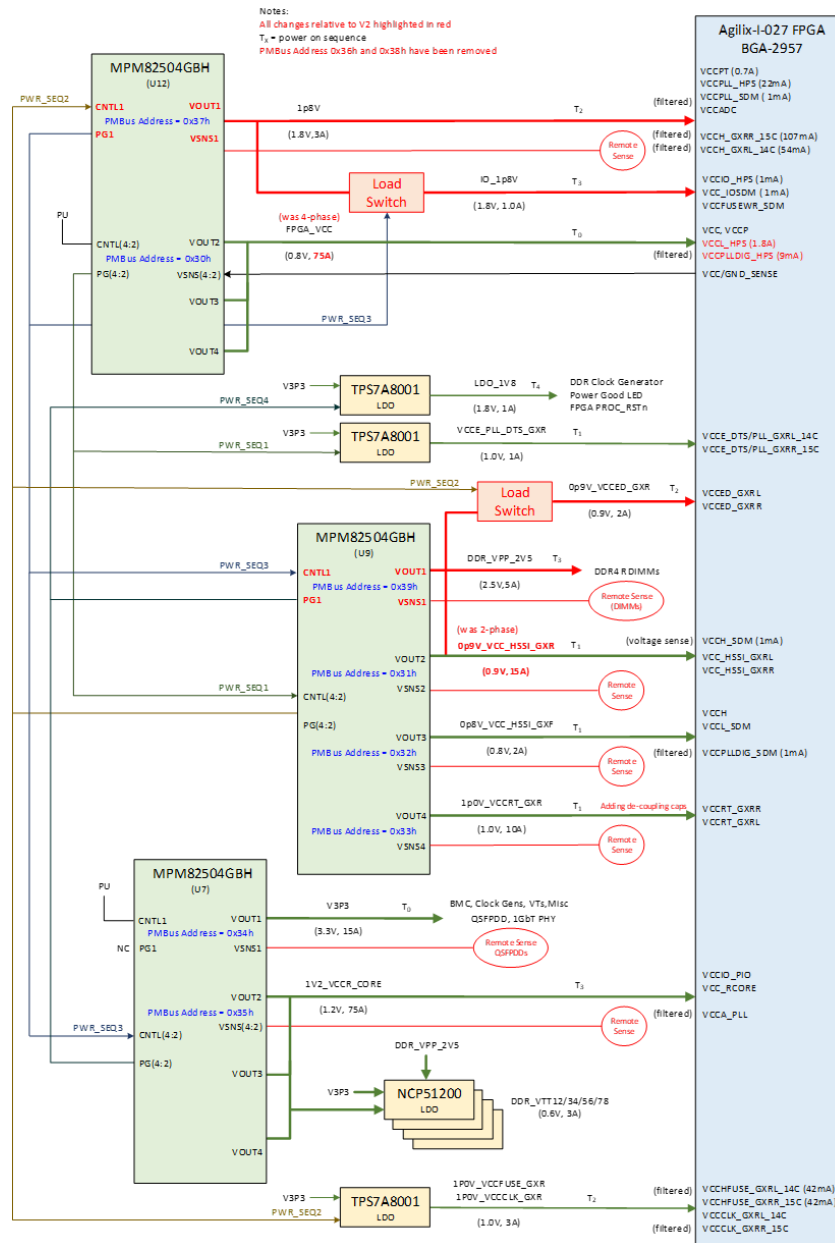


Figure 17. DC Power Diagram

8.9 CMA Blade Connector

The CMA Blade controller connects to the base plane with a single orthogonal right angle connector combining power and I/O.

- Molex 171574-7837

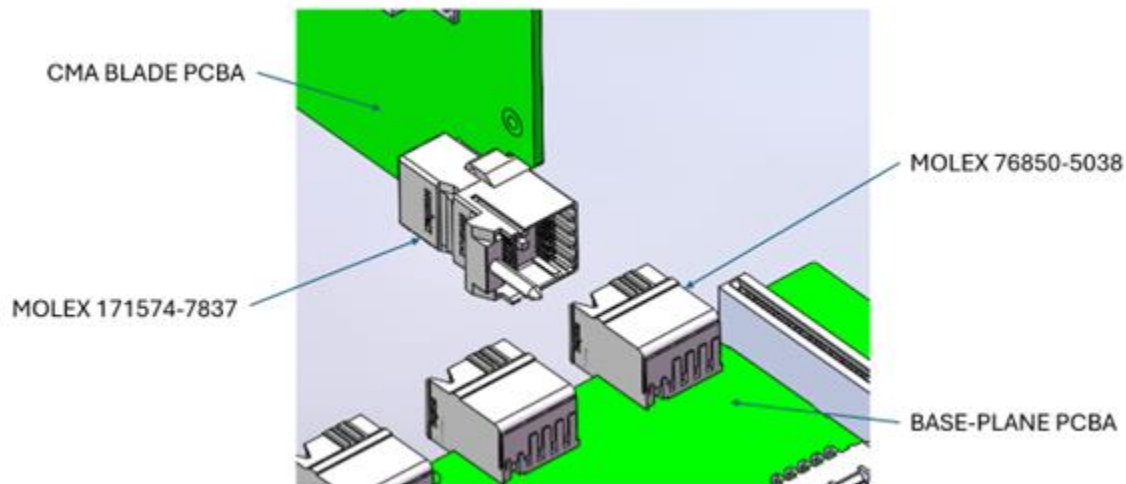


Figure 18. Molex Connector Blade to Base-Plane Matin

ACE PCBA Pin Number		Midplane PCBA Pin Number		ORTHO PIN MAPPING			
				POSITION 270° (OD RAM - RAF)			
A1-A1	A2-B1	A3-D1	A4-E1	A5-G1	A6-H1	A7-K1	A8-L1
B1-A2	B2-C1	B3-D2	B4-F1	B5-G2	B6-J1	B7-K2	B8-M1
C1-B2	C2-C2	C3-E2	C4-F2	C5-H2	C6-J2	C7-L2	C8-M2
D1-A3	D2-B3	D3-D3	D4-E3	D5-G3	D6-H3	D7-K3	D8-L3
E1-A4	E2-C3	E3-D4	E4-F3	E5-G4	E6-J3	E7-K4	E8-M3
F1-B4	F2-C4	F3-E4	F4-F4	F5-H4	F6-J4	F7-L4	F8-M4
G1-A5	G2-B5	G3-D5	G4-E5	G5-G5	G6-H5	G7-K5	G8-L5
H1-A6	H2-C5	H3-D6	H4-F5	H5-G6	H6-J5	H7-K6	H8-M5
J1-B6	J2-C6	J3-E6	J4-F6	J5-H6	J6-J6	J7-L6	J8-M6
K1-A7	K2-B7	K3-D7	K4-E7	K5-G7	K6-H7	K7-K7	K8-L7
L1-A8	L2-C7	L3-D8	L4-F7	L5-G8	L6-J7	L7-K8	L8-M7
M1-B8	M2-C8	M3-E8	M4-F8	M5-H8	M6-J8	M7-L8	M8-M8

NOTE: PINOUTS SHOWN IN BALLOONS ARE GROUNDS.
GROUND PATHS ARE NOT DISCRETE CIRCUITS.

Figure 19. Blade to Base-Plane Connectors Pin-Out

8.10 CMA Blade Connector Signal Table

The connector signal table below references I/O type relative to the base plane:

Pin No	Signal Name	Pin No	Signal Name	Pin No	Signal Name
A2	12VIN	A1	Ground	G2	BMC_VGAHS_GPIO2
A4	12VIN	A3	Ground	G4	BMC_PWRGD
A6	12VIN	A5	Ground	G6	NC
A8	12VIN	A7	Ground	G8	NC
B1	12VIN	C2	Ground	H1	BMC_I2C8_GPIO27
B2	12VIN	C4	Ground	H2	SLOT_PRSENT#
B3	12VIN	C6	Ground	H3	BMC_RESET#
B4	12VIN	C8	Ground	H4	BMC_GPIO1_SGPMI
B5	12VIN	D1	Ground	H5	NC
B6	12VIN	D3	Ground	H6	BMC_PWM7_GPIO18
B7	12VIN	D5	Ground	H7	BMC_PWM3_GPIO14_YEL_LED
B8	12VIN	D7	Ground	H8	BMC_PWM1_GPIO12_GEN_LED
C1	12VIN	F2	Ground	J1	BMC_GPIO49
C3	12VIN	F4	Ground	J3	BMC_CPU_RST#
C5	12VIN	F6	Ground	J5	NC
C7	12VIN	F8	Ground	J7	NC
D2	12VIN	G1	Ground	K2	BMC_SPI1MOSI_IO0_GP03
D4	12VIN	G3	Ground	K4	BMC_JTAG1TDI
D6	12VIN	G5	Ground	K6	BMC_I2C2SCL_GPIO67
D8	RSVD_BP_12VSB	G7	Ground	K8	NC
E1	12VIN	J2	Ground	L1	BMCSP11CK_GPIO122
E2	12VIN	J4	Ground	L2	BMC_SPI1MISO_IO1_GP04
E3	12VIN	J6	Ground	L3	BMC_JTAG1TCK
E4	12VIN	J8	Ground	L4	BMC_JTAG1TDO
E5	12VIN	K1	Ground	L5	BMC_I2C1SCL_GPIO90
E6	12VIN	K3	Ground	L6	BMC_I2C2SDA_GPIO89
E7	RSVD_BP_12VSB	K5	Ground	L7	NC
E8	RSVD_BP_12VSB	K7	Ground	L8	NC
F1	12VIN	M2	Ground	M1	BMC_SPI1CS0#_GPIO116
F3	12VIN	M4	Ground	M3	BMC_JTAG1TMS
F5	12VIN	M6	Ground	M5	BMC_I2C1SDA_GPIO92
F7	RSVD_BP_12VSB	M8	Ground	M7	NC

Table 3. Pin/signal table for CMA blade Molex connector 171574837

8.11 CMA Common Slot I/O Connector

These signals are common across all 8 slots:

Signal Name	I/O Type	Description	Pin Number
SLOT ID (2:0)	Output 3.3V	Base Plane Slot ID These pins are routed to BMC GPIO (General Purpose Input Output) on the controller The base plane either grounds or pulls up to for slots 0 through 7	A5, A6, B6
SLOT_PRESENT_L	Input	Controller Present (mated) Pin connects to ground through a 1K pull down on the controller. Connects to a resistor divider RC debounce circuit that enables the base plane 12V slot hot swap circuit	C5
BMC_RESET_L	Output 3.3V	BMC Main Reset Active low reset from the base plane CPLD Routes on the controller to the BMC module	D6
BMC_CPU_RST_L	Output 3.3V	BMC Processor Reset Active low reset from the base plane CPLD Routes on the controller to the BMC module	E6
BMC_PWRGD	Output 3.3V	BMC Input Power Good Active high from the base plane CPLD. Indicates the 12V and 3.3V power to the BMC module on the controller are good.	E5
12V	Output	Main 12V Power Hot swap over-current protected (20A trip) 12V power to the controller. Each slot has its own independent hot swap circuit	A2, A4, A6, A8, B1-B8, C1, C3, C5, C7, D2, D4, D6, D8, E1-E8, F1, F3, F5,
12VSB	Output	Standby 12V Power Reserved pins, not connected	D8, E7, E8, F7
VSS	Return	Digital Ground	A1, A3, A5, A7, C2, C4, C6, C8, D1, D3, D5, D7, F2, F4, F6, F8, G1-G3, G5, G7, J2, J4, J6, J8, K1, K3, K5, K7, M2, M4, M6, M8

Table 4. Base-Plane Common Slot I/O

8.12 Blade Slot-0 I/O Connector

Unique signals to slot 0. The controller installed in slot-0 manages the enclosure:

Signal Name	I/O Type	Description	Pin Number
SPI_BMC_SCLK	Input 3.3V	SPI Serial Clock This 16MHz SPI serial clock is driven from the BMC SPI initiator to the base plane CPLD target	L1
SPI_BMC_CS_L	Input 3.3V	SPI Chip Select This active low chip select is driven from the BMC SPI initiator to the base plane CPLD target	M1
SPI_BMC_MOSI	Input 3.3V	SPI Serial Data Output This is the BMC SPI initiator output data signal driven to the base plane CPLD target input	K2
SPI_BMC_MISO	Output 3.3V	SPI Serial Data Input This is the BMC SPI initiator input data signal driven from the base plane CPLD target output	L2
JTAG_BMC_TCK	Input 3.3V	JTAG Clock This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	L3
JTAG_BMC_TMS	Input 3.3V	JTAG TMS This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	M3
JTAG_BMC_TDI	Input 3.3V	JTAG Data Input This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	K4
JTAG_BMC_TDO	Output 3.3V	JTAG Data Output This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	L4
I2C_BP1_SCL	Input 3.3V	I2C Clock Bus 1 This 100KHz serial clock is driven from the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus 1	L5
I2C_BP1_SDA	Bi-Dir 3.3V	I2C Data Bus 1 This serial data signal connects the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus 1	M5
I2C_BP2_SCL	Input 3.3V	I2C Clock Bus 2 This 100KHz serial clock is driven from the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus 2	K6
I2C_BP2_SDA	Bi-Dir 3.3V	I2C Data Bus 2 This serial data signal connects the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus2	L6
CPLD_GPIO (3:15)	Bi-Dir 3.3V	General Purpose I/O These signals connect to the base plane CPLD. Some of these connect to the BMC on the controller. All are reserved and not defined for any functionality	G6, G8, H4-H8, J5, J7

Table 5. Slot-0 I/O

9. Base Plane

The CMA enclosure base plane assembly 60-00000616 provides 12V power to up to 8x CMA Blade controller blades. The plane includes a CPLD and I2C interfaces that support the slot 0 BMC to management.

Power Supplies and Fans:

- Adapter boards 60-00000617 for CRSP FRU connectivity
- Fan presence, PWM/TACH and eFuse 12V over-current protection (9.7A trip per rotor)

CPLD functions:

- SPI (Serial Peripheral Interface) target interface for register access and JTAG (Joint Test Action Group) target port for programming
- Slot presence detect and 12V hot swap enable.
 - Each slot is 12V over current protected (20A trip) with a hot swap circuit.
 - PSU and Fan FRU management

Redundant I2C Bus Interfaces (Slot 0 only):

- Redundant temperature sensors and VPD EEPROMs
- CRPS PMBus

9.1 Blade to Base-Plane Block Diagram

The diagram below illustrates the CMA Blade controller blade slot 0 management interface to the base plane CPLD. The CPLD can be on-board programmed from a Lattice dongle or in-system from the BMC.

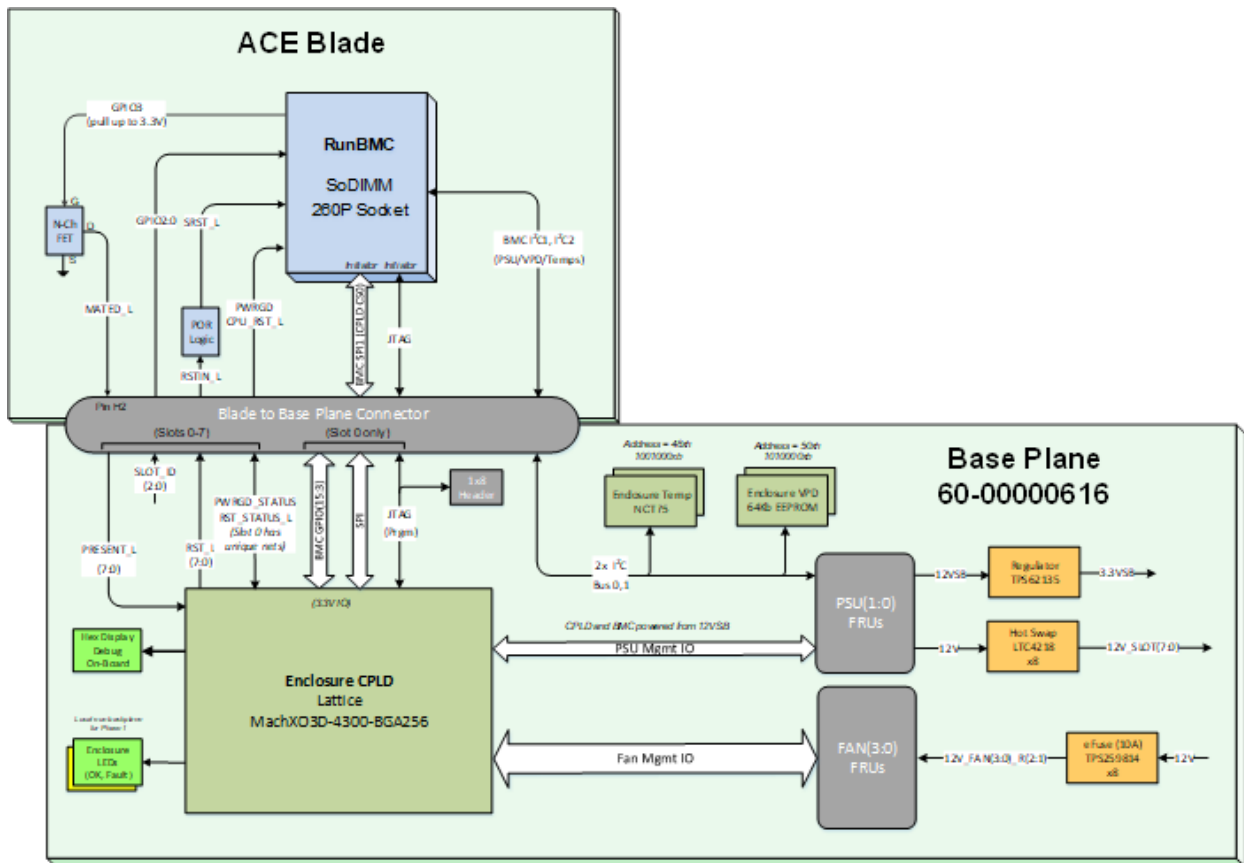


Figure 20. Base Plane Block Diagram

9.2 Base Plane PCB Design

The diagram below is a macro view of the PCB.

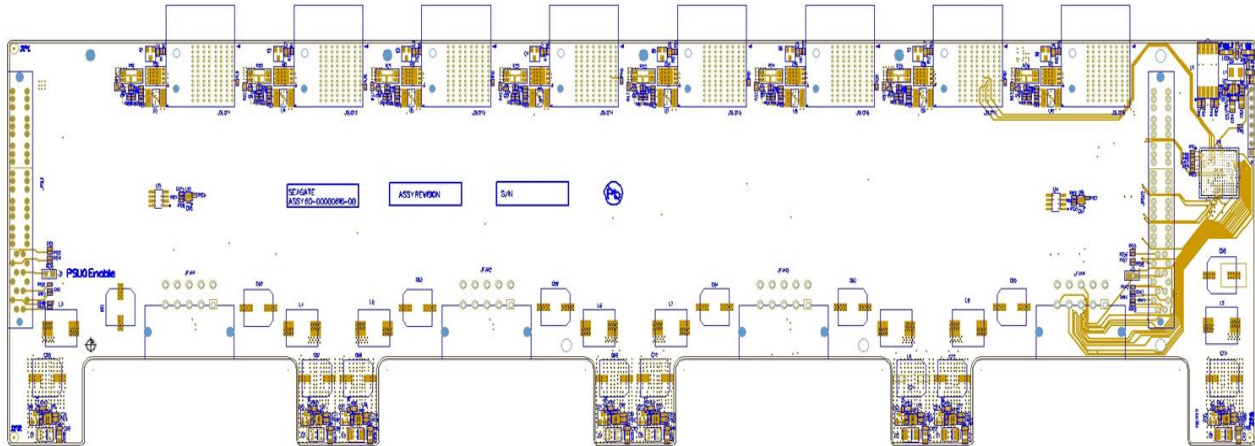


Figure 21. Base (PCB) Plane Macro Layout

9.3 Base-Plane Outline and Stack Up

The diagrams below are taken from the 61-00000616-00 fab drawing. The PCB outline is 4.429 x 17.362 inches. The PCB is fabricated with a standard cost-effective material, 370HR.

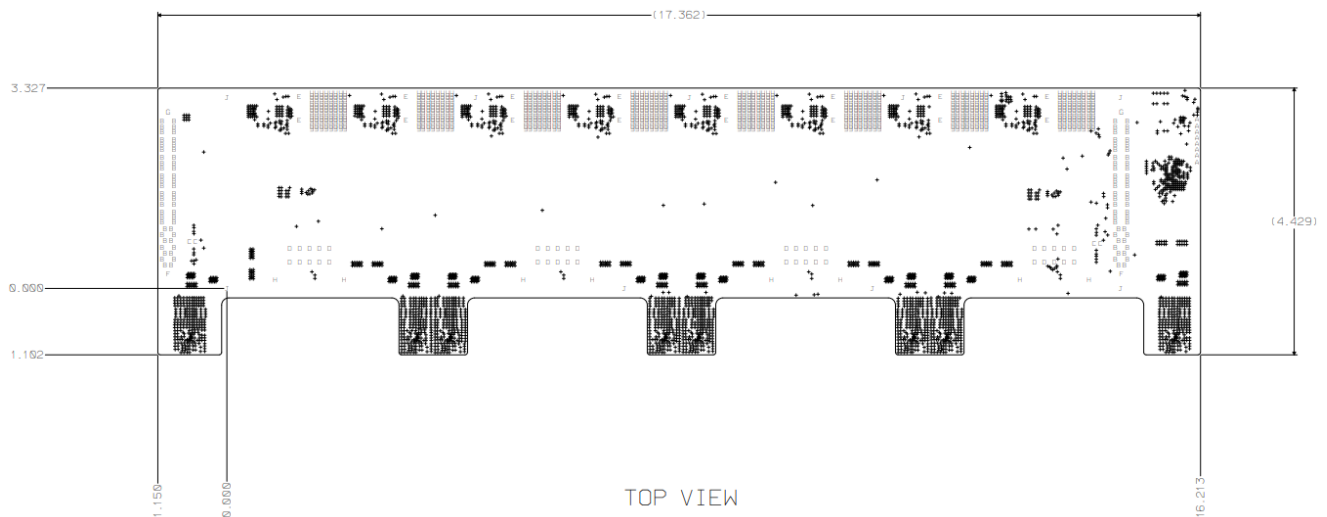


Figure 22. Base-Plane PCB Dimensions

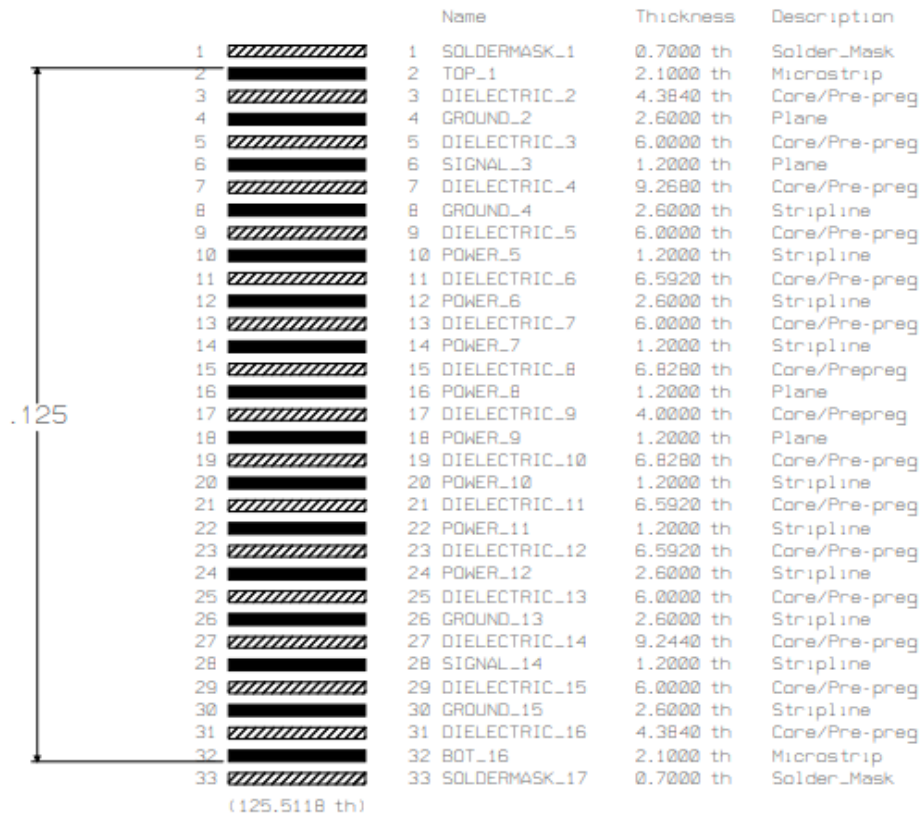


Figure 23. Base (PCB) Plane Macro Outline and Stack-up

IMPEDANCE CHART		
85 OHM DIFFERENTIAL +/- 10%		50 OHM SINGLE ENDED +/- 10%
LAYER	TRACE/SPACE/TRACE (MILS)	TRACE WIDTH (MILS)
1, 16	NONE	7.75
3, 14	NONE	6.5
5, 7, 10, 11	NONE	6.0

Figure 24. Base Plane Impedance

9.4 Base-Plane Connectors

The CMA Blade controller connects to the base plane with a single orthogonal right angle connector combining power and I/O.

Controller Connector

ACE PCBA
Pin Number

↓

Midplane PCBA
Pin Number

↓

ORTHO PIN MAPPING POSITION 270° (OD RAM - RAF)							
(A1-A1)	A2-B1	(A3-D1)	A4-E1	(A5-G1)	A6-H1	(A7-K1)	A8-L1
B1-A2	B2-C1	B3-D2	B4-F1	B5-G2	B6-J1	B7-K2	B8-M1
C1-B2	(C2-C2)	C3-E2	(C4-F2)	C5-H2	(C6-J2)	C7-L2	(C8-M2)
(D1-A3)	D2-B3	(D3-D3)	D4-E3	(D5-G3)	D6-H3	(D7-K3)	D8-L3
E1-A4	E2-C3	E3-D4	E4-F3	E5-G4	E6-J3	E7-K4	E8-M3
F1-B4	(F2-C4)	F3-E4	(F4-F4)	F5-H4	(F6-J4)	F7-L4	(F8-M4)
(G1-A5)	G2-B5	(G3-D5)	G4-E5	(G5-G5)	G6-H5	(G7-K5)	G8-L5
H1-A6	H2-C5	H3-D6	H4-F5	H5-G6	H6-J5	H7-K6	H8-M5
J1-B6	(J2-C6)	J3-E6	(J4-F6)	J5-H6	(J6-J6)	J7-L6	(J8-M6)
(K1-A7)	K2-B7	(K3-D7)	K4-E7	(K5-G7)	K6-H7	(K7-K7)	K8-L7
L1-A8	L2-C7	L3-D8	L4-F7	L5-G8	L6-J7	L7-K8	L8-M7
M1-B8	(M2-C8)	M3-E8	(M4-F8)	M5-H8	(M6-J8)	M7-L8	(M8-M8)

NOTE: PINOUTS SHOWN IN BALLOONS ARE GROUNDS.
GROUND PATHS ARE NOT DISCRETE CIRCUITS.

Figure 25. Blade to Base-Plane Connectors Pin-Out

- A single connector per controller combining both power and I/O is used to minimize board area and air flow impedance. (CONN, IMPACT, 4x8, 32 Diff Pair)

The connector signal table below references I/O type relative to the midplane:

Pin No	Signal Name	Pin No	Signal Name	Pin No	Signal Name
B1	12VIN	A1	Ground	B5	BMC_VGAHS_GPIO2
E4	12VIN	D1	Ground	E5	BMC_PWRGD
H1	12VIN	G1	Ground	H5	NC
L1	12VIN	K1	Ground	L5	NC
A2	12VIN	C2	Ground	A6	BMC_I2C8_GPIO27
C1	12VIN	F2	Ground	C5	SLOT_PRSNT#
D2	12VIN	J2	Ground	D6	BMC_RESET#
F1	12VIN	M2	Ground	F5	BMC_GPIO1_SGPMI
G2	12VIN	A3	Ground	G6	NC
J1	12VIN	D3	Ground	J5	BMC_PWM7_GPIO18
K2	12VIN	G3	Ground	K6	BMC_PWM3_GPIO14_YEL_LED
M1	12VIN	K3	Ground	M5	BMC_PWM1_GPIO12_GEN_LED
B2	12VIN	C4	Ground	B6	BMC_GPIO49
E2	12VIN	F4	Ground	E6	BMC_CPU_RST#
H2	12VIN	J4	Ground	H6	NC
L2	12VIN	M4	Ground	L6	NC
B3	12VIN	A5	Ground	B7	BMC_SPI1MOSI_IO0_GP03
E3	12VIN	D5	Ground	E7	BMC_JTAG1TDI
H3	12VIN	G5	Ground	H7	BMC_I2C2SCL_GPIO67
L3	RSVD_BP_12VSB	K5	Ground	L7	NC
A4	12VIN	C6	Ground	A8	BMCSP1CK_GPIO122
C3	12VIN	F6	Ground	C7	BMC_SPI1MISO_IO1_GP04
D4	12VIN	J6	Ground	D8	BMC_JTAG1TCK
F3	12VIN	M6	Ground	F7	BMC_JTAG1TDO
G4	12VIN	A7	Ground	G8	BMC_I2C1SCL_GPIO90
J3	12VIN	D7	Ground	J7	BMC_I2C2SDA_GPIO89
K4	RSVD_BP_12VSB	G7	Ground	K8	NC
M3	RSVD_BP_12VSB	K7	Ground	M7	NC
B4	12VIN	C8	Ground	B8	BMC_SPI1CS0#_GPIO116
E4	12VIN	F8	Ground	E8	BMC_JTAG1TMS
H4	12VIN	J8	Ground	H8	BMC_I2C1SDA_GPIO92
L4	RSVD_BP_12VSB	M8	Ground	L8	NC

Table 6. Pin/Signal table for Baseplane Molex connector 76850-5038

9.5 Base-Plane Common Slot I/O Connector

These signals are common across all 8 slots:

Signal Name	I/O Type	Description	Midplane Pin Number
SLOT ID (2:0)	Output 3.3V	Base Plane Slot ID These pins are routed to BMC GPIO (General Purpose Input Output) on the controller The base plane either grounds or pulls up to for slots 0 through 7	G1, H1, J1
SLOT_PRESENT_L	Input	Controller Present (mated) Pin connects to ground through a 1K pull down on the controller. Connects to a resistor divider RC debounce circuit that enables the base plane 12V slot hot swap circuit	H2
BMC_RESET_L	Output 3.3V	BMC Main Reset Active low reset from the base plane CPLD Routes on the controller to the BMC module	H3
BMC_CPU_RST_L	Output 3.3V	BMC Processor Reset Active low reset from the base plane CPLD Routes on the controller to the BMC module	J3
BMC_PWRGD	Output 3.3V	BMC Input Power Good Active high from the base plane CPLD Indicates the 12V and 3.3V power to the BMC module on the controller are good	G4
12V	Output	Main 12V Power Hot swap over-current protected (20A trip) 12V power to the controller. Each slot has its own independent hot swap circuit	A2, A4, A6, A8, B1-B8, C1, C3, C5, C7, D2, D4, D6, D8, E1-E8, F1, F3, F5
12VSB	Output	Standby 12V Power Reserved pins, not connected	D8, E7, E8, F7
VSS	Return	Digital Ground	A1, A3, A5, A7, D1, D3, D5, D7, G1, G3, G5, G7, K1, K3, K5, K7, C2, C4, C6, C8, F2, F4, F6, F8, J2, J4, J6, J8, M2, M4, M6, M8

Table 7. Base-Plane Common Slot I/O

9.6 Base-Plane Slot-0 I/O Connector

Unique signals to slot 0. The controller installed in slot-0 manages the enclosure:

Signal Name	I/O Type	Description	Pin Number
SPI_BMC_SCLK	Input 3.3V	SPI Serial Clock This 16MHz SPI serial clock is driven from the BMC SPI initiator to the base plane CPLD target	A8
SPI_BMC_CS_L	Input 3.3V	SPI Chip Select This active low chip select is driven from the BMC SPI initiator to the base plane CPLD target	B8
SPI_BMC_MOSI	Input 3.3V	SPI Serial Data Output This is the BMC SPI initiator output data signal driven to the base plane CPLD target input	B7
SPI_BMC_MISO	Output 3.3V	SPI Serial Data Input This is the BMC SPI initiator input data signal driven from the base plane CPLD target output	C7
JTAG_BMC_TCK	Input 3.3V	JTAG Clock This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	D8
JTAG_BMC_TMS	Input 3.3V	JTAG TMS This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	E8
JTAG_BMC_TDI	Input 3.3V	JTAG Data Input This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	E7
JTAG_BMC_TDO	Output 3.3V	JTAG Data Output This BMC JTAG initiator connects to the CPLD. The JTAG interface is used for CPLD programming	F7
I2C_BP1_SCL	Input 3.3V	I2C Clock Bus 1 This 100KHz serial clock is driven from the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus 1	G8
I2C_BP1_SDA	Bi-Dir 3.3V	I2C Data Bus 1 This serial data signal connects the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus 1	M5
I2C_BP2_SCL	Input 3.3V	I2C Clock Bus 2 This 100KHz serial clock is driven from the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus 2	H7
I2C_BP2_SDA	Bi-Dir 3.3V	I2C Data Bus 2 This serial data signal connects the BMC SPI initiator to the base plane VPD EEPROM, Temperature Sensor and Power Supply on bus2	J7

CPLD_GPIO (3:15)	Bi-Dir 3.3V	General Purpose I/O These signals connect to the base plane CPLD. Some of these connect to the BMC on the controller. All are reserved and not defined for any functionality	F5, G6, H5, H6, J5, K6, K8, L5-L8, M5, M7
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Table 8. Slot-0 I/O

9.7 Power Supply Connector

The Common Redundant Power Supply (CRPS) module connects through a passive adapter board, 60-00000617-00-01. The adapter connects to the base plane via edge.

- Amphenol 10160829-001LK
- CONN, Power Card Edge, 2x7, 2x6, Vert, PF

The original CRPS standard specs were owned by Intel and specs are not public documents, copy is per request basis. There is a new OCP M-CRPS Base Specification that is public domain. This spec defines the same pin out definition and footprint as the original CRSP. <https://www.opencompute.org/w/index.php?title=Server/MHS>

9.8 Fan Connector I/O

Each fan module contains two fan rotors. The Fan module connects to the base plane and is managed from the CPLD.

- Molex 43810-0092
- CONN, 10-Pin Header, 4.2mm Pitch, Dual Row, Clip, RA, TH

The connector signal table below references I/O type relative to the base plane. These signals are common across all 4 slots.

Signal Name	I/O Type	Description	Pin Number
FAN_R0_12V	Output	Fan Rotor 0 Power This 12V power is eFuse over current protected with a 9.7A trip setting. The eFuse enable is controlled by the CPLD. Fan rotor 0 has its own unique fused 12V input	1
VSS	Return	Digital Ground	2, 6, 10
PWM_L	Output 3.3V	Pulse Width Modulation This signal is an input to both fan rotors in the FRU. It is FET isolated and pulled up to 3.3V via a 10K ohm resistor	3
FAN_PRESENT_L	Input	Fan Module Present This active low presence signal routes to the CPLD, which has an internal pull up	4
TACH_R0	Input	Fan Rotor 0 Tachometer (Inlet) This signal is an input to the CPLD. It is pulse modulated decoded in registers read by the BMC	5
FAN_LED	Output 3.3V	Fan Fault LED This LED control signal is used to indicate a Fan module fault. The signal is driven from the CPLD	7
TACH_R1	Input	Fan Rotor 1 Tachometer (Outlet) This signal is an input to the CPLD. It is pulse modulated decoded in registers read by the BMC	8
FAN_R1_12V	Output	Fan Rotor 1 Power This 12V power is eFuse over current protected with a 9.7A trip setting. The eFuse enable is controlled by the CPLD. Fan rotor 1 has its own unique fused 12V input	9

Table 9. Connector Signal Table

10. Electrical Requirements

10.1 Base Plane CPLD

These sections describe CMA base plane CPLD interfaces and registers for the CMA Blade BMC. Only the CMA Blade board plugged into slot 0 has CPLD register access via a 4-wire SPI interface. All 8 slots have hot swap power enable, and presence detect.

10.2 SPI Protocol

The BMC ad/write access, Mode 3 (CPOL = 1, CPHA = 1), it is recommended to not exceed 25MHz. It SPI host port accesses CPLD registers from a single target port on the CPLD. The interface operates in single bit mode (MISO/MOSI). The CPLD SPI Interface is designed for byte only re supports two opcodes, Opcode 2 = Write Byte, Opcode 3 = Read Byte. Protocol supports MSB as first bit of the Instruction shifted out first, followed by a 24-bit address MSB then data is shifted out or in depending on Opcode. Timing diagrams are shown below.

10.3 HEX Display

In the CMA IOM, there is a 7-segment controlled by the CPLD to indicate fault in one of the voltage regulators. Below is a chart to show the possible power on states for corresponding power fault when the 7-segment display is displaying them and stuck.

PON State	Voltage Rail	Comments
N/A	PWROK_3.3VSB	If nothing is being displayed, then 3.3VSB is down
PON_ST0	PWROK_1.8VSB	Stuck in state 0, when 1.8VSB is not good
PON_ST1	PSU_PRESENT_N	Stuck in state 1, when neither PSU is present
PON_ST2	PSU_PWROK	Stuck in state 2, when power good on neither PSU
PON_ST3	SYS_3.3V_PWROK	Stuck in state 3, when system 3.3V is not good
PON_ST4	SFP_3.3V_PWROK	Stuck in state 4, when SFP cable is plugged in, and SFP 3.3V is not good
PON_ST5	FPGA_CORE_PWROK, FPGA_0v9_PWROK	Stuck in state 5, when FPGA core or 0.9v power not good, or both not good
PON_ST6	FPGA_1v2_PWROK, FPGA_1v8_PWROK	Stuck in state 6, when FPGA 1.2V or 1.8V power not good, or both not good
PON_ST7	Normal Functional State	Display '7' is the normal functional behavior

Table 10. Power Fault Indicators in CMA IOM

The BMC module, 60-00000588-01-01, is designed around the Open Compute Project (OCP) RunBMC Daughterboard Card Design Specification_v1.4.1. The BMC takes over as the out-of-band user interface management controller for the CMA Blade memory aggregator. The Slot 0 controller also acts as the CMA enclosure manager. The module plugs into an SoDIMM 260-pin socket on the CMA Blade main board.

The diagram illustrates the internal architecture of the ASPEED AST2620 iRMP. Key components and connections include:

- Power Management:**
 - 12V input feeds three TPS62135 Switching Regulators (1.8V, 1.0V Core, 1.2V VDDQ) and a Voltage Switch.
 - 3.3V input feeds an LDO (0.6V VTT) and another LDO (2.5V VPP).
 - 1.8V (1.0A), 1.0V Core (1.0A), 1.2V VDDQ (3.0A), 0.6V VTT (+/- 3A), and 2.5V VPP (0.5A) are distributed to various internal blocks.
- Storage and Memory:**
 - 25MHz OSC and ARM JTAG (2x6, 1.27mm) connect to the JTAG Slave.
 - eMMC 16GB (Kioxia TH GAMR G7T13BAIL) connects via eMMC 5.1 x8 Up to HS200 to the eMMC 1.8V IO.
 - DDR4 512Mx16 (Micron MT40A512M16LY-07E5E) connects via DDR4-1600 w/ECC to the DD-R4, allocating 8 bits of ECC memory for each 94 bits of code/data memory.
 - BMC EEPROM AT24008 and Temp Sensor NCT75 connect to the I2C Local bus.
- Internal Blocks and I/O:**
 - ASPEED AST2620 iRMP:** Dual ARM Cortex A7 1.2GHz.
 - FW SPI Master:** QSPI CS1 (Secondary Boot Flash).
 - SPI1 Master:** QSPI1 CS0/1 (CPUD/TPM).
 - SPI2 Master:** SPI CS0 (SYS Rsvd).
 - SQPIO Master:** SQPIO (CPUD Rsvd).
 - JTAG Master:** JTAG (CPUD Programming).
 - LPC Slave:** LPC (CPUD Rsvd).
 - MAC1 1.8V IO:** RGMII (MDI PHY - Ext RJ45).
 - MAC2 1.8V IO:** RGMII (SOM PHY-BMC ICL).
 - MAC3 1.8V IO:** RGMII (Expander - SAS IOM).
 - GPIO:** GPIO (CPUD - 20.0, RST Stat, WDT1/2, PWRGD, Temp Alert).
 - I2C:** I2C1-2 (I2C (Encl Mgmt - Midplane)), I2C3 (I2C (SAS Expander Temp Sensor, NVMe AIC Socket)), I2C4,9 (I2C (SoC/FRUID EEPROMs)), I2C5,6,8,10 (I2C (External Host Ports)), I2C7 (I2C (CPUD Rsvd)).
 - UART:** UART1, UART5 (UART (CLI / Debug)).
 - PCIE:** PCIE RC (PCle Gen2 x1 (Root Complex)), PCIE EP (PCle Gen2 x1 (End Point)), PCIE Analog MUX (PCle Gen2 x1 (NVMe IOM)).
 - Reset:** RST Delay (BMC_RESET_L, 1.0V PWR OK).
 - Status LED:** Status LED.
- External Interfaces:**
 - RunBMC Card Edge:** Connects to the RunBMC Card Edge.
 - SoDIMM 260P:** Connects to the SoDIMM 260P.

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10.5 BMC - Board Management Controller, Physical Layout

The 61-00000588-01 PCB layout is shown below. The layout meets the 50mm height 260P SoDIMM mechanical constraint.

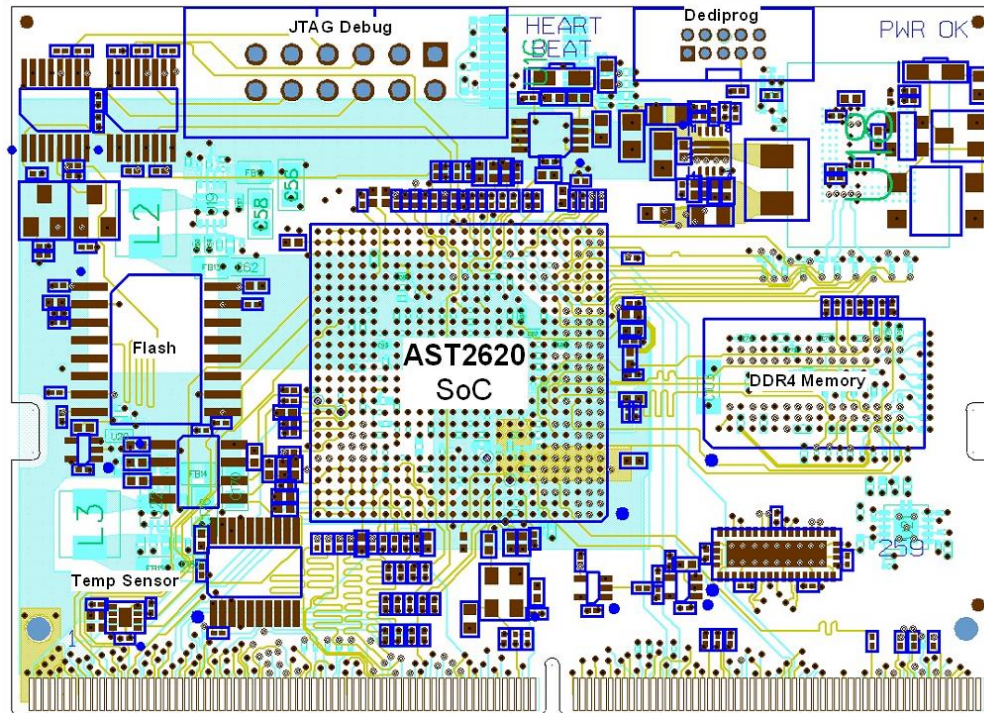


Figure 27. BMC Physical Layout

10.6 BMC - Board Management Controller, PCBA Debug Features

There are two LEDs on-board for power OK and SoC heartbeat. These are a visual aid for open frame debug and Mfg BFT.

There is a SoC reset push button on the module. This can be used for SW developers in open frame configurations to reset the AST2620.

Both the JTAG debug and Dediprog headers are populated on EB platforms for development and test. They are not stuffed for all operations builds (OB) and production.

10.7 BMC - Board Management Controller, Mechanical Constraints

The 60-00000588 BMC module adheres to the physical requirements of the OCP RunBMC specification SoDIMM mechanical definition. The board is designed to meet the “large” form factor 50mm height that is defined by the So-DIMM DDR4 JDEC registration.

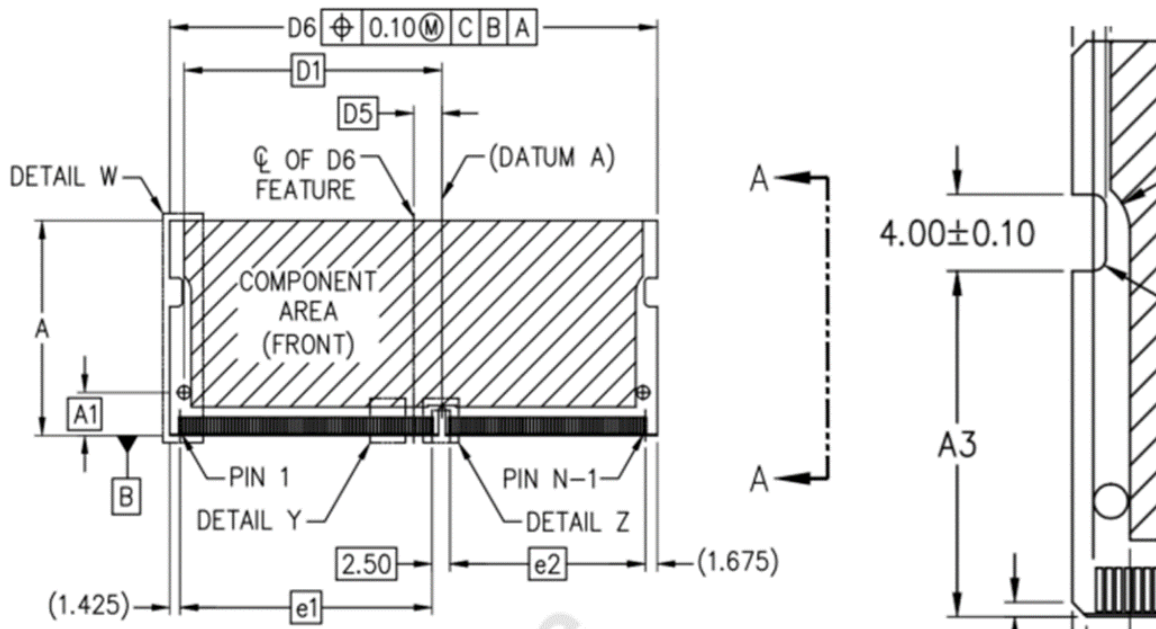


Figure 28. BMC Mechanical Constraints Outline

The RunBMC specification defines modules as having major components on the top side of the PCB with component height to not exceed dimension E1 in Figure below. Smaller components with low height are placed on the bottom, and not exceeding E2.

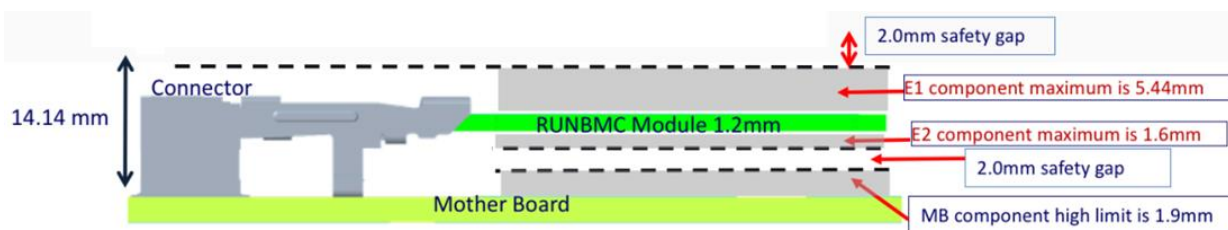


Figure 29. BMC Mechanical Constraints Outline #2

Design Note: The blade board uses a 9.25mm height right angle socket.

10.8 BMC - Board Management Controller, AST2620 SoC

The ASPEED AST2620 System-On-Chip processor was selected for the BMC application.

- CPU: 1.2GHz dual-core Cortex A7 32-bit
- Hardware Secure Boot
- PCIe Gen2 x1 (NVMe application)
- DDR4-1600 16-bit single device (allocates 8 bits of ECC memory for each 64 bits of code/data memory)
- BMC only (no VGA/KVM)
- Power 2.13W peak, TFBGA-624P 21x21mm, 0.8mm

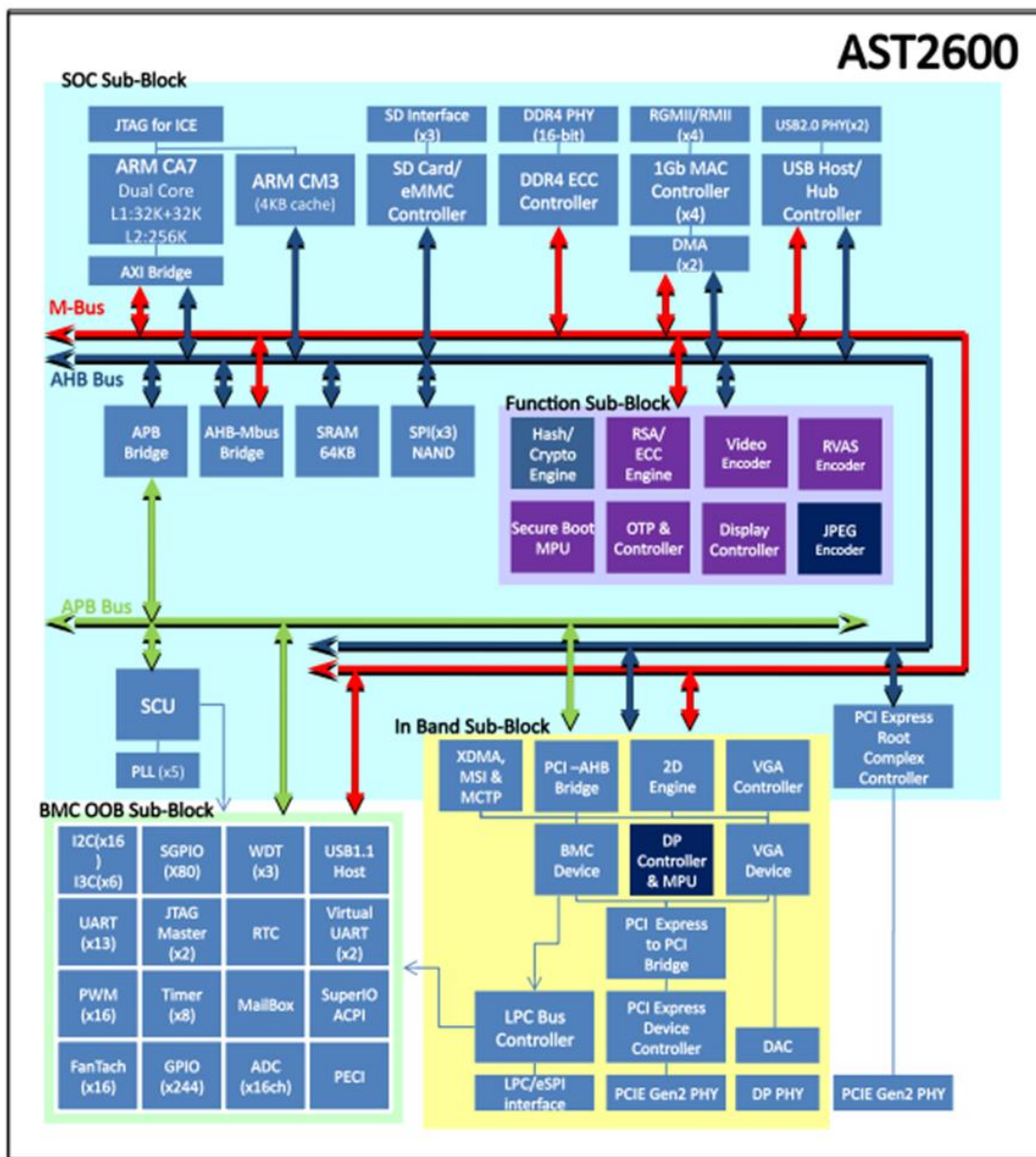


Figure 30. Block Diagram to AST2620

10.9 BMC, AST2620 Power Sequencing Requirement, Electrical or Firmware

CPLD output signal BMC_PWRGD_STATUS is equal to a direct connection of the PWROK_3.3VSB from the 3.3V standby regulator driven from VP_12VSB. BMC_PWRGD_STATUS is an open drain output from the CPLD.

10.10 BMC, AST2620 Clocks

The BMC board has a 25MHz oscillator that drives the AST2620. Internally in the AST2620 there is a PLL that generates the DDR4 clock domain equivalent 800MHz. There is also a SPI clock that operates below 100MHz. The AST2620 has an internal 1.2GHz dual-core ARM Cortex A7 also derived from an internal PLL.

10.11 BMC, AST2620 External Peripherals

The memory devices defined below are listed in AST2600_Aproved_Vendor_List_v04 document.

10.12 BMC, AST2620 Boot Flash

The BMC boots from a 512Mbit QSPI Flash on the module. The Flash is connected to the AST2620 FWSPI chip select CS0#.

Winbond W25Q512JVFIM

- 512Mbit (32Mbyte)
- VCC / VIO 3.3V
- Supports up to 104MHz operation
- SOIC16 package with active-low reset
- 100K program-erase cycle endurance

Reference data sheet for flexible sector architecture.

Design Note: There is an on-board 2x6 0.1 inch (2.54mm pin pitch) shrouded keyed header for Dediprog SF600 on-board Flash re-programming. The MUX circuitry on-board automatically handles the switching between AST2620 FWSPI bus and the Dediprog programming adapter. Dediprog provides a simple user-friendly method for recovering or updating Flash without any need for the EJTAG interface or a boot recovery watch dog disabling.

10.13 BMC, AST2620 Non-Volatile Memory

An embedded Multi-Media Card JEDEC v5.1 compatible 16GByte device is on-board. The interface will operate up to HS-200 data rate.

KIOXIA THGBMHG7C1LBAIL

- 16GByte
- VCC 3.3V, VCCQ 1.8V
- Supports up to 100MB/s enhanced mode (PSLC) sequential write operation
- 11.5 x 13mm BGA153 package

Reference data sheet for eMMC JEDEC v5.1 programming interface standard.

10.14 BMC, AST2620 DDR4 Memory

A single 512Mx16 DDR4 memory device is on-board. The AST2620 interface will operate up to DDR4-1600 speed.

Micron MT40A512M16LY-075

- 1GByte
- 512Mx16 8Gb device density
- CL=18
- PCB design supports 10 x 13mm FBGA96 package

10.15 BMC, Local I2C Devices

The on-board I2C devices listed below are connected to the AST2620 SCL/SDA bus 12.

10.16 BMC, VPD / FRUID EEPROM

There is an on-module EEPROM connected to the AST2620.

Target Device	Target Address	Comments
On-board serial EEPROM AT24C64D	A0h (0x50 7-bit) (1010,000X/b)	Serial EEPROM for controller VPD/FRUID (8Kbit)

Table 11. EEPROM Address Mapping

10.17 BMC, temperature Sensor

There is an on-module temperature sensor IC connected to the AST2620.

Target Device	Target Address	Comments
Temperature Sensor NCT75	98h (0x4C 7-bit) (1001,100X)	On-board module temperature sensor

Table 12. Temperature Sensor Target Address

10.18 BMC, SoC Interfaces - Interface

The AST2620 has multiple dedicated and configurable I/O interfaces. Not all are implemented on the 60-00000588 module.

10.19 BMC, SPI

The AST2620 has multiple SPI interfaces. Three are implemented on the 60-00000588 BMC module.

AST2620 SPI Interface	Logical Connection	Function
SPIFW	On-Module Primary Boot Flash	This BMC SPI master port is used to access the on-module boot Flash. The interface operates in Quad bit mode (QSPI). The 512Mbit Flash device supports up to a 104MHz clock rate
SPI1	Off-Module CPLD (Single CPLD on the CMA Base Plane) Off-Module TPM (Not implemented)	This BMC SPI master port is used to access CPLD registers. The interface operates in single bit mode (MISO/MOSI) and at a 12MHz clock rate This TPM module shares the same SPI interface as CPLD, but with a dedicated chip select for the TPM module <i>Note: the MISO signal of the SPI1 interface is used as a strapping signal during BMC power up, it needs to be strapped low for BMC heartbeat LED to be enabled. Thus, TPM reset is released after BMC reset is released to ensure no external SPI interface is driving MISO signal high before BMC boots.</i>

Table 13. SPI Connection and Function

10.20 BMC, RGMII

The AST2620 has four MAC interfaces. Three are implemented on the 60-00000588 module. All three are 1.8V I/O compatible RGMII and route off-module to the CMA Blade controller blade. Each MAC interface includes dedicated an MDC/MDIO management port.

The CMA platform supports one 1Gb Ethernet MAC with an RGMII interface the connects to the PHY on the CMA Blade controller blade. Only ETH0 is used. The ET_0 port is 1.8V IO directly connected to the BMC MAC1 RGMII interface.

AST2620 RGMII Interface	Logical Connection	Function
MAC1	External 1GbaseT RJ45	Marvell 88E1512 PHY on the CMA Blade board
MAC2 (Not implemented)	Reserved for dual BMC platform design Inter-BMC Control Link (ICL) 1.25Gbaud SGMII	Marvell 88E1512 PHY that would be populated on a BMC FRU in a CMA chassis redesign

Table 14. MAC Logical Connection and Function

10.21 BMC, UART

The AST2620 supports multiple UART ports. Three UART ports are routed off-modules to the CMA Blade controller blade. The Linux serial boot interface maps to the primary UART to the CMA Blade controller blade on-board USB FTDI controller and externalized via a USB Micro-B device port as COM-B (the 2nd UART COM port presented to the device manager). The other UARTs map to the CMA Blade MPS430 and FPGA.

AST2620 RunBMC Socket Signal	Signal Functional Description
UART1 TX/RX	FPGA Serial port between the BMC and FPGA voltage translator decoupled
UART2 TX/RX	FTDI FT4232 port B Presented as BMC main serial Linux OpenBMC interface from the USB 2 nd virtual COM port
UART3 TX/RX	MPS430 Direct connection between the MPS430 and the BMC

Table 15. BMC, UART Table

Design Note: The CMA Blade or base plane must never pull up or pull down the AST2620 TXD5 signal. This signal is also used as a power on reset strap for enabling the AST2620 internal ARM.

10.22 BMC, I2C Port Mapping

The RunBMC spec defines multiple I²C interfaces on the module interface. These ports are physically mapped on the AST2620 SoC defined in the table below. The AST2620 SoC support 3.3V IO on all I²C pins

AST2620 Signal	Logical Connection	Function
GPIOJ0_SCL1_HVI3C3SCL GPIOJ1_SDA1_HVI3C3SCL	RunBMC Socket I2C1 CMA Base Plane Bus 1	Current buffered 3.3V shared interface with the BMC to the enclosure base plane devices: • FRUID (VPD) EEPROM 1 • CRPS 1 • Temperature Sensor 1
GPIOJ2_SCL2_HVI3C4SCL GPIOJ3_SDA2_HVI3C4SCL	RunBMC Socket I2C2 CMA Base Plane Bus 2	Current buffered 3.3V shared interface with the BMC to the enclosure power midplane devices: • FRUID (VPD) EEPROM 2 • CRPS 2 • Temperature Sensor 2
GPIOJ4_SCL3_HVI3C5SCL GPIOJ5_SDA3_HVI3C5SCL	RunBMC Socket I2C3 FPGA Temperature Sensor Board Temperature Sensor BMC EEPROM	Off-module CMA Blade temperature sensors 1) MAX31730A device that connects to 4x FPGA on-die temperature diodes, Target Address 38h (0111,000X/b) 2) NCT75 air temperature sensor, Target Address 48h (1001,000X/b) 3) Off-module CMA Blade AT24C64D device defined in the RunBMC spec as the BMC SoC EEPROM, Target Address 51h (1010,001X/b)
GPIOJ6_SCL4_HVI3C6SCL GPIOJ7_SDA4_HVI3C6SCL	RunBMC Socket I2C4 Programmable Power Supplies (SVID) MPS430, MPM modules and FPGA	The MPS430 is the primary master device on this bus to monitor and manage the MPM power regulator modules The BMC is connected to this bus as an optional master for managing the power regulators This 3.3V bus is voltage translator decoupled connecting the FPGA
GPIOK0_SCL5 GPIOK1_SDA5	Not connected	
GPIOK2_SCL6 GPIOK3_SDA6	Not connected	

GPIOK4_SCL7 GPIOK5_SDA7	RunBMC Socket I2C7 FPGA management	This 3.3V bus is voltage translator decoupled connecting the BMC to the FPGA
GPIOK6_SCL8 GPIOK7_SDA8	Not connected	
GPIOL0_SCL9 GPIOL1_SDA9	Not connected	
GPIOL2_SCL10 GPIOL3_SDA10	Not connected	
GPIOA2_MDC4_SCL12 GPIOA3_MDC4_SDA12	Not connected	

Table 16. I2C Port Mapping

Design Note:

The I2C voltage translator device (TCA/PCA9517A) is used to decouple the 3.3V BMC from the 1.1V FPGA. These are populated on the CMA Blade controller blade.

10.23 BMC, GPIO

The AST2620 has multiple GPIO signals connected off-module to the CMA Blade controller blade and base plane CPLD. The table below summarizes the GPIO connectivity to the AST2620. RunBMC socket defined GPIO pins not defined in this table are no connects.

AST2620 Signal	Logical Connection	Function
GPIO1 GPIO2 GPIO18 GPIO27 GPIO49	Base Plane CPLD	Reserved
GPIO12	One board green LED	FRU Status LED This is an active high SoC output that drives the CMA Blade controller FRU external green LED This signal also routes to the base plan CPLD
GPIO14	One board yellow LED	FRU Fault LED This is an active high SoC output that drives the CMA Blade controller FRU external yellow LED This signal also routes to the base plan CPLD
GPIO25	PHY INT#	Ethernet 1GbaseT PHY Interrupt Connects via a 1.8V level shifter to the 88E1512 PHY LED2_INT_N pin
GPIO15 GPIO19	MPS430	These are reserved GPIO direct connections between the BMC and MPS430
GPIO7	BMC EEPROM WP	Write Protect for BMC VPD EEPROM Active high write protects

Table 17. GPIO Logical Connection

11. Thermal Design Requirements

This section outlines the thermal design requirements for the CMA-CFM proof of concept assembly.

The cooling solution should maintain all components below their respective temperature limits when the system is operating up to its maximum thermal power.

11.1 Ambient Temperature

The CMA enclosure has been designed to support ASHRAE A2 (max 35°C) inlet temperature. No performance degradation is permitted within the ASHRAE A2 (5°C – 35°C) temperature range.

11.2 Fans

The fan modules are hot swappable from the front of the chassis.

11.3 Fan Redundancy

The CMA assembly shall support N+1 fan redundancy. The system performance should not be adversely affected by a single fan failure.

11.4 Service

The CMA shall be able to thermally support all service events including fan, CMA Blade, and CRPS PSU replacement.

11.5 Blade Temperature Rise

The cooling air temperature rise through the enclosure should be above 12.5°C for all inlet temperatures within ASHRAE A2.

11.6 Cooling Overview

The CMA is currently designed for air cooling but could be configured for liquid cooling in the future. Figure 31 shows the cooling configuration. Cold air is brought in from the Cold Aisle and “pushed” towards the eight blades at the back end of the enclosure through the fans located at the front of the enclosure. The design currently has four fans providing

this cooling, but other designs could be used. The fan cooling configuration supports a single fan impeller failure. At 75% of the max fan speed, the current fan selection is estimated to produce a cooling airflow rate of around 32 cfm per blade. The fan speed will be controlled by the BMC. The BMC will monitor the temperatures of the main power dissipating components in the enclosure and then use a PID (Proportional Integral Differential) loop to adjust the fan % PWM to maintain the collected temperatures to below specified target values.

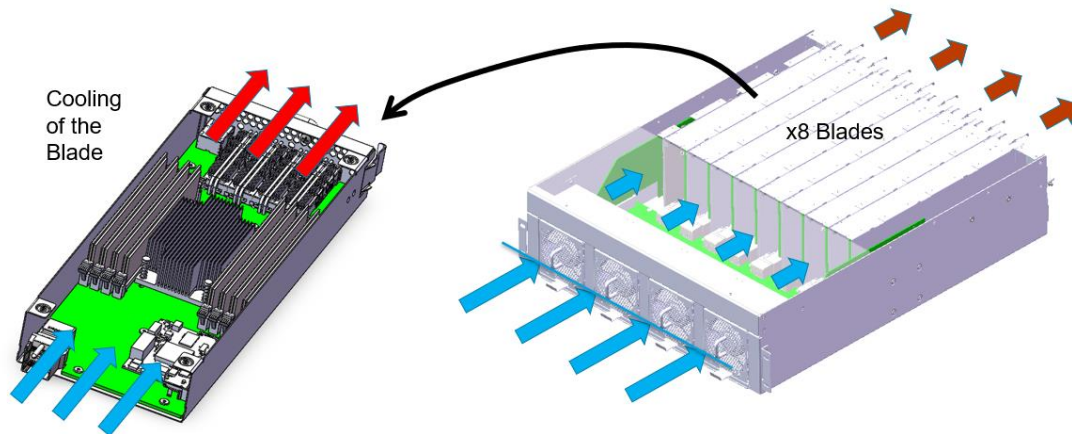


Figure 31. CMA Cooling Configuration

For the current configuration, each blade is estimated to dissipate up to ~200 Watts. Most of this power comes from the FPGA (~100 Watts) and the DDR DIMMs (~10 Watts each). Hand calculations estimate a cooling air temperature rise of around 13°C with 32 cfm per blade. Conjugate heat transfer and computational fluid dynamic (CFD) models predict that the max temperature of the various components on the blade should be able to be maintained. Figure 32 shows the cooling air velocity vectors from one of these analyses.

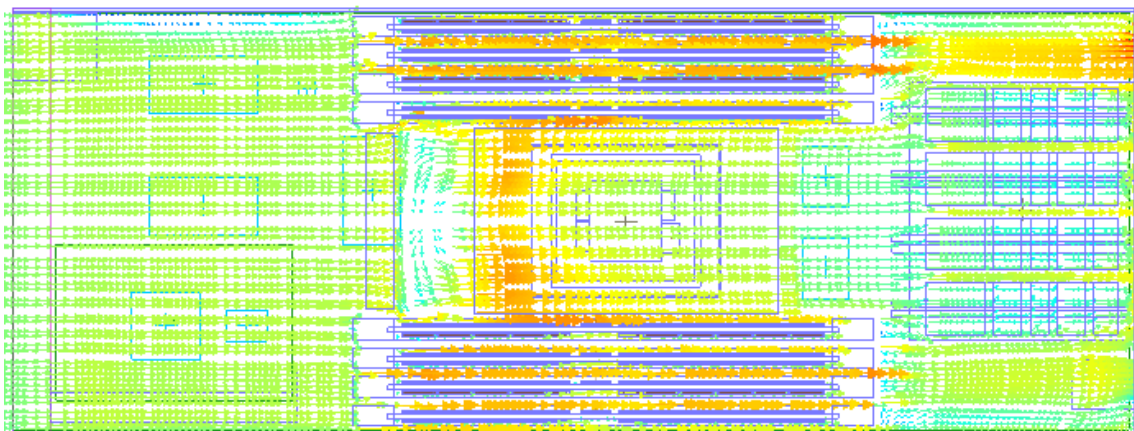


Figure 32. CMA Blade flow vector example

Flow guides may be required to direct the cooling air to the components that reach their target temperatures first. This could help in reducing the required fan speed and thus reduce the power required to cool the enclosure as well as to reduce acoustic generation.

The amount of power used in each blade and how to cool the blade will depend on what FPGA, or other ASIC, is used as well as what is used for the DIMMs. It is imperative that a thermal assessment be completed to ensure that all components remain below their respective temperature limits.

11.7 Thermal Assessment

A 3D conjugate heat transfer/flow model was created in FloTHERM (see Figure 33). Intel's Agilex-7 I-Series FPGA along with x8 DDR4 DIMMs and a BMC SoDIMM PCBA were used in this assessment.

The following assumptions were used:

- Intel Agilex 2957A (AGI 027R29A) FloTHERM model (from Intel)
 - 100 Watts (80 Watts for the "MAIN_P" and 5 Watts each for the four "HSSI_x_x_P")
 - Heatsink (aluminum):
 - Base: 90mm long by 55mm wide and 4mm thick
 - Internal Fins: 0.8mm wide, 25mm tall, x22 fins
- Samsung RDIMM 3200 FloTHERM model (from Samsung)
 - 10 Watts for each DIMM
- The QSFP-DD connectors = 0 Watts (passive cables were used)
- BMC = ~1.9 Watts ($q_{jc} = 11.1 \text{ K/W}$; $q_{jb} = 20 \text{ K/W}$)
- 18 Watts was spread along the CMA Blade board to account for power regulation.
 - This will be refined in future analyses to include the actual power regulator components.

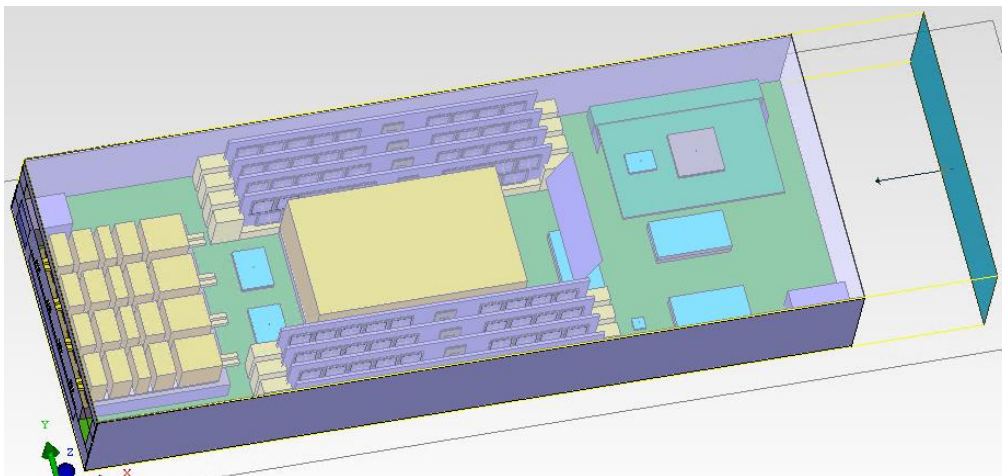


Figure 33. FloTHERM Model of CMA Blade

11.8 Thermal Results

Figure 34 shows some of the results of the thermal assessment at various ambient temperatures and fan speeds. Keeping the max DIMM temperature <70°C requires around 59% fan speed at an ambient temperature of 23°C. The fans end up using around 9% of the total enclosure power. The fan power percentage increases to ~16% at a 35°C ambient temperature. Figure 35 shows the predicted fluid temperature distribution for one of the thermal assessments.

	23°C Amb	27°C Amb	35°C Amb (no fan fail)	35°C Amb (single impeller failure)
ACE cfm	25	28	35	35
% PWM	59	65	81	90
Total Fan Power (W)	170	200	315	390
% Fan Power (of Total Enc Pwr)	9%	11%	16%	19%
FPGA (°C)	72	73	73	73
Max DIMM (°C)	70	70	70	70

Figure 34. Thermal Results - Max Power

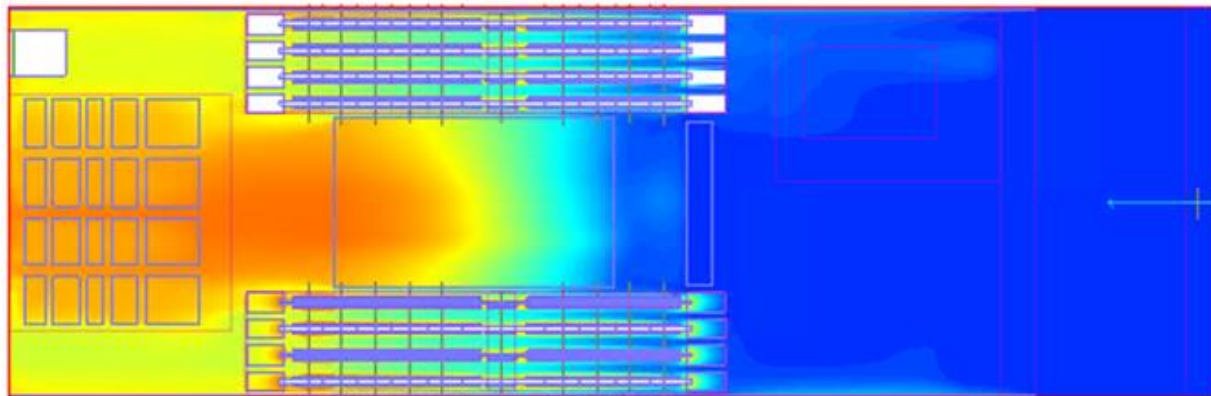


Figure 35. Fluid Temperature Predictions for CMA Blade Board

11.9 Thermal / Flow Datamatch

Prior to creating Section 11.8, some measurements of power (see Figure 36), temperature and flow were taken from the enclosure, subassemblies, and various components. A comparison was made with the measured results and the predictions to evaluate how well the thermal model matches the data. This was a first pass and additional, more detailed, analyses and thermal / flow testing will be done as the program continues.

Component Description	Power per Component (W)	Qty	Power Budget (W)	Measured Power (W)
AST2600 (BMC)	5	1	5	2*
DDR4-DRAM DIMM	10	8	80	36**
Fans - 80x80	98	0.5	49	49***
Ace1.0 FPGA Agilex-I Gen 5	100	1	100	40*
Misc Devices	2	1	2	3*

Blade Total	187	81
DC to DC Adder	28	9*
Blade Total	215	90
Appliance Total	2112	1112

* Estimated

** Some previous DDR measurements estimated to be around 36 Watts

*** If assume max fan speed (with fan fail) would be ~90% PWM

Figure 36. Measured vs Estimated Enclosure Power

Figure 37 shows a comparison of measured versus predicted data. All the circles are the temperature data pulled from the enclosure testing. The triangles are the predicted temperatures at sea-level. The X's are the predicted temperatures at an altitude of ~5000-ft, which is where the thermal testing was completed. This shows that the predicted temperature rise is within a few degrees of the measured.

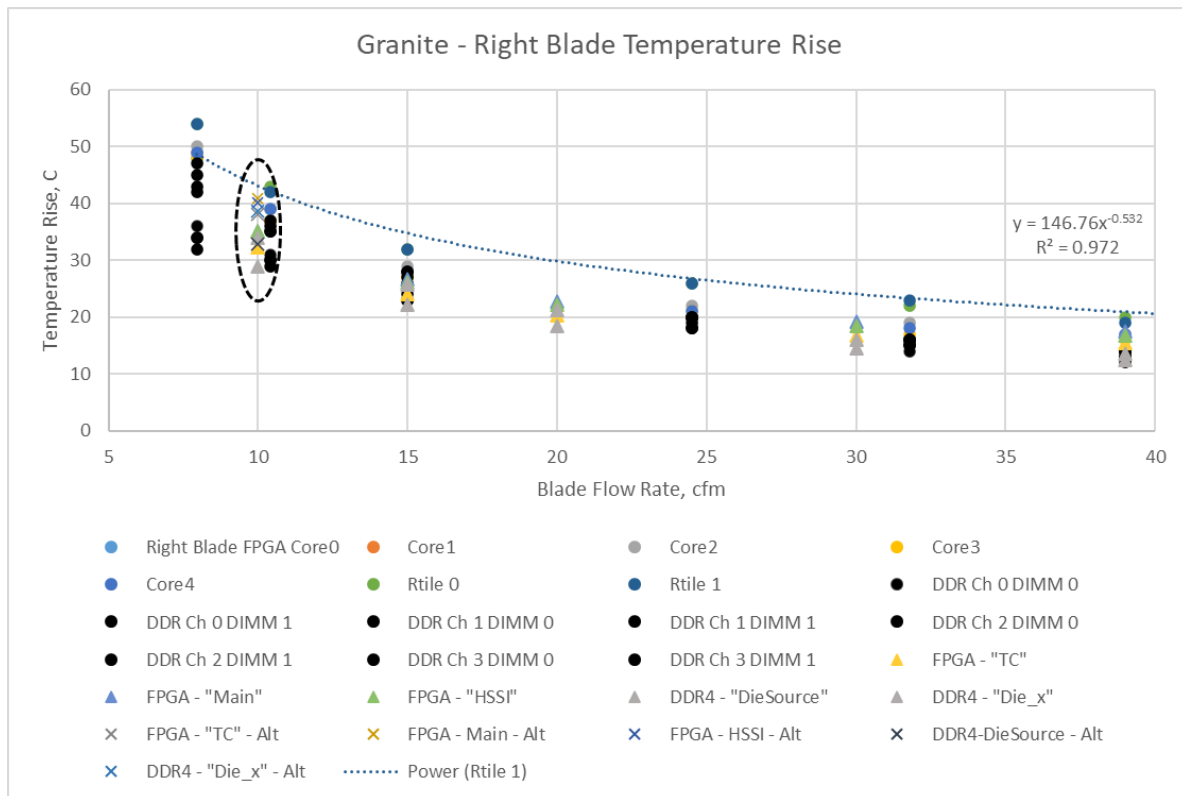


Figure 37. CMA Blade Measured vs Predicted Temperature Comparison

12. System Firmware

The controller FW is proprietary and will be provided with the product.

- FW shall be lightweight and fit within a SPI NOR Flash.
- FW update will be supported out of band.
- FW should generate logs and dumps to support diagnostics.
- FW shall have no direct interaction with the data path to avoid any latency adders.
- FW should support a reduced set of CCI commands to enable the Linux Kernel CXL driver but not commands that could impact system operation.

13. Hardware Management

The BMC runs a modified OBMC instance with a redfish service for OOB management of the system and memory allocation. Only the BMC in slot0 has control over the enclosure fans, power supplies and EEPROMS over an I2C interface.

The BMC communicates with the controller over an I2C/SMBus connection using CXL CCI commands tunneled over MCTP. Additional OEM CCI commands are implemented as needed.

13.1 Redfish Compliance

All Products shall have a completed Hardware Management Tab in the 2021 Supplier Requirements.

14. Security

As a POC effectively no security has been implemented, a production specification will need to define this.

15. Performance Data

The following performance measures were taken on a SuperMicro production server with two Intel Sapphire Rapids XCC CPUs. The following data was with a single CXL link configured to access the full 1TiB of DRAM with a 4-way interleave:

FPGA Configuration		Idle Latency	Bandwidth			
Speed Grade	DDR4 Data Rate		100% WR	100% RD	50/50 (sequential)	50/50 (random)
-2	1866MT/s	481.1ns	40.0GB/s	37.2GB/s	26.1GB/s	25.9GB/s
-2	2133MT/s	474.0ns	41.4GB/s	38.2GB/s	28.9GB/s	28.6GB/s
-1	2133MT/s	435.9ns	41.6GB/s	38.4GB/s	29.0GB/s	28.8GB/s
-1	2400MT/s	429.4ns	44.2GB/s	39.8GB/s	31.9GB/s	31.6GB/s

Table 18. Performance Table 1

The FPGA Configuration column indicates the FPGA speed grade (-1 being the fastest) and the DDR4 transfer rate.

The following table contains similar data taken on the same SuperMicro production server but with two CXL links each configured to access 512GiB of DRAM with a 4-way interleave:

FPGA Configuration		Idle Latency	Bandwidth			
Speed Grade	DDR4 Data Rate		100% WR	100% RD	50/50 (sequential)	50/50 (random)
-2	1866MT/s	489.4ns	40.4GB/s	37.2GB/s	26.2GB/s	25.8GB/s
-2	2133MT/s	470.6ns	41.6GB/s	38.4GB/s	28.9GB/s	28.6GB/s
-1	2133MT/s	437.1ns	41.6GB/s	38.3GB/s	29.0GB/s	28.8GB/s
-1	2400MT/s	429.4ns	44.4GB/s	39.8GB/s	31.9GB/s	31.7GB/s

Table 19. Performance Table 2

The next table contains similar data taken on an Intel CRB with two Emerald Rapids CPUs. The system was configured with a single CXL link that accessed the full 1TiB of DRAM with a 4-way interleave:

FPGA Configuration		Idle Latency	Bandwidth			
Speed Grade	DDR4 Data Rate		100% WR	100% RD	50/50 (sequential)	50/50 (random)
-2	1866MT/s	467.9ns	39.0GB/s	36.8GB/s	26.3GB/s	26.1GB/s
-2	2133MT/s	451.1ns	40.9GB/s	37.8GB/s	29.1GB/s	28.9GB/s
-1	2133MT/s	425.5ns	40.8GB/s	37.8GB/s	29.3GB/s	29.0GB/s
-1	2400MT/s	417.0ns	43.8GB/s	39.3GB/s	32.2GB/s	31.9GB/s

Table 20. Performance Table 3

The next table contains similar data taken on the same Intel CRB with two Emerald Rapids CPUs. The system was configured with two CXL links that each accessed 512GiB of DRAM with a 4-way interleave:

FPGA Configuration		Idle Latency	Bandwidth			
Speed Grade	DDR4 Data Rate		100% WR	100% RD	50/50 (sequential)	50/50 (random)
-2	1866MT/s	465.8ns	39.0GB/s	36.8GB/s	26.3GB/s	26.1GB/s
-2	2133MT/s	447.4ns	40.8GB/s	37.9GB/s	29.1GB/s	28.9GB/s
-1	2133MT/s	422.7ns	40.8GB/s	37.9GB/s	29.3GB/s	29.0GB/s
-1	2400MT/s	413.2ns	43.9GB/s	39.3GB/s	32.2GB/s	31.9GB/s

Table 21. Performance Table 4

16. References

The following links reference public domain specifications relative to the CMA platform.

1. Modular Hardware System - Common Redundant Power Supply (M-CRPS) Base Specification

- Version 1.02 RC2, August 28th, 2023
- <https://www.opencompute.org/w/index.php?title=Server/MHS>
 - https://drive.google.com/file/d/1bhVL_XddugiLCJB_D0tLynhOPv_1tT_9/view?usp=drive_link

2. RunBMC Daughter Board I/O Specification

- Version 1.4.1, August 11th, 2019
- <https://github.com/opencomputeproject/RunBMC>
 - https://github.com/opencomputeproject/RunBMC/blob/master/OCP_RunBMC_Daughterboard_Card_Design_Specification_v1.4.1.pdf

3. OpenBMC Specification

- <https://www.openbmc.org/>
- <https://github.com/openbmc/docs>

4. Universal Serial Bus Cables and Connectors Class Document

- Revision 2.0, August 2007
- <https://www.usb.org/sites/default/files/CabConn20.pdf>

5. Composable Fabric Manager (CFM) - Git Hub

- The Composable Fabric Manager (CFM) is a software system designed to manage memory composition on a CMA and the host servers. Multiple management interfaces including Redfish and web UI are implemented.
- Posted July 2024
- <https://github.com/Seagate/cfm>
- <https://github.com/Seagate/cfm/wiki>

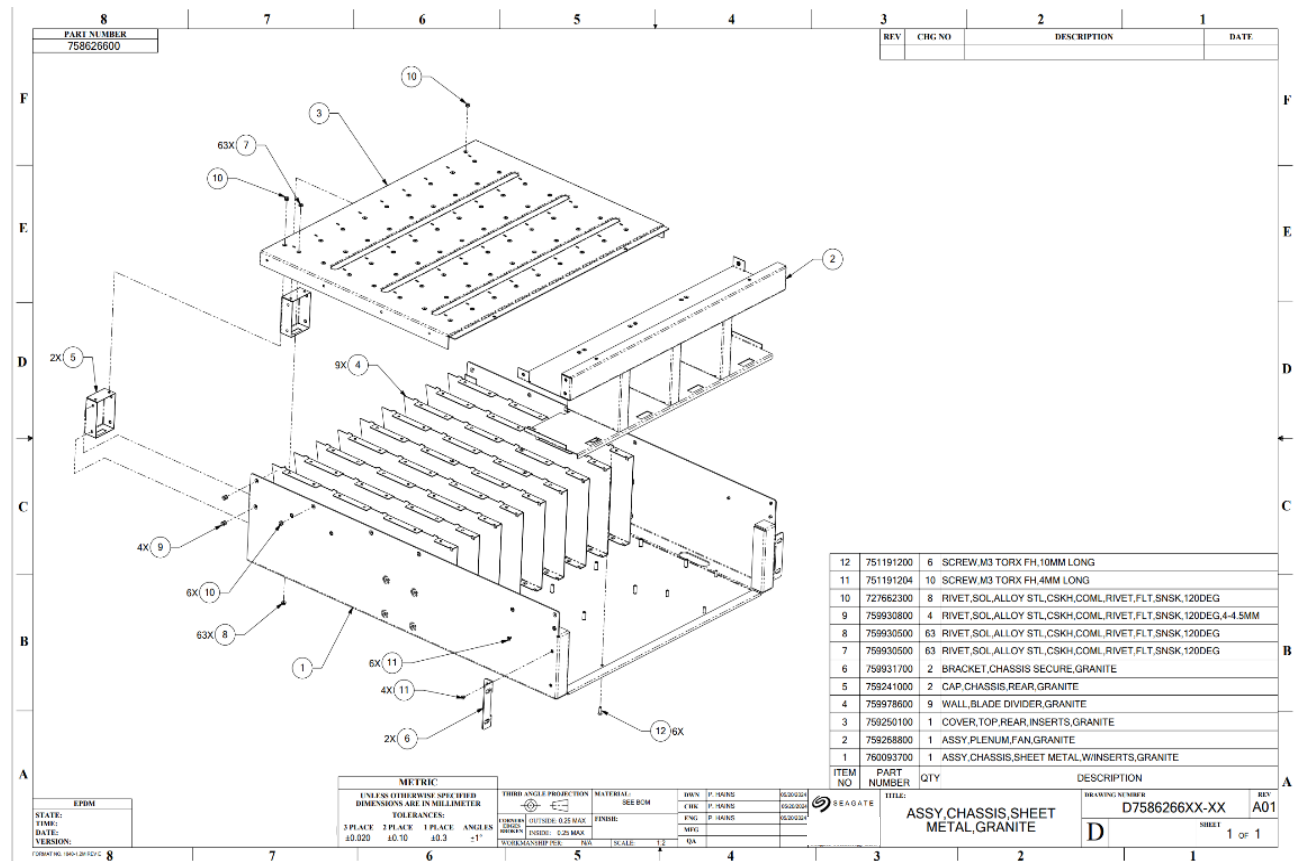


Figure 38. Exploded Enclosure Sheet Metal Overview Drawing

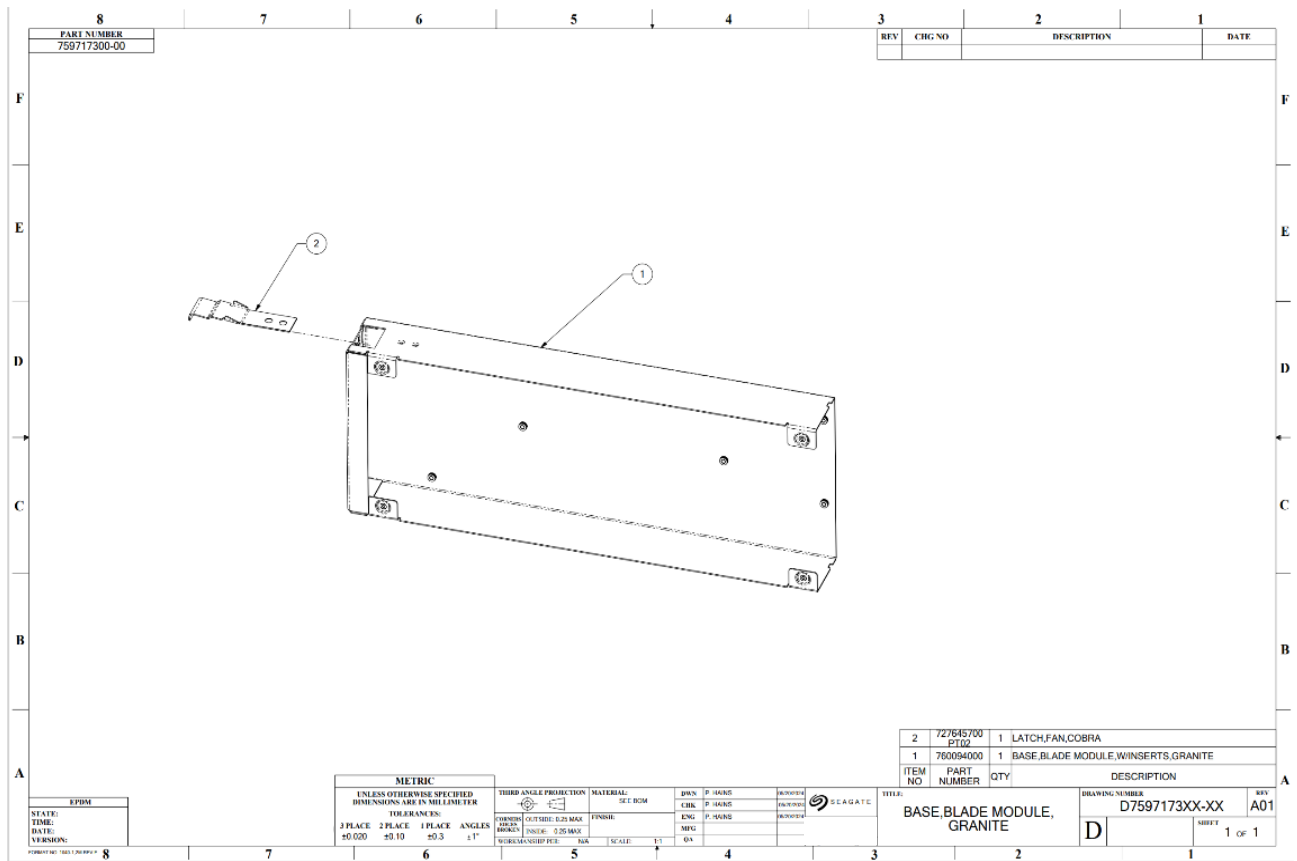


Figure 40. Blade Sled Sheet Metal Assembly Drawing

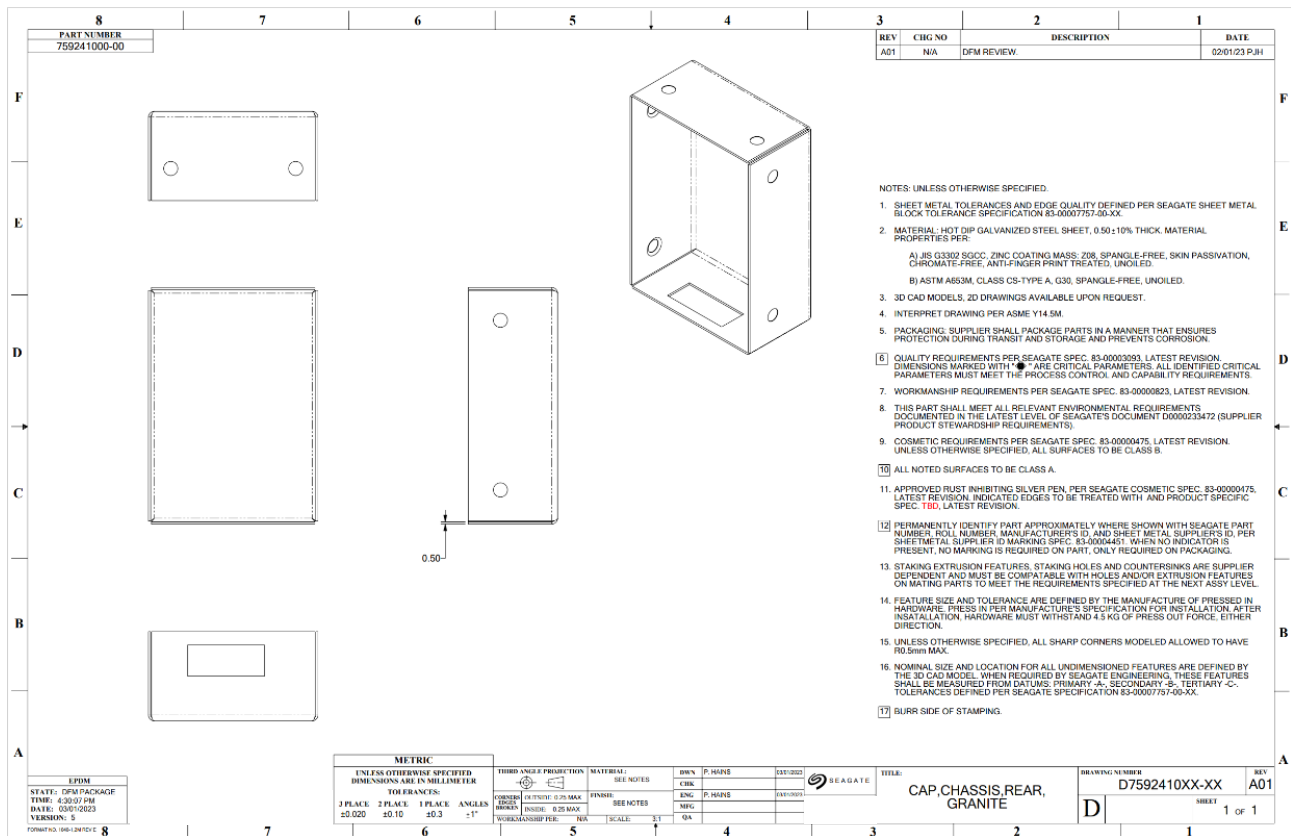


Figure 42. Enclosure - Rear Drawing

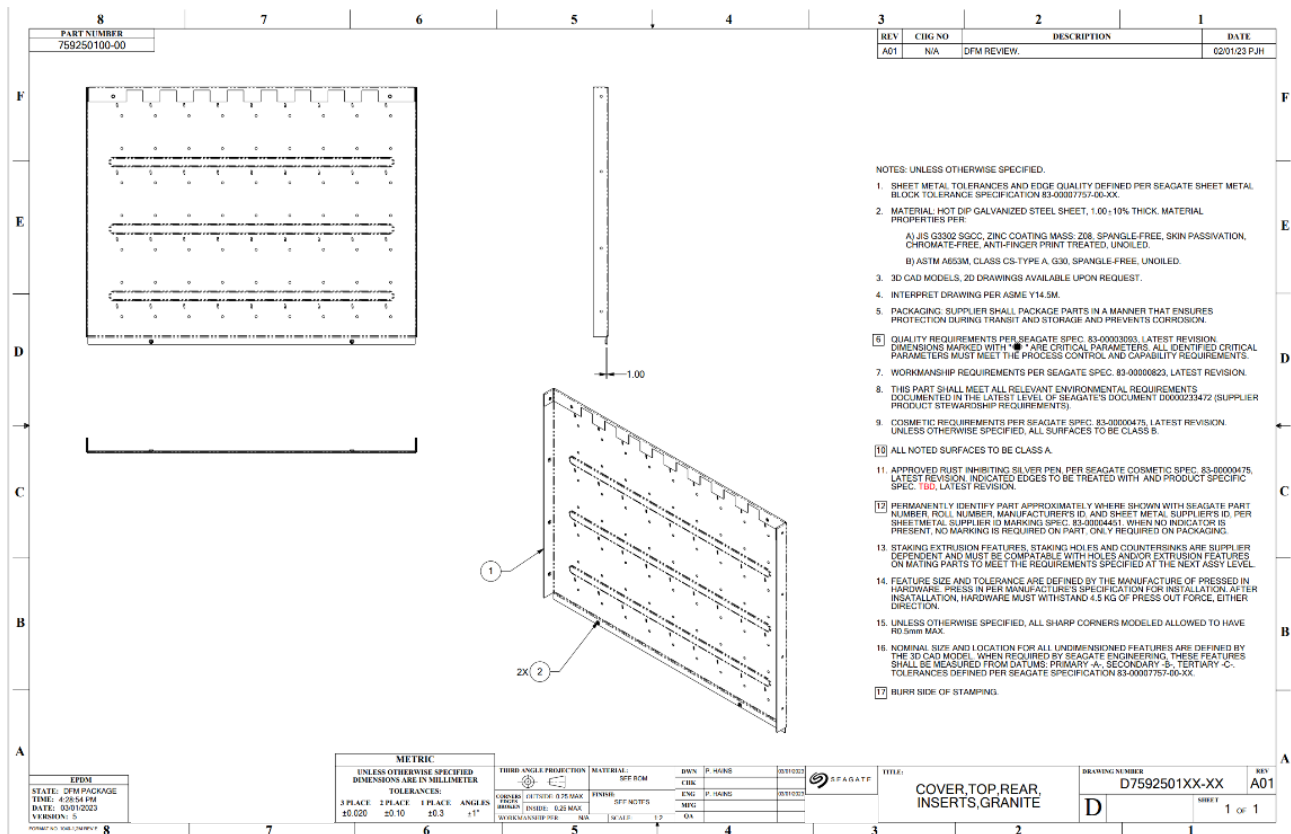


Figure 43. Enclosure - TOP Drawing

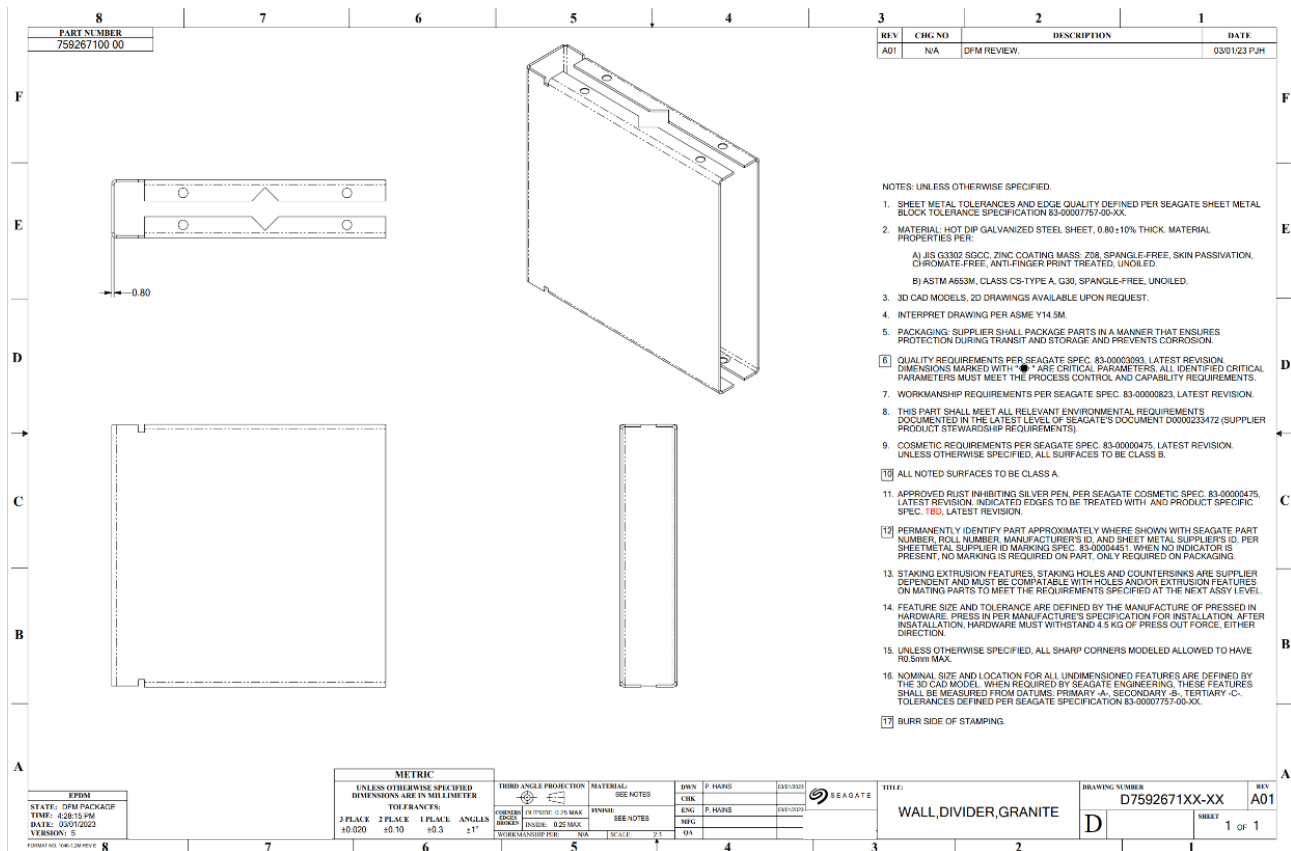


Figure 44. Enclosure - Side Casing Drawing

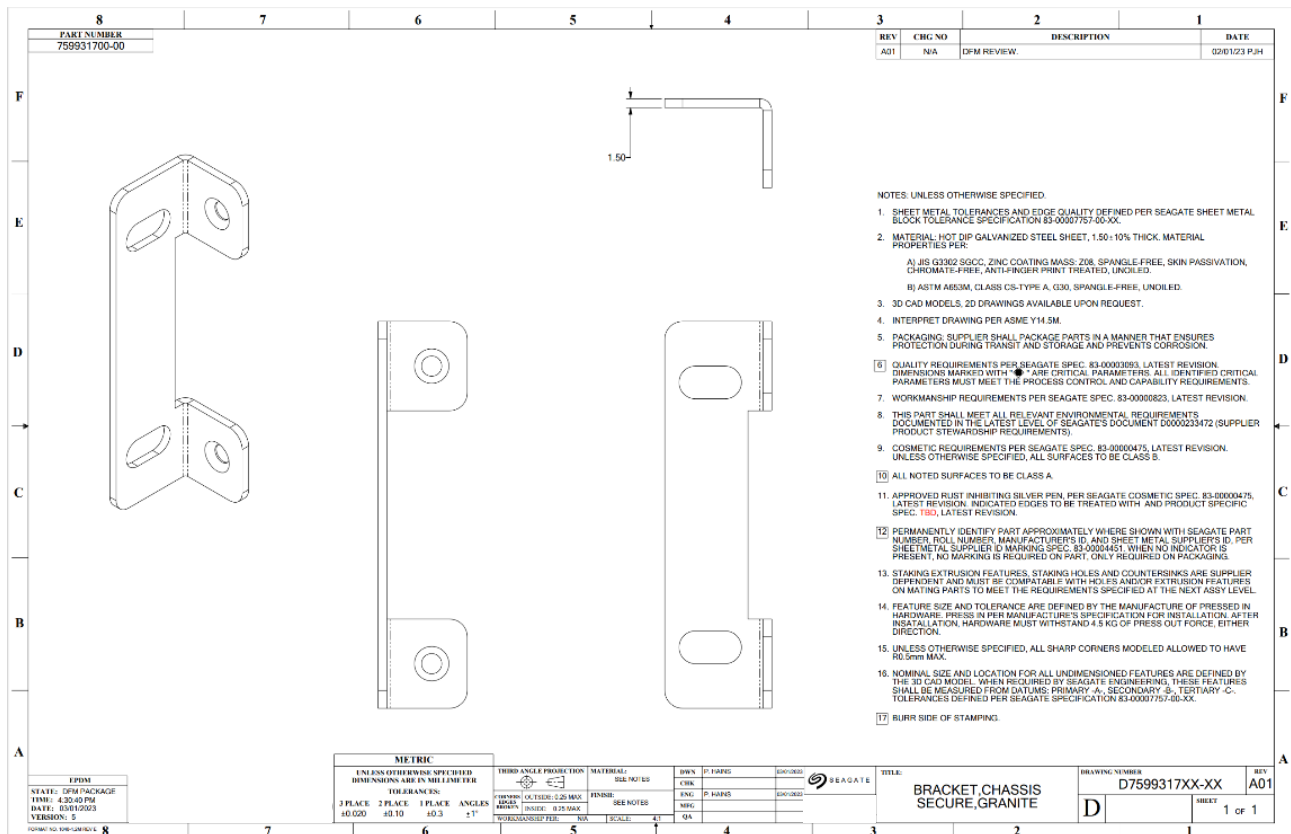


Figure 45. Enclosure - Securing Drawing

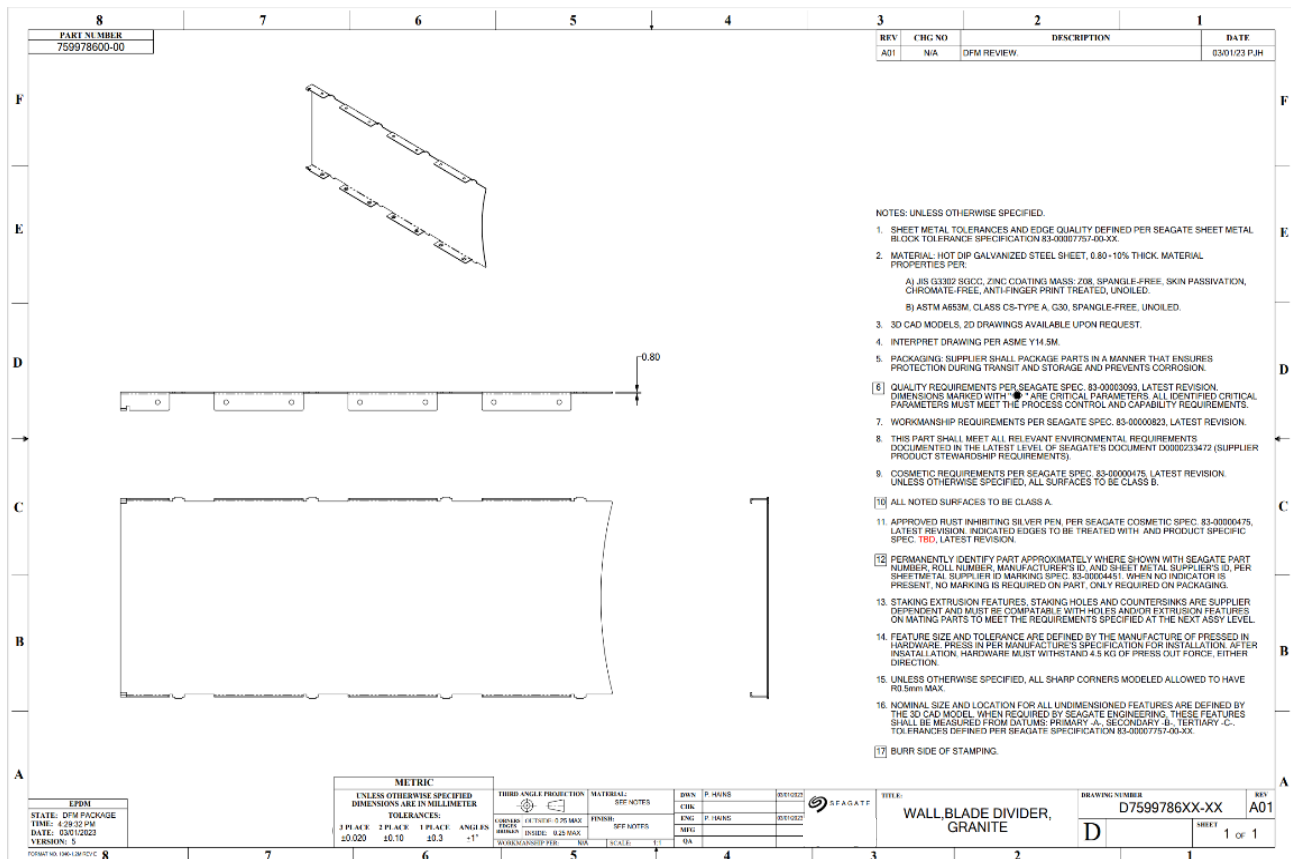


Figure 46. Wall Blade Drawing

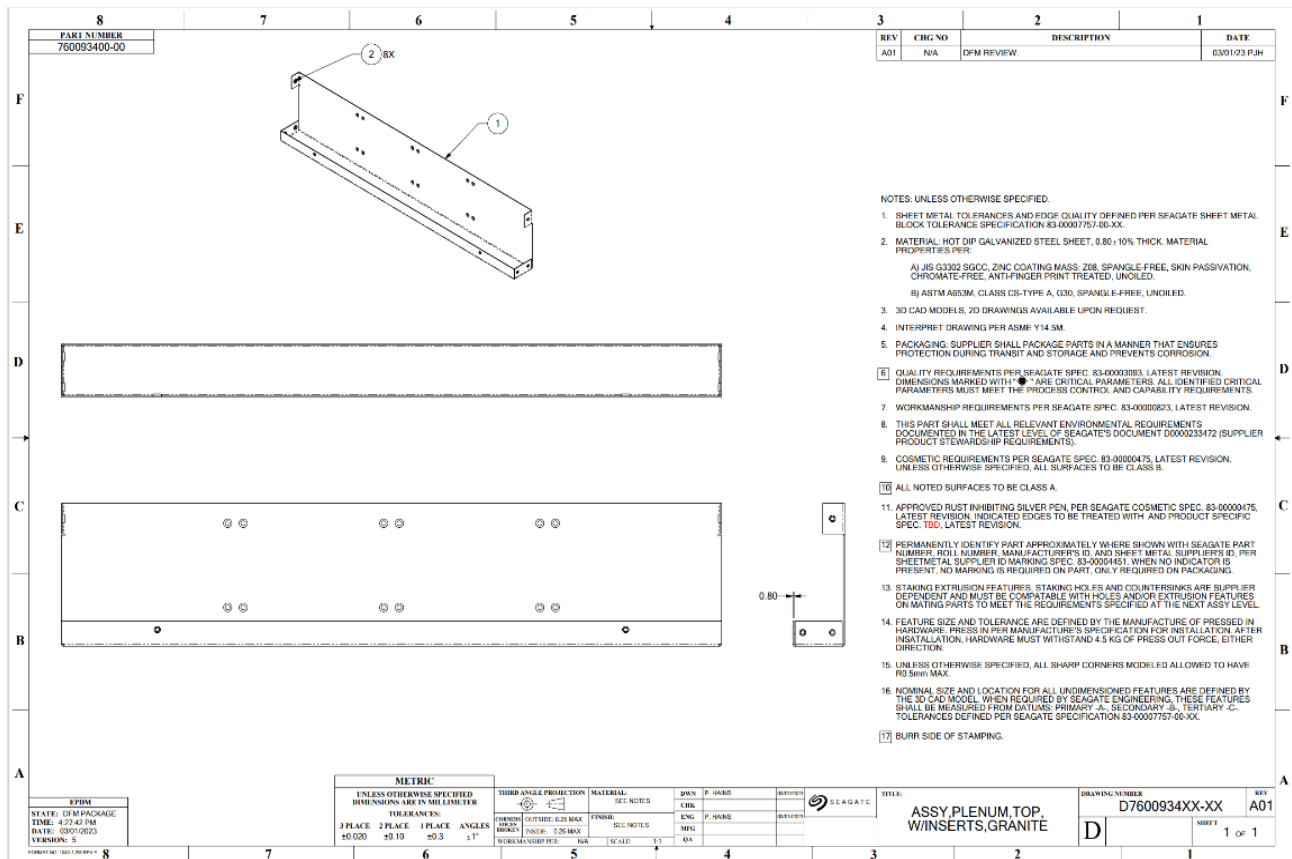


Figure 47. Plenum Sheet metal with Inserts (1) Drawing

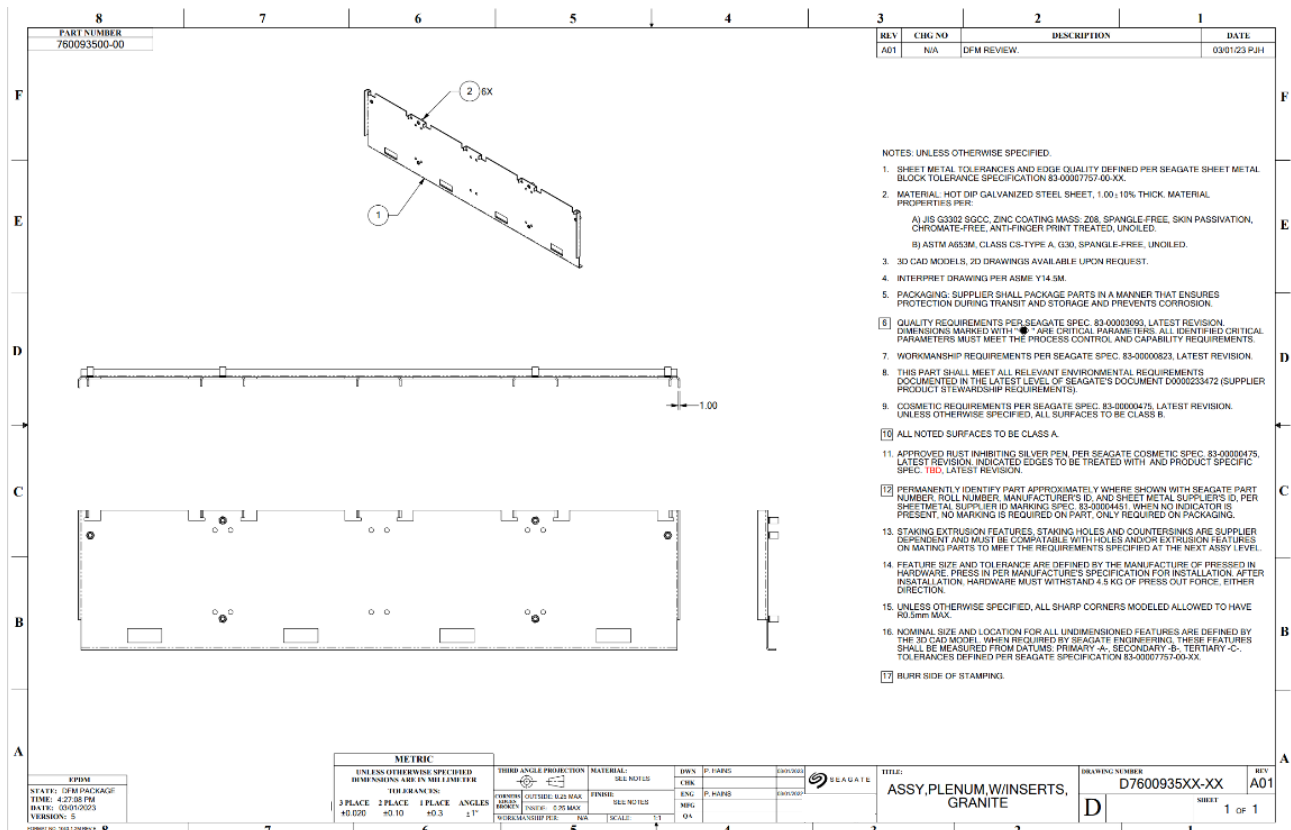


Figure 48. Plenum Sheet Metal W/Inserts (2) Assembly Drawing

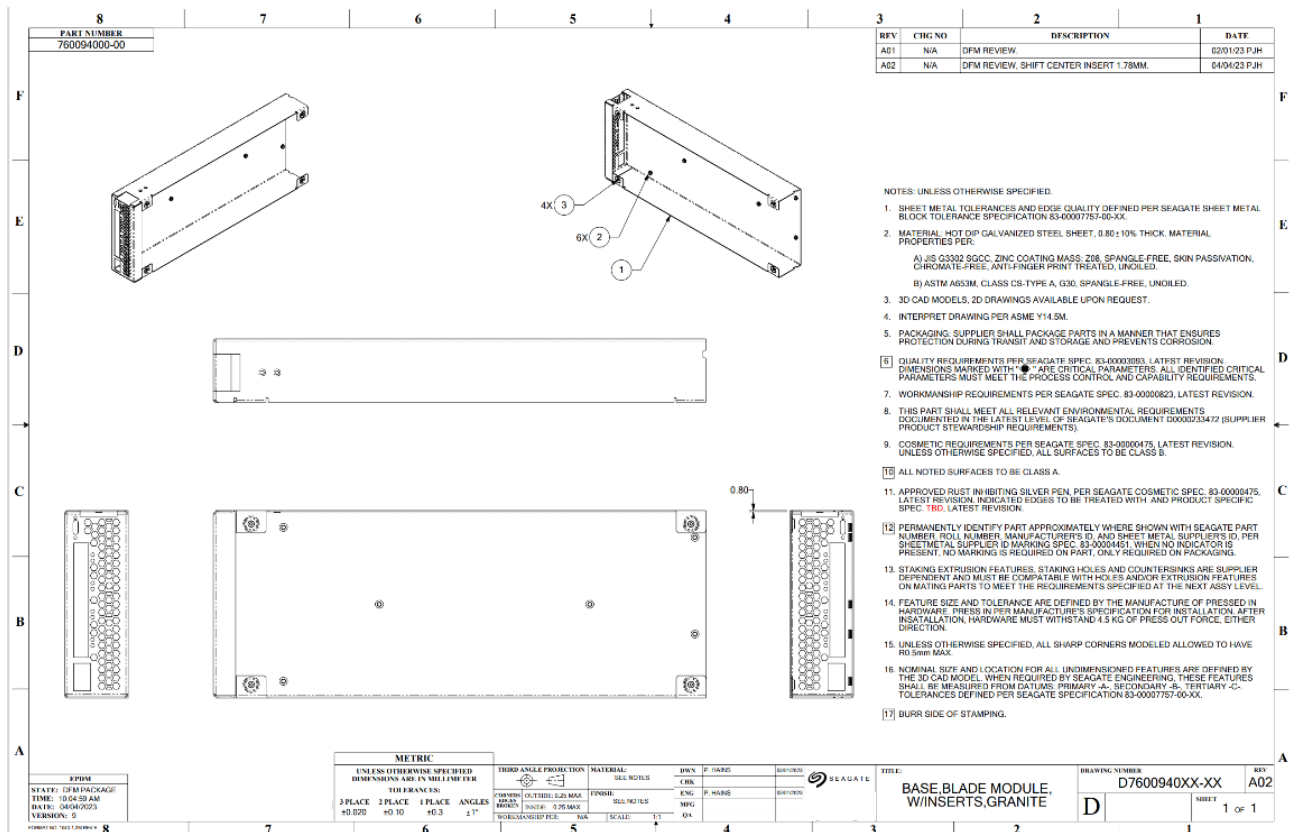


Figure 50. Blade Sled Base W / Inserts Assembly Drawing

18. Appendix A

Checklist for IC approval of this Specification (to be completed by contributor(s) of this Spec)

Item	Status	Link to detailed explanation
Has this contribution been presented to an OCP Project group during a project call or engineering workshop?	Yes	The contribution was presented to the Server-Project and the CMS-Workstream teams.
Approval by Project Leads	Yes	Approved by Server-Project and the CMS-Workstream teams
Is this contribution entered into the OCP Contribution Portal?	Yes	
Was it approved in the OCP Contribution Portal?		

Table 22. Appendix A Checklist