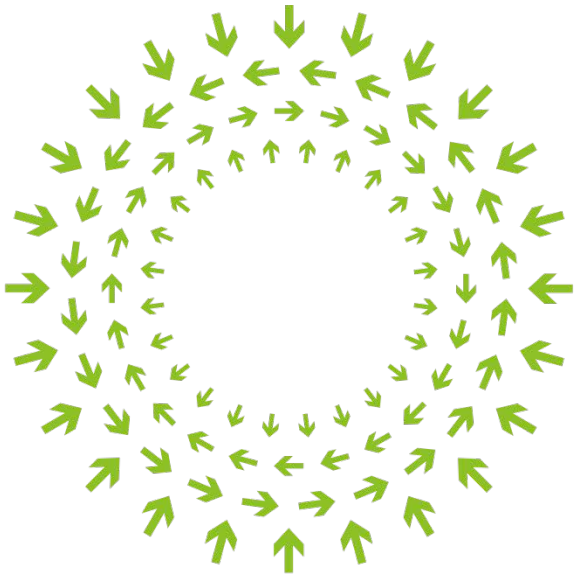

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Compute Project

Facebook – Wedge-100

32x100GE Top of Rack Switch

Authors:

Zhiping Yao, Network Hardware Engineer, Facebook

1. Revision History

Date	Version	Author	Description
09/16/2015	0.0	Zhiping Yao	Hardware specification update for DVT release. COM-e CPU information is added.
01/23/2016	0.1	Zhiping Yao	Initial OCP revision
01/31/2016	0.2	Zhiping Yao	Add CPLD register definition, add Open Rack bus bar pass-through card section
02/10/2016	0.3	Zhiping Yao	Clean up all table, figure caption, add OOB description
03/09/2016	0.4	Zhiping Yao	Update license to OCPHL-R for now
07/26/2016	0.9	Zhiping Yao	Change few pictures, update optic transceiver and DAC cable section, add LED scheme, update license to OCPHL-P
09/14/2016	1.0	Xu Wang	Added RackMon and JayBox GPIO connector pinout definition.

2. Scope

This document outlines the technical specifications for the Facebook Wedge-100 Open Switch Platform submitted to the Open Compute Foundation

3. Contents

4. Overview

This document describes the technical specifications of the wedge-100 Top of Rack/Leaf switch designed by Facebook. The wedge-100 is a cost optimized switch design focused on Top of Rack deployments which support 10G/25G/40G/50G/100G server connectivity and providing 100Gb uplinks to the aggregation layer of the network.

The wedge-100 switch supports thirty two QSFP28 ports that each can operate at 4x10G or 4x25G with QSFP28-4xSFP28 break out cables, 2x50G with QSFP28-2xQSFP28 break out cables, 40G with standard QSFP+ optics/DAC cables, and 100G with QSFP28 optics/DAC cables.

The Wedge-100 system uses Broadcom BCM56960 (a.k.a Tomahawk) Switch Chip which can support 32 x 100GE ports.

4.1. Wedge-100 Feature lists

Wedge-100 major features are:

- One Broadcom BCM56960 (a.k.a Tomahawk) Switch ASIC:
  - 32 falcon SERDES block supporting 128x25G SERDES ports
  - 32x100G, or 64x50G, or 128x25G, or 32x40G, or 128x10G
  - 25G serdes can be configured to work at lower 10G speed
  - PCIe Gen2 x4 Lane control interface
- COM-e CPU module
  - Intel® Atom™ processor E3800 family, 22nm process technology
  - Cache up to 2MB (for Quad Core)
  - DPM (Defect Per Million devices) <50
  - Support Intel® VT-x technology
- Network interface
  - 32 QSFP28 interface
  - Each QSFP28 port can be configured into 1x100G mode, or 2x50G mode, or 4x25G mode, or 1x40G mode, or 4x10G mode.
- Front panel management and debug interface
  - 10/100/1000 RJ45 GBE OOB port
  - RJ45 console port
  - Type-A USB2 port
  - Facebook proprietary 14-pin debug connector
- Rack Monitor Interface
  - Support Facebook Rack Monitor interface on rear panel
  - 3 RJ45 ports are used for Open Rack V2 Rack Monitor function.
  - 1 RJ45 port is used for JayBox GPIO.
- Fan tray
  - Five 40mmx56mm CR fan-tray on rear panel
  - Screw-less design.
- Power
  - Dual redundant PSU
  - Support Open Rack V2 bus bar input by using power passthrough card and 21-in adaptor
- Transceiver and DAC cables
  - DAC cable

- QSFP28 to QSFP28 DAC cable, 1M, 2M, 3M
- QSFP28 to dual QSFP28 DAC cable, a.k.a Y-cable, 1M, 2M, 3M. facebook proprietary cable
- QSFP28 to 4xSFP28 fanout DAC cable, 1M, 2M, 3M

o QSFP28 optics

- 100G CWDM4 optic

4.2. Wedge-100 block diagram

The following figure illustrates the functional block diagram of the wedge-100 system.

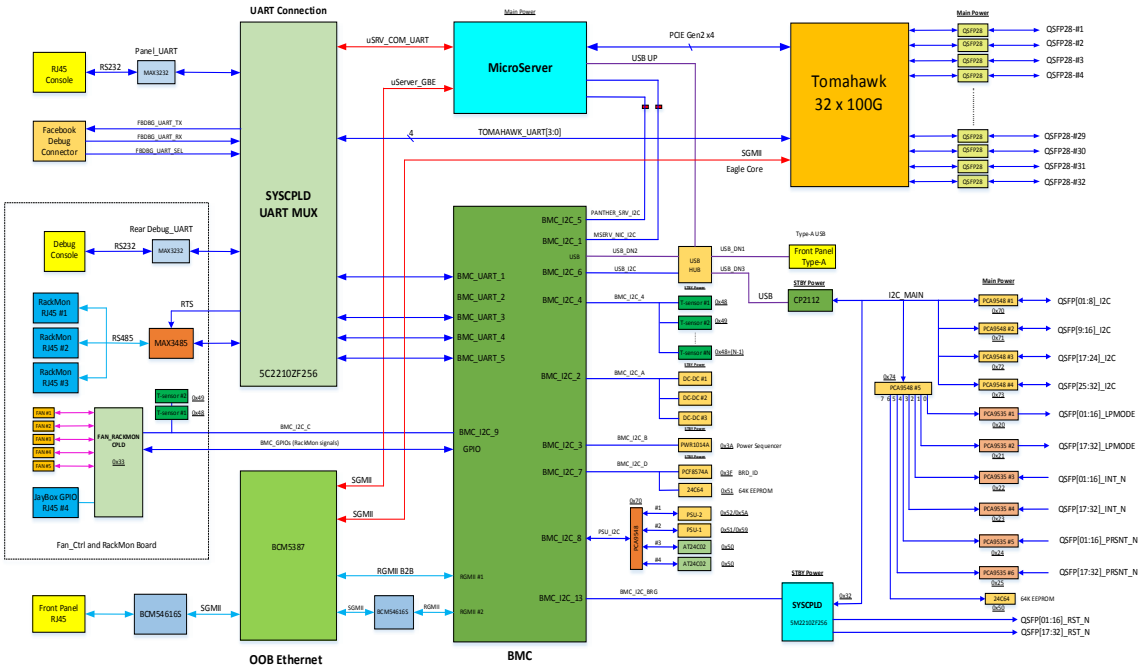

Figure 1: Wedge-100 Block Diagram

4.3. Wedge-100 SKUs and Configurations

The Two SKUs are defined for wedge-100: Standard 19-in SKU and Open Rack 21-in SKU.

- Standard 19-in SKU: wedge-100 system is powered by hot-pluggable PSU, PSU can be AC input, or DC (56V) input.
- Open Rack 21-in SKU: wedge-100 system is used in Open Rack V2, and is powered by 12.5V power bar.

Both standard SKU and Open Rack SKU share the same main board PCB.

4.3.1. Standard SKU

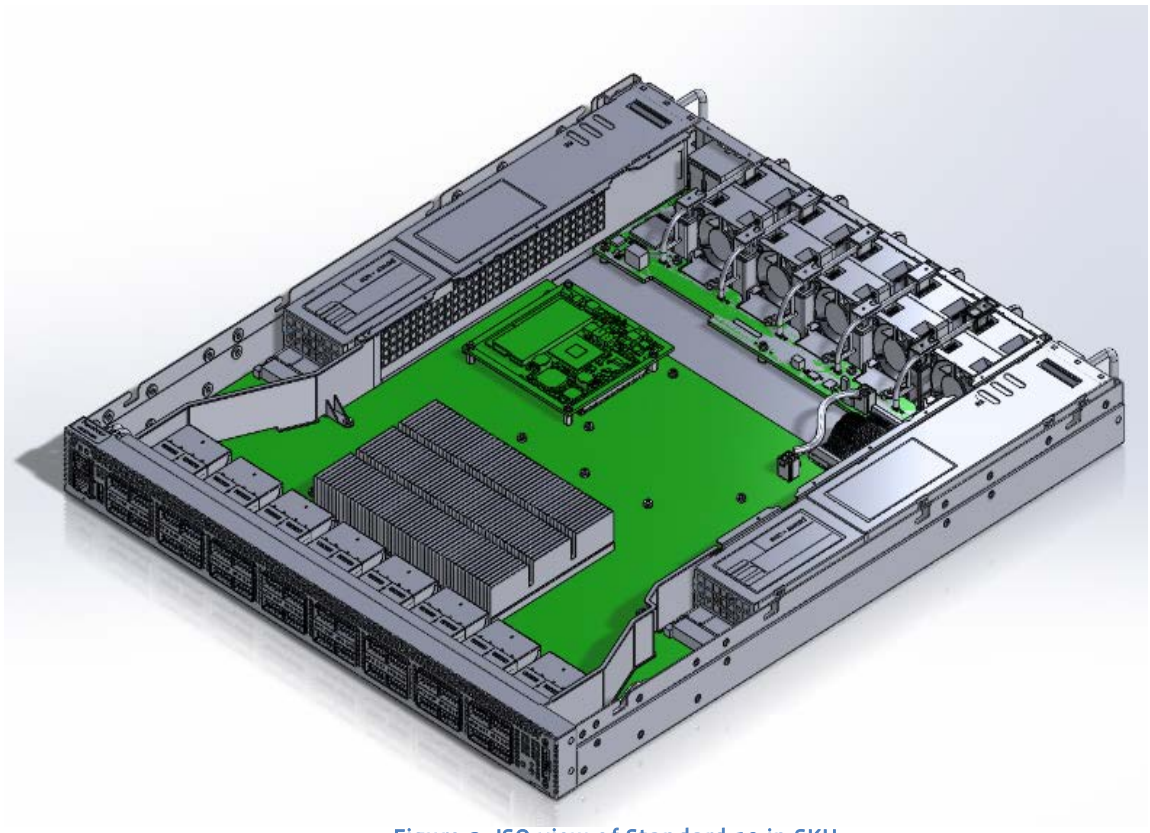

Figure 2: ISO view of Standard 19-in SKU

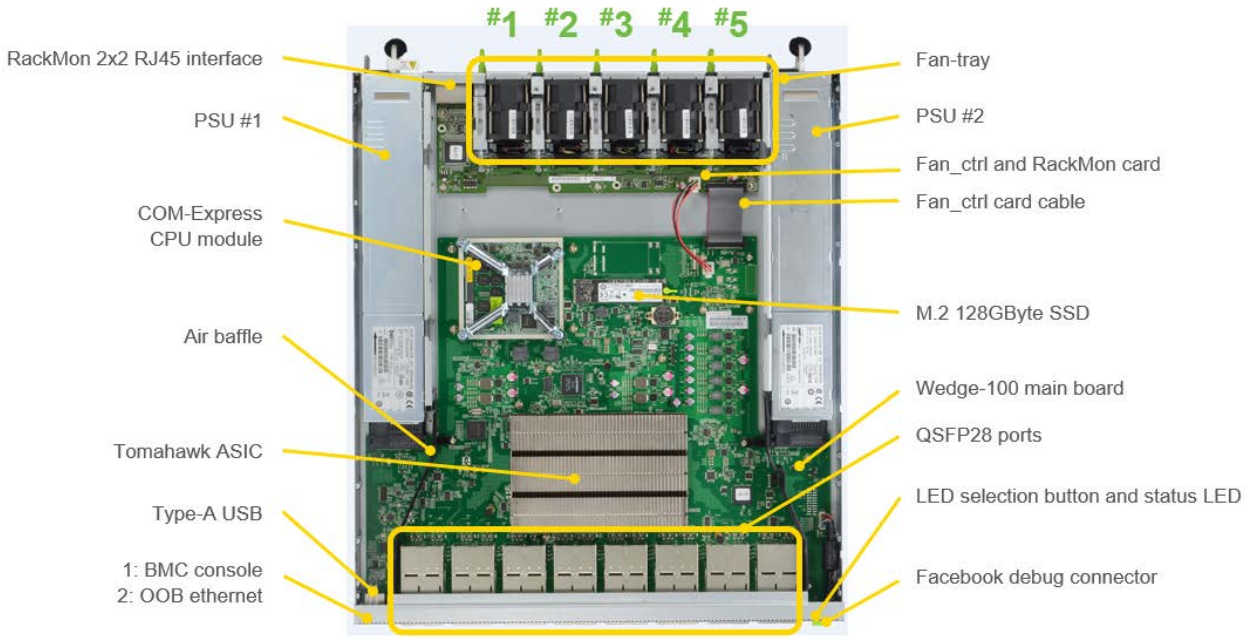

Figure 3: Top View of Standard 19-in SKU

4.3.1. Open Rack 21-in SKU

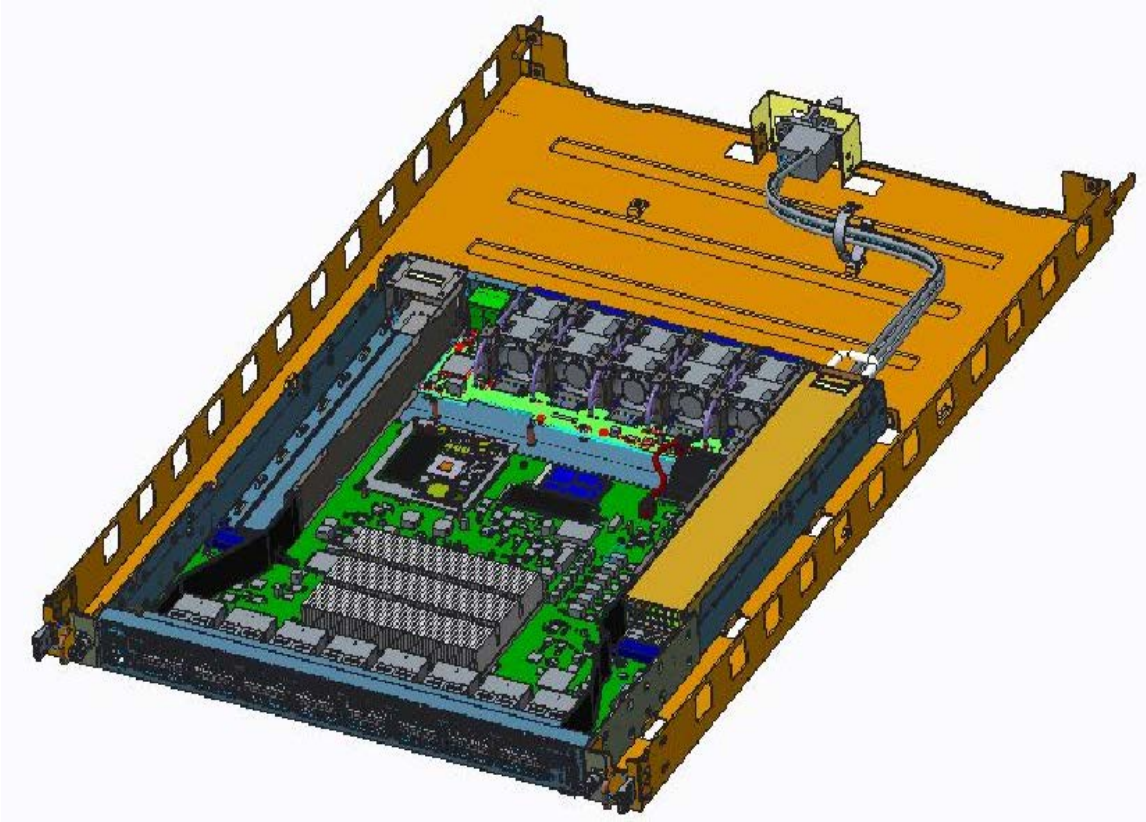

Figure 4: ISO View of OpenRack 21-In SKU

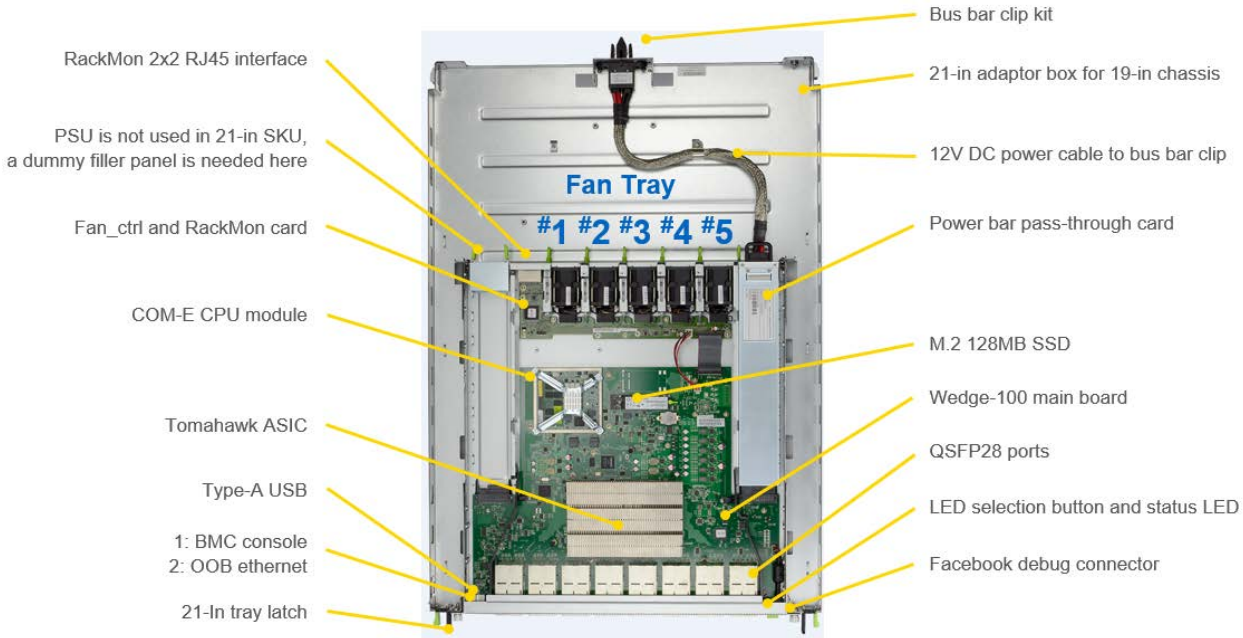

Figure 5: Top View of Open Rack 21-In SKU

5. Wedge-100 Mechanical

5.1. Dimension Requirement

Wedge-100 standard SKU is 1RU 19-in pizza box switch. Open Rack SKU is 1RU 21-in pizza box which combines standard 19-in box and 21-in Open Rack adaptor. Standard 19-in SKU box is placed inside Open Rack adaptor and can receive 12V power directly from Open Rack power bus bar.

5.1.1. Chassis

Feature Name	Description	Comment
Chassis width	440mm (17.32")	Outer dimension
Chassis depth	507mm (19.97")	Outer dimension
Chassis height	44mm (1.732")	Outer dimension

Table 1: Standard SKU chassis Dimension

Feature Name	Description	Comment
Chassis width	534mm(21")	Outer dimension
Chassis depth	797.5mm(31.4")	Outer dimension
Chassis height	46.3mm(1.82")	Outer dimension

Table 2: Open Rack SKU Chassis Dimension

5.2. COM-E PCB Dimension

The following two figures show the details of the COM-E PCB dimension. Its dimensions are as below:

95mm(L) x 95mm(W) x 2.0mm(H)

COM-e CPU module can be used in different platforms and systems.

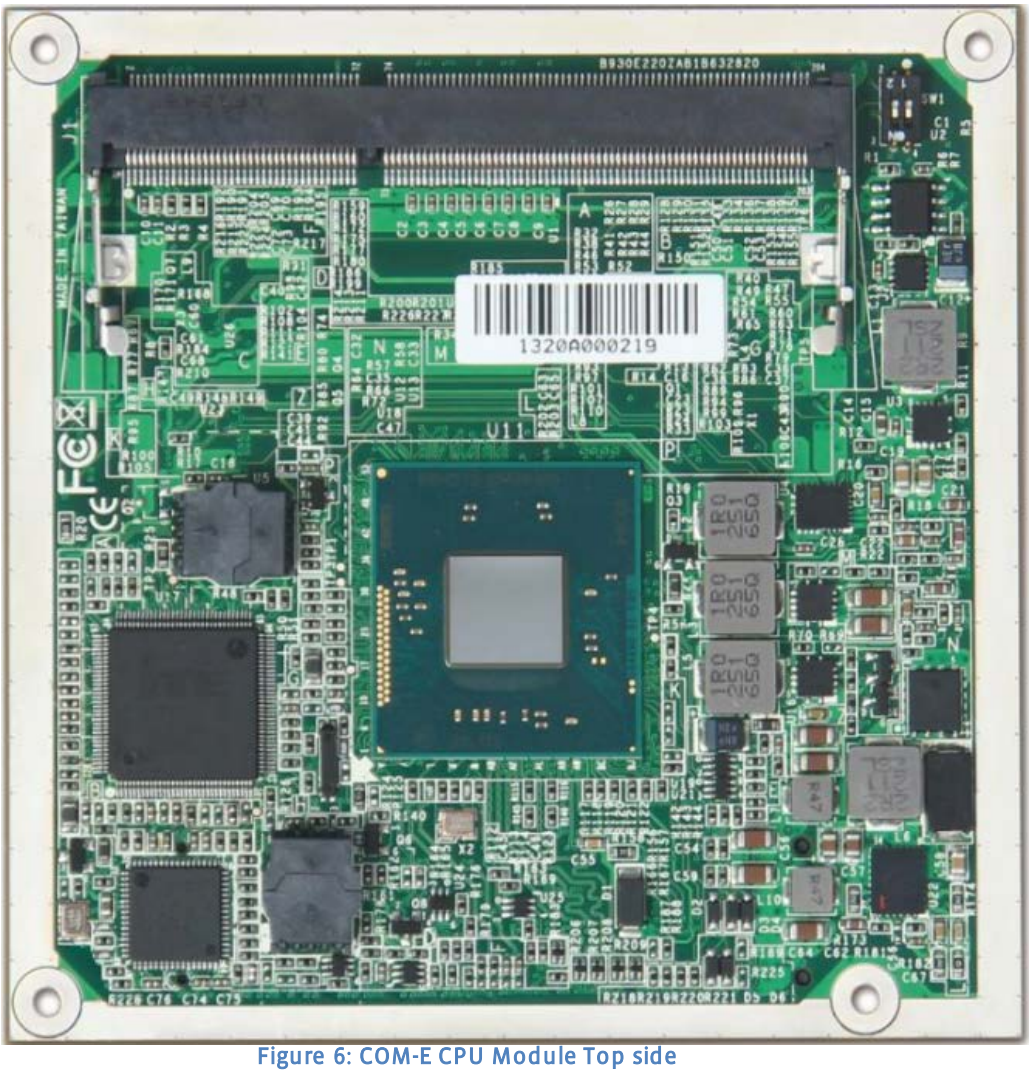

Figure 6: COM-E CPU Module Top side

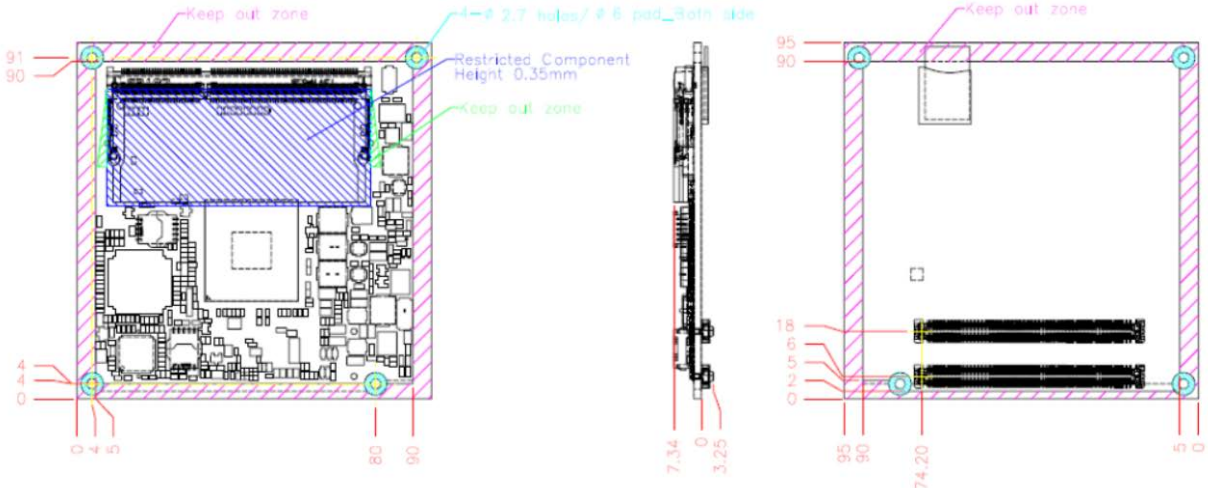

Figure 7: COM-E CPU Module Dimension

5.2.1. PSU

Wedge-100 19-in SKU can use the following PSU from Bel Power Solution:

- SPDFCBK-14G : AC input PSU, 750W
- SPDFCBK-15G : DC input PSU, 750W
- SPDFCBK-16G : DC input PSU, 400W

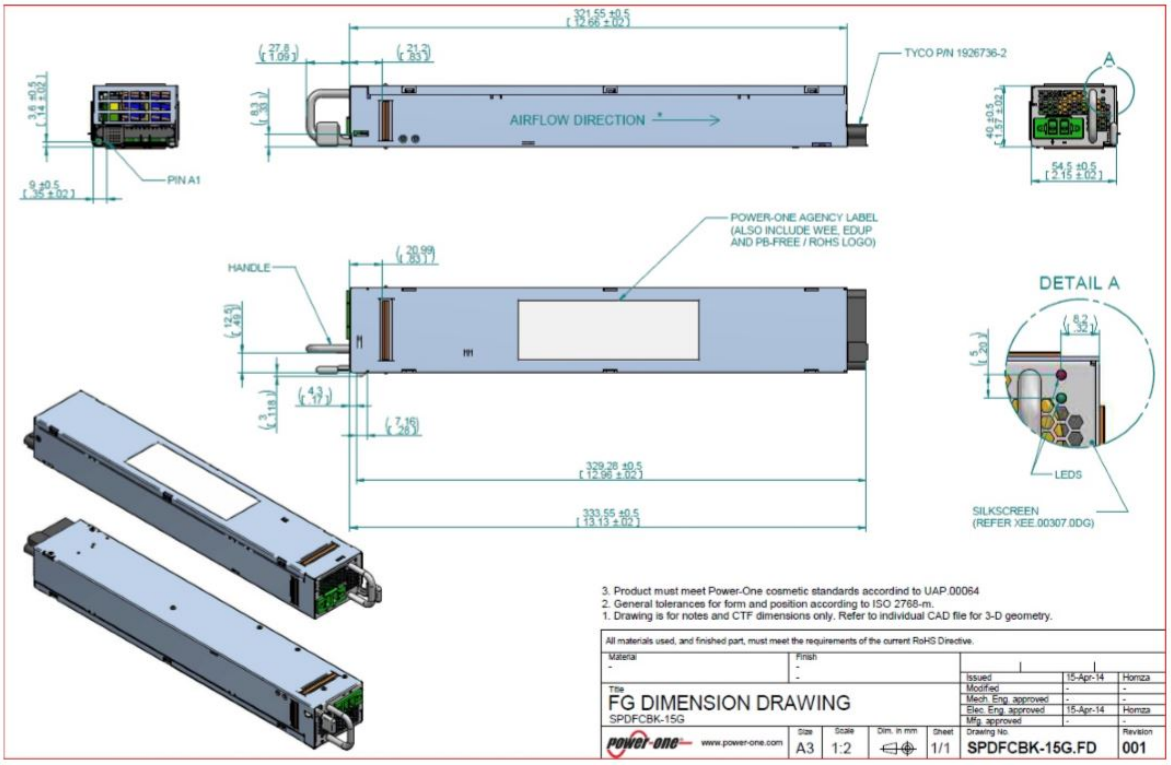

Figure 8: PSU Mechanic Drawing

5.2.1.1. AC PSU output

The following table shows the output ratings of PSU:

Input	Output	Voltage (V)	Current (A)	Power [W]	Ambient Temp Range	Model
54VDC typical 40V~72V	V1	12	62	750	-5C~55C	SPDFCBK-15G
	VSB	3.3	3	10		
54VDC typical 40V~72V	V1	12	33	400	-5C~55C	SPDFCBK-16G
	VSB	3.3	3	10		
120/240Vac	V1	12	62	750	-5C~55C	SPDFCBK-14G
	VSB	3.3	3	10		

Table 3: AC-PSU output

5.2.1.2. PSU output connector

	vendor	MPN	notes
PSU side	Tyco Electronics	2-1926736-2	
Chassis side	Tyco Electronics	2-1926733-5	

Table 4: PSU connectors

PS side: Tyco Electronics P/N: 2-1926736-2

Chassis side: Tyco Electronics P/N: 2-1926733-5

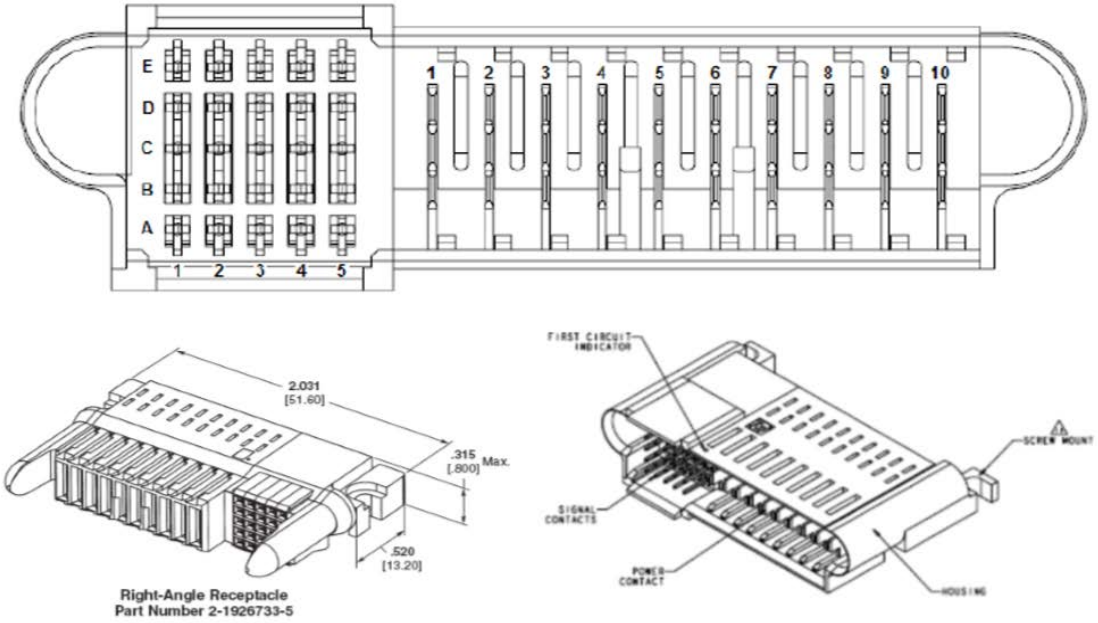

Figure 9: PSU Output Connector

5.2.1.3. PSU output signals

The following table shows the signal definition of the PSU.

Pin	Signal name	IO	Description	Amp per pin
1	PGND	GND	Power ground (return)	25
2	PGND	GND	Power ground (return)	25
3	PGND	GND	Power ground (return)	25
4	PGND	GND	Power ground (return)	25
5	PGND	GND	Power ground (return)	25
6	V1	PWR	12V VDC main output	25
7	V1	PWR	12V VDC main output	25
8	V1	PWR	12V VDC main output	25
9	V1	PWR	12V VDC main output	25
10	V1	PWR	12V VDC main output	25
A1	VSB	PWR	Standby positive output (+3.3V)	
B1	VSB	PWR	Standby positive output (+3.3V)	
C1	VSB	PWR	Standby positive output (+3.3V)	
D1	VSB	PWR	Standby positive output (+3.3V)	
E1	VSB	PWR	Standby positive output (+3.3V)	
A2	SGND	GND	Signal ground (return)	
B2	SGND	GND	Signal ground (return)	
C2	nc		No connect	
D2	nc		No connect	
E2	nc		No connect	
A3	PSKILL	In	Power supply kill (lagging pin), disable V1 output when PSKILL is high	
B3	nc		No connect	
C3	SDA	Inout	I2C data signal line	
D3	V1_SENSE_R		Main output negative sense	
E3	V1_SENSE		Main output positive sense	
A4	SCL	In	I2C clock signal line	
B4	PSON		PSU ON input connect (reference to A2/B2)	
C4	SMB_ALERT	Out	SMB alert signal output	
D4	ISHARE		Current share signal	
E4	INPUT_OK	Out	DC input OK signal, Active High	
A5	A0	In	Address 0	
B5	nc		No connect	
C5	PWOK	Out	Power OK signal output, Active High	
D5	A1	In	Address 1	
E5	PRESENT_L	Out	Power supply present	

Table 5: PSU Output Signals

5.2.1.4. PSU I2C address

PS_A1 and PS_A0 signals are used to set I2C address of PSU.

PS_A1	PS_A0	PSU_ID (MUC) Address	EEPROM Address
0	0	0x58	0x50
0	1	0x59	0x51
1	0	0x5A	0x52
1	1	0x5B	0x53

Table 6: PowerOne PSU I2C address

On wedge-100, in default PS_A0 is pull-up, PS_A1 is pull-down, so the PSU I2C should be 0x59 for MCU, and 0x51 for PSU EEPROM.

5.2.2. Power Pass-through Card for Open Rack

In order to support OCP V2 rack power bus 12V input, Power pass-through card is needed to provide power to 19-in wedge-100 from Open Rack V2 bus bar.

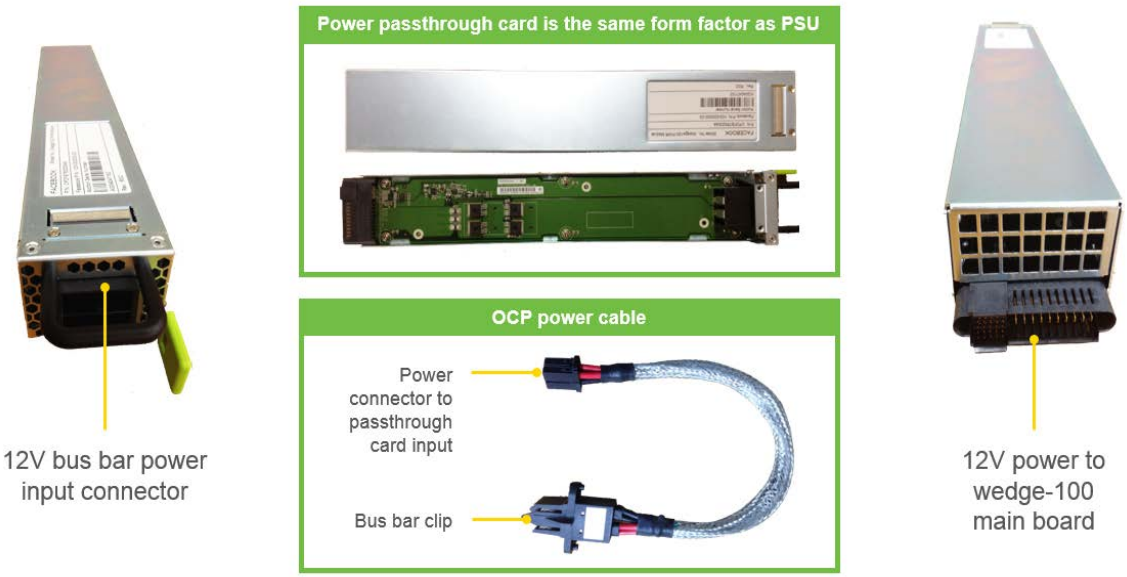

Figure 10: OCP Power Pass-through Card

Power pass-through card uses similar mechanic as AC PSU, and can be plugged into PSU slot. The input of power pass-through module is 12V DC cable, which can connect to bus bar via OCP bus bar clip. The following figure shows the block diagram of the power pass-through card.

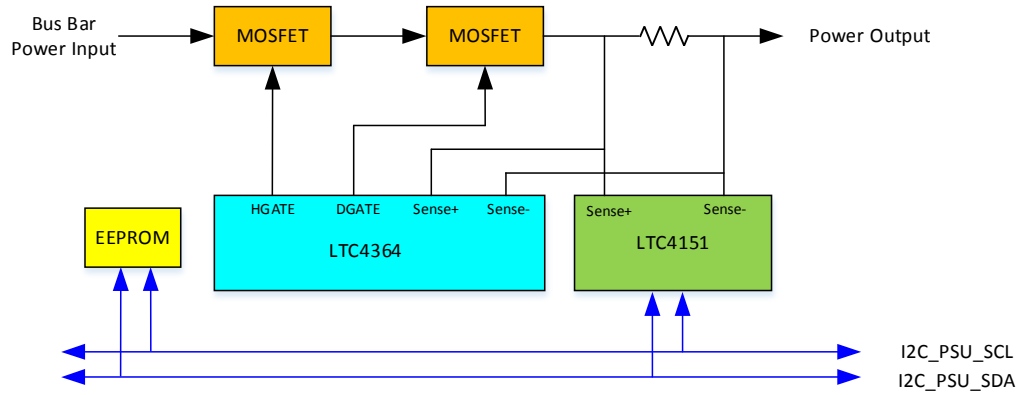

Figure 11: Open Rack Bus Bar Power Pass-through Card Architecture

Power pass-through card support the following features

- 12V input up to 60A

- Hotswap controller LTC4364 supporting hot swap, and ORing function.
- Current sense device LTC4151 for CPU to access current information to know total power consumption of the wedge-100 system
- 2Kb inventory EEPROM

I2C Device	I2C Address	note
LTC4151	0x6F	Current sensing chip
EEPROM	0x54	EEPROM is used for inventory information

Table 7: Pass-through modulcard I2C address

LTC4151 I2C device address is decided by the external pin A1 and A0 status. I2C address of LTC4151 is 0x6F, or 110_1111 in binary format.

5.2.3. Fan tray

Wedge-100 fan-tray uses one counter-rotating fan and is designed to support skew-less operation.

Figure 12: wedge-100 fan-tray

Fantray use Delta Counter-rotating fan GFB0412EHS-DA06

Item	Description
Rated voltage	12 VDC
Operating voltage	10.8 ~ 12.6 VDC
Input current	1.40A, 1.68A Max Safety Current on label: 1.82A
Input power	16.80W, Max 20.16W
speed	Front 16000, Rear 15400 RPM +/-10%
Max Air flow at zero static pressure	66.824 mmH2O, Min 54.127 mmH2O 2.63 InchH2O, Min 2.131 InchH2O

acoustic	64.5 dB-A
Lead Wire	Front Fan Black Wire Negative (-) Red Wire Positive (+) Yellow wire frequency (-FOO) Blue wire speed control (-PWM)
	Rear Fan grey Wire Negative (-) brown Wire Positive (+) white wire frequency (-FOO) green wire speed control (-PWM)

Table 8: Fan specification

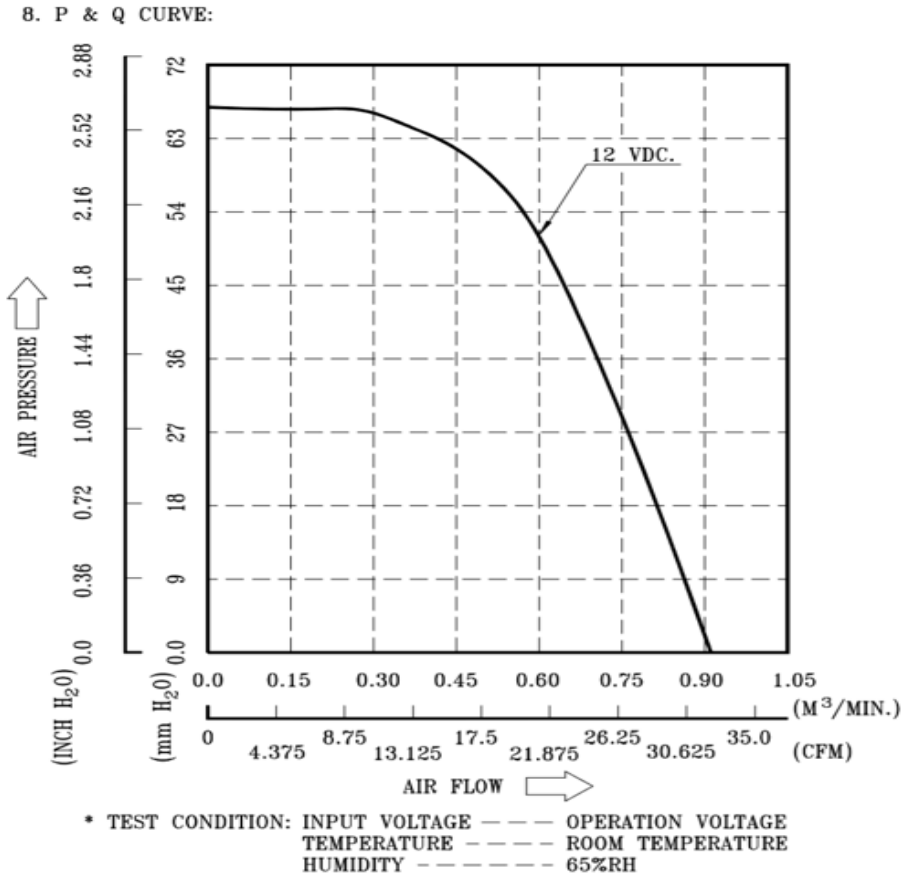

Figure 13: PQ curve of CR fan GFB0412EHS-DA06

5.3. Wedge-100 placement and layout

5.3.1. Wedge-100 top view

The following picture is the top view of wedge-100.

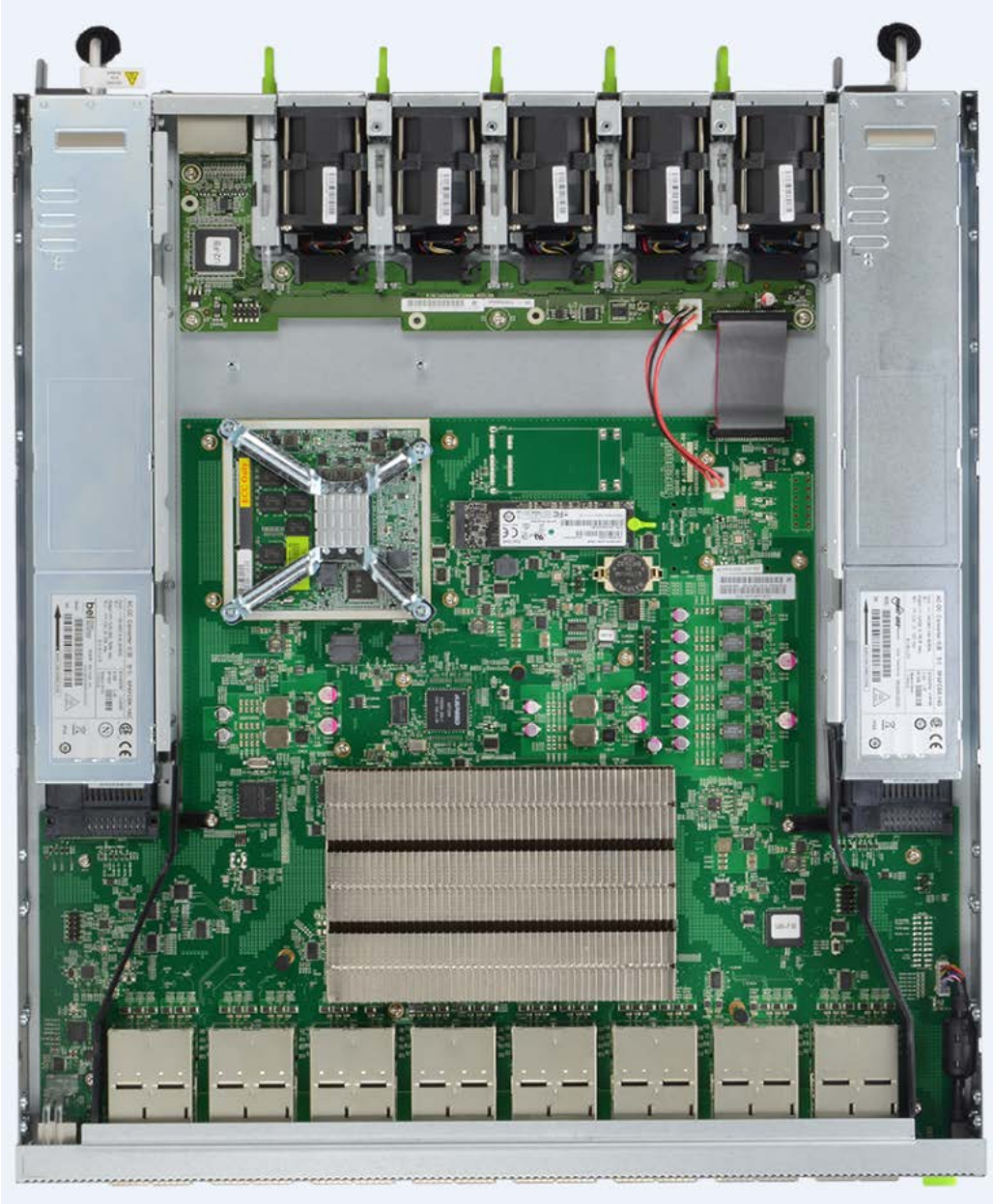

Figure 14: Wedge-100 TOP view

5.3.2. Wedge-100 front panel view

Front panel of wedge-100 has the following interfaces:

- 32 QSFP28 ports
- RJ45 OOB Ethernet interface
- RJ45 RS232 console interface
- USB2 Type-A interface
- Facebook 14-pin debug header
- Recessed push button reset
- Two System LEDs
- LED push button

Figure 15: front panel view of wedge-100

5.3.3. Wedge-100 rear panel view

Rear panel of wedge-100 has the following interfaces:

- PSU AC inlet, left and right
- 3 Rackmon RJ45 interface
- 1 Rackmon GPIO interface
- 5 fan-tray

Figure 16: rear panel view of wedge-100

6. Wedge-100 Thermal

6.1. System Airflow or Volumetric Flow

The unit of airflow (or volumetric flow) used for this specification is CFM (cubic feet per minute). The maximum allowable airflow per Watt in the system must be 0.16 CFM. The desired airflow per watt is 0.1 CFM or lower in the system at the mean temperature (plus or minus standard deviation).

6.2. Operational Ambient Temperatures

The operational ambient temperatures for Wedge-100 are:

- 0°C to 35°C, normal operation with 55°C QSFP28 optics
- 0°C to 45°C normal operation with 70C QSFP28 optics

6.3. Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The minimum 5% thermal margin in Tjunction / Tcase or both is allowed for every component on the card. The stabilized / operational target temperature for every components on the card should be at least 8% below its maximum theoretical safe temperature.

6.4. Separate air channel design for PSU

The fan used inside PSU is much less powerful than system CR fan, each PSU need dedicated air channel to separate main air flow channel from two PSU air channel. Metal air baffle is recommended to use. Proper methods need to be implemented to isolate the air channel as much as possible.

6.5. Tomahawk Heat Sink Requirements

Tomahawk consumes about 170W under typical condition, and 192W under worst scenario. It is required for Tomahawk to use advanced heat sink to support 192W operation of tomahawk. The heatsink could be the following design:

- Solder fin design
- Alumina base with embedded copper heat-pipe. 4 heat-pipe design is recommended.
- Proper heatsink mounting design to avoid tilting of heatsink during shock and vibration

BCM56960 Thermal Spec	Max	Note
Power dissipation (P)	192 W	
Max Junction temperature (Tj)	110 C	
Max Ambient temperature (Ta)	50 C	
Max calculated thermal resistance	0.31 C/W	(Tj - Ta)/P = 60/192 = 0.31

Table 9: Tomahawk(BCM56960) Thermal Specification

6.6. Temperature Sensors

Wedge-100 main board and fan-tray board need to provide multiple temperature sensors for the CPU to know the thermal status of the system. The following spots are critical for thermal policy and better to place sensors on the following spots:

- Left PSU air inlet on main board.
- Right PSU air inlet on main board
- The middle point between Front panel and tomahawk
- The middle point between tomahawk and COM-e CPU module
- two sensors on fan control board

Additionally, over-temperature thresholds are configurable and an alert mechanism is provided to enable thermal shutdown and / or an increase in airflow. The sensors are accurate to +/-2C.

The ambient temperature sensor uses *TMP75* from Texas Instruments or an equivalent part from other vendors. Its I2C address can be set to 0x98 to 0x9F. 8 TMP75 temperature sensors can share one i2c bus. 5 TMP75 are used in wedge-100 main board, and 2 TMP75 sensors are used on fan control card.

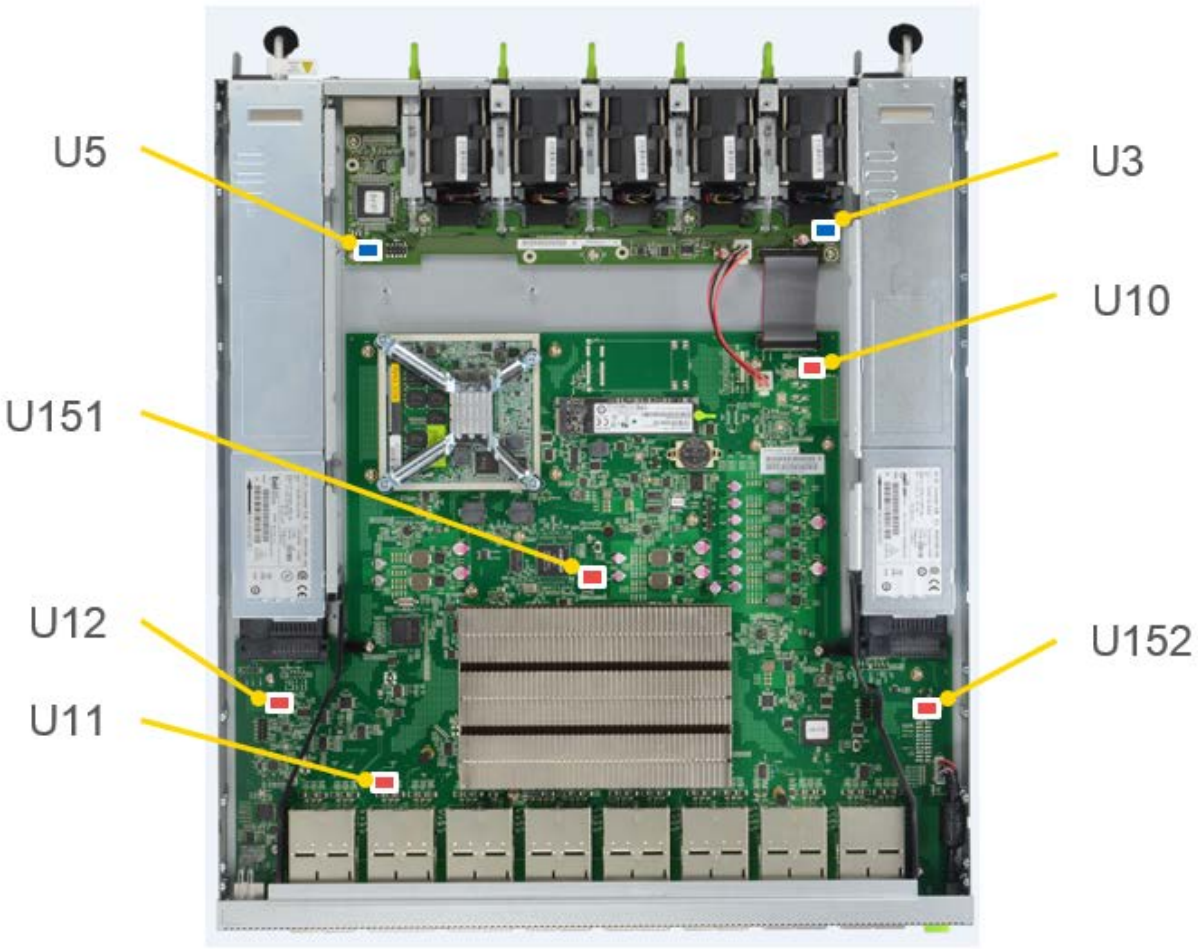

Figure 17: Temperature Sensor Placement

Temperature sensors provide a mechanism to provide thermal alerts and over temperature notifications. The BMC on baseboard must be able to receive these alerts in a timely fashion to allow the system to take action quickly. The I2C alert signal must be used. In some cases, an over temperature condition may occur which forces wedge-100 to power-off immediately. This condition must be logged before shutdown.

7. Wedge-100 Main board Electrical

7.1. BCM56960 Switch ASIC Port Mapping

Wedge-100 qsfp28 ports are numbered in the following sequence.

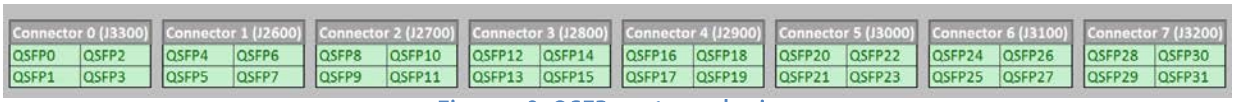

Figure 18: QSFP port numbering

The following table shows the tomahawk SERDES port mapping to external signals.

ASIC	PIN NUM	PIN NAME	NET NAME	QSFP Port	QSFP CHANNEL	Swapping Details	QSFP connector
U900	AE45	FC0_RD0N	P1_RD-	QSFP5	RX CH-1N		CONN-1 J2600
U900	AE46	FC0_RD0P	P1_RD+		RX CH-1P		
U900	AF48	FC0_RD1N	P2_RD-		RX CH-2N		
U900	AF49	FC0_RD1P	P2_RD+		RX CH-2P		
U900	AG45	FC0_RD2N	P3_RD-		RX CH-3N		
U900	AG46	FC0_RD2P	P3_RD+		RX CH-3P		
U900	AH48	FC0_RD3N	P4_RD-		RX CH-4N		
U900	AH49	FC0_RD3P	P4_RD+		RX CH-4P		
U900	AH54	FC0_TD0N	P1_TD-		TX CH-1N		
U900	AH53	FC0_TD0P	P1_TD+		TX CH-1P		
U900	AG52	FC0_TD1N	P2_TD-		TX CH-2N		
U900	AG51	FC0_TD1P	P2_TD+		TX CH-2P		
U900	AF54	FC0_TD2N	P3_TD-		TX CH-3N		
U900	AF53	FC0_TD2P	P3_TD+		TX CH-3P		
U900	AE52	FC0_TD3N	P4_TD-		TX CH-4N		
U900	AE51	FC0_TD3P	P4_TD+		TX CH-4P		
U900	AA45	FC1_RD0N	P5_RD-	QSFP4	RX CH-1N		
U900	AA46	FC1_RD0P	P5_RD+		RX CH-1P		
U900	AB48	FC1_RD1N	P6_RD-		RX CH-2N		
U900	AB49	FC1_RD1P	P6_RD+		RX CH-2P		
U900	AC45	FC1_RD2N	P7_RD-		RX CH-3N		
U900	AC46	FC1_RD2P	P7_RD+		RX CH-3P		
U900	AD48	FC1_RD3N	P8_RD-		RX CH-4N		
U900	AD49	FC1_RD3P	P8_RD+		RX CH-4P		

U900	AD54	FC1_TD0N	P5_TD-		TX CH-1N		
U900	AD53	FC1_TD0P	P5_TD+		TX CH-1P		
U900	AC52	FC1_TD1N	P6_TD-		TX CH-2N		
U900	AC51	FC1_TD1P	P6_TD+		TX CH-2P		
U900	AB54	FC1_TD2N	P7_TD-		TX CH-3N		
U900	AB53	FC1_TD2P	P7_TD+		TX CH-3P		
U900	AA52	FC1_TD3N	P8_TD-		TX CH-4N		
U900	AA51	FC1_TD3P	P8_TD+		TX CH-4P		
U900	U45	FC2_RD0N	P9_RD-		RX CH-1N		
U900	U46	FC2_RD0P	P9_RD+		RX CH-1P		
U900	V48	FC2_RD1N	P10_RD-		RX CH-2N		
U900	V49	FC2_RD1P	P10_RD+		RX CH-2P		
U900	W45	FC2_RD2N	P11_RD-		RX CH-3N		
U900	W46	FC2_RD2P	P11_RD+		RX CH-3P		
U900	Y48	FC2_RD3N	P12_RD-		RX CH-4N		
U900	Y49	FC2_RD3P	P12_RD+		RX CH-4P		
U900	Y54	FC2_TD0N	P9_TD-	QSFP7	TX CH-1N		
U900	Y53	FC2_TD0P	P9_TD+		TX CH-1P		
U900	W52	FC2_TD1N	P10_TD-		TX CH-2N		
U900	W51	FC2_TD1P	P10_TD+		TX CH-2P		
U900	V54	FC2_TD2N	P11_TD-		TX CH-3N		
U900	V53	FC2_TD2P	P11_TD+		TX CH-3P		
U900	U52	FC2_TD3N	P12_TD-		TX CH-4N		
U900	U51	FC2_TD3P	P12_TD+		TX CH-4P		
U900	N45	FC3_RD0N	P13_RD-		RX CH-1N		
U900	N46	FC3_RD0P	P13_RD+		RX CH-1P		
U900	P48	FC3_RD1N	P14_RD-		RX CH-2N		
U900	P49	FC3_RD1P	P14_RD+		RX CH-2P		
U900	R45	FC3_RD2N	P15_RD-		RX CH-3N		
U900	R46	FC3_RD2P	P15_RD+		RX CH-3P		
U900	T48	FC3_RD3N	P16_RD-		RX CH-4N		
U900	T49	FC3_RD3P	P16_RD+		RX CH-4P		
U900	T54	FC3_TD0N	P13_TD-	QSFP6	TX CH-1N		
U900	T53	FC3_TD0P	P13_TD+		TX CH-1P		
U900	R52	FC3_TD1N	P14_TD-		TX CH-2N		
U900	R51	FC3_TD1P	P14_TD+		TX CH-2P		
U900	P54	FC3_TD2N	P15_TD-		TX CH-3N		
U900	P53	FC3_TD2P	P15_TD+		TX CH-3P		
U900	N52	FC3_TD3N	P16_TD-		TX CH-4N		
U900	N51	FC3_TD3P	P16_TD+		TX CH-4P		

U900	F52	FC4_RD0N	P19_RD-	QSFP9	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	CONN-2 J2700
U900	G52	FC4_RD0P	P19_RD+		RX CH-3P		
U900	J51	FC4_RD1N	P20_RD-		RX CH-4N		
U900	K51	FC4_RD1P	P20_RD+		RX CH-4P		
U900	F50	FC4_RD2N	P17_RD-		RX CH-1N		
U900	G50	FC4_RD2P	P17_RD+		RX CH-1P		
U900	J49	FC4_RD3N	P18_RD-		RX CH-2N		
U900	K49	FC4_RD3P	P18_RD+		RX CH-2P		
U900	B52	FC4_TD0N	P17_TD-		TX CH-1N		
U900	A52	FC4_TD0P	P17_TD+		TX CH-1P		
U900	D51	FC4_TD1N	P18_TD-		TX CH-2N		
U900	C51	FC4_TD1P	P18_TD+		TX CH-2P		
U900	B50	FC4_TD2N	P19_TD-		TX CH-3N		
U900	A50	FC4_TD2P	P19_TD+		TX CH-3P		
U900	D49	FC4_TD3N	P20_TD-		TX CH-4N		
U900	C49	FC4_TD3P	P20_TD+		TX CH-4P		
U900	K45	FC5_RD0N	P22_RD-	QSFP8	RX CH-2N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	J45	FC5_RD0P	P22_RD+		RX CH-2P		
U900	G46	FC5_RD1N	P21_RD-		RX CH-1N		
U900	F46	FC5_RD1P	P21_RD+		RX CH-1P		
U900	K47	FC5_RD2N	P24_RD-		RX CH-4N		
U900	J47	FC5_RD2P	P24_RD+		RX CH-4P		
U900	G48	FC5_RD3N	P23_RD-		RX CH-3N		
U900	F48	FC5_RD3P	P23_RD+		RX CH-3P		
U900	C45	FC5_TD0N	P23_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	D45	FC5_TD0P	P23_TD+		TX CH-3P		
U900	A46	FC5_TD1N	P24_TD-		TX CH-4N		
U900	B46	FC5_TD1P	P24_TD+		TX CH-4P		
U900	C47	FC5_TD2N	P21_TD-		TX CH-1N		
U900	D47	FC5_TD2P	P21_TD+		TX CH-1P		
U900	A48	FC5_TD3N	P22_TD-		TX CH-2N		
U900	B48	FC5_TD3P	P22_TD+		TX CH-2P		
U900	F44	FC6_RD0N	P27_RD-	QSFP11	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	G44	FC6_RD0P	P27_RD+		RX CH-3P		
U900	J43	FC6_RD1N	P28_RD-		RX CH-4N		
U900	K43	FC6_RD1P	P28_RD+		RX CH-4P		
U900	F42	FC6_RD2N	P25_RD-		RX CH-1N		
U900	G42	FC6_RD2P	P25_RD+		RX CH-1P		
U900	J41	FC6_RD3N	P26_RD-		RX CH-2N		
U900	K41	FC6_RD3P	P26_RD+		RX CH-2P		

U900	B44	FC6_TD0N	P25_TD-		TX CH-1N		
U900	A44	FC6_TD0P	P25_TD+		TX CH-1P		
U900	D43	FC6_TD1N	P26_TD-		TX CH-2N		
U900	C43	FC6_TD1P	P26_TD+		TX CH-2P		
U900	B42	FC6_TD2N	P27_TD-		TX CH-3N		
U900	A42	FC6_TD2P	P27_TD+		TX CH-3P		
U900	D41	FC6_TD3N	P28_TD-		TX CH-4N		
U900	C41	FC6_TD3P	P28_TD+		TX CH-4P		
U900	K37	FC7_RD0N	P29_RD-		RX CH-1N		
U900	J37	FC7_RD0P	P29_RD+		RX CH-1P		
U900	G38	FC7_RD1N	P30_RD-		RX CH-2N		
U900	F38	FC7_RD1P	P30_RD+		RX CH-2P		
U900	K39	FC7_RD2N	P31_RD-		RX CH-3N		
U900	J39	FC7_RD2P	P31_RD+		RX CH-3P		
U900	G40	FC7_RD3N	P32_RD-		RX CH-4N		
U900	F40	FC7_RD3P	P32_RD+	QSFP10	RX CH-4P		
U900	C37	FC7_TD0N	P31_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	D37	FC7_TD0P	P31_TD+		TX CH-3P		
U900	A38	FC7_TD1N	P32_TD-		TX CH-4N		
U900	B38	FC7_TD1P	P32_TD+		TX CH-4P		
U900	C39	FC7_TD2N	P29_TD-		TX CH-1N		
U900	D39	FC7_TD2P	P29_TD+		TX CH-1P		
U900	A40	FC7_TD3N	P30_TD-		TX CH-2N		
U900	B40	FC7_TD3P	P30_TD+		TX CH-2P		
U900	K18	FC8_RD0N	P35_RD-		RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	CONN-3 J2800
U900	J18	FC8_RD0P	P35_RD+		RX CH-3P		
U900	G17	FC8_RD1N	P36_RD-		RX CH-4N		
U900	F17	FC8_RD1P	P36_RD+		RX CH-4P		
U900	K16	FC8_RD2N	P33_RD-		RX CH-1N		
U900	J16	FC8_RD2P	P33_RD+		RX CH-1P		
U900	G15	FC8_RD3N	P34_RD-		RX CH-2N		
U900	F15	FC8_RD3P	P34_RD+	QSFP13	RX CH-2P		
U900	C18	FC8_TD0N	P33_TD-		TX CH-1N		
U900	D18	FC8_TD0P	P33_TD+		TX CH-1P		
U900	A17	FC8_TD1N	P34_TD-		TX CH-2N		
U900	B17	FC8_TD1P	P34_TD+		TX CH-2P		
U900	C16	FC8_TD2N	P35_TD-		TX CH-3N		
U900	D16	FC8_TD2P	P35_TD+		TX CH-3P		
U900	A15	FC8_TD3N	P36_TD-		TX CH-4N		
U900	B15	FC8_TD3P	P36_TD+		TX CH-4P		

U900	F11	FC9_RD0N	P38_RD-	QSFP12	RX CH-2N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	G11	FC9_RD0P	P38_RD+		RX CH-2P		
U900	J12	FC9_RD1N	P37_RD-		RX CH-1N		
U900	K12	FC9_RD1P	P37_RD+		RX CH-1P		
U900	F13	FC9_RD2N	P40_RD-		RX CH-4N		
U900	G13	FC9_RD2P	P40_RD+		RX CH-4P		
U900	J14	FC9_RD3N	P39_RD-		RX CH-3N		
U900	K14	FC9_RD3P	P39_RD+		RX CH-3P		
U900	B11	FC9_TD0N	P39_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	A11	FC9_TD0P	P39_TD+		TX CH-3P		
U900	D12	FC9_TD1N	P40_TD-		TX CH-4N		
U900	C12	FC9_TD1P	P40_TD+		TX CH-4P		
U900	B13	FC9_TD2N	P37_TD-		TX CH-1N		
U900	A13	FC9_TD2P	P37_TD+		TX CH-1P		
U900	D14	FC9_TD3N	P38_TD-		TX CH-2N		
U900	C14	FC9_TD3P	P38_TD+		TX CH-2P		
U900	K10	FC10_RD0N	P43_RD-	QSFP15	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	J10	FC10_RD0P	P43_RD+		RX CH-3P		
U900	G9	FC10_RD1N	P44_RD-		RX CH-4N		
U900	F9	FC10_RD1P	P44_RD+		RX CH-4P		
U900	K8	FC10_RD2N	P41_RD-		RX CH-1N		
U900	J8	FC10_RD2P	P41_RD+		RX CH-1P		
U900	G7	FC10_RD3N	P42_RD-		RX CH-2N		
U900	F7	FC10_RD3P	P42_RD+		RX CH-2P		
U900	C10	FC10_TD0N	P41_TD-		TX CH-1N		
U900	D10	FC10_TD0P	P41_TD+		TX CH-1P		
U900	A9	FC10_TD1N	P42_TD-		TX CH-2N		
U900	B9	FC10_TD1P	P42_TD+		TX CH-2P		
U900	C8	FC10_TD2N	P43_TD-		TX CH-3N		
U900	D8	FC10_TD2P	P43_TD+		TX CH-3P		
U900	A7	FC10_TD3N	P44_TD-		TX CH-4N		
U900	B7	FC10_TD3P	P44_TD+		TX CH-4P		
U900	F3	FC11_RD0N	P45_RD-	QSFP14	RX CH-1N		
U900	G3	FC11_RD0P	P45_RD+		RX CH-1P		
U900	J4	FC11_RD1N	P46_RD-		RX CH-2N		
U900	K4	FC11_RD1P	P46_RD+		RX CH-2P		
U900	F5	FC11_RD2N	P47_RD-		RX CH-3N		
U900	G5	FC11_RD2P	P47_RD+		RX CH-3P		
U900	J6	FC11_RD3N	P48_RD-		RX CH-4N		
U900	K6	FC11_RD3P	P48_RD+		RX CH-4P		

U900	B3	FC11_TD0N	P47_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	A3	FC11_TD0P	P47_TD+		TX CH-3P		
U900	D4	FC11_TD1N	P48_TD-		TX CH-4N		
U900	C4	FC11_TD1P	P48_TD+		TX CH-4P		
U900	B5	FC11_TD2N	P45_TD-		TX CH-1N		
U900	A5	FC11_TD2P	P45_TD+		TX CH-1P		
U900	D6	FC11_TD3N	P46_TD-		TX CH-2N		
U900	C6	FC11_TD3P	P46_TD+		TX CH-2P		
U900	N7	FC12_RD0N	P51_RD-	QSFP17	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	CONN-4 J2900
U900	N6	FC12_RD0P	P51_RD+		RX CH-3P		
U900	P10	FC12_RD1N	P52_RD-		RX CH-4N		
U900	P9	FC12_RD1P	P52_RD+		RX CH-4P		
U900	R7	FC12_RD2N	P49_RD-		RX CH-1N		
U900	R6	FC12_RD2P	P49_RD+		RX CH-1P		
U900	T10	FC12_RD3N	P50_RD-		RX CH-2N		
U900	T9	FC12_RD3P	P50_RD+		RX CH-2P		
U900	T3	FC12_TD0N	P51_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	T4	FC12_TD0P	P51_TD+		TX CH-3P		
U900	R1	FC12_TD1N	P52_TD-		TX CH-4N		
U900	R2	FC12_TD1P	P52_TD+		TX CH-4P		
U900	P3	FC12_TD2N	P49_TD-		TX CH-1N		
U900	P4	FC12_TD2P	P49_TD+		TX CH-1P		
U900	N1	FC12_TD3N	P50_TD-		TX CH-2N		
U900	N2	FC12_TD3P	P50_TD+		TX CH-2P		
U900	U7	FC13_RD0N	P55_RD-	QSFP16	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	U6	FC13_RD0P	P55_RD+		RX CH-3P		
U900	V10	FC13_RD1N	P56_RD-		RX CH-4N		
U900	V9	FC13_RD1P	P56_RD+		RX CH-4P		
U900	W7	FC13_RD2N	P53_RD-		RX CH-1N		
U900	W6	FC13_RD2P	P53_RD+		RX CH-1P		
U900	Y10	FC13_RD3N	P54_RD-		RX CH-2N		
U900	Y9	FC13_RD3P	P54_RD+		RX CH-2P		
U900	Y3	FC13_TD0N	P55_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	Y4	FC13_TD0P	P55_TD+		TX CH-3P		
U900	W1	FC13_TD1N	P56_TD-		TX CH-4N		
U900	W2	FC13_TD1P	P56_TD+		TX CH-4P		
U900	V3	FC13_TD2N	P53_TD-		TX CH-1N		
U900	V4	FC13_TD2P	P53_TD+		TX CH-1P		
U900	U1	FC13_TD3N	P54_TD-		TX CH-2N		
U900	U2	FC13_TD3P	P54_TD+		TX CH-2P		

U900	AA7	FC14_RD0N	P59_RD-	QSFP19	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AA6	FC14_RD0P	P59_RD+		RX CH-3P		
U900	AB10	FC14_RD1N	P60_RD-		RX CH-4N		
U900	AB9	FC14_RD1P	P60_RD+		RX CH-4P		
U900	AC7	FC14_RD2N	P57_RD-		RX CH-1N		
U900	AC6	FC14_RD2P	P57_RD+		RX CH-1P		
U900	AD10	FC14_RD3N	P58_RD-		RX CH-2N		
U900	AD9	FC14_RD3P	P58_RD+		RX CH-2P		
U900	AD3	FC14_TD0N	P59_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AD4	FC14_TD0P	P59_TD+		TX CH-3P		
U900	AC1	FC14_TD1N	P60_TD-		TX CH-4N		
U900	AC2	FC14_TD1P	P60_TD+		TX CH-4P		
U900	AB3	FC14_TD2N	P57_TD-		TX CH-1N		
U900	AB4	FC14_TD2P	P57_TD+		TX CH-1P		
U900	AA1	FC14_TD3N	P58_TD-		TX CH-2N		
U900	AA2	FC14_TD3P	P58_TD+		TX CH-2P		
U900	AE7	FC15_RD0N	P63_RD-	QSFP18	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AE6	FC15_RD0P	P63_RD+		RX CH-3P		
U900	AF10	FC15_RD1N	P64_RD-		RX CH-4N		
U900	AF9	FC15_RD1P	P64_RD+		RX CH-4P		
U900	AG7	FC15_RD2N	P61_RD-		RX CH-1N		
U900	AG6	FC15_RD2P	P61_RD+		RX CH-1P		
U900	AH10	FC15_RD3N	P62_RD-		RX CH-2N		
U900	AH9	FC15_RD3P	P62_RD+		RX CH-2P		
U900	AH3	FC15_TD0N	P63_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AH4	FC15_TD0P	P63_TD+		TX CH-3P		
U900	AG1	FC15_TD1N	P64_TD-		TX CH-4N		
U900	AG2	FC15_TD1P	P64_TD+		TX CH-4P		
U900	AF3	FC15_TD2N	P61_TD-		TX CH-1N		
U900	AF4	FC15_TD2P	P61_TD+		TX CH-1P		
U900	AE1	FC15_TD3N	P62_TD-		TX CH-2N		
U900	AE2	FC15_TD3P	P62_TD+		TX CH-2P		
U900	AN7	FC16_RD0N	P65_RD-	QSFP21	RX CH-1N		CONN-5 J3000
U900	AN6	FC16_RD0P	P65_RD+		RX CH-1P		
U900	AM10	FC16_RD1N	P66_RD-		RX CH-2N		
U900	AM9	FC16_RD1P	P66_RD+		RX CH-2P		
U900	AL7	FC16_RD2N	P67_RD-		RX CH-3N		
U900	AL6	FC16_RD2P	P67_RD+		RX CH-3P		
U900	AK10	FC16_RD3N	P68_RD-		RX CH-4N		
U900	AK9	FC16_RD3P	P68_RD+		RX CH-4P		

U900	AK3	FC16_TD0N	P65_TD-		TX CH-1N		
U900	AK4	FC16_TD0P	P65_TD+		TX CH-1P		
U900	AL1	FC16_TD1N	P66_TD-		TX CH-2N		
U900	AL2	FC16_TD1P	P66_TD+		TX CH-2P		
U900	AM3	FC16_TD2N	P67_TD-		TX CH-3N		
U900	AM4	FC16_TD2P	P67_TD+		TX CH-3P		
U900	AN1	FC16_TD3N	P68_TD-		TX CH-4N		
U900	AN2	FC16_TD3P	P68_TD+		TX CH-4P		
U900	AR7	FC17_RD0N	P71_RD-	QSFP20	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AR6	FC17_RD0P	P71_RD+		RX CH-3P		
U900	AT10	FC17_RD1N	P72_RD-		RX CH-4N		
U900	AT9	FC17_RD1P	P72_RD+		RX CH-4P		
U900	AU7	FC17_RD2N	P69_RD-		RX CH-1N		
U900	AU6	FC17_RD2P	P69_RD+		RX CH-1P		
U900	AV10	FC17_RD3N	P70_RD-		RX CH-2N		
U900	AV9	FC17_RD3P	P70_RD+		RX CH-2P		
U900	AV3	FC17_TD0N	P71_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AV4	FC17_TD0P	P71_TD+		TX CH-3P		
U900	AU1	FC17_TD1N	P72_TD-		TX CH-4N		
U900	AU2	FC17_TD1P	P72_TD+		TX CH-4P		
U900	AT3	FC17_TD2N	P69_TD-		TX CH-1N		
U900	AT4	FC17_TD2P	P69_TD+		TX CH-1P		
U900	AR1	FC17_TD3N	P70_TD-		TX CH-2N		
U900	AR2	FC17_TD3P	P70_TD+		TX CH-2P		
U900	AW7	FC18_RD0N	P75_RD-	QSFP23	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AW6	FC18_RD0P	P75_RD+		RX CH-3P		
U900	AY10	FC18_RD1N	P76_RD-		RX CH-4N		
U900	AY9	FC18_RD1P	P76_RD+		RX CH-4P		
U900	BA7	FC18_RD2N	P73_RD-		RX CH-1N		
U900	BA6	FC18_RD2P	P73_RD+		RX CH-1P		
U900	BB10	FC18_RD3N	P74_RD-		RX CH-2N		
U900	BB9	FC18_RD3P	P74_RD+		RX CH-2P		
U900	BB3	FC18_TD0N	P75_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BB4	FC18_TD0P	P75_TD+		TX CH-3P		
U900	BA1	FC18_TD1N	P76_TD-		TX CH-4N		
U900	BA2	FC18_TD1P	P76_TD+		TX CH-4P		
U900	AY3	FC18_TD2N	P73_TD-		TX CH-1N		
U900	AY4	FC18_TD2P	P73_TD+		TX CH-1P		
U900	AW1	FC18_TD3N	P74_TD-		TX CH-2N		
U900	AW2	FC18_TD3P	P74_TD+		TX CH-2P		

U900	BF4	FC19_RD0N	P80_RD-	QSFP22	RX CH-4N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BE4	FC19_RD0P	P80_RD+		RX CH-4P		
U900	BJ3	FC19_RD1N	P78_RD-		RX CH-2N		
U900	BH3	FC19_RD1P	P78_RD+		RX CH-2P		
U900	BF6	FC19_RD2N	P79_RD-		RX CH-3N		
U900	BE6	FC19_RD2P	P79_RD+		RX CH-3P		
U900	BJ5	FC19_RD3N	P77_RD-		RX CH-1N		
U900	BH5	FC19_RD3P	P77_RD+		RX CH-1P		
U900	BN3	FC19_TD0N	P77_TD-		TX CH-1N		
U900	BP3	FC19_TD0P	P77_TD+		TX CH-1P		
U900	BL4	FC19_TD1N	P78_TD-		TX CH-2N		
U900	BM4	FC19_TD1P	P78_TD+		TX CH-2P		
U900	BN5	FC19_TD2N	P79_TD-		TX CH-3N		
U900	BP5	FC19_TD2P	P79_TD+		TX CH-3P		
U900	BL6	FC19_TD3N	P80_TD-		TX CH-4N		
U900	BM6	FC19_TD3P	P80_TD+		TX CH-4P		
U900	BH9	FC20_RD0N	P81_RD-	QSFP25	RX CH-1N		CONN-6 J3100
U900	BJ9	FC20_RD0P	P81_RD+		RX CH-1P		
U900	BE10	FC20_RD1N	P82_RD-		RX CH-2N		
U900	BF10	FC20_RD1P	P82_RD+		RX CH-2P		
U900	BH7	FC20_RD2N	P83_RD-		RX CH-3N		
U900	BJ7	FC20_RD2P	P83_RD+		RX CH-3P		
U900	BE8	FC20_RD3N	P84_RD-		RX CH-4N		
U900	BF8	FC20_RD3P	P84_RD+		RX CH-4P		
U900	BM10	FC20_TD0N	P83_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BL10	FC20_TD0P	P83_TD+		TX CH-3P		
U900	BP9	FC20_TD1N	P84_TD-		TX CH-4N		
U900	BN9	FC20_TD1P	P84_TD+		TX CH-4P		
U900	BM8	FC20_TD2N	P81_TD-		TX CH-1N		
U900	BL8	FC20_TD2P	P81_TD+		TX CH-1P		
U900	BP7	FC20_TD3N	P82_TD-		TX CH-2N		
U900	BN7	FC20_TD3P	P82_TD+		TX CH-2P		
U900	BF12	FC21_RD0N	P88_RD-	QSFP24	RX CH-4N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BE12	FC21_RD0P	P88_RD+		RX CH-4P		
U900	BJ11	FC21_RD1N	P87_RD-		RX CH-3N		
U900	BH11	FC21_RD1P	P87_RD+		RX CH-3P		
U900	BF14	FC21_RD2N	P86_RD-		RX CH-2N		
U900	BE14	FC21_RD2P	P86_RD+		RX CH-2P		
U900	BJ13	FC21_RD3N	P85_RD-		RX CH-1N		
U900	BH13	FC21_RD3P	P85_RD+		RX CH-1P		

U900	BN11	FC21_TD0N	P85_TD-		TX CH-1N		
U900	BP11	FC21_TD0P	P85_TD+		TX CH-1P		
U900	BL12	FC21_TD1N	P86_TD-		TX CH-2N		
U900	BM12	FC21_TD1P	P86_TD+		TX CH-2P		
U900	BN13	FC21_TD2N	P87_TD-		TX CH-3N		
U900	BP13	FC21_TD2P	P87_TD+		TX CH-3P		
U900	BL14	FC21_TD3N	P88_TD-		TX CH-4N		
U900	BM14	FC21_TD3P	P88_TD+		TX CH-4P		
U900	BH17	FC22_RD0N	P89_RD-	QSFP27	RX CH-1N		
U900	BJ17	FC22_RD0P	P89_RD+		RX CH-1P		
U900	BE18	FC22_RD1N	P90_RD-		RX CH-2N		
U900	BF18	FC22_RD1P	P90_RD+		RX CH-2P		
U900	BH15	FC22_RD2N	P91_RD-		RX CH-3N		
U900	BJ15	FC22_RD2P	P91_RD+		RX CH-3P		
U900	BE16	FC22_RD3N	P92_RD-		RX CH-4N		
U900	BF16	FC22_RD3P	P92_RD+		RX CH-4P		
U900	BM18	FC22_TD0N	P91_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BL18	FC22_TD0P	P91_TD+		TX CH-3P		
U900	BP17	FC22_TD1N	P92_TD-		TX CH-4N		
U900	BN17	FC22_TD1P	P92_TD+		TX CH-4P		
U900	BM16	FC22_TD2N	P89_TD-		TX CH-1N		
U900	BL16	FC22_TD2P	P89_TD+		TX CH-1P		
U900	BP15	FC22_TD3N	P90_TD-		TX CH-2N		
U900	BN15	FC22_TD3P	P90_TD+		TX CH-2P		
U900	BF20	FC23_RD0N	P95_RD-	QSFP26	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BE20	FC23_RD0P	P95_RD+		RX CH-3P		
U900	BJ19	FC23_RD1N	P96_RD-		RX CH-4N		
U900	BH19	FC23_RD1P	P96_RD+		RX CH-4P		
U900	BF22	FC23_RD2N	P93_RD-		RX CH-1N		
U900	BE22	FC23_RD2P	P93_RD+		RX CH-1P		
U900	BJ21	FC23_RD3N	P94_RD-		RX CH-2N		
U900	BH21	FC23_RD3P	P94_RD+		RX CH-2P		
U900	BN19	FC23_TD0N	P93_TD-		TX CH-1N		
U900	BP19	FC23_TD0P	P93_TD+		TX CH-1P		
U900	BL20	FC23_TD1N	P94_TD-		TX CH-2N		
U900	BM20	FC23_TD1P	P94_TD+		TX CH-2P		
U900	BN21	FC23_TD2N	P95_TD-		TX CH-3N		
U900	BP21	FC23_TD2P	P95_TD+		TX CH-3P		
U900	BL22	FC23_TD3N	P96_TD-		TX CH-4N		
U900	BM22	FC23_TD3P	P96_TD+		TX CH-4P		

U900	BF35	FC24_RD0N	P97_RD-	QSFP29	RX CH-1N		CONN-7 J3200
U900	BE35	FC24_RD0P	P97_RD+		RX CH-1P		
U900	BJ36	FC24_RD1N	P98_RD-		RX CH-2N		
U900	BH36	FC24_RD1P	P98_RD+		RX CH-2P		
U900	BF33	FC24_RD2N	P99_RD-		RX CH-3N		
U900	BE33	FC24_RD2P	P99_RD+		RX CH-3P		
U900	BJ34	FC24_RD3N	P100_RD-		RX CH-4N		
U900	BH34	FC24_RD3P	P100_RD+		RX CH-4P		
U900	BN36	FC24_TD0N	P99_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BP36	FC24_TD0P	P99_TD+		TX CH-3P		
U900	BL35	FC24_TD1N	P100_TD-		TX CH-4N		
U900	BM35	FC24_TD1P	P100_TD+		TX CH-4P		
U900	BN34	FC24_TD2N	P97_TD-		TX CH-1N		
U900	BP34	FC24_TD2P	P97_TD+		TX CH-1P		
U900	BL33	FC24_TD3N	P98_TD-		TX CH-2N		
U900	BM33	FC24_TD3P	P98_TD+		TX CH-2P		
U900	BH38	FC25_RD0N	P104_RD-	QSFP28	RX CH-4N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BJ38	FC25_RD0P	P104_RD+		RX CH-4P		
U900	BE37	FC25_RD1N	P103_RD-		RX CH-3N		
U900	BF37	FC25_RD1P	P103_RD+		RX CH-3P		
U900	BH40	FC25_RD2N	P102_RD-		RX CH-2N		
U900	BJ40	FC25_RD2P	P102_RD+		RX CH-2P		
U900	BE39	FC25_RD3N	P101_RD-		RX CH-1N		
U900	BF39	FC25_RD3P	P101_RD+		RX CH-1P		
U900	BM37	FC25_TD0N	P101_TD-		TX CH-1N		
U900	BL37	FC25_TD0P	P101_TD+		TX CH-1P		
U900	BP38	FC25_TD1N	P102_TD-		TX CH-2N		
U900	BN38	FC25_TD1P	P102_TD+		TX CH-2P		
U900	BM39	FC25_TD2N	P103_TD-		TX CH-3N		
U900	BL39	FC25_TD2P	P103_TD+		TX CH-3P		
U900	BP40	FC25_TD3N	P104_TD-		TX CH-4N		
U900	BN40	FC25_TD3P	P104_TD+		TX CH-4P		
U900	BF43	FC26_RD0N	P105_RD-	QSFP31	RX CH-1N		
U900	BE43	FC26_RD0P	P105_RD+		RX CH-1P		
U900	BJ44	FC26_RD1N	P106_RD-		RX CH-2N		
U900	BH44	FC26_RD1P	P106_RD+		RX CH-2P		
U900	BF41	FC26_RD2N	P107_RD-		RX CH-3N		
U900	BE41	FC26_RD2P	P107_RD+		RX CH-3P		
U900	BJ42	FC26_RD3N	P108_RD-		RX CH-4N		
U900	BH42	FC26_RD3P	P108_RD+		RX CH-4P		

U900	BN44	FC26_TD0N	P107_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BP44	FC26_TD0P	P107_TD+		TX CH-3P		
U900	BL43	FC26_TD1N	P108_TD-		TX CH-4N		
U900	BM43	FC26_TD1P	P108_TD+		TX CH-4P		
U900	BN42	FC26_TD2N	P105_TD-		TX CH-1N		
U900	BP42	FC26_TD2P	P105_TD+		TX CH-1P		
U900	BL41	FC26_TD3N	P106_TD-		TX CH-2N		
U900	BM41	FC26_TD3P	P106_TD+		TX CH-2P		
U900	BH46	FC27_RD0N	P111_RD-	QSFP30	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BJ46	FC27_RD0P	P111_RD+		RX CH-3P		
U900	BE45	FC27_RD1N	P112_RD-		RX CH-4N		
U900	BF45	FC27_RD1P	P112_RD+		RX CH-4P		
U900	BH48	FC27_RD2N	P109_RD-		RX CH-1N		
U900	BJ48	FC27_RD2P	P109_RD+		RX CH-1P		
U900	BE47	FC27_RD3N	P110_RD-		RX CH-2N		
U900	BF47	FC27_RD3P	P110_RD+		RX CH-2P		
U900	BM45	FC27_TD0N	P109_TD-		TX CH-1N		
U900	BL45	FC27_TD0P	P109_TD+		TX CH-1P		
U900	BP46	FC27_TD1N	P110_TD-		TX CH-2N		
U900	BN46	FC27_TD1P	P110_TD+		TX CH-2P		
U900	BM47	FC27_TD2N	P111_TD-		TX CH-3N		
U900	BL47	FC27_TD2P	P111_TD+		TX CH-3P		
U900	BP48	FC27_TD3N	P112_TD-		TX CH-4N		
U900	BN48	FC27_TD3P	P112_TD+		TX CH-4P		
U900	BF51	FC28_RD0N	P113_RD-	QSFP1	RX CH-1N		CONN-0 J3300
U900	BE51	FC28_RD0P	P113_RD+		RX CH-1P		
U900	BJ52	FC28_RD1N	P114_RD-		RX CH-2N		
U900	BH52	FC28_RD1P	P114_RD+		RX CH-2P		
U900	BF49	FC28_RD2N	P115_RD-		RX CH-3N		
U900	BE49	FC28_RD2P	P115_RD+		RX CH-3P		
U900	BJ50	FC28_RD3N	P116_RD-		RX CH-4N		
U900	BH50	FC28_RD3P	P116_RD+		RX CH-4P		
U900	BN52	FC28_TD0N	P115_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	BP52	FC28_TD0P	P115_TD+		TX CH-3P		
U900	BL51	FC28_TD1N	P116_TD-		TX CH-4N		
U900	BM51	FC28_TD1P	P116_TD+		TX CH-4P		
U900	BN50	FC28_TD2N	P113_TD-		TX CH-1N		
U900	BP50	FC28_TD2P	P113_TD+		TX CH-1P		
U900	BL49	FC28_TD3N	P114_TD-		TX CH-2N		
U900	BM49	FC28_TD3P	P114_TD+		TX CH-2P		

U900	AW45	FC29_RD0N	P118_RD-	QSFP0	RX CH-2N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AW46	FC29_RD0P	P118_RD+		RX CH-2P		
U900	AY48	FC29_RD1N	P117_RD-		RX CH-1N		
U900	AY49	FC29_RD1P	P117_RD+		RX CH-1P		
U900	BA45	FC29_RD2N	P120_RD-		RX CH-4N		
U900	BA46	FC29_RD2P	P120_RD+		RX CH-4P		
U900	BB48	FC29_RD3N	P119_RD-		RX CH-3N		
U900	BB49	FC29_RD3P	P119_RD+		RX CH-3P		
U900	BB54	FC29_TD0N	P117_TD-		TX CH-1N		
U900	BB53	FC29_TD0P	P117_TD+		TX CH-1P		
U900	BA52	FC29_TD1N	P118_TD-		TX CH-2N		
U900	BA51	FC29_TD1P	P118_TD+		TX CH-2P		
U900	AY54	FC29_TD2N	P119_TD-		TX CH-3N		
U900	AY53	FC29_TD2P	P119_TD+		TX CH-3P		
U900	AW52	FC29_TD3N	P120_TD-		TX CH-4N		
U900	AW51	FC29_TD3P	P120_TD+		TX CH-4P		
U900	AR45	FC30_RD0N	P121_RD-	QSFP3	RX CH-1N		
U900	AR46	FC30_RD0P	P121_RD+		RX CH-1P		
U900	AT48	FC30_RD1N	P122_RD-		RX CH-2N		
U900	AT49	FC30_RD1P	P122_RD+		RX CH-2P		
U900	AU45	FC30_RD2N	P123_RD-		RX CH-3N		
U900	AU46	FC30_RD2P	P123_RD+		RX CH-3P		
U900	AV48	FC30_RD3N	P124_RD-		RX CH-4N		
U900	AV49	FC30_RD3P	P124_RD+		RX CH-4P		
U900	AV54	FC30_TD0N	P121_TD-		TX CH-1N		
U900	AV53	FC30_TD0P	P121_TD+		TX CH-1P		
U900	AU52	FC30_TD1N	P122_TD-		TX CH-2N		
U900	AU51	FC30_TD1P	P122_TD+		TX CH-2P		
U900	AT54	FC30_TD2N	P123_TD-		TX CH-3N		
U900	AT53	FC30_TD2P	P123_TD+		TX CH-3P		
U900	AR52	FC30_TD3N	P124_TD-		TX CH-4N		
U900	AR51	FC30_TD3P	P124_TD+		TX CH-4P		
U900	AN45	FC31_RD0N	P127_RD-	QSFP2	RX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AN46	FC31_RD0P	P127_RD+		RX CH-3P		
U900	AM48	FC31_RD1N	P128_RD-		RX CH-4N		
U900	AM49	FC31_RD1P	P128_RD+		RX CH-4P		
U900	AL45	FC31_RD2N	P125_RD-		RX CH-1N		
U900	AL46	FC31_RD2P	P125_RD+		RX CH-1P		

U900	AK48	FC31_RD3N	P126_RD-		RX CH-2N		
U900	AK49	FC31_RD3P	P126_RD+		RX CH-2P		
U900	AK54	FC31_TD0N	P127_TD-		TX CH-3N	QSFP CHANNELS SWAPPED WITH IN THE QUAD	
U900	AK53	FC31_TD0P	P127_TD+		TX CH-3P		
U900	AL52	FC31_TD1N	P128_TD-		TX CH-4N		
U900	AL51	FC31_TD1P	P128_TD+		TX CH-4P		
U900	AM54	FC31_TD2N	P125_TD-		TX CH-1N		
U900	AM53	FC31_TD2P	P125_TD+		TX CH-1P		
U900	AN52	FC31_TD3N	P126_TD-		TX CH-2N		
U900	AN51	FC31_TD3P	P126_TD+		TX CH-2P		

Table 10: wedge-100 tomahawk port mapping

7.2. PCIe Bus

COM-e CPU module has four PCIe lanes, lane3 is used by COM-e CPU module for Ethernet, lane[0:1] is used for Tomahawk switch ASIC PCIe interface:

- PCIe Bus 0: Lane[0:1]
- PCIe Bus 1: Lane[2], unused
- PCIe Bus 2: Lane[3], used by Ethernet interface of COM-e CPU module

PCIe clock input of tomahawk is driven by the PCIe clock from micro-server.

7.3. USB bus

COM-e CPU is the USB master, USB hub USB2513 is used to connect CPU to three USB slave devices:

- Front port Type-A USB port
- BCM USB slave interface
- CP2112 US-I2C bridge

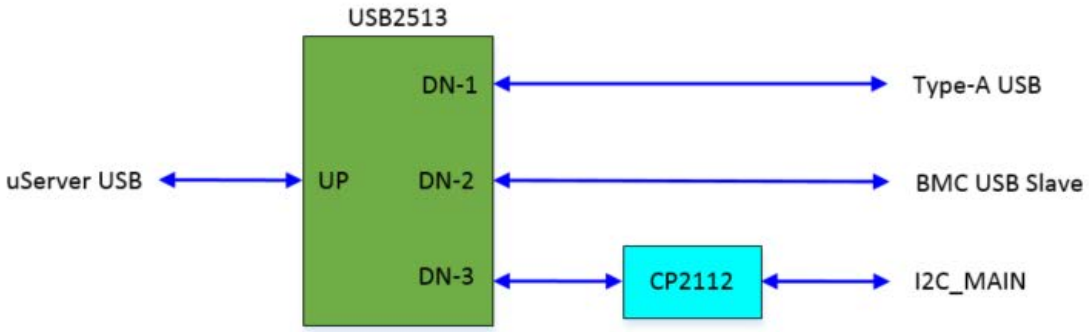

Figure 19: wedge-100 USB connection

7.4. UART Connection

The following UART interfaces are provided:

- Front panel console interface, RJ45 connector
- Rackmon RS485 UART port, rear facebook rackmon RJ45 connector
- Debug UART port in Facebook proprietary 14-pin debug interface
- On-board debug UART(if needed)

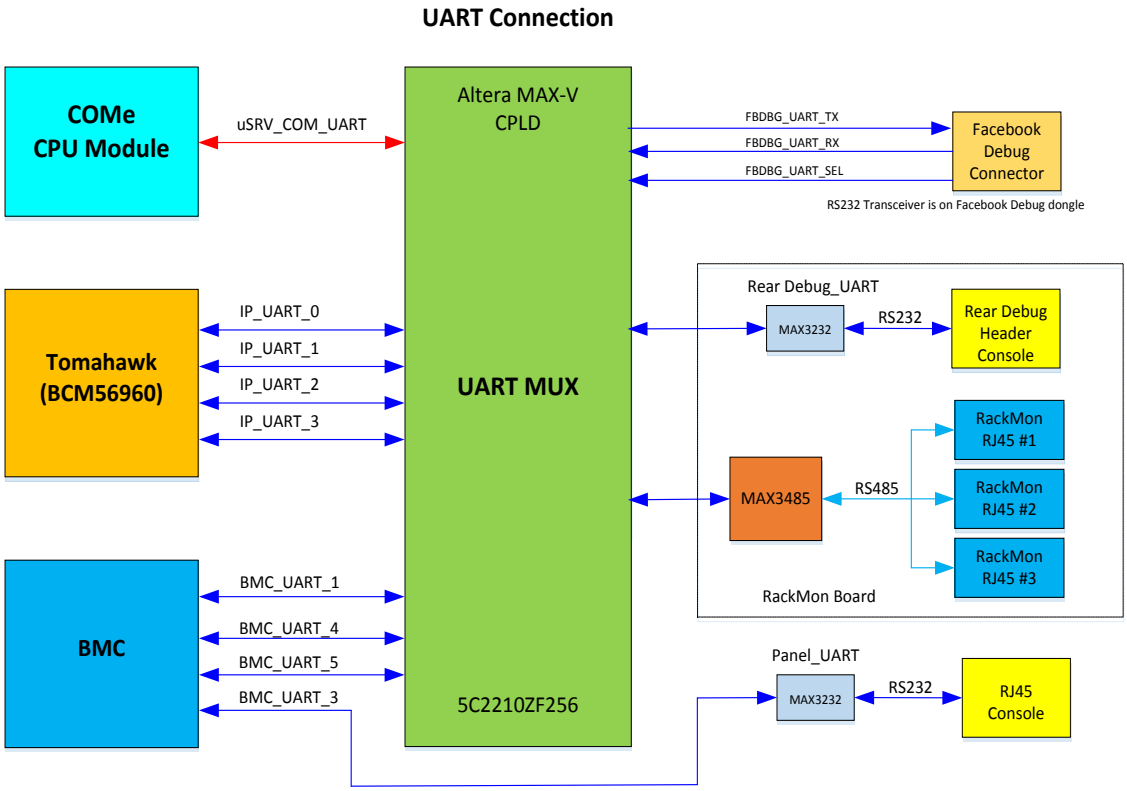

Figure 20: wedge-100 UART Connection

7.5. OOB Ethernet Connection

Wedge-100 uses one 5-port SGMII switch as out-of-band control interface. The following 45 ports are used in wedge-100:

- BMC Ethernet interface via BCM54616 PHY
- BMC RGMII to BCM5387 RGMII direct connection (wired but not used)
- COM-e Ethernet interface via BCM54616 PHY
- Tomahawk Eagle Core 10G port used as SGMII port(wired and reserved for future)
- Front panel port via BCM54616 PHY

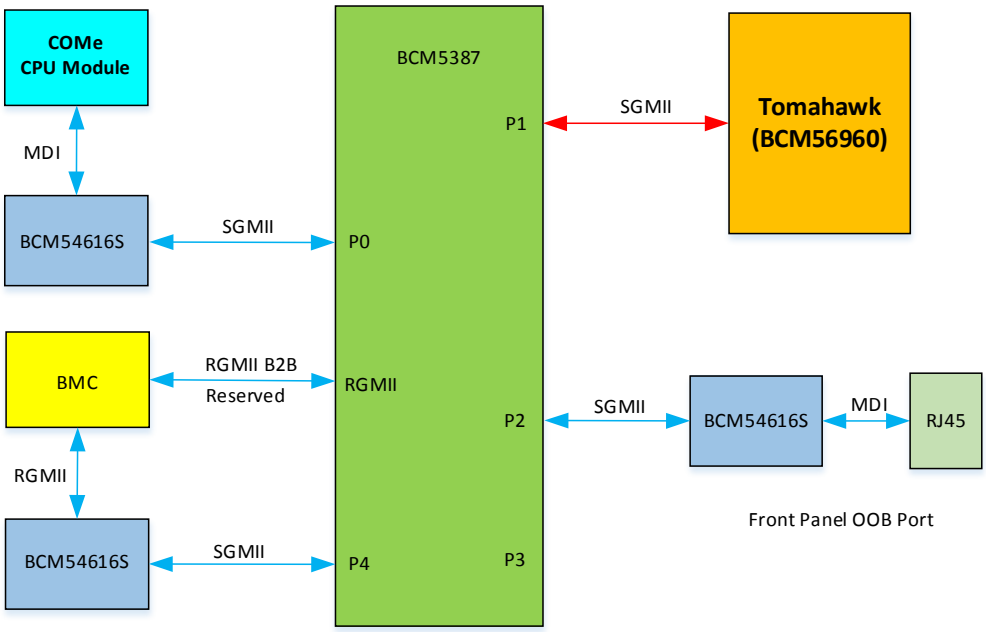

Figure 21: wedge-100 OOB ethernet diagram

7.6. I2C Bus

There are multiple I2C buses on wedge-100. The following diagram show the complete i2c design architecture of BMC.

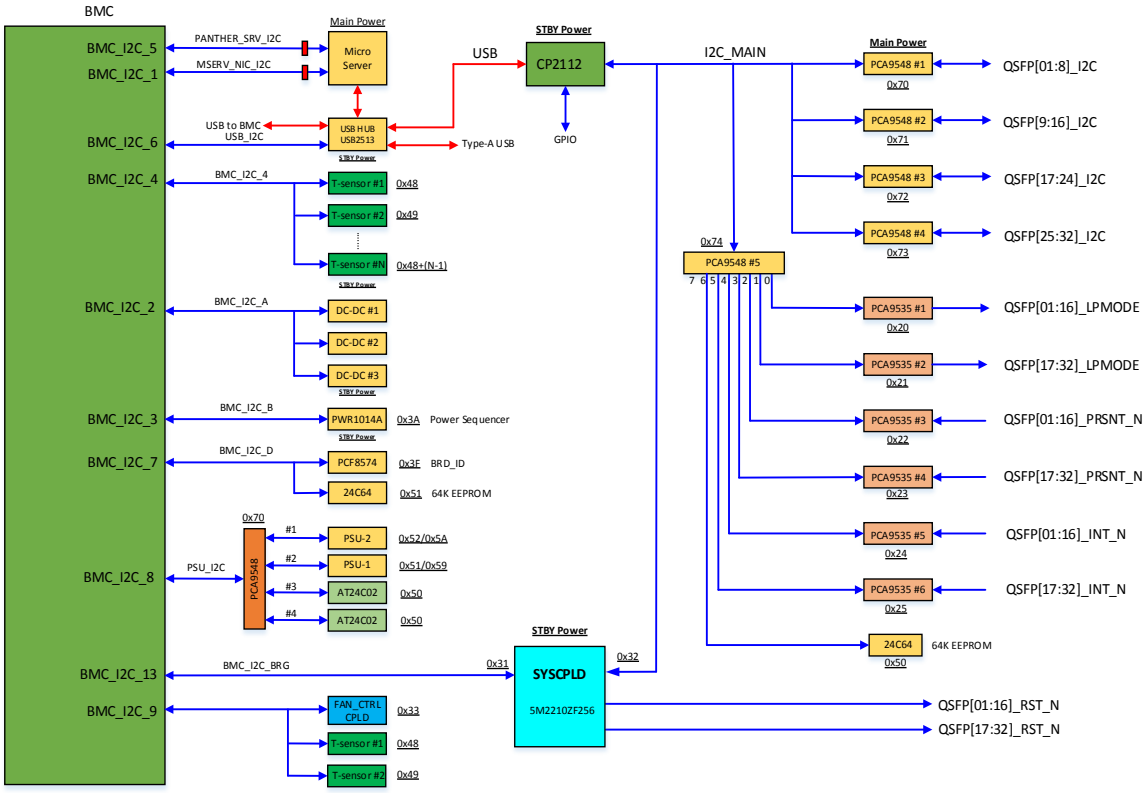

Figure 22: wedge-100 I2C Diagram

7.6.1. I2C Address

The following table shows the I2C devices of BMC:

BMC I2C Space							
BMC I2C	I2C MUX (PCA9548)	I2C Mux Addr	Sub Channel	Dev #	Sub-Device	I2C Addr	Note
BMC_I2C_1	N/A	N/A	Direct	#1	COM-e NIC I2C		COM-e NIC I2C
BMC_I2C_2	N/A	N/A	Direct	#1	DC-DC #1	0x10	IR3581, 160A 1.0V ROV
	N/A	N/A	Direct	#2	DC-DC #2	0x12	IR3584. 50A 1.0V_ANALOG
	N/A	N/A	Direct	#3	DC-DC #3	0x14	IR3584, 50A 3.3V
BMC_I2C_3	N/A	N/A	Direct	#1	PWR1014A	0x3A	Power sequencer and monitor
BMC_I2C_4	N/A	N/A	Direct	#1	TMP75 #1	0x48	Temperature sensor #1
	N/A	N/A	Direct	#2	TMP75 #2	0x49	Temperature sensor #2
	N/A	N/A	Direct	#3	TMP75 #3	0x4A	Temperature sensor #3
	N/A	N/A	Direct	#4	TMP75 #4	0x4B	Temperature sensor #4
	N/A	N/A	Direct	#5	TMP75 #5	0x4C	Temperature sensor #5
BMC_I2C_5	N/A	N/A	Direct	#1	COM-e		
	N/A	N/A	Direct	#2			
BMC_I2C_6	N/A	N/A	Direct	#1	USB Hub	0x2C	SM bus of USB hub
BMC_I2C_7	N/A	N/A	Direct	#1	PCF8574	0x3F	I2C bus to USB hub
	N/A	N/A	Direct	#2	24C64 EEPROM	0x50	I2C bus to USB hub
BMC_I2C_8	PCA9548 (U5704)	0x70	CH0:	#1	PSU #2 MCU	0x5A	PSU2 I2C address for PSU MCU
				#2	PSU #2 EEPROM	0x52	PSU2 I2C address for PSU EEPROM
			CH1:	#1	PSU #1 MCU	0x59	PSU1 I2C address for PSU MCU
				#2	PSU #1 EEPROM	0x51	PSU1 I2C address for PSU EEPROM
			CH2:	#1	BMC_PHY EEPROM	0x50	on-board BMC PHY EEPROM U55 AT24C02
			CH3:	#1	FP_PHY EEPROM	0x50	front port BMC PHY EEPROM U103 AT24C02
			CH[4:7]:				unused

BMC_I2C_9	N/A	N/A	Direct	#1	FAN_RACKMON CPLD	0x33	I2C bus to fan_rmon card CPLD
	N/A	N/A	Direct	#2	TMP75 #1	0x48	temperature sensor #1 on fan_rmon card
	N/A	N/A	Direct	#3	TMP75 #2	0x49	temperature sensor #2 on fan_rmon card
BMC_I2C_13	N/A	N/A	Direct	#1	SYSCPLD	0x31	SYSCPLD I2C access interface SYSCPLD can also be accessed by Panther+ from MAIN_I2C bus, the I2C address is 0x32

Table 11: BMC I2C Space

The following table shows the I2C devices and their i2c address of CP2112 main I2C bus which can be accessed by Com-e CPU module:

CP2112 Main I2C space					
Device	I2C Addr	Note	Sub-Device	I2C Addr	Note
PCA9548 #1	0x70	CH0:	QSFP28 Port #1	0x50	QSFP28_PORT_1 I2C space
		CH1:	QSFP28 Port #0	0x50	QSFP28_PORT_0 I2C space
		CH2:	QSFP28 Port #3	0x50	QSFP28_PORT_3 I2C space
		CH3:	QSFP28 Port #2	0x50	QSFP28_PORT_2 I2C space
		CH4:	QSFP28 Port #5	0x50	QSFP28_PORT_5 I2C space
		CH5:	QSFP28 Port #4	0x50	QSFP28_PORT_4 I2C space
		CH6:	QSFP28 Port #7	0x50	QSFP28_PORT_7 I2C space
		CH7:	QSFP28 Port #6	0x50	QSFP28_PORT_6 I2C space
PCA9548 #2	0x71	CH0:	QSFP28 Port #9	0x50	QSFP28_PORT_9 I2C space
		CH1:	QSFP28 Port #8	0x50	QSFP28_PORT_8 I2C space
		CH2:	QSFP28 Port #11	0x50	QSFP28_PORT_11 I2C space
		CH3:	QSFP28 Port #10	0x50	QSFP28_PORT_10 I2C space
		CH4:	QSFP28 Port #13	0x50	QSFP28_PORT_13 I2C space
		CH5:	QSFP28 Port #12	0x50	QSFP28_PORT_12 I2C space
		CH6:	QSFP28 Port #15	0x50	QSFP28_PORT_15 I2C space
		CH7:	QSFP28 Port #14	0x50	QSFP28_PORT_14 I2C space
PCA9548 #3	0x72	CH0:	QSFP28 Port #17	0x50	QSFP28_PORT_17 I2C space
		CH1:	QSFP28 Port #16	0x50	QSFP28_PORT_16 I2C space
		CH2:	QSFP28 Port #19	0x50	QSFP28_PORT_19 I2C space
		CH3:	QSFP28 Port #18	0x50	QSFP28_PORT_18 I2C space
		CH4:	QSFP28 Port #21	0x50	QSFP28_PORT_21 I2C space
		CH5:	QSFP28 Port #20	0x50	QSFP28_PORT_20 I2C space
		CH6:	QSFP28 Port #23	0x50	QSFP28_PORT_23 I2C space
		CH7:	QSFP28 Port #22	0x50	QSFP28_PORT_22 I2C space
PCA9548 #4	0x73	CH0:	QSFP28 Port #25	0x50	QSFP28_PORT_25 I2C space
		CH1:	QSFP28 Port #24	0x50	QSFP28_PORT_24 I2C space
		CH2:	QSFP28 Port #27	0x50	QSFP28_PORT_27 I2C space

		CH3:	QSFP28 Port #26	0x50	QSFP28_PORT_26 I2C space
		CH4:	QSFP28 Port #29	0x50	QSFP28_PORT_29 I2C space
		CH5:	QSFP28 Port #28	0x50	QSFP28_PORT_28 I2C space
		CH6:	QSFP28 Port #31	0x50	QSFP28_PORT_31 I2C space
		CH7:	QSFP28 Port #30	0x50	QSFP28_PORT_30 I2C space
PCA9548 #5	0x74	CH0:	PCA9535 #1	0x20	QSFP28_LPMODE[0:15]
		CH1:	PCA9535 #2	0x21	QSFP28_LPMODE[16:31]
		CH2:	PCA9535 #3	0x22	QSFP28_PRSNT_N[0:15]
		CH3	PCA9535 #4	0x23	QSFP28_PRSNT_N[16:31]
		CH4:	PCA9535 #5	0x24	QSFP28_INT_N[0:15]
		CH5:	PCA9535 #6	0x25	QSFP28_INT_N[16:31]
		CH6:	PCA9535 #7	0x50	24C64 EEPROM
		CH7	unused		
SYSCPLD	0x32				SYSTEM CPLD I2C address is 0x32 in MAIN_I2C space

Table 12: Micro-server Main I2C Space

DEVICE	ADDR	I2C SIGNAL	IO	SIGNAL	QSFP PORT	SIGNAL NAME	CONNECTOR
U5701	0X20	P0EXP_SCL/SDA	IO0_0	LPMODE	QSFP1	LPMODE_PORT28	CONNECTOR 0 (J3300)
			IO0_1	LPMODE	QSFP0	LPMODE_PORT29	
			IO0_2	LPMODE	QSFP3	LPMODE_PORT30	
			IO0_3	LPMODE	QSFP2	LPMODE_PORT31	
			IO0_4	LPMODE	QSFP5	LPMODE_PORT0	CONNECTOR 1 (J2600)
			IO0_5	LPMODE	QSFP4	LPMODE_PORT1	
			IO0_6	LPMODE	QSFP7	LPMODE_PORT2	
			IO0_7	LPMODE	QSFP6	LPMODE_PORT3	
			IO1_0	LPMODE	QSFP9	LPMODE_PORT4	CONNECTOR 2 (J2700)
			IO1_1	LPMODE	QSFP8	LPMODE_PORT5	
			IO1_2	LPMODE	QSFP11	LPMODE_PORT6	
			IO1_3	LPMODE	QSFP10	LPMODE_PORT7	
			IO1_4	LPMODE	QSFP13	LPMODE_PORT8	CONNECTOR 3 (J2800)
			IO1_5	LPMODE	QSFP12	LPMODE_PORT9	
			IO1_6	LPMODE	QSFP15	LPMODE_PORT10	
			IO1_7	LPMODE	QSFP14	LPMODE_PORT11	

U5702	0X21	P1EXP_SCL/SDA	IO0_0	LPMODE	QSFP17	LPMODE_PORT12	CONNECTOR 4 (J2900)
			IO0_1	LPMODE	QSFP16	LPMODE_PORT13	
			IO0_2	LPMODE	QSFP19	LPMODE_PORT14	
			IO0_3	LPMODE	QSFP18	LPMODE_PORT15	
			IO0_4	LPMODE	QSFP21	LPMODE_PORT16	CONNECTOR 5 (J3000)
			IO0_5	LPMODE	QSFP20	LPMODE_PORT17	
			IO0_6	LPMODE	QSFP23	LPMODE_PORT18	
			IO0_7	LPMODE	QSFP22	LPMODE_PORT19	
			IO1_0	LPMODE	QSFP25	LPMODE_PORT20	CONNECTOR 6 (J3100)
			IO1_1	LPMODE	QSFP24	LPMODE_PORT21	
			IO1_2	LPMODE	QSFP27	LPMODE_PORT22	
			IO1_3	LPMODE	QSFP26	LPMODE_PORT23	
			IO1_4	LPMODE	QSFP29	LPMODE_PORT24	CONNECTOR 7(J3200)
			IO1_5	LPMODE	QSFP28	LPMODE_PORT25	
			IO1_6	LPMODE	QSFP31	LPMODE_PORT26	
			IO1_7	LPMODE	QSFP30	LPMODE_PORT27	
U5801	0X22	P2EXP_SCL/SDA	IO0_0	PRSNT	QSFP1	PRSNT_PORT28	CONNECTOR 0 (J3300)
			IO0_1	PRSNT	QSFP0	PRSNT_PORT29	
			IO0_2	PRSNT	QSFP3	PRSNT_PORT30	
			IO0_3	PRSNT	QSFP2	PRSNT_PORT31	
			IO0_4	PRSNT	QSFP5	PRSNT_PORT0	CONNECTOR 1 (J2600)
			IO0_5	PRSNT	QSFP4	PRSNT_PORT1	
			IO0_6	PRSNT	QSFP7	PRSNT_PORT2	
			IO0_7	PRSNT	QSFP6	PRSNT_PORT3	
			IO1_0	PRSNT	QSFP9	PRSNT_PORT4	CONNECTOR 2 (J2700)
			IO1_1	PRSNT	QSFP8	PRSNT_PORT5	
			IO1_2	PRSNT	QSFP11	PRSNT_PORT6	
			IO1_3	PRSNT	QSFP10	PRSNT_PORT7	
			IO1_4	PRSNT	QSFP13	PRSNT_PORT8	CONNECTOR 3 (J2800)
			IO1_5	PRSNT	QSFP12	PRSNT_PORT9	

			IO1_6	PRSNT	QSFP15	PRSNT_PORT10	
			IO1_7	PRSNT	QSFP14	PRSNT_PORT11	
U5802	0X23	P3EXP_SCL/SDA	IO0_0	PRSNT	QSFP17	PRSNT_PORT12	CONNECTOR 4 (J2900)
			IO0_1	PRSNT	QSFP16	PRSNT_PORT13	
			IO0_2	PRSNT	QSFP19	PRSNT_PORT14	
			IO0_3	PRSNT	QSFP18	PRSNT_PORT15	
			IO0_4	PRSNT	QSFP21	PRSNT_PORT16	CONNECTOR 5 (J3000)
			IO0_5	PRSNT	QSFP20	PRSNT_PORT17	
			IO0_6	PRSNT	QSFP23	PRSNT_PORT18	
			IO0_7	PRSNT	QSFP22	PRSNT_PORT19	
			IO1_0	PRSNT	QSFP25	PRSNT_PORT20	CONNECTOR 6 (J3100)
			IO1_1	PRSNT	QSFP24	PRSNT_PORT21	
			IO1_2	PRSNT	QSFP27	PRSNT_PORT22	
			IO1_3	PRSNT	QSFP26	PRSNT_PORT23	
			IO1_4	PRSNT	QSFP29	PRSNT_PORT24	CONNECTOR 7(J3200)
			IO1_5	PRSNT	QSFP28	PRSNT_PORT25	
			IO1_6	PRSNT	QSFP31	PRSNT_PORT26	
			IO1_7	PRSNT	QSFP30	PRSNT_PORT27	
U5803	0X24	P4EXP_SCL/SDA	IO0_0	RXLOSS	QSFP1	RXLOSS_PORT28	CONNECTOR 0 (J3300)
			IO0_1	RXLOSS	QSFP0	RXLOSS_PORT29	
			IO0_2	RXLOSS	QSFP3	RXLOSS_PORT30	
			IO0_3	RXLOSS	QSFP2	RXLOSS_PORT31	
			IO0_4	RXLOSS	QSFP5	RXLOSS_PORT0	CONNECTOR 1 (J2600)
			IO0_5	RXLOSS	QSFP4	RXLOSS_PORT1	
			IO0_6	RXLOSS	QSFP7	RXLOSS_PORT2	
			IO0_7	RXLOSS	QSFP6	RXLOSS_PORT3	
			IO1_0	RXLOSS	QSFP9	RXLOSS_PORT4	CONNECTOR 2 (J2700)
			IO1_1	RXLOSS	QSFP8	RXLOSS_PORT5	
			IO1_2	RXLOSS	QSFP11	RXLOSS_PORT6	

			IO1_3	RXLOSS	QSFP10	RXLOSS_PORT7	
			IO1_4	RXLOSS	QSFP13	RXLOSS_PORT8	CONNECTOR 3 (J2800)
			IO1_5	RXLOSS	QSFP12	RXLOSS_PORT9	
			IO1_6	RXLOSS	QSFP15	RXLOSS_PORT10	
			IO1_7	RXLOSS	QSFP14	RXLOSS_PORT11	
U5804	0X25	P5EXP_SCL/SDA	IO0_0	RXLOSS	QSFP17	RXLOSS_PORT12	CONNECTOR 4 (J2900)
			IO0_1	RXLOSS	QSFP16	RXLOSS_PORT13	
			IO0_2	RXLOSS	QSFP19	RXLOSS_PORT14	
			IO0_3	RXLOSS	QSFP18	RXLOSS_PORT15	
			IO0_4	RXLOSS	QSFP21	RXLOSS_PORT16	CONNECTOR 5 (J3000)
			IO0_5	RXLOSS	QSFP20	RXLOSS_PORT17	
			IO0_6	RXLOSS	QSFP23	RXLOSS_PORT18	
			IO0_7	RXLOSS	QSFP22	RXLOSS_PORT19	
			IO1_0	RXLOSS	QSFP25	RXLOSS_PORT20	CONNECTOR 6 (J3100)
			IO1_1	RXLOSS	QSFP24	RXLOSS_PORT21	
			IO1_2	RXLOSS	QSFP27	RXLOSS_PORT22	
			IO1_3	RXLOSS	QSFP26	RXLOSS_PORT23	
			IO1_4	RXLOSS	QSFP29	RXLOSS_PORT24	CONNECTOR 7 (J3200)
			IO1_5	RXLOSS	QSFP28	RXLOSS_PORT25	
			IO1_6	RXLOSS	QSFP31	RXLOSS_PORT26	
			IO1_7	RXLOSS	QSFP30	RXLOSS_PORT27	

Table 13: QSFP28 Low speed signals

7.7. System CPLD

One non-volatile instant-on CPLD MAX-V 5M2210ZF256 is used in standby power domain for wedge-100 system control. It supports the following features:

- Control the reset signals for system and different chips and modules
- Support multiple UART multiplexer and de-multiplexer function for easy debug.
- Provide system status to BMC and micro-server via I2C interface. An I2C slave agent is implemented inside cpld.
- BMC can online upgrade CPLD via dedicated GPIO interface
- PSU control and status interface

SYSCPLD can be accessed from either BMC or COM-E CPU. Its I2C address is 0x31 if access from BMC, its I2C address is 0x32 if access from COM-E/CP2112.

7.7.1. Board Revision Register

Offset	Bit Fields	Default	R/W	Description
BOARD Revision Register				
0x00	D[3:0]	0000	R	BRD_REV[3:0]: PCB revision
	D[5:4]	00	R	MODEL_ID[1:0] 00: wedge100 01: 6-pack line card 10: 6-pack fabric card 11: reserved
	D[7:6]	00	R	reserved

7.7.2. CPLD Revision Register

Offset	Bit Fields	Default	R/W	Description
CPLD Revision Register				
0x01	D[5:0]	010000	R	CPLD Revision[5:0]
	D[6]	0	R	Released Bit 0= not released, 1= Released version after PVT
	D[7]	0	R	Reserved

7.7.3. CPLD sub-version Register

Offset	Bit Fields	Default	R/W	Description
CPLD Sub-version Register				
0x02	D[7:0]	0x01	R	CPLD sub-version, used for HW debug only

7.7.4. Slot ID register

Offset	Bit Fields	Default	R/W	Description
Slot ID register (Reserved for 6-pack100)				
0x03	D[4:0]	10000	R	***Reserved*** for Chassis slot information 00000: line card slot-1 00001: line card slot-2 00010: line card slot-3 00011: line card slot-4 00100: line card slot-5 00101: line card slot-6 00110: line card slot-7 00111: line card slot-8 01000: fabric slot-1, block-0 01001: fabric slot-1, block-1 01010: fabric slot-1, block-0 01011: fabric slot-1, block-1 10000: TOR wedge100
	D[7:5]	000	X	Reserved

7.7.5. Module Present Register

Offset	Bit Fields	Default	R/W	Description
Module Present register				
0x08	D[0]	1	R	PSU-1 Present 0: present 1: not present
	D[1]	1	R	PSU-2 Present 0: present 1: not present
	D[2]	1	R	FAN_RACKMON Present 0: present 1: not present
	D[3]	1	R	MICRO_SRV Present 0: present 1: not present
	D[4]	1	R	Reserved
	D[7:5]	111	R	Reserved

7.7.6. ROV Status Register

Offset	Bit Fields	Default	R/W	Description
ROV status register				
0x0b	D[3:0]	1000	R	TH_ROV[3:0] ROV[3:0] Voltage

				4'b00001.2000 4'b00011.1750 4'b00101.1500 4'b00111.1250 4'b01001.1000 4'b01011.0750 4'b01101.0500 4'b01111.0250 4'b10001.0000 4'b10010.9750 4'b10100.9500 4'b10110.9250 4'b11000.9000 4'b11010.8750 4'b11100.8500 4'b11110.8250
	D[6:4]	000	R	VCORE_IDSEL[2:0] IR3581 VID setting Loop-1 VID0: 1.200V (reg 0x52 = 0x8F) Loop-1 VID1: 1.150V (reg 0x52 = 0x87) Loop-1 VID2: 1.100V (reg 0x52 = 0x7F) Loop-1 VID3: 1.050V (reg 0x52 = 0x77) Loop-1 VID4: 1.000V (reg 0x52 = 0x6F) Loop-1 VID5: 0.950V (reg 0x52 = 0x67) Loop-1 VID6: 0.900V (reg 0x52 = 0x5f) Loop-1 VID7: 0.850V (reg 0x52 = 0x57)
	D[7]	0	R	reserved

7.7.7. Reset Reason Register

Offset	Bit Fields	Default	R/W	Description
Reset Reason Register				
0x0D	D[7:0]	0x00	R	Reset reason register 0x00: default state (unknown) 0x01: power domain standby reset 0x02: power domain main reset 0x03: front panel push button reset 0x04: on board debug push button reset 0x05: facebook debug header reset 0x10: SW reg 0x31_bit4 hot reset 0x11: SW reg 0x31_bit5 warm reset 0x12: SW reg 0x31_bit6 cold reset 0x13: SW reg 0x31_bit7 power reset

				0x20: BMC request reset, BMC only 0x21: BMC request to reset tomahawk 0x22: BMC request to reset COM-e CPU module 0x23: BMC request to reset main power domain 0x24: BMC request to reset all board 0x25: BMC watchdog timer-1 reset 0x26: BMC watchdog timer-2 reset

7.7.8. Reset Reason Source Register 1

Offset	Bit Fields	Default	R/W	Description
RESET Reason Source Register 1				
0x0E	D[0]	0	R	Front Panel Push Button Reset Active 0: Reset not happened 1: Reset Active
	D[1]	0	R	On board debug Push Button Reset Active 0: Reset not happened 1: Reset Active
	D[2]	0	R	Facebook debug header Reset Active 0: Reset not happened 1: Reset Active
	D[3]	0	R	reserved
	D[4]	0	R	SW Hot Reset Active (register 0x31_bit4) 0: Reset not happened 1: Reset Active
	D[5]	0	R	SW Warm Reset Active (register 0x31_bit5) 0: Reset not happened 1: Reset Active
	D[6]	0	R	SW cold Reset Active (register 0x31_bit6) 0: Reset not happened 1: Reset Active
	D[7]	0	R	SW power Reset Active (register 0x31_bit7) 0: Reset not happened 1: Reset Active

7.7.1. Reset Reason Source Register 2

Offset	Bit Fields	Default	R/W	Description
RESET Reason Source Register 2				
0x0F	D[0]	0	R	BMC Request Reset Active 0: Reset not happened 1: Reset Active
	D[1]	0	R	BMC request Tomahawk Reset Active 0: Reset not happened 1: Reset Active

	D[2]	0	R	BMC request Micro-server Reset Active 0: Reset not happened 1: Reset Active
	D[3]	0	R	BMC request Main power domain Reset Active 0: Reset not happened 1: Reset Active
	D[4]	0	R	BMC request All Reset Active 0: Reset not happened 1: Reset Active
	D[5]	0	R	BMC WatchDog Timer-1 Reset Active 0: Reset not happened 1: Reset Active
	D[6]	0	R	BMC WatchDog Timer-2 Reset Active 0: Reset not happened 1: Reset Active
	D[7]	0	R	reserved

7.7.2. PSU Status Register

Offset	Bit Fields	Default	R/W	Description
PSU status register				
0x10	D[0]	1	R	PSU-1 Present 0: present 1: not present
	D[1]	1	R	PSU-1 Power Output OK 0: PSU 12V power output is bad 1: PSU 12V power output is OK
	D[2]	1	R	PSU-1 Power Input OK 0: PSU 12V power input is bad 1: PSU 12V power input is OK
	D[3]	1	R	PSU-1 Alarm 0: PSU-1 has Alarm 1: Normal
	D[4]	1	R	PSU-2 Present 0: present 1: not present
	D[5]	1	R	PSU-2 Power Output OK 0: PSU 12V power output is bad 1: PSU 12V power output is OK
	D[6]	1	R	PSU-2 Power Input OK 0: PSU 12V power input is bad 1: PSU 12V power input is OK
	D[7]	1	R	PSU-2 Alarm 0: PSU-1 has Alarm 1: Normal

7.7.3. On-board Power Status Register 1

Offset	Bit Fields	Default	R/W	Description
On Board Power Status register 1				
0x11	D[0]	1	R	PWR_STBY_OK 0: power not OK 1: Power is OK
	D[1]	0	R	reserved
	D[2]	0	R	reserved
	D[3]	0	R	reserved
	D[4]	0	R	reserved
	D[5]	0	R	reserved
	D[6]	0	R	reserved
	D[7]	0	R	reserved

7.7.1. On-board Power Status Register 2

Offset	Bit Fields	Default	R/W	Description
On Board Power Status register 2				
0x12	D[0]	1	R	VCORE_VRDY1 0: power not OK 1: Power is OK
	D[1]	1	R	VCORE_HOT 0: over temperature is negative 1: over temperature is active
	D[2]	1	R	VANLOG_VRDY1 0: power not OK 1: Power is OK
	D[3]	1	R	VANLOG_HOT 0: over temperature is negative 1: over temperature is active
	D[4]	1	R	V3V3_VRDY1 0: power not OK 1: Power is OK
	D[5]	1	R	V3V3_HOT 0: over temperature is negative 1: over temperature is active
	D[6]	0	R	reserved
	D[7]	0	R	reserved

7.7.2. PCA9535 Interrupt Status Register 1

Offset	Bit Fields	Default	R/W	Description
PCA9535 Interrupt status register 1				

0x13	D[0]	1	R	PCA9535_0_INT_N 0: PCA9535 U0 interrupt active 1: Normal
	D[1]	1	R	PCA9535_1_INT_N 0: PCA9535 U1 interrupt active 1: Normal
	D[2]	1	R	PCA9535_2_INT_N 0: PCA9535 U2 interrupt active 1: Normal
	D[3]	1	R	PCA9535_3_INT_N 0: PCA9535 U3 interrupt active 1: Normal
	D[4]	1	R	PCA9535_4_INT_N 0: PCA9535 U4 interrupt active 1: Normal
	D[5]	1	R	PCA9535_5_INT_N 0: PCA9535 U5 interrupt active 1: Normal
	D[6]	1	R	reserved
	D[7]	1	R	reserved

7.7.3. PCA9535 Interrupt Status Register 2

Offset	Bit Fields	Default	R/W	Description
PCA9535 Interrupt status register 2				
0x14	D[0]	1	R	PSU_INT_N 0: PSU interrupt active 1: Normal
	D[1]	1	R	PWR_INT_N 0: power interrupt active 1: Normal
	D[2]	1	R	IR_PWR_INT_N 0: IR power interrupt active 1: Normal
	D[3]	1	R	PCA9535_ALL_INT_N 0: PCA9535 interrupt active 1: Normal
	D[4]	0	R	TPM_SPI_INT_N 0: SPI TPM interrupt active 1: Normal
	D[5]	0	R	reserved
	D[6]	0	R	reserved
	D[7]	0	R	reserved

7.7.4. COM-E Status Register

Offset	Bit Fields	Default	R/W	Description
COM-E Status Register				
0x18	D[2:0]	1	R	B_COM_TYPE[2:0]: COM-E board type
	D[3]	1	R	COM_GBE0_LINK1000_N
	D[4]	0	R	COM_SUS_STAT_N
	D[5]	0	R	COM_SUS_S3_N
	D[6]	0	R	COM_SUS_S4_N
	D[7]	0	R	COM_SUS_S5_N

7.7.5. LED Button Status Register

Offset	Bit Fields	Default	R/W	Description
LED selection Button Status				
0x1B	D[0]	1	R	TOP_LED_ACTIVE_N 0: TOP LED active 1: Normal
	D[1]	1	R	BOT_LED_ACTIVE_N 0: BOTTOM LED active 1: Normal
	D[2]	1	R	reserved
	D[3]	1	R	reserved
	D[4]	0	R	reserved
	D[5]	0	R	reserved
	D[6]	0	R	reserved
	D[7]	0	R	reserved

7.7.6. Hardware Debug Status Register 1

Offset	Bit Fields	Default	R/W	Description
Hardware Debug status register 1				
0x1C	D[0]	1	R	PUSHBUTTON_RST_N Front panel push button status
	D[1]	1	R	CPLD_PUSH_BTN_RST_IN_N On board debug push button status
	D[2]	1	R	DEBUG_RST_BTN_N Debug reset button from FB debug header
	D[3]	1	R	CPLD_QSFP_LED_POSITION Push button for LED selection
	D[4]	0	R	DEBUG_PORT_UART_SEL_N Debug port UART selection from FB debug header
	D[5]	0	R	DEBUG_UART_SEL_0 Debug selection signal from BMC
	D[6]	0	R	reserved

	D[7]	0	R	MICROSERVER_PCIE_RST_N

7.7.1. CP2112 GPIO Status Register

Offset	Bit Fields	Default	R/W	Description
CP2112 bridge GPIO status register				
0x1F	D[0]	1	R	CP2112_GPIO_IN[0]
	D[1]	1	R	CP2112_GPIO_IN[1]
	D[2]	1	R	CP2112_GPIO_IN[2]
	D[3]	1	R	CP2112_GPIO_IN[3]
	D[4]	1	R	reserved
	D[5]	1	R	reserved
	D[6]	1	R	reserved
	D[7]	1	R	reserved

7.7.2. PSU Interrupt Block Register

Offset	Bit Fields	Default	R/W	Description
PSU Interrupt Block register				
0x20	D[0]	0	R/W	PSU-1 Present Interrupt block 0: pass 1: blocked
	D[1]	0	R/W	PSU-1 Power Output OK Interrupt block 0: pass 1: blocked
	D[2]	0	R/W	PSU-1 Power Input OK Interrupt block 0: pass 1: blocked
	D[3]	0	R/W	PSU-1 Alarm Interrupt block 0: pass 1: blocked
	D[4]	0	R/W	PSU-2 Present Interrupt block 0: pass 1: blocked
	D[5]	0	R/W	PSU-2 Power Output OK Interrupt block 0: pass 1: blocked
	D[6]	0	R/W	PSU-2 Power Input OK Interrupt block 0: pass 1: blocked
	D[7]	0	R/W	PSU-2 Alarm Interrupt block 0: pass 1: blocked

7.7.3. On-Board Power Status Interrupt Block Register 1

Offset	Bit Fields	Default	R/W	Description
On Board Power Status Interrupt Block register 1				
0x21	D[0]	0	R/W	PWR_STBY_OK Interrupt block 0: pass 1: blocked
	D[1]	0	R/W	reserved
	D[2]	0	R/W	reserved
	D[3]	0	R/W	reserved
	D[4]	0	R/W	reserved
	D[5]	0	R/W	reserved
	D[6]	0	R/W	reserved
	D[7]	0	R/W	reserved

7.7.4. On-Board Power Status Interrupt Block Register 2

Offset	Bit Fields	Default	R/W	Description
On Board Power status interrupt Block register 2				
0x22	D[0]	0	R/W	VCORE_VRDY1 Interrupt block 0: pass 1: blocked
	D[1]	0	R/W	VCORE_HOT Interrupt block 0: pass 1: blocked
	D[2]	0	R/W	VANLOG_VRDY1 Interrupt block 0: pass 1: blocked
	D[3]	0	R/W	VANLOG_HOT Interrupt block 0: pass 1: blocked
	D[4]	0	R/W	V3V3_VRDY1 Interrupt block 0: pass 1: blocked
	D[5]	0	R/W	V3V3_HOT Interrupt block 0: pass 1: blocked
	D[6]	0	R/W	reserved
	D[7]	0	R/W	reserved

7.7.5. PCA9535 Interrupt Block Register

Offset	Bit Fields	Default	R/W	Description
PCA9535 Interrupt Block register				
0x23	D[0]	0	R/W	PCA9535_0_INT_N Interrupt block

				0: pass 1: blocked
	D[1]	0	R/W	PCA9535_1_INT_N Interrupt block 0: pass 1: blocked
	D[2]	0	R/W	PCA9535_2_INT_N Interrupt block 0: pass 1: blocked
	D[3]	0	R/W	PCA9535_3_INT_N Interrupt block 0: pass 1: blocked
	D[4]	0	R/W	PCA9535_4_INT_N Interrupt block 0: pass 1: blocked
	D[5]	0	R/W	PCA9535_5_INT_N Interrupt block 0: pass 1: blocked
	D[6]	0	R/W	reserved
	D[7]	0	R/W	reserved

7.7.6. On-board Power Status Interrupt Block Register 3

Offset	Bit Fields	Default	R/W	Description
On Board Power Status Interrupt Block register 3				
0x24	D[0]	0	R/W	PM_SM_ALERT_N Interrupt block 0: pass 1: blocked
	D[1]	0	R/W	VCORE_SMB_N Interrupt block 0: pass 1: blocked
	D[2]	0	R/W	V3V3_SMB_N Interrupt block 0: pass 1: blocked
	D[3]	0	R/W	VANALOG_SMB_N Interrupt block 0: pass 1: blocked
	D[4]	0	R/W	TEMP_ALERT_N Interrupt block 0: pass 1: blocked
	D[5]	0	R/W	
	D[6]	0	R/W	
	D[7]	0	R/W	

7.7.7. Global Interrupt Block Register

Offset	Bit Fields	Default	R/W	Description
Global Interrupt Block register				
0x25	D[0]	0	R/W	PSU_INT_N Interrupt block 0: pass 1: blocked
	D[1]	0	R/W	PWR_MB_INT_N Interrupt block 0: pass 1: blocked
	D[2]	0	R/W	PWR_IR_INT_N Interrupt block 0: pass 1: blocked
	D[3]	0	R/W	PCA9535_ALL_INT_N Interrupt block 0: pass 1: blocked
	D[4]	0	R/W	SMB_ALERT_INT_N Interrupt block 0: pass 1: blocked
	D[5]	0	R/W	TPM_SPI_INT_N interrupt block 0: pass 1: Blocked
	D[6]	0	R/W	BMC_CPLD_PWR_INT_BLK 0: pass 1: blocked
	D[7]	0	R/W	BMC_CPLD_QSFP_INT_BLK 0: pass 1: blocked

7.7.8. UART MUX Control Register

Offset	Bit Fields	Default	R/W	Description
UART MUX Control register				
0x26	D[1:0]	10	R/W	00: UART_SELECT_BMC 01: UART_SELECT_DBG 10: force to select 0 11: force to select 1 UART_SEL 1: UART port of panther+ connect to BMC UART-1, and FB Debug UART connect to BMC UART-5 0: UART port of panther+ connect to FB Debug UART,
	D[2]	0	R/W	reserved
	D[3]	0	R/W	reserved
	D[4]	0	R/W	reserved
	D[5]	0	R/W	reserved
	D[7:6]	00	R/W	REAR_DBG_UART selection 00: Tomahawk UART-0

				01: Tomahawk UART-2 10: Tomahawk UART-3 11: reserved

BMC_UART-3 connect to front panel console directly; BMC_UART-4 connect to rackmon RS485 directly. For UART-1 and 5, and panther console, they can be selected by UART_SELECT_BMC pin, BMC GPIO(pin D15(GPIOE0)), or by UART _SELECT_DBG pin from facebook debug header.

0: COM-e UART ⇔ FB_DEBUG dongle uart

1: COM-e UART ⇔ BMC_YART-1; FB_DEBUG dongle uart ⇔ BMC_UART-5

7.7.9. COM-E Control Register 1

Offset	Bit Fields	Default	R/W	Description
COM-E Control register 1				
0x28	D[0]	1	R/W	TPM_LPC_RST_N 0: reset LPC TPM 1: normal
	D[1]	1	R/W	TPM_SPI_RST_N 0: reset LPC TPM 1: normal
	D[2]	1	R/W	COM_PHY_RST_N 0: reset COM-E PHY 1: normal
	D[3]	1	R/W	LPC_RST_N 0: reset BMC LPC bus 1: normal
	D[4]	0	R/W	COM_NIC_ISOBUF_EN 0: disabled 1: enabled COM-e NIC I2C isolation Buffer
	D[5]	0	R/W	COM_PANTHER_ISOBUF_EN 0: disabled 1: enabled isolation buffer
	D[6]	0	R/W	COM_PWR_OK_EN 0: disable 1: enable
	D[7]	0	R/W	reserved

7.7.10. COM-e Control Register 2

Offset	Bit Fields	Default	R/W	Description
COM-E Control register 2				
0x29	D[0]	0	R/W	BMC_PHY_WP

				0: enabled write of BMC PHY 1: disable write of BMC PHY
	D[1]	0	R/W	FP_PHY_WP 0: enable write of front PHY EEPROM 1: disable write of front PHY EEPROM
	D[2]	0	R/W	COM_SPI_BOOT_WP_N 0: enable 1: disable
	D[3]	1	R/W	reserved
	D[4]	0	R/W	reserved
	D[5]	0	R/W	reserved
	D[6]	0	R/W	reserved
	D[7]	0	R/W	reserved

7.7.11. CP2112 GPIO Output Enable Register

Offset	Bit Fields	Default	R/W	Description
CP2112 bridge GPIO OE register				
0x2C	D[0]	1	R/W	CP2112_GPIO_OE[0]
	D[1]	1	R/W	CP2112_GPIO_OE[1]
	D[2]	1	R/W	CP2112_GPIO_OE[2]
	D[3]	1	R/W	CP2112_GPIO_OE[3]
	D[4]	1	R/W	reserved
	D[5]	1	R/W	reserved
	D[6]	1	R/W	reserved
	D[7]	1	R/W	reserved

7.7.12. CP2112 GPIO Output Register

Offset	Bit Fields	Default	R/W	Description
CP2112 bridge GPIO Output register				
0x2D	D[0]	1	R/W	CP2112_GPIO_OUT[0]
	D[1]	1	R/W	CP2112_GPIO_OUT[1]
	D[2]	1	R/W	CP2112_GPIO_OUT[2]
	D[3]	1	R/W	CP2112_GPIO_OUT[3]
	D[4]	1	R/W	reserved
	D[5]	1	R/W	reserved
	D[6]	1	R/W	reserved
	D[7]	1	R/W	reserved

7.7.13. System Debug Control Register 1

Offset	Bit Fields	Default	R/W	Description
System Debug Control register				
0x2E	D[3:0]	1000	R/W	ROV_TEST_VALUE[3:0]

	D[4]	1	R/W	VID_EN 0: force IR5381 VID_SEL to 100(1.0V) 1: Dynamic ROV VID control
	D[5]	0	R/W	ROV_TEST_EN 0: normal 1: use ROV_TEST_VALUE[3:0]
	D[6]	0	R/W	Reserved
	D[7]	1	R/W	HEART_ATTACK_EN 0: no fan tray fatal error attack 1: fan-tray fatal error attack mode enabled

Heart attack is a feature implemented by fan CPLD. It monitors the status of 5 fan-tray and decide if it is fatal scenario, then SYSCPLD will shut down the main power of main board. Current design enters fatal scenario if all 5 fan-trays are bad, or missing.

7.7.14. System Debug Control Register 2

Offset	Bit Fields	Default	R/W	Description
System Debug Control register				
0x2F	D[0]	1	R/W	DUAL_BOOT_EN 0: single boot 1: dual boot
	D[1]	0	R/W	EN_2ND_Flash_WP 0: writable 1: write protected
	D[2]	1	R/W	Force_2nd_WR 0: normal mode 1: always writable, debug mode
	D[3]	0	R/W	COM-E_PWR_BTN_BYPASS 0: normal, under BMC or button control 1: only under button control
	D[4]	0	R/W	ISO_FORCE_USRV Data to enable or disable isolation buffer for micro-server. 0: disable 1: buffer enabled
	D[5]	0	R/W	ISO_FORCE_BUF Data to enable or disable isolation buffer for ASIC 0: disabled 1: buffer enabled for micro-server
	D[6]	0	R/W	ISO_FORCE_MODE 0: BMC control 1: CPLD forced mode
	D[7]	0	R/W	Reserved for CPLD_IN3 of PWR1014A

This register is for hardware debug only, do not change it!

7.7.15. System Power Control Register

Offset	Bit Fields	Default	R/W	Description
System Power Control register				
0x30	D[0]	1	R/W	PWR_CYC_ALL_N 0: Write 0 to this bit will trigger PWR1014A to start power cycling of all power of wedge100 1: normal
	D[1]	1	R/W	PWR_MAIN_EN 0: Main power is OFF 1: Main Power is enabled
	D[2]	1	R/W	PWR_USRV_EN 0: COM-e cpu module power is OFF 1: COM-e cpu module power is ON
	D[3]	1	R/W	PWR_USRV_BTN_EN 0: COM-e cpu module power button is OFF 1: COM-e cpu module power button is ON
	D[4]	1	R/W	reserved
	D[5]	1	R/W	reserved
	D[6]	1	R/W	PWR_USRV_FORCE
	D[7]	1	R/W	PWR_MAIN_FORCE

7.7.16. System Reset Control Register

Offset	Bit Fields	Default	R/W	Description
System Reset Control Register 1				
0x31	D[0]	1	R/W	reserved
	D[1]	1	R/W	reserved
	D[2]	1	R/W	reserved
	D[3]	1	R/W	reserved
	D[4]	1	R/W	HOT_RST_REQ_N 0: write 0 to trigger hot reset 1: normal
	D[5]	1	R/W	WARM_RST_REQ_N 0: write 0 to trigger warm reset 1: normal
	D[6]	1	R/W	COLD_RST_REQ_N 0: write 0 to trigger cold reset 1: normal
	D[7]	1	R/W	PWR_RST_REQ_N 0: write 0 to trigger power reset 1: normal

7.7.17. System Reset Control Register 2

Offset	Bit Fields	Default	R/W	Description
System Reset Control register 2				
0x32	D[0]	1	R/W	COM-E_RST_N 0: write 0 to trigger COM-e micro-server reset 1: normal
	D[1]	1	R/W	TH_SYS_RST_N 0: write 0 to trigger tomahawk system reset 1: normal
	D[2]	1	R/W	TH_PCIE_RST_N 0: write 0 to trigger tomahawk PCIe reset 1: normal
	D[3]	1	R/W	reserved
	D[4]	1	R/W	reserved
	D[5]	1	R/W	reserved
	D[6]	1	R/W	reserved
	D[7]	1	R/W	reserved

7.7.18. Debug Control Register

Offset	Bit Fields	Default	R/W	Description
Misc Debug Control Register				
0x33	D[0]	0	R/W	DPLL_SEL (reserved)
	D[1]	1	R/W	COM-EXP_TEST_DISABLE 0: com-exp test card is enabled 1: com-exp test card is disabled
	D[2]	1	R/W	USRV_UART_ISO_EN 0: micro-server UART isolation buffer is disabled 1: micro-server UART isolation buffer is enabled
	D[3]	0	R/W	reserved
	D[4]	0	R/W	reserved
	D[5]	0	R/W	reserved
	D[6]	0	R/W	reserved
	D[7]	0	R/W	reserved

7.7.19. QSFP28 Reset Control Register 1

Offset	Bit Fields	Default	R/W	Description
QSFP28 Reset Control Register 1				
0x34	D[0]	1	R/W	QSFP_RESET_N[0] 0: reset QSFP 0 1: normal
	D[1]	1	R/W	QSFP_RESET_N[1] 0: reset QSFP 1

				1: normal
	D[2]	1	R/W	QSFP_RESET_N[2] 0: reset QSFP 2 1: normal
	D[3]	1	R/W	QSFP_RESET_N[3] 0: reset QSFP 3 1: normal
	D[4]	1	R/W	QSFP_RESET_N[4] 0: reset QSFP 4 1: normal
	D[5]	1	R/W	QSFP_RESET_N[5] 0: reset QSFP 5 1: normal
	D[6]	1	R/W	QSFP_RESET_N[6] 0: reset QSFP 6 1: normal
	D[7]	1	R/W	QSFP_RESET_N[7] 0: reset QSFP 7 1: normal

7.7.20. QSFP28 Reset Control Register 2

Offset	Bit Fields	Default	R/W	Description
QSFP28 Reset Control register 3				
0x35	D[0]	1	R/W	QSFP_RESET_N[8] 0: reset QSFP 8 1: normal
	D[1]	1	R/W	QSFP_RESET_N[9] 0: reset QSFP 9 1: normal
	D[2]	1	R/W	QSFP_RESET_N[10] 0: reset QSFP 10 1: normal
	D[3]	1	R/W	QSFP_RESET_N[11] 0: reset QSFP 11 1: normal
	D[4]	1	R/W	QSFP_RESET_N[12] 0: reset QSFP 12 1: normal
	D[5]	1	R/W	QSFP_RESET_N[13] 0: reset QSFP 13 1: normal
	D[6]	1	R/W	QSFP_RESET_N[14] 0: reset QSFP 14 1: normal
	D[7]	1	R/W	QSFP_RESET_N[15]

				0: reset QSFP 15 1: normal

7.7.21. QSFP28 Reset Control Register 3

Offset	Bit Fields	Default	R/W	Description
QSFP28 Reset Control register 3				
0x36	D[0]	1	R/W	QSFP_RESET_N[16] 0: reset QSFP 16 1: normal
	D[1]	1	R/W	QSFP_RESET_N[17] 0: reset QSFP 17 1: normal
	D[2]	1	R/W	QSFP_RESET_N[18] 0: reset QSFP 18 1: normal
	D[3]	1	R/W	QSFP_RESET_N[19] 0: reset QSFP 19 1: normal
	D[4]	1	R/W	QSFP_RESET_N[20] 0: reset QSFP 20 1: normal
	D[5]	1	R/W	QSFP_RESET_N[21] 0: reset QSFP 21 1: normal
	D[6]	1	R/W	QSFP_RESET_N[22] 0: reset QSFP 22 1: normal
	D[7]	1	R/W	QSFP_RESET_N[23] 0: reset QSFP 23 1: normal

7.7.22. QSFP28 Reset Control Register 4

Offset	Bit Fields	Default	R/W	Description
QSFP Reset Control register 4				
0x37	D[0]	1	R/W	QSFP_RESET_N[24] 0: reset QSFP 24 1: normal
	D[1]	1	R/W	QSFP_RESET_N[25] 0: reset QSFP 25 1: normal
	D[2]	1	R/W	QSFP_RESET_N[26] 0: reset QSFP 26

				1: normal
	D[3]	1	R/W	QSFP_RESET_N[27] 0: reset QSFP 27 1: normal
	D[4]	1	R/W	QSFP_RESET_N[28] 0: reset QSFP 28 1: normal
	D[5]	1	R/W	QSFP_RESET_N[29] 0: reset QSFP 29 1: normal
	D[6]	1	R/W	QSFP_RESET_N[30] 0: reset QSFP 30 1: normal
	D[7]	1	R/W	QSFP_RESET_N[31] 0: reset QSFP 31 1: normal

7.7.23. I2C_MUX Reset Control Register

Offset	Bit Fields	Default	R/W	Description
I2C MUX Reset Control register				
0x38	D[0]	1	R/W	I2C_MUX0_RST_N 0: reset I2C MUX 0 1: normal
	D[1]	1	R/W	I2C_MUX1_RST_N 0: reset I2C MUX 1 1: normal
	D[2]	1	R/W	I2C_MUX2_RST_N 0: reset I2C MUX 2 1: normal
	D[3]	1	R/W	I2C_MUX3_RST_N 0: reset I2C MUX 3 1: normal
	D[4]	1	R/W	I2C_MUX_PSU_RST_N 0: reset I2C MUX PSU 1: normal
	D[5]	1	R/W	I2C_MUX_LLI_RST_N 0: reset I2C MUX for PCA9535 LLI signals 1: normal
	D[6]	1	R/W	reserved
	D[7]	1	R/W	reserved

7.7.24. Device Reset Control Register

Offset	Bit Fields	Default	R/W	Description

Device Reset Control register				
0x39	D[0]	1	R/W	FAN_RACKMON_RST_N 0: reset FAN_RACKMON Card 1: normal
	D[1]	1	R/W	USB_BRG_RST_N 0: reset USB Bridge CP2112 1: normal
	D[2]	1	R/W	USB_HUB_RST_N 0: reset USB HUB 1: normal
	D[3]	1	R/W	BCM5387_RST_N 0: reset OOB Switch BCM5387 1: normal
	D[4]	1	R/W	FP_PHY_RST_N 0: reset front port PHY 1: normal
	D[5]	1	R/W	OB_PHY_RST_N 0: reset on-board PHY 1: normal
	D[6]	1	R/W	USB_SPI_BRG_RST_N(Reserved) 0: reset USB SPI bridge 1: normal
	D[7]	1	R/W	DPLL_RST_N(Reserved) 0: reset DPLL 1: normal

7.7.25. BMC Reset Enable Register

Offset	Bit Fields	Default	R/W	Description
BMC Reset Enable register				
0x3A	D[0]	0	R/W	BMC_MAIN_REQ_EN 0: BMC main reset request is disabled 1: BMC main reset request is enabled
	D[1]	0	R/W	BMC_RESET1_EN 0: BMC reset 1 request is disabled 1: BMC reset 1 request is enabled
	D[2]	0	R/W	BMC_RESET2_EN 0: BMC reset 2 request is disabled 1: BMC reset 2 request is enabled
	D[3]	0	R/W	BMC_RESET3_EN 0: BMC reset 3 request is disabled 1: BMC reset 3 request is enabled
	D[4]	0	R/W	BMC_RESET4_EN 0: BMC reset 4 request is disabled 1: BMC reset 4 request is enabled

	D[5]	0	R/W	BMC_WDT1_EN 0: BMC reset 4 request is disabled 1: BMC reset 4 request is enabled
	D[6]	0	R/W	BMC_WDT1_EN 0: BMC reset 4 request is disabled 1: BMC reset 4 request is enabled
	D[7]	1	R/W	reserved

7.7.26. General Reset Enable Register

Offset	Bit Fields	Default	R/W	Description
General Reset Enable Register				
0x3B	D[0]	1	R/W	PB_FRONT_EN 0: front panel push button reset request is disabled 1: front panel push button reset request is enabled
	D[1]	1	R/W	PB_ONBOARD_EN 0: on board push button reset request is disabled 1: On board push button reset request is enabled
	D[2]	1	R/W	FB_RST_EN 0: facebook push button reset request is disabled 1: facebook push button reset request is enabled
	D[3]	1	R/W	USRV_PCIE_RST_EN 0: userver PCIe reset will not reset tomahawk PCIe 1: userver PCIe reset will reset tomahawk PCIe
	D[4]	0	R/W	BMC_TH_PWR_EN 0: BMC cannot enable or disable tomahawk power 1: BMC can enable or disable tomahawk power
	D[5]	0	R/W	BMC_USRV_PWR_EN 0: BMC cannot enable or disable micro-server power 1: BMC can enable or disable micro-server power
	D[6]	0	R/W	reserved
	D[7]	1	R/W	reserved

7.7.27. Tomahawk LED Control Register

Offset	Bit Fields	Default	R/W	Description
Tomahawk LED Control register				
0x3C	D[0]	0	R/W	TH_LED_CLR 0: Tomahawk LED stream 0/1 normal 1: Tomahawk LED stream 0/1 reset clear
	D[1]	0	R/W	TH_LED_EN 0: Tomahawk LED stream 0/1 disabled 1: Tomahawk LED stream 0/1 enabled
	D[2]	0	R/W	FB_STREAM _EN 0: FB LED stream format disabled

				1: FB LED stream format enabled
	D[3]	0	R/W	WALK_TEST_EN 0: LED walk test disabled 1: LED walk test enabled
	D[5:4]	10	R/W	00: stream-0 single led check, led number and color is decided by register 0x3d, constant 01: stream-1 single led check, led number and color is decided by register 0x3d, constant 10: stream-0 all led check, led color is decided by register 0x3d, constant 11: stream-1 all led check, led color is decided by register 0x3d, constant
	D[6]	1	R/W	LED_TEST_BLINK_EN 0: normal constant 1: Blinking during LED test
	D[7]	1	R/W	LED_TEST_MODE_EN 0: normal 1: Port LED test mode enabled

7.7.28. Test LED Control Register

Offset	Bit Fields	Default	R/W	Description
TEST LED Control register				
0x3D	D[4:0]	00000	R/W	LED_TEST_NUM[4:0] Indicate one of 32 tri-color LED in one stream Each QSFP28 port has two tri-color LED, and 16 QSFP28 are in one LED stream.
	D[5]	1	R/W	LED_TEST_GREEN 0: green led is disabled in LED test mode 1: green led is enabled in LED test mode
	D[6]	1	R/W	LED_TEST_BLUE 0: blue led is disabled in LED test mode 1: blue led is enabled in LED test mode
	D[7]	1	R/W	LED_TEST_RED 0: red led is disabled in LED test mode 1: red led is enabled in LED test mode

7.7.29. System LED 1 Control Register

Offset	Bit Fields	Default	R/W	Description
SYSTEM LED 1 Control register				
0x3E	D[0]	00	R/W	LED_1_RED 0: LED 1 RED is OFF 1: LED 1 RED is ON

	D[1]	1	R/W	LED_1_GREEN 0: LED 1 GREEN is OFF 1: LED 1 GREEN is ON
	D[2]	1	R/W	LED_1_BLUE 0: LED 1 BLUE is OFF 1: LED 1 NLUE is ON
	D[3]	1	R/W	LED_1_BLINK_EN 0: LED 1 No blink 1: LED 1 Blink is ON
	D[4]	1	R/W	reserved
	D[5]	1	R/W	reserved
	D[6]	1	R/W	reserved
	D[7]	1	R/W	reserved

7.7.30. System LED 2 Control Register

Offset	Bit Fields	Default	R/W	Description
SYSTEM LED 2 Control register				
0x3F	D[0]	00	R/W	LED_2_RED 0: LED 2 RED is OFF 1: LED 2 RED is ON
	D[1]	1	R/W	LED_2_GREEN 0: LED 2 GREEN is OFF 1: LED 2 GREEN is ON
	D[2]	1	R/W	LED_2_BLUE 0: LED 2 BLUE is OFF 1: LED 2 NLUE is ON
	D[3]	1	R/W	LED_2_BLINK_EN 0: LED 2 No blink 1: LED 2 Blink is ON
	D[4]	1	R/W	reserved
	D[5]	1	R/W	reserved
	D[6]	1	R/W	reserved
	D[7]	1	R/W	reserved

7.7.31. LED Test Register 0

Offset	Bit Fields	Default	R/W	Description
LED Test register 0				
0x40	D[2:0]	0	RW	RGB_DATA_0_TOP[2:0]
	D[5:3]	0	RW	RGB_DATA_1_TOP[2:0]
	D[6]	0	RW	reserved
	D[7]	0	RW	TOP_LED_TEST_EN

7.7.32. LED Test Register 1

Offset	Bit Fields	Default	R/W	Description
LED Test register 1				
0x41	D[2:0]	0	RW	RGB_DATA_2_TOP[2:0]
	D[5:3]	0	RW	RGB_DATA_3_TOP[2:0]
	D[6]	0	RW	reserved
	D[7]	0	RW	reserved

7.7.33. LED Test Register 2

Offset	Bit Fields	Default	R/W	Description
LED Test register 2				
0x42	D[2:0]	0	RW	RGB_DATA_0_BOT[2:0]
	D[5:3]	0	RW	RGB_DATA_1_BOT[2:0]
	D[6]	0	RW	reserved
	D[7]	0	RW	BOT_LED_TEST_EN

7.7.34. LED Test Register 3

Offset	Bit Fields	Default	R/W	Description
LED Test register 3				
0x43	D[2:0]	0	RW	RGB_DATA_2_BOT[2:0]
	D[5:3]	0	RW	RGB_DATA_3_BOT[2:0]
	D[6]	0	RW	reserved
	D[7]	0	RW	reserved

7.7.35. Stream 0 LED Swap Register 0

Offset	Bit Fields	Default	R/W	Description
Stream 0 LED Swap Register 0				
0x44	D[7:0]	0	RW	ST0_LED_SWAP[7:0]

7.7.36. Stream 0 LED Swap Register 1

Offset	Bit Fields	Default	R/W	Description
Stream 0 LED Swap Register 1				
0x45	D[7:0]	0	RW	ST0_LED_SWAP[15:8]

7.7.37. Stream 1 LED Swap Register 0

Offset	Bit Fields	Default	R/W	Description
Stream 1 LED Swap Register 0				
0x46	D[7:0]	0	RW	ST1_LED_SWAP[7:0]

7.7.38. Stream 1 LED Swap Register 1

Offset	Bit Fields	Default	R/W	Description
Stream 1 LED Swap Register 1				
0x47	D[7:0]	0	RW	ST1_LED_SWAP[15:8]

7.7.39. FLIP BUTTON Register

Offset	Bit Fields	Default	R/W	Description
Flip LED Button Register				
0x48	D[0]	0	W	BUTTON_FLIP write 1 to this bit will flip the LED selection button
	D[7:1]	0	RW	Reserved

7.7.40. LED Stream Control Register

Offset	Bit Fields	Default	R/W	Description
LED Stream Control Register				
0x49	D[0]	0	W	SWAP_UP_DOWN 0: UP port led status output first 1: Down port LED status output first In wedge100, SW team choose to output down port status first.
	D[7:1]	0	RW	Reserved

7.8. Fan Control CPLD

Fan Control CPLD is on Fan card, it connects to BMC I2C bus 9, I2C address is 0x33. It supports the following functions:

- Fan FRU control and status reading
- RackMon GPIO control

7.8.1. Board Revision Register

Offset	Bit Fields	Default	R/W	Description
BOARD Revision Register				
0x00	D[3:0]	0000	R	BRD_REV[3:0]: PCB revision
	D[5:4]	00	R	MODEL_ID[1:0] 00: wedge100 01: 6-pack100 line card 10: 6-pack100 fabric card 11: reserved
	D[7:6]	00	R	reserved

7.8.2. CPLD Revision Register

Offset	Bit Fields	Default	R/W	Description
CPLD Revision Register				
0x01	D[5:0]	000000	R	CPLD Revision[5:0]
	D[6]	0	R	Released Bit 0= not released, 1= Released version after PVT
	D[7]	0	R	Reserved

7.8.3. CPLD Sub-revision

Offset	Bit Fields	Default	R/W	Description
CPLD Sub-version Register				
0x02	D[7:0]	0x02	R	CPLD sub-version register For HW debug only

7.8.4. GPIO Status Register

Offset	Bit Fields	Default	R/W	Description
GPIO Status Register				
0x04	D[0]	0	R	JAYBOX_GPIO1
	D[1]	0	R	JAYBOX_GPIO2

	D[2]	0	R	JAYBOX_GPIO3
	D[3]	0	R	JAYBOX_GPIO4
	D[4]	0	R	JAYBOX_GPIO5
	D[5]	0	R	JAYBOX_GPIO6
	D[6]	0	R	JAYBOX_GPIO7
	D[7]	0	R	JAYBOX_GPIO8

7.8.5. GPIO JayBox Status

Offset	Bit Fields	Default	R/W	Description
JAYBOX Status Register				
0x05	D[0]	0	R	JAYBOX_FEED1_CLOSED
	D[1]	0	R	JAYBOX_FEED2_CLOSED
	D[2]	0	R	Reserved
	D[3]	0	R	Reserved
	D[4]	0	R	Reserved
	D[5]	0	R	Reserved
	D[6]	0	R	Reserved
	D[7]	0	R	Reserved

7.8.6. Interrupt Status Register

Offset	Bit Fields	Default	R/W	Description
Interrupt Status Register				
0x07	D[0]	1	R	FanTray failure 0: fan tray has failure 1: all fan tray is good and alive
	D[1]	1	R	FanTray Present interrupt 0: Interrupt active 1: normal
	D[2]	1	R	TEMP_SENSOR1 0: temp sensor 1 interrupt active 1: normal
	D[3]	1	R	TEMP_SENSOR2 0: temp sensor 2 interrupt active 1: normal
	D[4]	1	R	Alarm_N 0: fan_rackmon board has alarm asserted to main board 1: normal
	D[7:5]	111	R	Reserved

7.8.7. Fan-tray Present Status Register

Offset	Bit Fields	Default	R/W	Description

FanTray Present Status register				
0x08	D[0]	1	R	FanTray-1 Present 0: present 1: not present
	D[1]	1	R	FanTray-2 Present 0: present 1: not present
	D[2]	1	R	FanTray-3 Present 0: present 1: not present
	D[3]	1	R	FanTray-4 Present 0: present 1: not present
	D[4]	1	R	FanTray-5 Present 0: present 1: not present
	D[7:5]	111	R	Reserved

7.8.8. Fan-tray Failure Status Register

Offset	Bit Fields	Default	R/W	Description
Fan tray failure status register				
0x09	D[0]	0	R	FanTray-1 failure 0: fan tray has failure 1: fan tray is good and alive
	D[1]	0	R	FanTray-2 failure 0: fan tray has failure 1: fan tray is good and alive
	D[2]	0	R	FanTray-3 failure 0: fan tray has failure 1: fan tray is good and alive
	D[3]	0	R	FanTray-4 failure 0: fan tray has failure 1: fan tray is good and alive
	D[4]	0	R	FanTray-5 failure 0: fan tray is good and alive 1: fan tray has failure
	D[7:5]	111	R	Reserved

7.8.9. Fan-tray 1 Front Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 1 Front Fan Speed				
0x10	D[7:0]	0x00	R	FanTray-1 front Fan Speed

7.8.10. Fan-tray 1 Rear Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 1 Rear Fan Speed				
0x11	D[7:0]	0x00	R	FanTray-1 rear Fan Speed

7.8.11. Fan-tray 2 Front Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 2 Front Fan Speed				
0x12	D[7:0]	0x00	R	FanTray-2 front Fan Speed

7.8.12. Fan-tray 2 Rear Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 2 Rear Fan Speed				
0x13	D[7:0]	0x00	R	FanTray-2 rear Fan Speed

7.8.13. Fan-tray 3 Front Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 3 Front Fan Speed				
0x14	D[7:0]	0x00	R	FanTray-3 front Fan Speed

7.8.14. Fan-tray 3 Rear Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 3 Rear Fan Speed				
0x15	D[7:0]	0x00	R	FanTray-3 rear Fan Speed

7.8.15. Fan-tray 4 Front Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 4 Front Fan Speed				
0x16	D[7:0]	0x00	R	FanTray-4 front Fan Speed

7.8.16. Fan-Tray 4 Rear Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 4 Rear Fan Speed				
0x17	D[7:0]	0x00	R	FanTray-4 rear Fan Speed

7.8.17. Fan-tray 5 Front Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 5 Front Fan Speed				
0x18	D[7:0]	0x00	R	FanTray-5 front Fan Speed

7.8.18. Fan-tray 5 Rear Fan Speed Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 5 Rear Fan Speed				
0x19	D[7:0]	0x00	R	FanTray-5 rearFan Speed

Front fan max speed is 16000RPM, rear fan max speed is 15400RPM. Period time is 200ms, CPLD count negative waveform and record it at 0x10~0x17

200ms/m = 1/2 * TS

TS = 60/N

N=60/TS= 60/0.4*m=150*m

SW must multiple 150 and show it as RPM(Revolutions per minute)

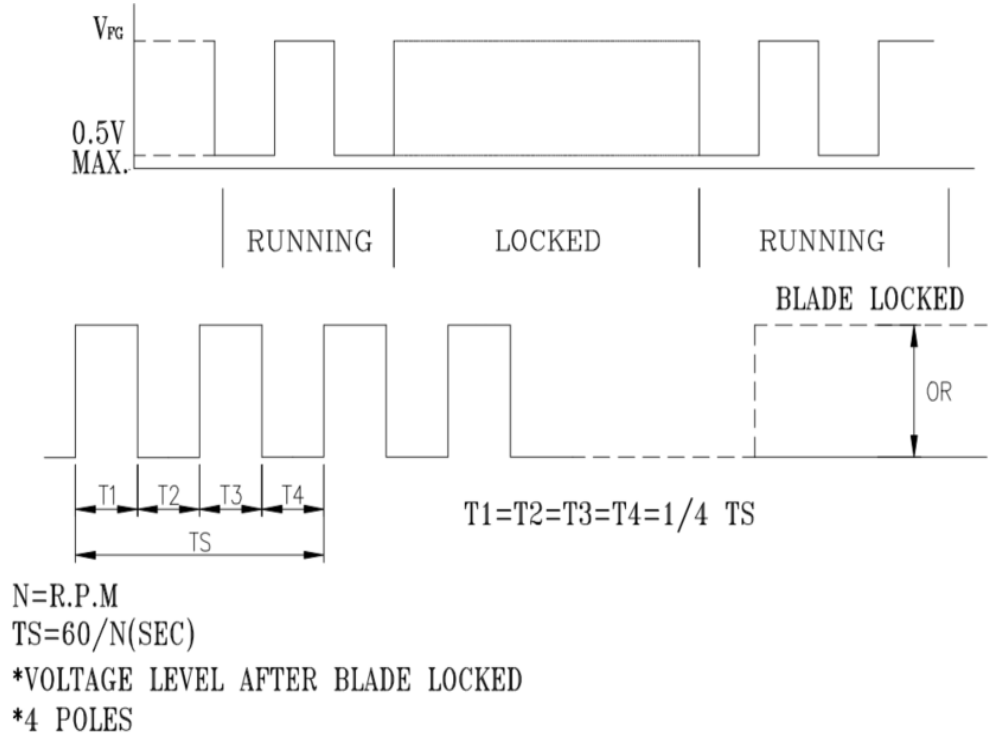

Figure 23: RPM reading of fan tray

7.8.19. Front Fan Alive Register

Offset	Bit Fields	Default	R/W	Description
Front Fan Alive register				
0x1A	D[4:0]	10000	R	FRONT_FAN_ALIVE_N[4:0] 0: alive 1: bad
	D[7:5]	000	R	reserved

7.8.20. Rear Fan Alive Register

Offset	Bit Fields	Default	R/W	Description
Rear Fan Alive register				
0x1B	D[4:0]	10000	R	REAR_FAN_ALIVE_N[4:0] 0: alive 1: bad
	D[7:5]	000	R	reserved

7.8.21. Fan-tray Alive Register

Offset	Bit Fields	Default	R/W	Description
FAN-TRAY Alive register				
0x1C	D[4:0]	10000	R	FANTRAY_ALIVE_N[4:0] 0: alive 1: bad
	D[7:5]	000	R	reserved

7.8.22. Fan-tray Present Register

Offset	Bit Fields	Default	R/W	Description
Fan Tray Present Register				
0x1D	D[4:0]	10000	R	FANTRAY_PRSNT_N[4:0] 0: present 1: not available
	D[7:5]	000	R	reserved

7.8.23. Fan-tray 1 PWM Control Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 1 PWM control Register				
0x20	D[4:0]	10000	R/W	FAN1_PWM[4:0] FanTray-1 PWM control signal
	D[7:5]	000	R	reserved

7.8.24. Fan-tray 2 PWM Control Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 2 PWM control Register				
0x21	D[4:0]	10000	R/W	FAN2_PWM[4:0] FanTray-2 PWM control signal
	D[7:5]	000	R	reserved

7.8.25. Fan-tray 3 PWM Control Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 3 PWM control Register				

0x22	D[4:0]	10000	R/W	FAN3_PWM[4:0] FanTray-3 PWM control signal
	D[7:5]	000	R	reserved

7.8.26. Fan-tray 4 PWM Control Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 4 PWM control Register				
0x23	D[4:0]	10000	R/W	FAN4_PWM[4:0] FanTray-4 PWM control signal
	D[7:5]	000	R	reserved

7.8.27. Fan-tray 5 PWM Control Register

Offset	Bit Fields	Default	R/W	Description
Fan tray 5 PWM control Register				
0x24	D[4:0]	10000	R/W	FAN5_PWM[4:0] FanTray-5 PWM control signal
	D[7:5]	000	R	reserved

FAN_PWM[4:0]	
0_0000	0/32 or 0% duty cycle
0_0001	1/32 or 3.125% duty cycle
0_0010	2/32 or 6.25% duty cycle
0_0011	3/32 or 9.375% duty cycle
0_0100	4/32 or 12.5% duty cycle
0_0101	5/32 or 16.625% duty cycle
0_0110	6/32 or 18.725% duty cycle
0_0111	7/32 or 21.875% duty cycle
0_1000	8/32 or 25% duty cycle
0_1001	9/32 or 28.125% duty cycle
0_1010	10/32 or 31.25% duty cycle
0_1011	11/32 or 34.375% duty cycle
0_1100	12/32 or 37.5% duty cycle
0_1101	13/32 or 41.625% duty cycle
0_1110	14/32 or 43.725% duty cycle
0_1111	15/32 or 46.875% duty cycle
1_0000	16/32 or 50% duty cycle
1_0001	17/32 or 53.125% duty cycle
1_0010	18/32 or 56.25% duty cycle
1_0011	19/32 or 59.375% duty cycle
1_0100	20/32 or 62.5% duty cycle
1_0101	21/32 or 66.625% duty cycle
1_0110	22/32 or 68.725% duty cycle

1_0111	23/32 or 71.875% duty cycle
1_1000	24/32 or 75% duty cycle
1_1001	25/32 or 78.125% duty cycle
1_1010	26/32 or 81.25% duty cycle
1_1011	27/32 or 84.375% duty cycle
1_1100	28/32 or 87.5% duty cycle
1_1101	29/32 or 91.625% duty cycle
1_1110	30/32 or 93.725% duty cycle
1_1111	32/32 or 100% duty cycle

Table 14: Fan PWM Control table

7.8.28. FAN-Tray 1/2 LED Control

Offset	Bit Fields	Default	R/W	Description
Fan tray 1 PWM control register				
0x25	D[1:0]	00	R/W	FAN1_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON 10: Red ON, Blue OFF 11: OFF If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF
	D[2]	0	R/W	FAN1_LED_BLINK 0: no blink 1: Blink LED 1
	D[3]	0	R/W	reserved
	D[5:4]	00	R/W	FAN2_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON 10: Red ON, Blue OFF 11: OFF If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF
	D[6]	0	R/W	FAN2_LED_BLINK 0: no blink 1: Blink LED 1
	D[7]	0	R/W	reserved

7.8.29. FAN-Tray 3/4 LED Control

Offset	Bit Fields	Default	R/W	Description

Fan tray 3/4 PWM control register				
0x26	D[1:0]	00	R/W	FAN3_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON 10: Red ON, Blue OFF 11: OFF If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF
	D[2]	0	R/W	FAN3_LED_BLINK 0: no blink 1: Blink LED 1
	D[3]	0	R/W	reserved
	D[5:4]	00	R/W	FAN4_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON 10: Red ON, Blue OFF 11: OFF If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF
	D[6]	0	R/W	FAN4_LED_BLINK 0: no blink 1: Blink LED 1
	D[7]	0	R/W	reserved

7.8.30. FAN-Tray 5LED Control

Offset	Bit Fields	Default	R/W	Description
Fan tray 5 PWM control register				
0x27	D[1:0]	00	R/W	FAN5_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON 10: Red ON, Blue OFF 11: OFF If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF
	D[2]	0	R/W	FAN5_LED_BLINK 0: no blink

				1: Blink LED 5
	D[3]	0	R/W	reserved
	D[5:4]	00	R/W	reserved
	D[6]	0	R/W	reserved
	D[7]	0	R/W	reserved

7.8.31. Interrupt Block Register

Offset	Bit Fields	Default	R/W	Description
Interrupt Block register				
0x28	D[0]	0	R/W	TEMP_SENSOR_1_BLK 0: normal 1: Block temperature sensor 1 interrupt
	D[1]	0	R/W	TEMP_SENSOR_2_BLK 0: normal 1: Block temperature sensor 2 interrupt
	D[3]	0	R/W	FAN_PRSNT_BLK 0: normal 1: Block fan present interrupt
	D[4]	00	R/W	FAN_FAILURE_BLK 0: normal 1: block fan failure interrupt
	D[7:5]	000	R/W	reserved

7.8.32. Debug Test Register 1

Offset	Bit Fields	Default	R/W	Description
Debug test register 1				
0x29	D[2:0]	0	R/W	TEST_SEL[2:0]
	D[3]	0	R/W	FRU_INT_TEST 0: normal 1: enable FRU Interrupt test
	D[7:4]	00000	R/W	reserved

7.8.33. GPIO Output Enable Register

Offset	Bit Fields	Default	R/W	Description
GPIO Output Enable Register				
0x2a	D[0]	0		JAYBOX_GPIO1 Output Enable 0: tri-state GPIO1 1: GPIO1 is output, reg_0x2b[0] is the output data

	D[1]	0		JAYBOX_GPIO2 Output Enable 0: tri-state GPIO2 1: GPIO1 is output, reg_0x2b[1] is the output data
	D[2]	0		JAYBOX_GPIO3 Output Enable 0: tri-state GPIO3 1: GPIO1 is output, reg_0x2b[2] is the output data
	D[3]	0		JAYBOX_GPIO4 Output Enable 0: tri-state GPIO4 1: GPIO1 is output, reg_0x2b[3] is the output data
	D[4]	0		JAYBOX_GPIO5 Output Enable 0: tri-state GPIO5 1: GPIO1 is output, reg_0x2b[4] is the output data
	D[5]	0		JAYBOX_GPIO6 Output Enable 0: tri-state GPIO6 1: GPIO1 is output, reg_0x2b[5] is the output data
	D[6]	0		JAYBOX_GPIO7 Output Enable 0: tri-state GPIO7 1: GPIO1 is output, reg_0x2b[6] is the output data
	D[7]	0		JAYBOX_GPIO8 Output Enable 0: tri-state GPIO8 1: GPIO1 is output, reg_0x2b[7] is the output data

7.8.34. GPIO Output Data Register

Offset	Bit Fields	Default	R/W	Description
GPIO Output Data Register				
0x2b	D[0]	0		JAYBOX_GPIO1 Output Data
	D[1]	0		JAYBOX_GPIO2 Output Data

	D[2]	0		JAYBOX_GPIO3 Output Data
	D[3]	0		JAYBOX_GPIO4 Output Data
	D[4]	0		JAYBOX_GPIO5 Output Data
	D[5]	0		JAYBOX_GPIO6 Output Data
	D[6]	0		JAYBOX_GPIO7 Output Data
	D[7]	0		JAYBOX_GPIO8 Output Data

7.9. Fan Card Heartbeat

FAN card will send heartbeat signal to main board SYSCPLD to indicate the healthy status of fan trays. If any fatal scenario happen, such as all 5 fan-tray fail, then heartbeat signal will notify main board SYSCPLD and main board need to take prevention method, such as shutdown the main power within certain time.

7.10. CPLD upgrade

Both SYSCPLD and FAN_RACKMON CPLD can be online upgraded by BMC. BMC use the following GPIO to emulate CPLD JTAG signals to upgrade CPLD.

BMC GPIO	Pin	IO	CPLD JTAG	Note
GPIOJ4	T4	Out	FANCARD_TMS	FAN_RACKMON CPLD TMS input, BMC output
GPIOJ5	U2	Out	FANCARD_TCK	FAN_RACKMON CPLD TCK input, BMC output
GPIOJ6	T2	Out	FANCARD_TDI	FAN_RACKMON CPLD TDI input, BMC output
GPIOJ7	T1	In	FANCARD_TDO	FAN_RACKMON CPLD TDO output, BMC input
GPIOM0	V3	Out	FANCARD_UPD_N	FAN_RACKMON CPLD upgrade enable, active low. To enable fan_rackmon CPLD upgrade
GPIOM4	W3	Out	SYSCPLD_TMS	SYSTEM CPLD TMS input, BMC output
GPIOM6	AA1	Out	SYSCPLD_TCK	SYSTEM CPLD TCK input, BMC output
GPIOM5	Y2	Out	SYSCPLD_TDI	SYSTEM CPLD TDI input, BMC output
GPIOM7	V5	In	SYSCPLD_TDO	SYSTEM CPLD TDO output, BMC input
GPIOF2	A20	Out	SYSCPLD_UPD	SYSTEM CPLD upgrade enable, active High. To enable SYSTEM CPLD upgrade

Table 15: BMC GPIO signals for CPLD online Upgrade

Please note that CPLD upgrade enable signals have different polarity for SYSCPLD and FAN_RACKMON CPLD.

7.11. LED

QSFP28 data port can be configured as single 100G mode, or dual 50G mode, or four 10G mode. However, only two LEDs can be assigned to one QSFP28 port to indicate the port status. R/G/B tri-color LED is used to display more information, but it is difficult to display all four 10G port status if the QSFP28 is configured as 4x10G mode.

Each QSFP28 port has 2 tri-color LED, totally 64 tri-color LED for 32 QSFP28 ports. Serial to parallel shift register 74LV164 can be used to implement these 64 tri-color LED, or 192 bit of LED. 24 piece of 74LV595 or 74LV164 are needed.

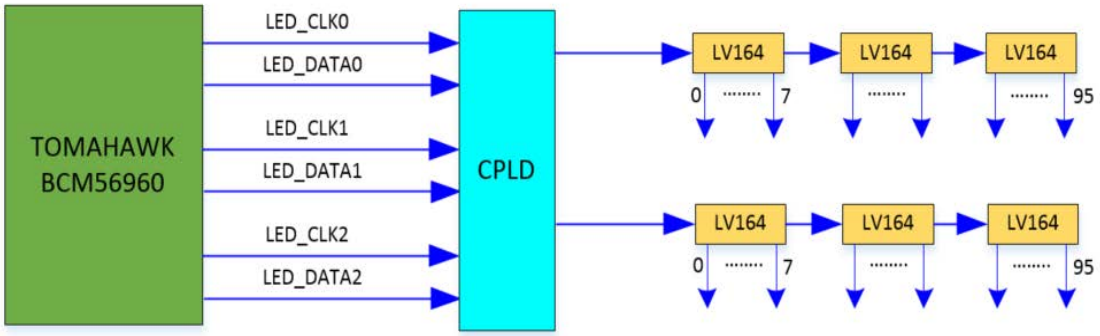

Figure 24: wedge-100 QSFP port LED

Each 2x1 QSFP28 cage has 4 LED, so each QSFP28 port has two LEDs. The LEDs are named a/b/c/d from left to right.

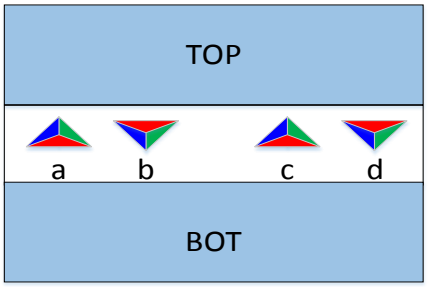

Figure 25: 2x2 QSFP28 Cage LED

The following diagram show the physical mapping of the LED stream. Software need to program tomahawk internal LED micro-controller to output serial stream which match the external LED shift register sequence.

Each QSFP28 port has 12-bit LED stream format, the following table shows the definition. Each line has 3 bit to indicate the RGB status of tri-color LED.

Port	Bit	Name	Definition
QSFP-1 BOT	[0:2]	Lane_1_led[0:2]	B-G-R LED status Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001
	[3:5]	Lane_2_led[0:2]	B-G-R LED status Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001
	[6:8]	Lane_3_led[0:2]	B-G-R LED status Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001
	[9:11]	Lane_4_led[0:2]	B-G-R LED status

			Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001
QSFP-0 TOP	[0:2]	Lane_1_led[0:2]	B-G-R LED status Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001
	[3:5]	Lane_2_led[0:2]	B-G-R LED status Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001
	[6:8]	Lane_3_led[0:2]	B-G-R LED status Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001
	[9:11]	Lane_4_led[0:2]	B-G-R LED status Blue 100 Green 010 Aqua 110 Yellow 011 Purple 101 OFF 000 Red 001

Table 16: Port LED color Definition

Attention: LSB shift out of Tomahawk first

The following are LED stream format, please note that LED stream from Tomahawk, bit-0 is shift out first, and bit-191 is shifted out last.

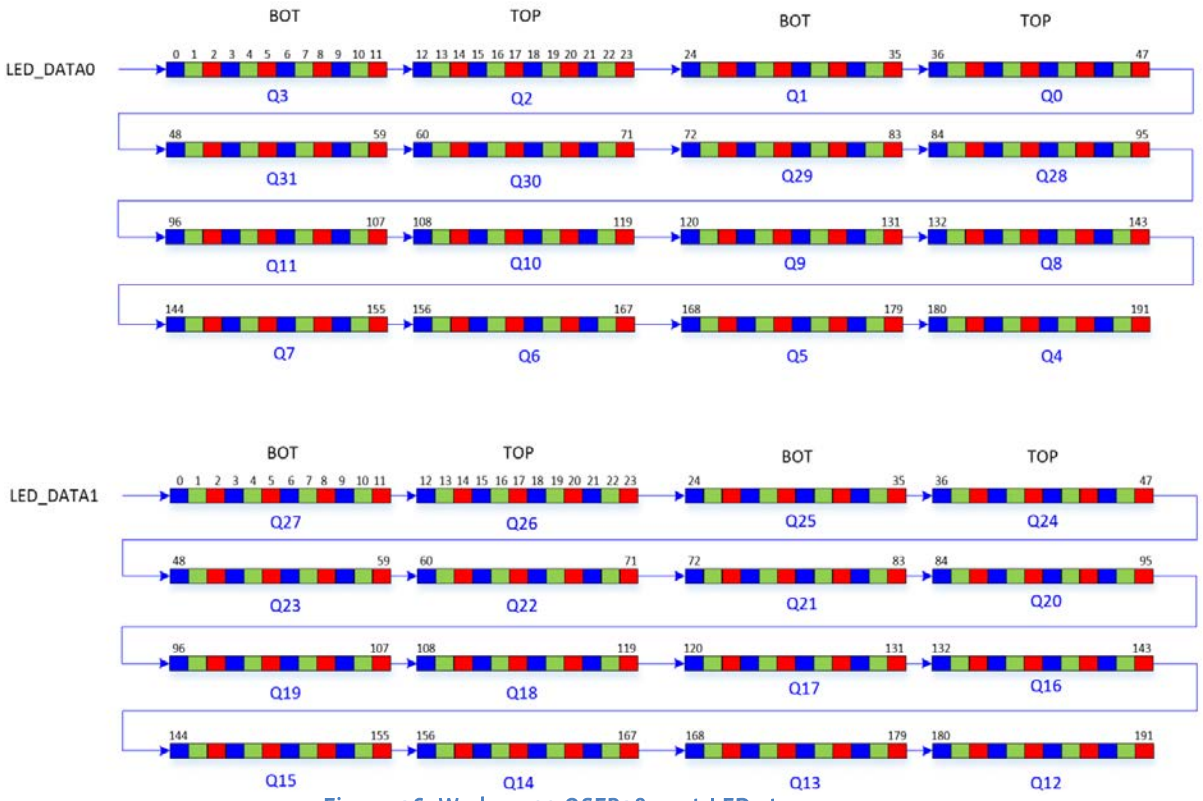

Figure 26: Wedge-100 QSFP28 port LED stream

The led definition is based on facebook's special requirements for data center application, it is more important for switch to display link status, and alarm status than displaying link activity (blinking rx/tx status).

Please note that lane_1_led, lane_2_led, lane_3_led1, and lane_4_led are four LED of one logic 100G port, the status of these four LEDs are from tomahawk LED stream. Each 100G port has four logic LED associated to it. Software can chose to output led status based on port configuration and port status.

For QSFP28 physical port, there are four LED for two QSFP28 port. LED_A, LED_B, LED_C, and LED_D are real tri-color LED built in QSFP28 2x1 cage. Each QSFP28 port only has two tri-color LED. External LED select button (LED_SEL) is used to select LED to display. The following are mapping between LED[1:4] and LED_A/B/C/D.

The CPLD does not care about the mode. It does not ever try to display info for both top and bottom ports at the same time, regardless of the port modes. It just display either the top or bottom info depending on the button status. If both top and bottom ports are in 1x100G mode and we want the LEDs to show info about both, then software will handle this in software. Software will just emit a bitstream that has info for both ports in.

For instance, if ports 1 and 2 are both in 1x100G mode, software can emit info for both port 1 and 2 in the 12-bit value for port 1, and it can replicate the same data in the 12-bit value for port 2. Then regardless of the button state the LEDs displayed will have info for both ports.

To make things clear, here are some examples showing the bitstreams that would be sent for the first two QSFPs in various modes:

- Both in 1x100G mode, both link up:
  - 010 000 000 010 010 000 000 010
- Both in 2x50G mode, with link up on eth1/1, eth1/2, and eth2/2, but errors on eth2/1:
  - 010 100 010 010 010 100 010 010
  - (Assuming that LEDs 1 and 3 are the up arrows and LEDs 2 and 4 are the down arrows.)
- Top port in 2x50G mode, with both links up, bottom port in 4x25G mode, with only the last 3 ports up:
  - 010 000 010 000 000 010 010 010

The following diagrams show some typical modes:

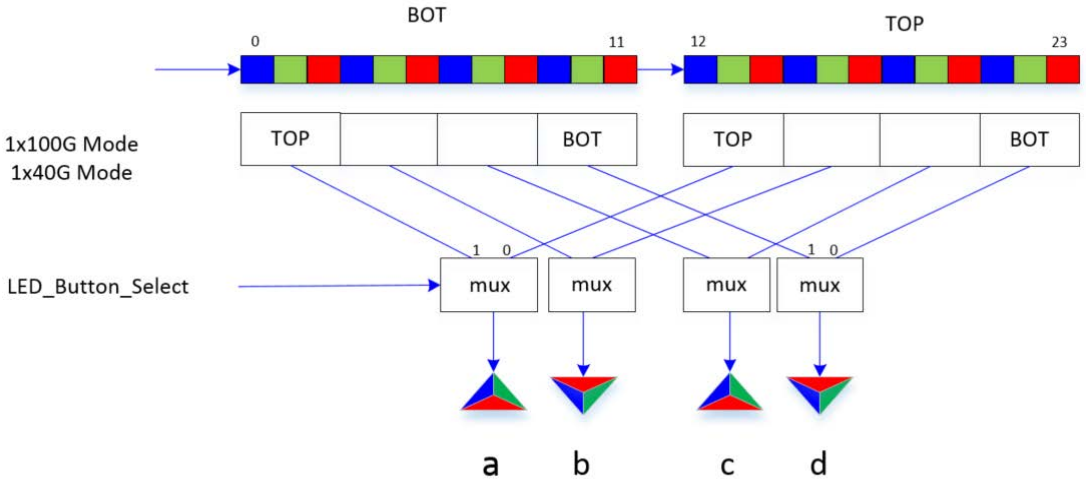

Figure 27: LED MUX in 1x100G mode or 1x40G Mode

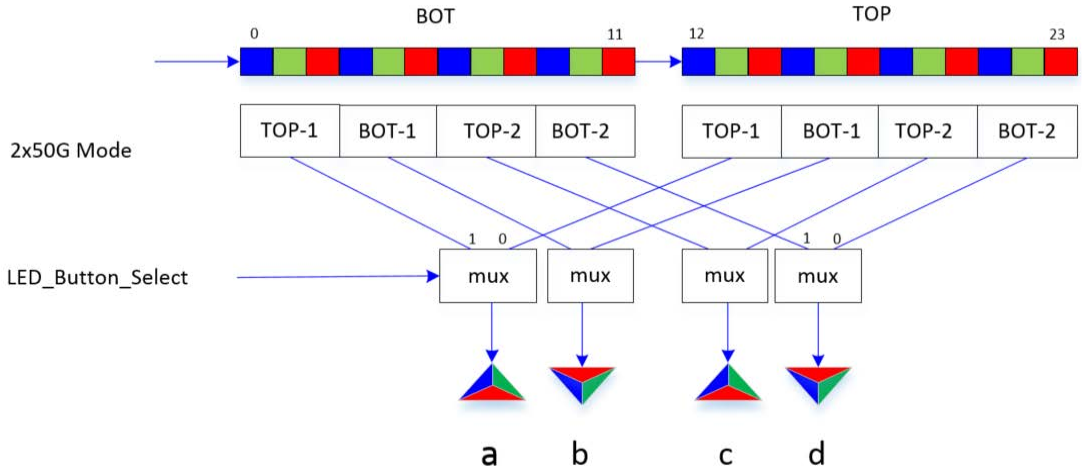

Figure 28: LED MUX in 2x50G Mode

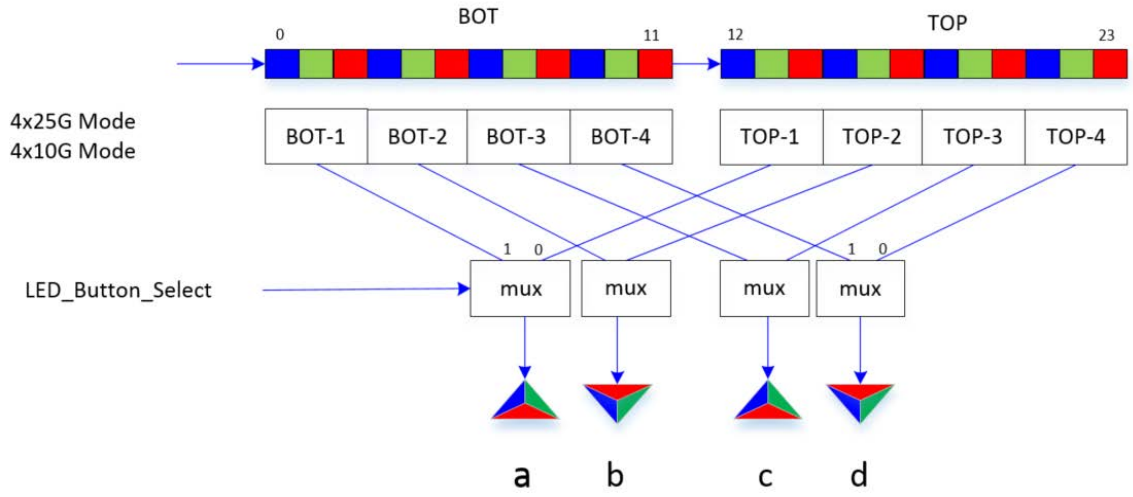

Figure 29: LED MUX in 4x25G mode or 4x10G Mode

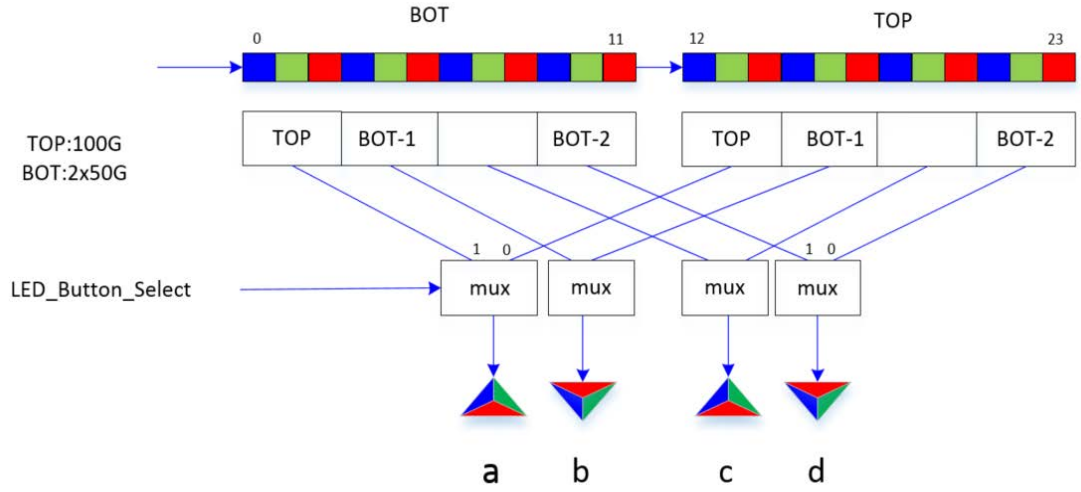

Figure 30: LED MUX in 1x100G mode and 2x50G Mode

Wedge100 CPLD can support different LED mode

- Port LEDs are directly driven by tomahawk stream: reg_0x3C[2:0] = 3'b010
- Port LEDs use FB 12bit stream format: reg_0x3c[2:0] =3'b110
- Port LEDs are driven by CPLD test logic: reg_0x3c[2:0] =3'b000

Software need to set both bit1 TH_LED_EN and bit2 FB_STREAM_EN to high to enable the 12-bit format.

Tomahawk LED Control register				
0x3C	D[0]	0	R/W	TH_LED_CLR 0: Tomahawk LED stream 0/1 normal 1: Tomahawk LED stream 0/1 reset clear

	D[1]	0	R/W	TH_LED_EN 0: Tomahawk LED stream 0/1 disabled 1: Tomahawk LED stream 0/1 enabled
	D[2]	0	R/W	FB_STREAM_EN 0: direct stream from tomahawk 1: 12-bit FB stream format used
	D[3]	0	R/W	WALK_TEST_EN 0: LED walk test disabled 1: LED walk test enabled
	D[5:4]	10	R/W	00: stream-0 single led check, led number and color is decided by register 0x3d, constant 01: stream-1 single led check, led number and color is decided by register 0x3d, constant 10: stream-0 all led check, led color is decided by register 0x3d, constant 11: stream-1 all led check, led color is decided by register 0x3d, constant
	D[6]	1	R/W	LED_TEST_BLINK_EN 0: normal constant 1: Blinking during LED test
	D[7]	1	R/W	LED_TEST_MODE_EN 0: normal 1: Port LED test mode enabled

Table 17: Tomahakw LED Control and debug Register

7.12. On Board Power Design

Tomahawk 1.0V core voltage 160A rail with ROV:

- IR3581 + 6xIR3556 six phase design
- Power stage IR3556
- Inductor

Tomahawk fixed 1.0V analog 50A rail:

- IR3584 + 2x IR3556 two phase design
- Power stage IR3556
- Inductor

Wedge-100 3.3V main power 50A rail:

- IR3584 + 2x IR3556 two phase design
- Power stage IR3556
- Inductor

Voltage rails with small current can use TI TPS54339 (3A), TPS53318 (6A)

7.13. Voltage Rail control and Monitor

In order to ensure proper operation of all power rails at all times, wedge-100 need to support the following voltage rail control and monitor functions

- The power up and power sequence of all voltage rails need to be controlled in sub-ms delay.
- All voltage rails need to be closely monitored, Under voltage threshold and over voltage threshold need to be specified by design and can be adjustable by software if needed.
- All voltage rails need to be measured in reasonable accuracy

Lattice semiconductor programmable power controller PWR1014A is recommended to implement all these three functions. Power control and status information can be accessed via i2c interface

Voltages are reported as part of the system enclosure status information. The power rails to be monitored are shown in Table 18.

Table 18 Monitored Power Rails on Wedge-100

Power domain	Power Rail	Voltage
Main Power	P3.3V	3.3V
	P1.8V	1.8V
	P1.25V	1.25V
	P1.0V_ROV	0.970V to 1.03V
	P1.0V_A	1.0V
Standby power	P3.3V_STBY	3.3V
	P1.8V_STBY	1.8V
	P1.5V_STBY	1.5V
Input Power	Input 12V	12.5V

7.14. Power sequencer and monitor

Wedge-100 will use programmable power manager chip PWR1014A from lattice semiconductor. PWR1014A support the following features:

- Power rail sequence control up to 12 rails
- Monitor 10 voltage rails
- Perform voltage measurement on 10 voltage rails
- I2C interface

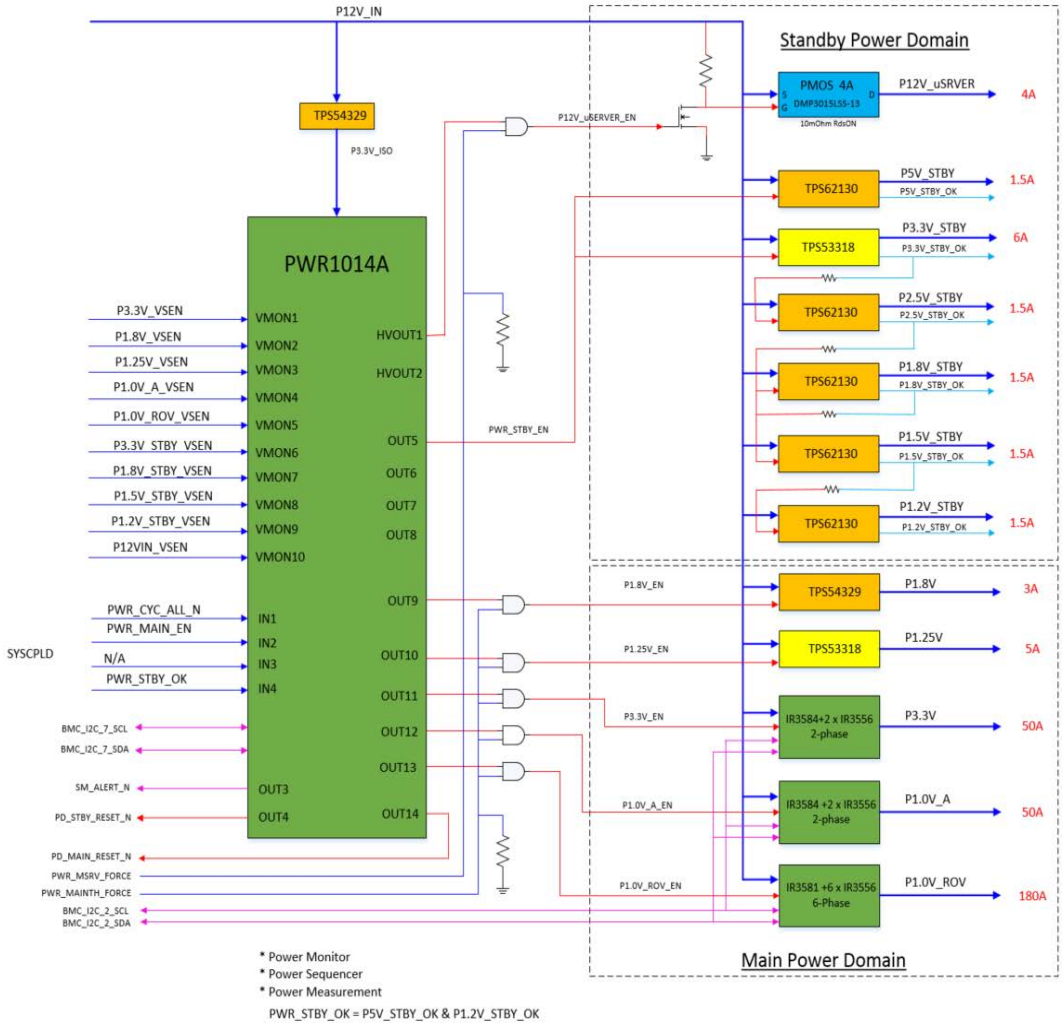

Figure 31: Power sequencer and power circuit diagram

7.15. System reset

Wedge-100 system reset diagram is shown in the following diagram.

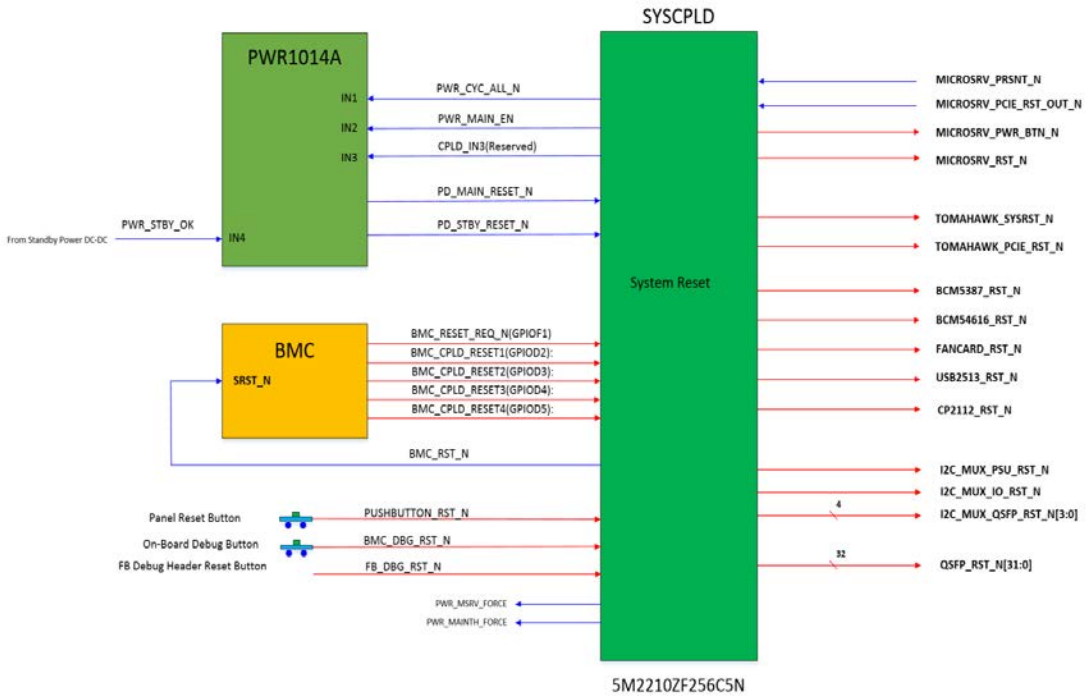

Figure 32: Wedge-100 reset architecture

8. Rack Monitor and fan control card

8.1. Block Diagram

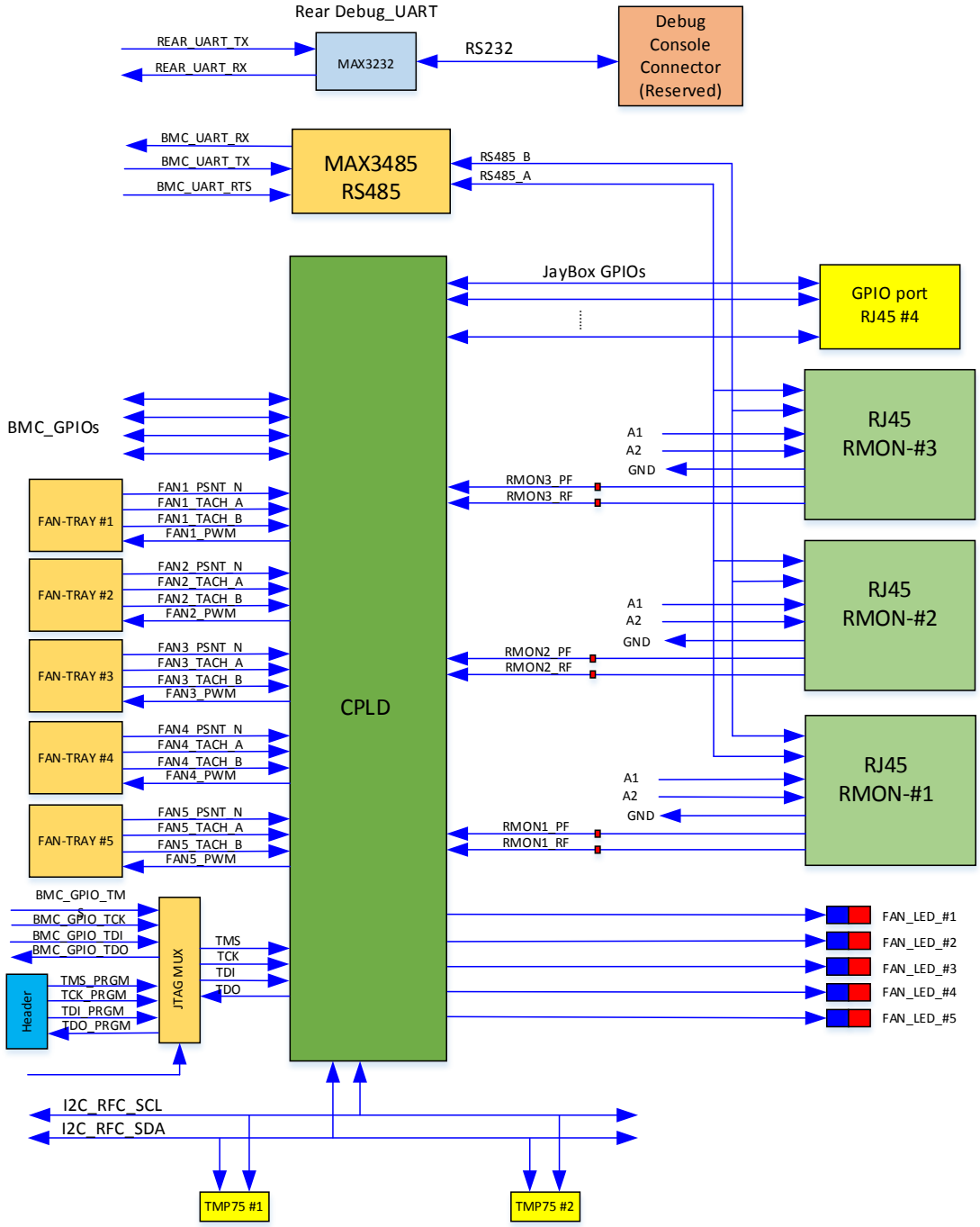

Figure 33: Rackmon and fan control card diagram (Standard SKU)

Rackmon and fan control card (RMF card) support the following features:

- Provide 3 Rack Monitor RJ45 connector for Open Rack V2 Rack Monitor. One RS485 UART among all 3 Rackmon RJ45 ports connected to BMC, and PSU status of three racks
- Provide 1 RJ45 Connector for GPIO signals of JayBox
- 5 B/R bi-color LED to indicate the fan tray status of 5 CR fantray
- Control and status of 5 CR fantray
- I2C interface to main board BMC

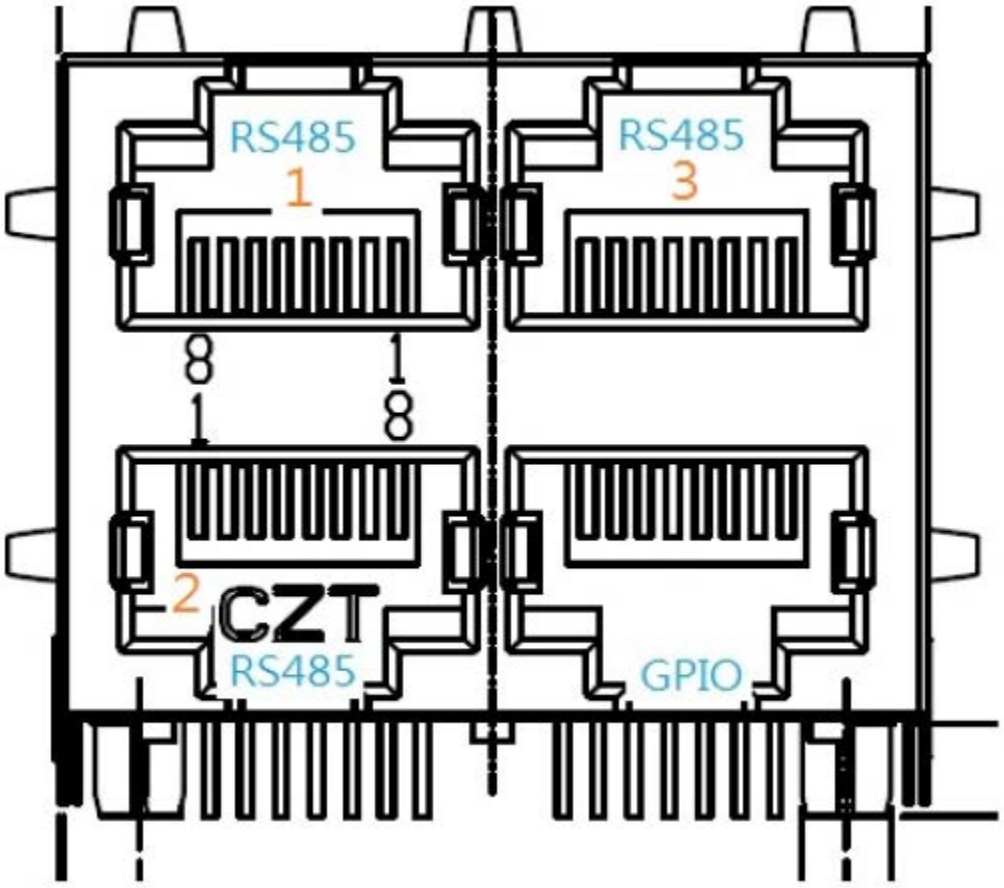

Figure 34: RackMon and GPIO RJ45 Connectors

The RS-485 signals on the three RackMon RJ45 connectors are connected to one RS-485 transceiver on the RMF card, and are connected to BMC UART #4 (TXD4, RXD4, and NRTS4).

Table 19: RackMon RJ45 Connector Pin-out Definition

Pin Number	Pin Name	Signal Level	Descriptions
1	GND	Signal Ground	
2	GPIO	LVCMOS	

3	GPIO	LVCMOS	Each of these two signals is connected to one of the GPIOs on BMC (GPIOP0 ~ 5). There are six GPIOs total across the three RackMon connectors.
4	RS485_A	RS-485	Non-inverting signal of the RS-485 differential pair.
5	RS485_B		Inverting signal of the RS-485 pair.
6	NC	N/A	No Connect
7	A1	LVCMOS	These two signals are strapping pins on the three RackMon connectors. They are either connected to Ground through 33-Ohm resistor or to +3.3V through 10KOhm resistor. Here are the strapping values for A[2:1] – RS485 #1: "00" RS485 #2: "01" RS485 #3: "10"
8	A2		

Table 20: GPIO RJ45 Connector Pin-out Definition

Pin Number	Pin Name	Signal Level	Descriptions
1	GPIO1	LVCMOS	These eight GPIO signals are connected to the CPLD on the RMF card. GPIO1, GPIO3 are pulled up to +3.3V through 1KOhm resistors, while GPIO2, GPIO4 are pulled down to GND through 10KOhm resistors on RMF. The programming information of these GPIOs is described in 7.8.4, 7.8.33, and 7.8.34.
2	GPIO2	LVCMOS	
3	GPIO3	LVCMOS	
4	GPIO4	LVCMOS	
5	GPIO5	LVCMOS	
6	GPIO6	LVCMOS	
7	GPIO7	LVCMOS	
8	GPIO8	LVCMOS	

9. COM-E CPU Module

COM-E CPU module is used as control plane CPU in wedge-100.

9.1. COM-E CPU Module Feature List

Wedge-100 uses PCOM-B632VG COM-E CPU module based on Intel Atom Processor E3800 family (Code Name BayTrail) SoC, Main feature list of PCOM-B632VG is as following:

- Processor
  - Intel® AtomTM processor E3800 family, 22nm process technology
  - Cache up to 2MB (for Quad Core)
  - DPM (Defect Per Million devices) <50
  - Support Intel® VT-x technology
- BIOS
  - Phoenix BIOS
- Memory - Support up to 8GB DDR3L 1066/1333 SDRAM on one 204pin SODIMM
- Storage Devices
  - Two SATA 2.0
  - One Micro-SD slot
- Watchdog Timer
  - Programmable by embedded controller
- Expansion Interface
  - Supports up to four PCI Express lanes by LAN disable, four x 1 lanes can be configured to one x 4 lane (default 3x PCI-Express lanes)
  - SPI Interface
  - SM Bus interface
  - I2C interface
- I/O Interface
  - Audio - HDA controller integrated in SoC
  - Ethernet - Onboard Intel I210IT
  - Serial Port - Two series RX/TX supported from onboard EC (embedded controller)
  - USB
    - 6 ports USB2.0
    - 1 port USB3.0
  - Keyboard & Mouse - KB controller integrated in embedded controller
- Mechanic and Environment
  - Dimension - 95mm(L) x 95mm(W) x 2.0mm(H)
  - Power Supply - DC 6V~16.8V
  - Environment
    - Operation temperature: -40~80°C
    - Storage temperature: -40~80°C
    - Relative humidity : 5~95%, non-condensing
  - MTBF
    - Over 180000hrs at 55°C

9.2. COM-E Block Diagram

The following figure illustrates the functional block diagram of the COM-E CPU card.

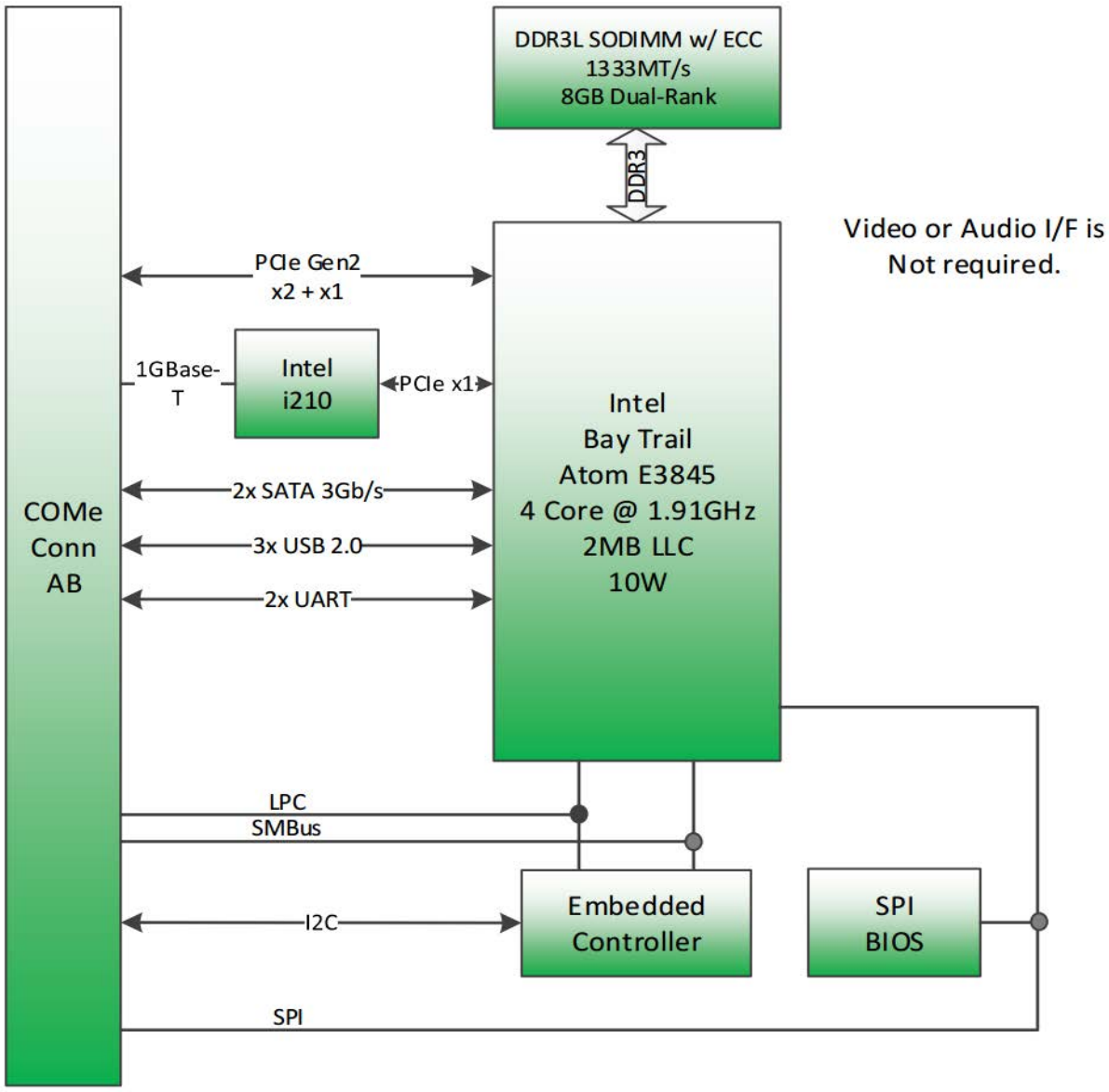

Figure 35: Portwell COM-E CPU Module Block Diagram

9.3. Pin Definition of COM-E Connector

COM-E CPU module has J5 and J6 two connectors, the signal definition of these two connectors are shown in the following tables:

J6					
Row A			Row B		
Pin No.	Signal	Required?	Pin No.	Signal	Required?
A1	GND	Required	B1	GND	Required
A2	GBE0_MDI3-	Required	B2	GBE0_ACT#	
A3	GBE0_MDI3+	Required	B3	LPC_FRAME#	Required
A4	GBE0_LINK100#		B4	LPC_AD0	Required
A5	GBE0_LINK1000#		B5	LPC_AD1	Required
A6	GBE0_MDI2-	Required	B6	LPC_AD2	Required
A7	GBE0_MDI2+	Required	B7	LPC_AD3	Required
A8	GBE0_LINK#		B8	LPC_DRQ0#	
A9	GBE0_MDI1-	Required	B9	LPC_DRQ1#	
A10	GBE0_MDI1+	Required	B10	LPC_PCLK	Required
A11	GND	Required	B11	GND	Required
A12	GBE0_MDI0-	Required	B12	PWRBTN#	Required
A13	GBE0_MDI0+	Required	B13	SMB_CLK	Required
A14	GBE0_CTREF	Required	B14	SMB_DAT	Required
A15	SUS_S3#	Required if the module supports S3	B15	SMB_ALERT#	Required
A16	SATA0_TX+	Required	B16	SATA1_TX+	
A17	SATA0_TX-	Required	B17	SATA1_TX-	
A18	SUS_S4#	Required if the module supports S4	B18	SUS_STAT#	Required
A19	SATA0_RX+	Required	B19	SATA1_RX+	
A20	SATA0_RX-	Required	B20	SATA1_RX-	
A21	GND	Required	B21	GND	Required
A22	SATA2_TX+		B22	SATA3_TX+	
A23	SATA2_TX-		B23	SATA3_TX-	
A24	SUS_S5#	Required if the module supports S5	B24	PWROK	Required
A25	SATA2_RX+		B25	SATA3_RX+	
A26	SATA2_RX-		B26	SATA3_RX-	
A27	BATLOW#	Required	B27	WDT	Required
A28	ATA_ACT#		B28	HDA_SDIN2	
A29	HDA_SYNC		B29	HDA_SDIN1	
A30	HDA_RST#		B30	HDA_SDIN0	
A31	GND	Required	B31	GND	Required
A32	HDA_BITCLK		B32	SPKR	

A33	HDA_SDOUT		B33	I2C_CLK	Required
A34	BIOS_DIS0#	Required	B34	I2C_DAT	Required
A35	THRMTRIP#	Required	B35	THRM#	Required
A36	USB6-		B36	USB7-	
A37	USB6+		B37	USB7+	
A38	USB_6_7_OC#		B38	USB_4_5_OC#	
A39	USB4-		B39	USB5-	
A40	USB4+		B40	USB5+	
A41	GND	Required	B41	GND	Required
A42	USB2-		B42	USB3-	
A43	USB2+		B43	USB3+	
A44	USB_2_3_OC#		B44	USB_0_1_OC#	
A45	USB0-	Required	B45	USB1-	
A46	USB0+	Required	B46	USB1+	
A47	VCC_RTC	Required	B47	EXCD1_PERST#	
A48	EXCD0_PERST#		B48	EXCD1_CPPE#	
A49	EXCD0_CPPE#		B49	SYS_RST#	Required
A50	LPC_SERIRQ	Required	B50	CB_RESET#	Required
A51	GND	Required	B51	GND	Required
A52	PCIE_TX5+	NC	B52	PCIE_RX5+	
A53	PCIE_TX5-	NC	B53	PCIE_RX5-	
A54	GPI0	Required	B54	GPO1	
A55	PCIE_TX4+		B55	PCIE_RX4+	
A56	PCIE_TX4-		B56	PCIE_RX4-	
A57	GND		B57	GPO2	
A58	PCIE_TX3+	Preferred to have	B58	PCIE_RX3+	Preferred to have
A59	PCIE_TX3-	Preferred to have	B59	PCIE_RX3-	Preferred to have
A60	GND	Required	B60	GND	Required
A61	PCIE_TX2+	Preferred to have	B61	PCIE_RX2+	Preferred to have
A62	PCIE_TX2-	Preferred to have	B62	PCIE_RX2-	Preferred to have
A63	GPI1		B63	GPO3	
A64	PCIE_TX1+	Required	B64	PCIE_RX1+	Required
A65	PCIE_TX1-	Required	B65	PCIE_RX1-	Required
A66	GND	Required	B66	WAKE0#	
A67	GPI2		B67	WAKE1#	
A68	PCIE_TX0+	Required	B68	PCIE_RX0+	Required
A69	PCIE_TX0-	Required	B69	PCIE_RX0-	Required
A70	GND	Required	B70	GND	Required
A71	LVDS_A0+		B71	LVDS_B0+	

A72	LVDS_A0-		B72	LVDS_B0-	
A73	LVDS_A1+		B73	LVDS_B1+	
A74	LVDS_A1-		B74	LVDS_B1-	
A75	LVDS_A2+		B75	LVDS_B2+	
A76	LVDS_A2-		B76	LVDS_B2-	
A77	LVDS_VDDEN		B77	LVDS_B3+	
A78	LVDS_A3+		B78	LVDS_B3-	
A79	LVDS_A3-		B79	LVDS_BKLT_EN	
A80	GND	Required	B80	GND	Required
A81	LVDS_CLKA+		B81	LVDS_CLKB+	
A82	LVDS_CLKA-		B82	LVDS_CLKB-	
A83	LVDS_I2CCK		B83	LVDS_BKLT_CTRL	
A84	LVDS_I2CDAT		B84	VCC_5V_SBY	Required
A85	GPI3		B85	VCC_5V_SBY	Required
A86	NC		B86	VCC_5V_SBY	Required
A87	NC		B87	VCC_5V_SBY	Required
A88	PCIE0_CK_REF+	Required	B88	BIOS_DIS1#	Required
A89	PCIE0_CK_REF-	Required	B89	VGA_RED	
A90	GND	Required	B90	GND	Required
A91	SPI_POWER	Required	B91	VGA_GRN	
A92	SPI_MISO	Required	B92	VGA_BLU	
A93	GPO0	Required	B93	VGA_HSYNC	
A94	SPI_CLK	Required	B94	VGA_VSYNC	
A95	SPI_MOSI	Required	B95	VGA_DDC_CLK	
A96	NC		B96	VGA_DDC_DAT	
A97	TYPE10#	Required	B97	SPI_CS#	Required
A98	SER0_TX	Required	B98	NC	
A99	SER0_RX	Required	B99	NC	
A100	GND	Required	B100	GND	Required
A101	SER1_TX		B101	FAN_PWNOUT	
A102	SER1_RX		B102	FAN_TACHIN	
A103	LID#		B103	SLEEP#	
A104	VCC_12V	Required	B104	VCC_12V	Required
A105	VCC_12V	Required	B105	VCC_12V	Required
A106	VCC_12V	Required	B106	VCC_12V	Required
A107	VCC_12V	Required	B107	VCC_12V	Required

A108	VCC_12V	Required	B108	VCC_12V	Required
A109	VCC_12V	Required	B109	VCC_12V	Required
A110	GND	Required	B110	GND	Required

Table 21: Signal Definition of COM-e Connector(1st)

COM-E J5 Connector pin assignment is shown in the following table:

J5					
Row C			Row D		
Pin No.	Signal	Required?	Pin No.	Signal	Required?
C1	GND	Required	D1	GND	Required
C2	GND	Required	D2	GND	Required
C3	USB0_SSRX-		D3	USB0_SSTX-	
C4	USB0_SSRX+		D4	USB0_SSTX+	
C5	GND	Required	D5	GND	Required
C6	USB1_SSRX-		D6	USB1_SSTX-	
C7	USB1_SSRX+		D7	USB1_SSTX+	
C8	GND	Required	D8	GND	Required
C9	USB2_SSRX-		D9	USB2_SSTX-	
C10	USB2_SSRX+		D10	USB2_SSTX+	
C11	GND	Required	D11	GND	Required
C12	USB3_SSRX-		D12	USB3_SSTX-	
C13	USB3_SSRX+		D13	USB3_SSTX+	
C14	GND	Required	D14	GND	Required
C15	DP1_LANE6		D15	DP1_CTRLCLK_AUX	
C16	DP1_LANE6#		D16	DP1_CTRLDATA_AUX#	
C17	NC		D17	NC	
C18	NC		D18	NC	
C19	PCIE_RX6+		D19	PCIE_TX6+	
C20	PCIE_RX6-		D20	PCIE_TX6-	
C21	GND	Required	D21	GND	Required
C22	NC		D22	NC	
C23	NC		D23	NC	
C24	DP1_HDP		D24	NC	
C25	DP1_LANE4		D25	NC	
C26	DP1_LANE4#		D26	DP1_LANE0	
C27	NC		D27	DP1_LANE0#	
C28	NC		D28	NC	

C29	DP1_LANE5		D29	DP1_LANE1	
C30	DP1_LANE5#		D30	DP1_LANE1#	
C31	GND	Required	D31	GND	Required
C32	DP2_CTRLCLK_AUX		D32	DP1_LANE2	
C33	DP2_CTRLDATA_AUX#		D33	DP1_LANE2#	
C34	DP2_AUX_SEL		D34	DP1_AUX_SEL	
C35	NC		D35	NC	
C36	DP3_CTRLCLK_AUX		D36	DP1_LANE3	
C37	DP3_CTRLDATA_AUX#		D37	DP1_LANE3#	
C38	DP3_AUX_SEL		D38	NC	
C39	DP3_LANE0		D39	DP2_LANE0	
C40	DP3_LANE0#		D40	DP2_LANE0#	
C41	GND	Required	D41	GND	Required
C42	DP3_LANE1		D42	DP2_LANE1	
C43	DP3_LANE1#		D43	DP2_LANE1#	
C44	DP3_HPD		D44	DP2_HPD	
C45	NC		D45	NC	
C46	DP3_LANE2		D46	DP2_LANE2	
C47	DP3_LANE2#		D47	DP2_LANE2#	
C48	NC		D48	NC	
C49	DP3_LANE3		D49	DP2_LANE3	
C50	DP3_LANE3#		D50	DP2_LANE3#	
C51	GND	Required	D51	GND	Required
C52	PEG_RX0+		D52	PEG_TX0+	
C53	PEG_RX0-		D53	PEG_TX0-	
C54	TYPE0#	Required	D54	PEG_LANE_RV#	
C55	PEG_RX1+		D55	PEG_TX1+	
C56	PEG_RX1-		D56	PEG_TX1-	
C57	TYPE1#	Required	D57	TYPE2#	Required
C58	PEG_RX2+		D58	PEG_TX2+	
C59	PEG_RX2-		D59	PEG_TX2-	
C60	GND	Required	D60	GND	Required
C61	PEG_RX3+		D61	PEG_TX3+	
C62	PEG_RX3-		D62	PEG_TX3-	

C63	NC		D63	NC	
C64	NC		D64	NC	
C65	PEG_RX4+		D65	PEG_TX4+	
C66	PEG_RX4-		D66	PEG_TX4-	
C67	NC		D67	GND	Required
C68	PEG_RX5+		D68	PEG_TX5+	
C69	PEG_RX5-		D69	PEG_TX5-	
C70	GND	Required	D70	GND	Required
C71	PEG_RX6+		D71	PEG_TX6+	
C72	PEG_RX6-		D72	PEG_TX6-	
C73	GND	Required	D73	GND	Required
C74	PEG_RX7+		D74	PEG_TX7+	
C75	PEG_RX7-		D75	PEG_TX7-	
C76	GND	Required	D76	GND	Required
C77	NC		D77	NC	
C78	PEG_RX8+		D78	PEG_TX8+	
C79	PEG_RX8-		D79	PEG_TX8-	
C80	GND	Required	D80	GND	Required
C81	PEG_RX9+		D81	PEG_TX9+	
C82	PEG_RX9-		D82	PEG_TX9-	
C83	NC		D83	NC	
C84	GND	Required	D84	GND	Required
C85	PEG_RX10+		D85	PEG_TX10+	
C86	PEG_RX10-		D86	PEG_TX10-	
C87	GND	Required	D87	GND	Required
C88	PEG_RX11+		D88	PEG_TX11+	
C89	PEG_RX11-		D89	PEG_TX11-	
C90	GND	Required	D90	GND	Required
C91	PEG_RX12+		D91	PEG_TX12+	
C92	PEG_RX12-		D92	PEG_TX12-	
C93	GND	Required	D93	GND	Required
C94	PEG_RX13+		D94	PEG_TX13+	
C95	PEG_RX13-		D95	PEG_TX13-	
C96	GND	Required	D96	GND	Required
C97	NC		D97	NC	
C98	PEG_RX14+		D98	PEG_TX14+	
C99	PEG_RX14-		D99	PEG_TX14-	
C100	GND	Required	D100	GND	Required
C101	PEG_RX15+		D101	PEG_TX15+	

C102	PEG_RX15-		D102	PEG_TX15-	
C103	GND	Required	D103	GND	Required
C104	VCC_12V	Required	D104	VCC_12V	Required
C105	VCC_12V	Required	D105	VCC_12V	Required
C106	VCC_12V	Required	D106	VCC_12V	Required
C107	VCC_12V	Required	D107	VCC_12V	Required
C108	VCC_12V	Required	D108	VCC_12V	Required
C109	VCC_12V	Required	D109	VCC_12V	Required
C110	GND	Required	D110	GND	Required

Table 22: Signal Definition of COM-e Connector(2nd)

10. PCB Stack-up

The PCB thickness of the wedge-100 main board is about 120mil or 3mm. 22 layer PCB stackup is recommended. Low loss PCB material with HVLP copper roughness should be used. The following ultra low loss PCB materials are recommended

- TUC-933 (a.k.a T3), HVLP copper foil
- TUC-883 (a.k.a T2), HVLP copper foil
- Doosan DS-7409DV(N), HVLP copper foil
- Doosan DS-7409DV, HVLP copper foil

TUC-933 and DS-7409DV(N) are ultra low loss material, Df is about 0.005 range, and S21 insertion loss could be about 0.7db/in at 12.89Ghz; TUC-883 and DS-7409DV are very low loss material, Df is about 0.006 range, and S21 insertion loss is about 0.9db/in at 12.89Ghz. TUC-933 material is used in the following stackup (courtesy of ISU-Petasys) as example.

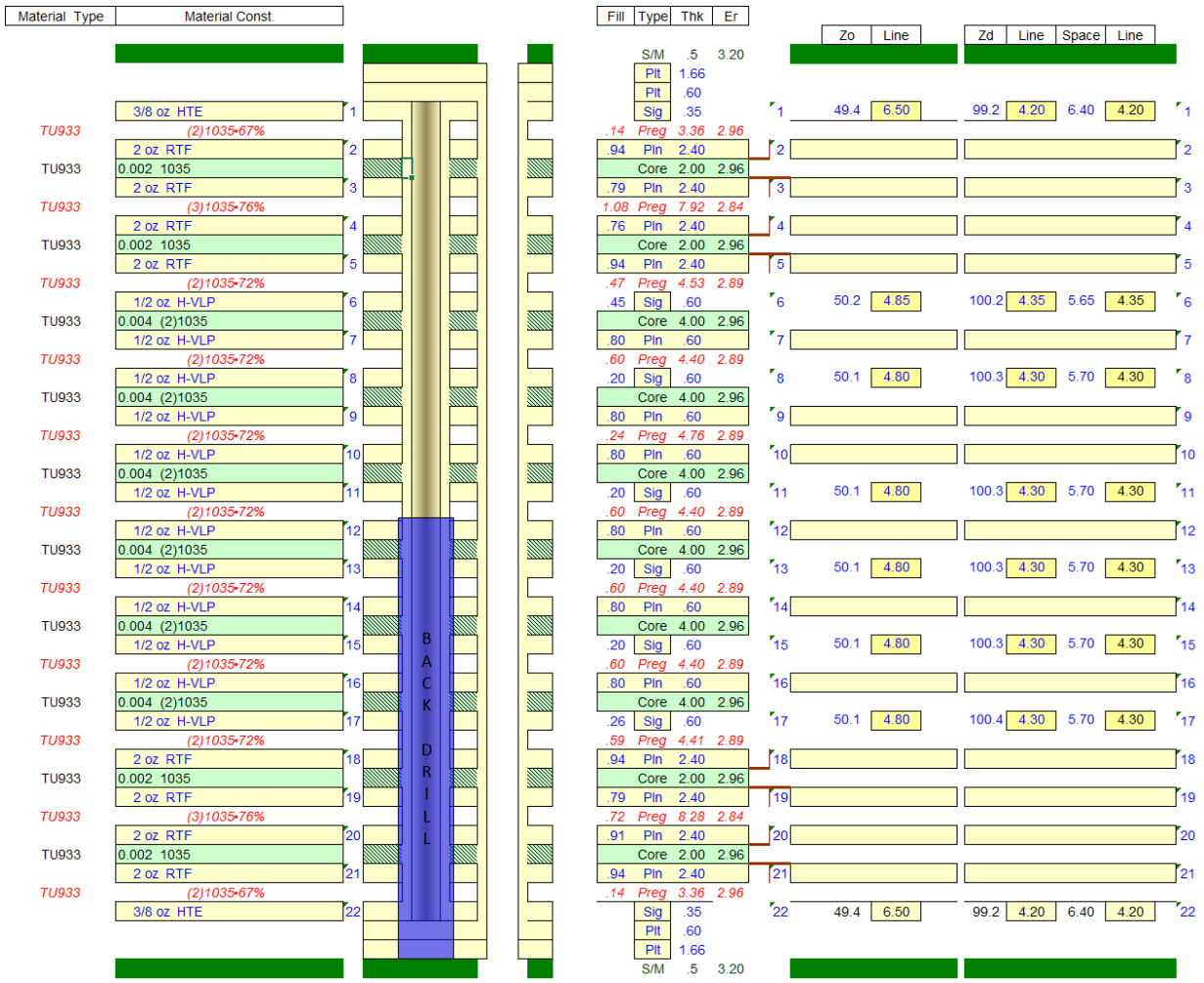

Figure 36: Wedge-100 TUC-933 PCB Stackup(Courtesy of ISU-Petasys)

11. Wedge-100 Power

11.1. Power Budget

Board level power budget of wedge-100 is estimated to be 436W, assuming all 32 QSFP ports have 3.5W QSFP28 optic module mounted. The following table shows the summary of calculation power as of now.

	qty	Unit Power	Power

Micro Server	1	30	30
Tomahawk	1	200	200
QSFP28	32	3.5	112
Fantray	5	16.8	84
Other	1	10	10
Total Power			436

Table 23: wedge-100 power estimate

In wedge-100's typical application, 8 uplink ports will use QSFP28 optic, which could have 3.5W power consumption, and all other 24 ports are populated with passive cable, which has almost no power consumption. So typical power consumption will be about 350W, 84 W less than the estimate in table 20.

The following table shows the real measured power consumption under different working scenarios:

Power consumption with no/Full load on different FAN speed (30%~100%)			
AC input: 110V/60Hz			
FAN Speed	Idea_no load transceivers (W)	Idea_load transceivers (W)	CPU Full Load (mprime) + linespeed
30%	132.6	252	303
40%	137.7	257.4	309
50%	145.4	264.5	316.5
60%	155.1	274.1	325.5
70%	166.1	284.5	336.4
80%	184.2	303	357
90%	202	320	374
100%	217.3	334	389

Table 24: wedge-100 Measured Power Consumption

11.2. Tomahawk Power Design

Tomahawk switch ASIC requires ROV support for its main core power rail. Four ROV output pins driven by tomahawk ASIC indicate the optimized core voltage required by ASIC.

ROV[3:0]	Voltage	Note
4'b0000	1.2000	
4'b0001	1.1750	
4'b0010	1.1500	
4'b0011	1.1250	
4'b0100	1.1000	
4'b0101	1.0750	
4'b0110	1.0500	

4'b0111	1.0250	
4'b1000	1.0000	Default value
4'b1001	0.9750	
4'b1010	0.9500	
4'b1011	0.9250	
4'b1100	0.9000	
4'b1101	0.8750	
4'b1110	0.8500	
4'b1111	0.8250	

Table 25: Tomahawk ROV definition

In wedge-100, SYSCPLD is used to decode the ROV output of tomahawk ASIC, and then drive the VIDSEL[2:0] input of IR3581 DC-DC controller to adjust the output voltage of VDD_ROV for tomahawk core voltage rail.

12. Wedge-100 Functional

12.1. COM-E BIOS Feature List

The COM-Express module vendor shall be responsible for supplying and customizing the BIOS for the SOC. The requirements are outlined in this section.

- UEFI compatible
- Configuration and features
  - Disable unused devices
  - BIOS setup menu
  - SoC settings to allow tuning to achieve the optimal combination of performance and power consumption
- BIOS settings tool
- Default boot device priority
  - Network / PXE -> 1st off-module SATA (M.2 SSD) -> Other removable devices (USB drive)
- PXE boot (UEFI Mode)
  - Supports PXE boot and provide the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first Ethernet device (eth0).
  - PXE timeout timer set to 10 seconds
- Other boot options
  - Also supports booting from SATA and USB interfaces
  - Provides the capability to select boot options
- Remote BIOS update
  - Scenario 1: Sample / audit BIOS settings
  - Scenario 2: Update BIOS with pre-configured set of BIOS settings
  - Scenario 3: BIOS / firmware update with a new revision
  - Update from the operating system over the LAN
  - Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
  - No user interaction (e.g., prompts)
  - BIOS updates and option changes do not take longer than five minutes to complete
  - Can be scripted and propagated to multiple machines
- Event log
  - Implement SMBIOS type 15 per SMBIOS specification Rev 2.6
  - Hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB)
  - Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID
  - A system access interface and application software to retrieve and clear the event log from the BIOS
- Logged errors
  - CPU / memory errors
  - PCIe errors
  - SATA errors
  - POST errors
  - System reboot events
  - Sensor values exceeding warning or critical thresholds
- Error thresholds
  - Setting must be enabled for both correctable and uncorrectable errors.

    - Threshold for Memory Correctable ECC is TBD.
    - PCIe error threshold follows chipset vendor's suggestion.
- POST codes
    - To be provided on the serial console
    - To be provided on the LPC bus
- DMI
    - Model
    - Serial Number
    - Additional information requested by Facebook
- Processor
    - Atom processor
    - Execute-Disable Bit Capability
    - Active Processor Core Count
    - C-State Technology (C0, C1, C1E, and C6)
    - Intel® Virtualization Technology (VT)
    - Advanced Encryption standard New Instruction (AES-NI)
- Memory
    - Slot detection and Sizing
    - Memory Frequency
- AC Power Loss
    - Power On
    - Power Off
    - Last State
- LED
    - Port 80 LED
- Button
    - Power Button
    - ACPI MP 1.4
    - Platform PCI Routing
    - Sub-System ID
    - Onboard Device enable/disable
    - Spread Spectrum Clock
    - Clock disabled for unused slot/device
    - Popup Menu F11
    - PXE Boot F12
- Post/Setup Message
    - BIOS Date
    - BIOS Version
    - CPU String
    - CPU Speed
    - Hot keys (F2/DEL/F11/F12)
    - Memory Info
- Serial Console Redirection
    - POST
    - SETUP
    - DOS
- Flash
    - Supported Flash Parts
    - DOS Flash Utility
    - Linux Flash Utility
    - BIOS Recovery during BIOS post
    - non-BIOS region update

- **Storage**
  - SATA
  - AHCI Mode
- **USB**
  - Legacy USB Boot/Hot plug
  - USB OverCurrent
- **BIOS Security**
- **SMBIOS**
  - Type 0 : BIOS Information
  - Type 1 : System Information
  - Type 2 : Base Board Information
  - Type 3 : System Enclosure or Chassis
  - Type 4 : Processor Information
  - Type 7 : Cache Information
  - Type 8 : Port Connector Information
  - Type 10 : On Board Devices Information
  - Type 11 : OEM String
  - Type 13 : BIOS Language Information
  - Type 15: System Event Log
  - Type 16 : Physical Memory Array
  - Type 17 : Memory Device
  - Type 19 : Memory Array Mapped Address
  - Type 38 : IPMI device Information
  - Type 127 : End of Table
- SPD reading retry 3 times mechanism
- **Event Logging**
  - Single ECC Error
  - Multi-bit ECC Error
  - PCI-Express Error
  - NMI on Error
  - POST Error
  - Filter OEM POST Error for SMBIOS error log
  - OEM SMBIOS error log (only BIOS error)

12.2. BMC Feature Support

The BMC on wedge-100 support the following features:

- All SEL commands
- All sensor commands
- All SDR commands
- Power on/off/cycle / hardware reset / soft reset commands
- I2C access to Power Sequencer, and DC-DC convertor
- Inventory EEPROM access
- Fan-tray present status check, fan PWM control and speed status read
- Dual SPI boot
- On-board OOB switch MDIO interface access
- On-board PHY MDIO interface access
- CPLD online upgrade(disabled in MP)

13. Transceivers and cables

13.1. 100G optics

Wedge100 support the following 100G optics

- QSFP28 CWDM4 100G transceiver
- Other MSA based on QSFP28 form factor
  - QSFP28 CLR4 100G transceiver
  - QSFP28 LR4/LR4-lite 100G transceiver

Wedge100 also support QSFP+ 40G optics

- QSFP+ 40G SR4 transceiver(Multi-mode OM3/OM4)
- QSFP+ 40G LR4 transceiver(Single mode fiber)

Figure 37: QSFP28 CWDM4 100G Optic transceiver

13.2. 100G DAC Cables

- QSFP28 100GE to QSFP28 100GE cable, 1M, 2M, 3M
- QSFP28 100GE to 2 QSFP28 50GE split cable, a.k.a Y-cable, 1M, 2M, 3M
- QSFP28 100GE to 4 SFP28 25GE fanout cable, 1M, 2M, 3M

Figure 38: QSFP28 to QSFP28 100G DAC cable

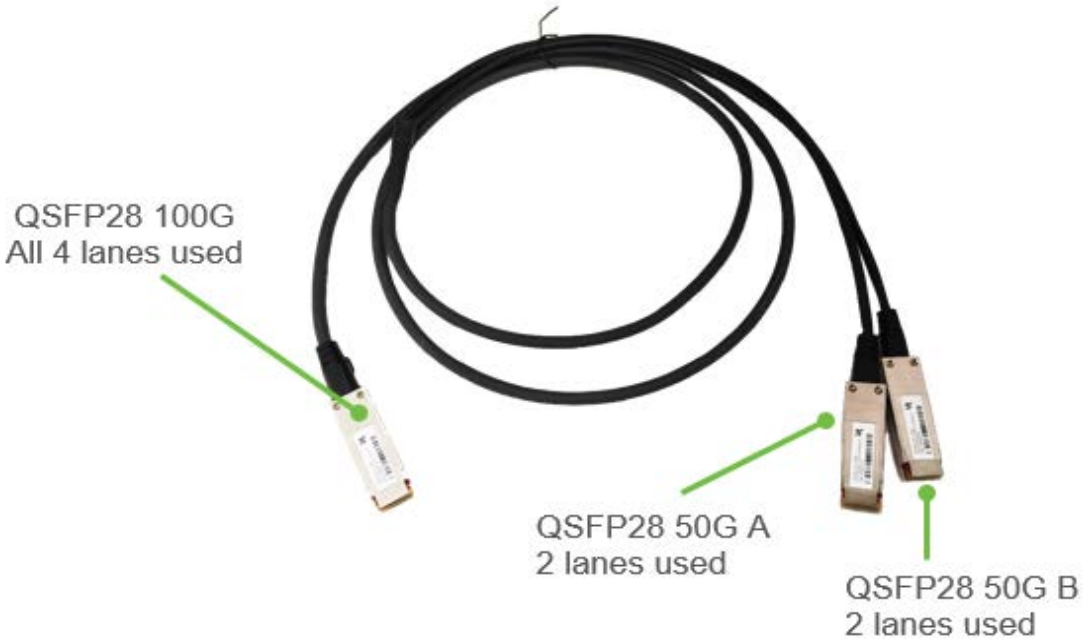

Figure 39: QSFP28 to 2xQSFP28 DAC cable

QSFP28 to 2xQSFP28 cable is facebook proprietary designed cable. It is used to support our 50G NIC, which use two lanes of four lanes inside QSFP28 cable.

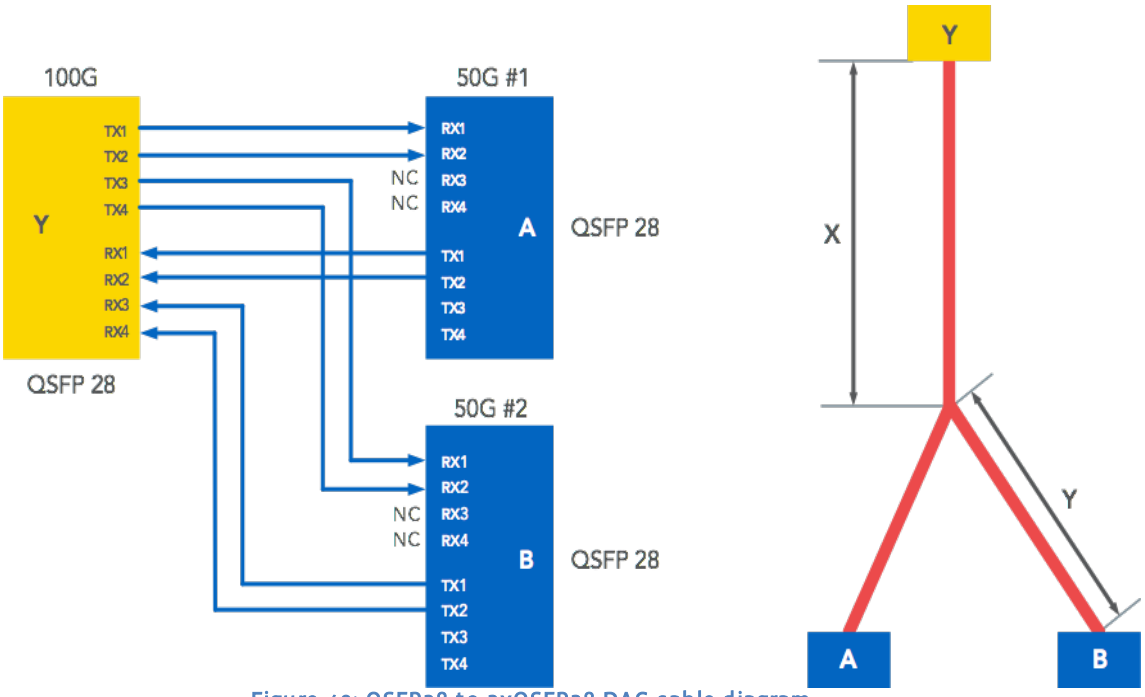

Figure 40: QSFP28 to 2xQSFP28 DAC cable diagram

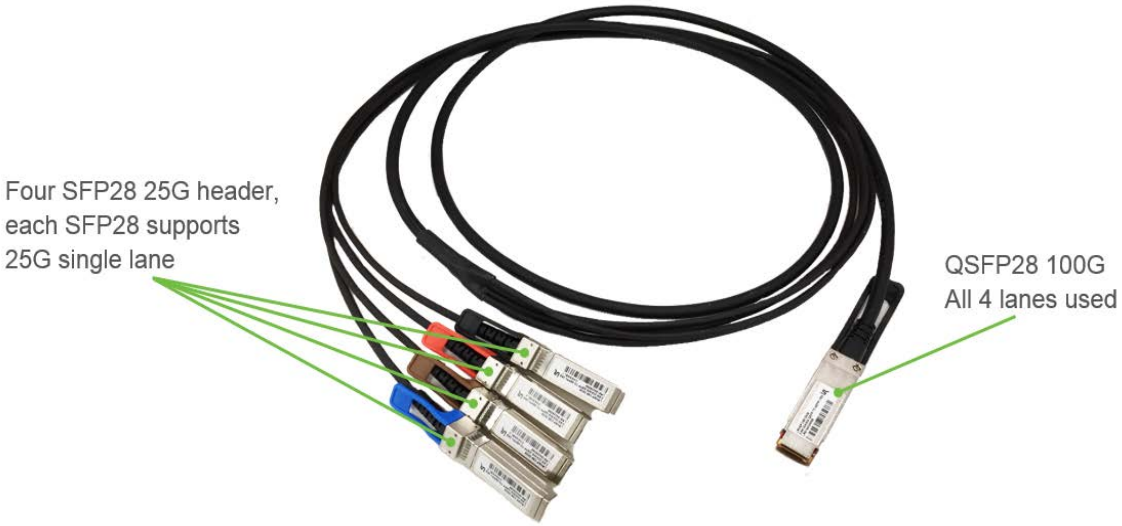

Figure 41: QSFP28 to 4 x SFP28 Fanout DAC cable

14. Environmental Requirements and Reliability

14.1. Environmental Requirements

The wedge-100 should support the related system(s) to meet the following environmental requirements:

- Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C (long-term storage)
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-rating to 1,000m (3,300 feet)

14.2. Vibration and Shock

The wedge-100 system should support the related system(s) to meet shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) & IEC721-3-(*) Standard & Levels. The testing requirements are listed in **Error! Reference source not found.**.

	Operating	Non-Operating
Vibration	0.5g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave/minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks per each of the three axes	12g, half-sine 11mS, 10 shocks per each of the three axes

Table 26: Vibration and Shock Requirements

14.3. Mean Time between Failures (MTBF) Requirements

The wedge-100 should support the related system(s) to have a minimum calculated MTBF of 300,000 hours at 95% confidence level at 25°C ambient temperature while running at full load.

The system(s) shall meet a demonstrated MTBF of minimum 300,000 hours at 95% confidence level prior to the mass production ramp.

The system(s) shall have a minimum service life of 5 years (24 hours/day, full load, at 35°C ambient temperature).

14.4. Regulations

The wedge-100 system should support the related system(s) to obtain CB reports by the vendor(s). Facebook will need these documents to have rack level CE.

15. Labels and Markings

15.1. PCBA Labels and Markings

Wedge-100 PCBAs shall include the following labels on the component side of the boards. The labels shall not be placed in such a way that may cause them to disrupt the functionality or the airflow path of the system.

Description	Type	Barcode Required?
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Facebook P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol:  The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

Table 27: PCBA Label Requirements

15.2. Chassis Labels and Markings

The wedge-100 chassis shall carry the following adhesive barcoded labels in visible locations where they can be easily scanned during integration. Vendor and Facebook will have an agreement for the label locations.

Description
Vendor P/N, S/N, REV (revision would increment for any approved changes)
Facebook P/N
Date code (industry standard: WEEK/YEAR)
The assembly shall be marked "THIS SIDE UP", "TOP SIDE", "UP ^" or other approved marking in bright, large characters in a color TBD. This printing may be on the PCB itself, or on an installed component such as an air baffle. The label should be clear and easy to read in low light conditions, when viewed from above or below from 2 feet away and at an angle of approximately 60 degrees off horizontal.

Table 28: Chassis Label Requirements

16. Prescribed Materials

16.1. Sustainable Materials

Materials and finishes that reduce the life cycle impact of servers should be used where cost and performance are not compromised. This includes the use of non-hexavalent metal finishes, recycled and recyclable base materials and materials made from renewable resources, with associated material certifications.

Facebook identified plastic alternatives including polypropylene plus natural fiber (PP+NF) compounds that meet functionality requirements while reducing cradle to gate

environmental impact when compared to PC/ABS. GreenGranF023T is one acceptable alternate material. JPSECO also offers a PP+NF material that is acceptable; the model number will be available at a later date. It is strongly preferred that such alternatives are identified and used. If vendor is unable to use this, or a similar alternate material, vendor will provide a list of materials that were considered and why they were not successfully incorporated.

16.2. Disallowed Components

The following components shall not be used in the design of the motherboard: Components disallowed by the European Union's Restriction of Hazardous Substances Directive (RoHS)Trimmers and/or potentiometers Dip switches

16.3. Capacitors and Inductors

The following limitations shall be applied to the use of capacitors:

Only aluminum organic polymer capacitors from high-quality manufacturers are used; they must be rated 105°C All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under worst conditions Tantalum capacitors are forbidden SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 still allowed when installed far from PCB edge, and with a correct orientation that minimizes risks of cracks) Ceramics material for SMT capacitors must be X7R or better material (COG or NP0 type should be used in critical portions of the design)

Only SMT inductors may be used. The use of through-hole inductors is disallowed.

16.4. Component De-Rating

For all inductors, capacitors and FETs, de-rating analysis should be based on at least 20% de-rating.

17. Appendix

17.1. Appendix: Commonly Used Acronyms

This section provides definitions of acronyms used in the system specifications.

ANSI – American National Standards Institute

BIOS – basic input/output system

BMC – baseboard management controller

CFM – cubic feet per minute (measure of volume flow rate)

CPLD – complex Programmable Logic Device

DCMI – Data Center Manageability Interface

DDR3 – double data rate type 3

DHCP – dynamic host configuration protocol

DIMM – dual inline memory module

DPC - DIMMs per memory channel

DRAM – dynamic random access memory

ECC – error-correcting code

EEPROM - electrically erasable programmable read-only memory

EMI – electromagnetic interference

FRU – field replaceable unit

GPIO – general purpose input output

I²C – inter-integrated circuit

IPMI – intelligent plattform management interface

LPC – low pin count

MAC – media access control

MTBF – mean time between failures

MUX – multiplexer

NIC – network interface card

OOB – out of band

ORv1 – Open Rack Version One

ORv2 – Open Rack Version Two

OU – Open Compute Rack Unit (48mm)

PCB – printed circuit board

PCIe – peripheral component interconnect express

PCH – platform control hub

POST – power-on self-test

PSU – power supply unit

PWM – pulse-width modulation

PXE – preboot execution environment

QSFP – Quad small form-factor pluggable

QSFP28 – Quad small form-factor pluggable for 4x28Gbps.

RU – rack unit (1.75")

SAS – serial-attached small computer system interface (SCSI)

SATA – serial AT attachment

SCK – serial clock

SDA – serial data signal

SDR – sensor data record

SFP - small form-factor pluggable

SMBUS – systems management bus

TOR – top of rack

TPM – trusted platform module

COM-e: COM express Module