Edgecore AS7315-27X

Disaggregated Cell Site Gateway (DCSG) Specification

Revision 1.0

OPEN Compute Project

Revision History

Revision	Date	Author	Description
1.0	9/25/2019	Jeff Catlin	Initial OCP Release

Contents

Revision History 2
Licenses 5
Scope 7
Overview 7
Environmental 7
Stacking support 7
Timing support 8
Alarm port 8
Switch Silicon 8
CPU Module 8
Physical Overview 8
Front View 8
Rear View 8
Dimensions 9
Top View 9
Front View Detail 9
Front Panel LEDs 10
System LEDs 11
Console Port 12
System Overview: 13
Main PCB Block Diagram 13
CPU Module block diagram 14
PCB Board Set 14
PCB Dimensions 15
Main board PCB Dimension 15
Backplane PCB 16
Connection PCB 16
Fan PCB 17

Placement 18
Main board: 18
Connection board: 20
Backplane board: 21
FAN board: 21
Mechanical 22
Placement 23
Cooling Method 23
Fan module 23
Power Supplies 26
Pinout&DC inlet connector 27
MISC 28
Push Button 28
Cable 29
GPS Module to Main Board 30
I2C Diagram 31
BCM88470 Serdes Mapping 32
System CPLDs and FPGA 34
Specifications and Standards 35
Software Support 37
BIOS support 37
ONIE 37
Open Network Linux 37

Licenses

All semiconductor devices that may be referred to in this specification, or required to manufacture products described in this specification, will be considered referenced only, and no intellectual property rights embodied in or covering such semiconductor devices shall be licensed as a result of this specification or such references. Notwithstanding anything to the contrary in the CLA, the licenses set forth therein do not apply to the intellectual property rights included in or related to the semi-conductor devices identifies in the specification. These references include without limitation the reference to devices listed below. For clarity, no patent claim that reads on such semiconductor devices will be considered a "Granted Claim" under the applicable Contributor License Agreement for this specification

Feature	AS7315-27X
CPU sub-system	CPU: Intel ® Atom™ Processor C3508,1.6GHZ DDR SDRAM: 8GB x 2 2400MHz with ECC (SO-DIMM) DDR4 SPI Flash (Boot): 16MB x 2 M.2 SSD: 32GB MLC TPM: SLB 9665XT2.0 FW5.63 INFINEON
Management	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45), Alarm port on fantray (RJ45).
Timing	GNSS GPS Receiver(SMB), Stack Sync (RJ45), 1GE Stack (RJ45), BITS (RJ45), TOD PPS (RJ45)
MAC	BroadcomBCM88470, 300Gbsfull duplex switching
Ethernet Ports	3x100GE QSFP28 (two support stacking), 4x1/10/25G SFP28 and 20x1/10G SFP+
CPLD	Altera 5M2210ZF324I5N (FBGA324) and 5M1270ZF256I5 (FBGA256)
FPGA	Altera EP4CGX30CF23I7N
PCB	20-Layers, EM891Kfor Mainboard 14-Layers,CPU module 8-Layers,TG 150 Power Connection Board 4-Layers, TG 150 FAN Board 4-Layers, TG 150Backplane Board
Power Supply	Max 300W PSU, DC to DC, 1+1 redundant load-sharing, hot-swappable Notes: The airflow is left to right (PSU side is inlet) from chassis system view.
Cooling	5 fan-tray modules with 5 pcs of 40mm x40mm x 28mm 12V fans, hot-swappable
Dimension	L(Depth):299.8±0.5mm(11.8031±0.0196inch) x W(Width):438.4±0.5mm(17.259808 ± 0.0196 inch) x H(Height):43.25±0.5 mm(1.7027±0.0196inch)

As of September 25, 2019, this specification is contributed under the OCP Contributor Licensing Agreement (OCP-CLA) by the following entities:
Acton Technology Corporation, through its subsidiary Edgecore Networks Corporation

Limitations of the OCP CLA license are noted below:
No Limitations

You can review the signed copies of the OCP-CLA for this specification on the OCP website. http://www.opencompute.org/products/specsanddesign
Usage of this specification is governed by the OCPHL permissive. You can review this license at http://www.opencompute.org/participate/legal-documents/

Your use of this Specification may be subject to other third-party rights. THIS SPECIFICATION IS PROVIDED "AS IS." The contributors expressly disclaim any warranties (express, implied, or otherwise), including implied warranties of merchantability, non-infringement, fitness for a particular purpose, or title, related to the Specification. The entire risk as to implementing or otherwise using the Specification is assumed by the Specification implementer and user. IN NO EVENT WILL ANY PARTY BE LIABLE TO ANY OTHER PARTY FOR LOST PROFITS OR ANY FORM OF INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION OR ITS GOVERNING AGREEMENT, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.
.

Scope

This document outlines the technical specifications for the Edgecore AS7315-27X Disaggregated Cell Site Gateway (DCSG) Platform submitted to the Open Compute Project (OCP).

Overview

This document describes the technical specifications of the AS7315-27X Disaggregated Cell Site Gateway designed by Edgecore Networks Corporation. The AS7315-27X is a cost optimized design focused on the aggregation of 10G/25G cellular equipment and providing 100G backhaul connections. AS7315-27X supports a broad set of IEEE 1588 /SyncE features geared towards 4G and 5G timing needs. The AS7515-27X can support "Stacking" of units in order to provide a larger Disaggregated Cell Site Gateway with additional networking interfaces (Dependent on Network Operating System support).

The AS7315-27X supports twenty seven network ports as follows:

- Twenty SFP+ ports capable of 1G/10G operation
- Four SFP28 ports capable of 1G/10G/25G operation
- Three QSFP28 ports capable of 1G/10G/25G/100G operation

The AS7315-27X is a PHY-Less design with the network interface connections directly attaching to the Serdes interfaces of the Broadcom BCM88470 switching silicon providing the lowest cost, latency, and power. The AS7315-27X supports traditional features found in Carrier class switches such as:

- Field replaceable redundant AC or DC power supplies
- Field replaceable fan module with redundant fans
- Support for "Side to Side " air flow direction
- Support a modular CPU card that allows flexibility in the CPU and/or memory configurations that can be offered.
- A full set of SyncE/1588 functions

Environmental

The AS7315-27X is designed for outside plant deployments in non-temperature controlled environments. The AS7315-27X supports deployment in operational environments ranging in temperature from -40C to +65C.

Stacking support

The AS7315-27X provides the connections that are needed in order to support stacking of units together to form one larger system. These stacking connections are as follows:

- TwoQSFP28 100G stacking ports for carrying user traffic between units. If stacking is not required these ports can be used a standard QSFP28 100G network connections
- Stack Sync RJ45 port which carries timing information between the FPGA(s) in the timing circuits of the AS7315-27X units
- Stack Control RJ45 which carries Ethernet connectivity between the master and slave AS7315-27X units, this can be used to synchronize and manage the two timing control logic on the COMe CPU modules of the stacked AS7315-27X

Timing support

The AS7315-27X supports a wide range of SyncE/1588 support including Grand Master, Boundary , Ordinary, and Transparent Clock support. The AS7315-27X supports timing ports such as BITS, TOD, SMA connector for GPS input, and a "Stack Sync" RJ45 port that carriers timing information between the two timing circuits of two different AS7315-27X units in a stacked configuration.

Alarm port

A RJ45 Alarm port is provided on the system fan module. This interface connects to the Fan CPLD which is on the fan tray backplane. This Alarm RJ45 can be used to control a relay switch outside of the AS7315-27X system, and also used to feed in 4x monitoring signals (these can be for example thermal sensor readings). The AS7315 system will have comparators to monitor these 4 inputs and the CPLD can then control the relay switch control to turn control, for example, a fan unit inside the cabinet.

Switch Silicon

The AS7316-27X utilizes the Broadcom BCM88470 "Qumran-AX" switching silicon. This solution provides support for deep routing tables, large number of virtual output queues for QOS, and external expandable packet buffering. The AS7315-27X is populated 6GB of external packet buffering supported by the BCM88470

CPU Module

The AS7315-27X supports a COM Express Type 7 CPU module. The CPU module chosen for the AS7315-27X is the Portwell PCOM-B702G. This is a Type 7 COM Express basic (95mm x 95mm) module and is designed with an Intel® Atom® processor product family known as Denverton.

Physical Overview

Front View

Rear View

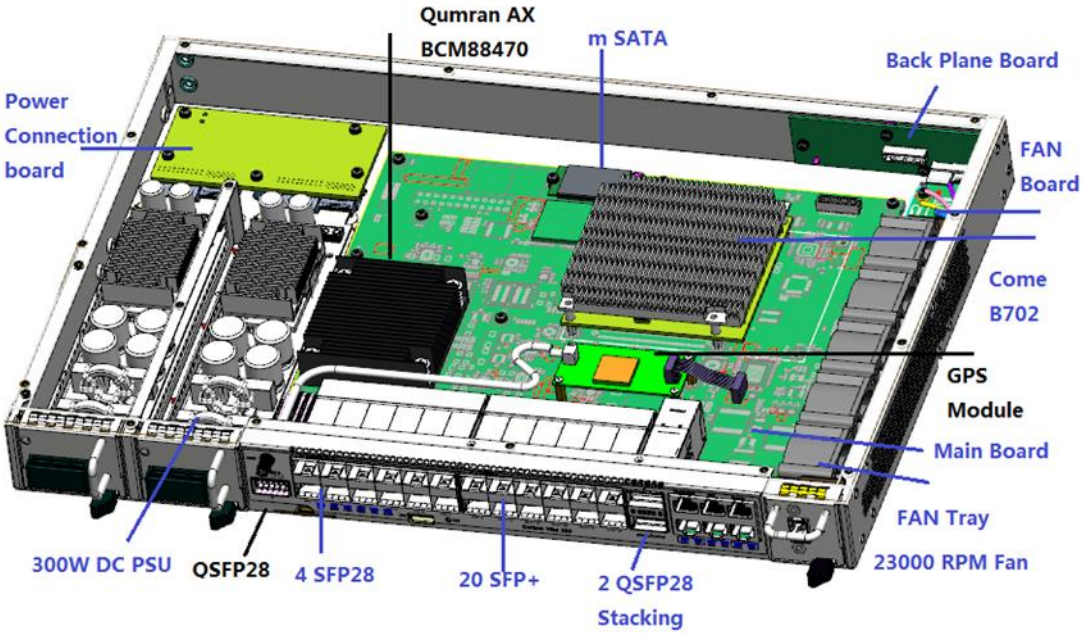
The rear view of AS7315-27X includes the following key components:

- Chassis Grounding Location

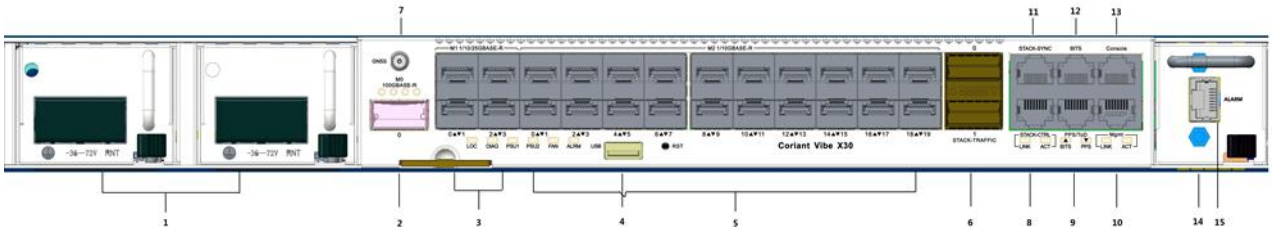
Dimensions

	Inches	Millimeters
Length (depth)	11.8031±0.0196inch	299.8±0.5mm
Width	17.259808 ± 0.0196 inch	438.4±0.5mm
Height	1.7027±0.0196inch	43.25±0.5 mm

Top View



Front View Detail



The front panel view of AS7315-27X includes the following key components:

Description	
1- Power Supply	9- PPS-Tod RJ45 port
2-100 Gigabit Ethernet QSFP28 ports	10- Management Ethernet port (**MGMT**)

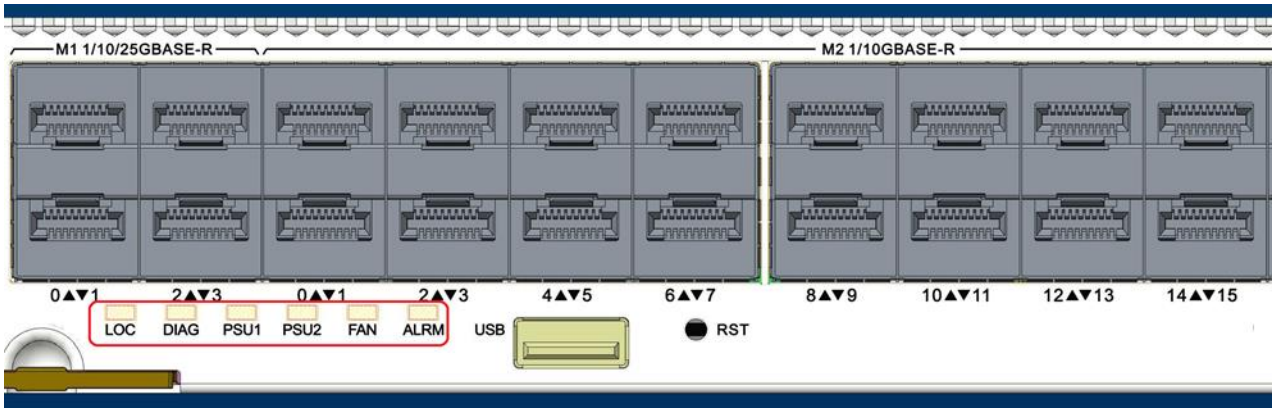
3-25 Gigabit Ethernet SFP28 ports	11- Stack-Sync RJ45port
4-USB storage port	12- Building-Integrated Timing System port (**BITS**)
5-10 Gigabit Ethernet SFP+ ports	13-RJ45 console port
6-100 Gigabit Stacking QSFP28 ports	14-Fan Tray
7- GPS antenna port	15-Alarm RJ45 port
8-Stack-CtrlRJ45 port	

Front Panel LEDs

LED	CONDITION	STATUS
SFP+ Port LED (Port00 to Port19)	On/Flashing Green	SFP+ port has a valid activity at 10G mode and the flashing to indicate activity.
	On/Flashing Amber	SFP+ port has a valid activity at 1G mode and the flashing to indicate activity.
	Off	There is no link on the port.
SFP28 Port LED (Port00 to Port03)	On/Flashing Blue	SFP28 port has a valid activity at 25G mode and the flashing to indicate activity.
	On/Flashing Green	SFP28 port has a valid activity at 10G mode and the flashing to indicate activity.
	Off	There is no link on the port.
QSFP28 Traffic Port LED in 40G/100G Mode.	On/Flashing Green	QSFP28 port has a valid activity at 100G mode and the flashing to indicate activity.
	On/Flashing Blue	QSFP28 port has a valid activity at 40 G mode and the flashing to indicate activity.
	Off	There is no link on the port.
QSFP28 Traffic Port LED in 25G Fan Out Mode. (With Breakout cable)	On/Flashing Amber	QSFP28 port has a valid link at 25G via break out cable. The LED on 100G QSFP28 end is also present OFF. Flashing indicates activity.
	Off	There is no link on the port.
QSFP28 Traffic Port LED in 10G Fan Out Mode. (With Breakout cable)	On/Flashing Purple	QSFP28 port has a valid link at 10G via break out cable. The LED on 40G QSFP28 end is also present OFF. Flashing indicates activity.
	Off	There is no link on the port.
QSFP28 Stacking Port LED in 40G/100G Mode.	On/Flashing Green	QSFP28 port has a valid activity at 100G mode and the flashing to indicate activity.
	On/Flashing Blue	QSFP28 port has a valid activity at 40 G mode and the flashing to indicate activity.
	Off	There is no link on the port.

OOB Port LED (Link)	On / Green	Port has a valid link
	Off	There is no link on the port
OOB Port LED (Activity)	Flashing / Green	Flashing indicates activity
	Off	There is no link on the port
ToD Status LED	On/Flashing Green	ToD port has activity and the flashing to indicate activity.
	Off	There is no link on the port
BITS Status LED	On/Flashing Green	Bits port has activity and the flashing to indicate activity.
	Off	There is no link on the port
STACK-CTRL Port LED(Link)	On / Green	Port has a valid link
	Off	There is no link on the port
STACK-CTRL Port LED(Activity)	Flashing / Green	Flashing indicates activity
	Off	There is no link on the port

System LEDs



LABEL	COLOR	DESCRIPTION
PSU1 (Power Supply Status)	Green	This power is operating normally.
	Orange	PWR present but not power on or this power is fault.
	Off	Power supply not present.
PSU2 (Power Supply Status)	Green	This power is operating normally.
	Orange	PWR present but not power on or this power is fault.
	Off	Power supply not present.
DIAG (Diagnostic)	Green	System self-diagnostic test successfully completed.
	Green Blink	System self-diagnostic test is in progress

	Orange	System self-diagnostic test has detected a fault.
FAN	Green	System FAN operating normally.
	Green Blink	System FAN tray is power off when ambient temperature is less than 10 degree C.
	Orange	System FAN tray present but is fault.
ALRM	Green	System Alrm port operating normally.
	Red	System Alrm port is fault.
LOC	Blue Flashing	Flashing by remote management command. Assists the technician in finding the right device for service in the rack.
	OFF	Not a particular switch that technician need to find

Console Port

The console port interface conforms to the RJ45 electrical specification.

The interface supports asynchronous mode with default eight data bits, one stop bit, and no parity.

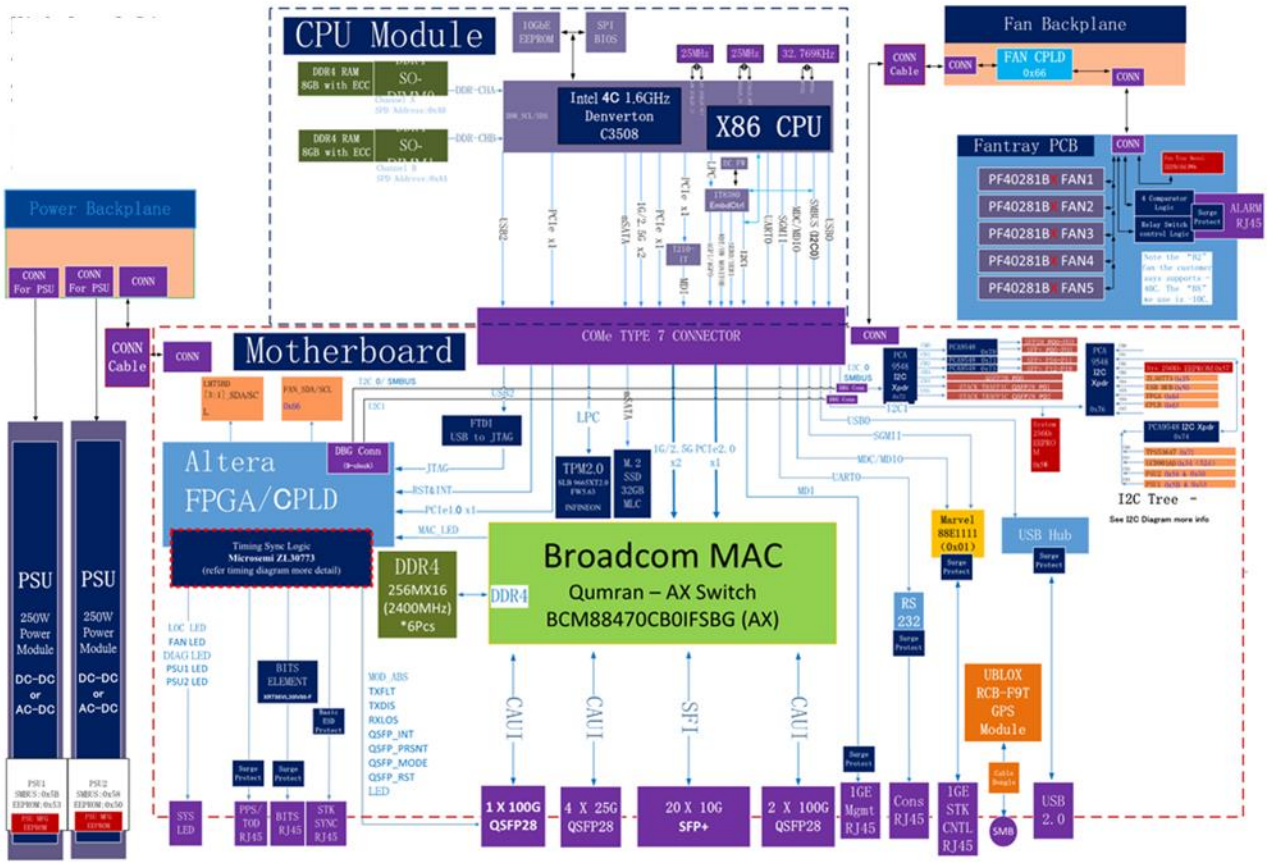
The unit will operate at any one of the following baud rates:

- 9600, 19200, 38400, 57600, **115200 (Default)**

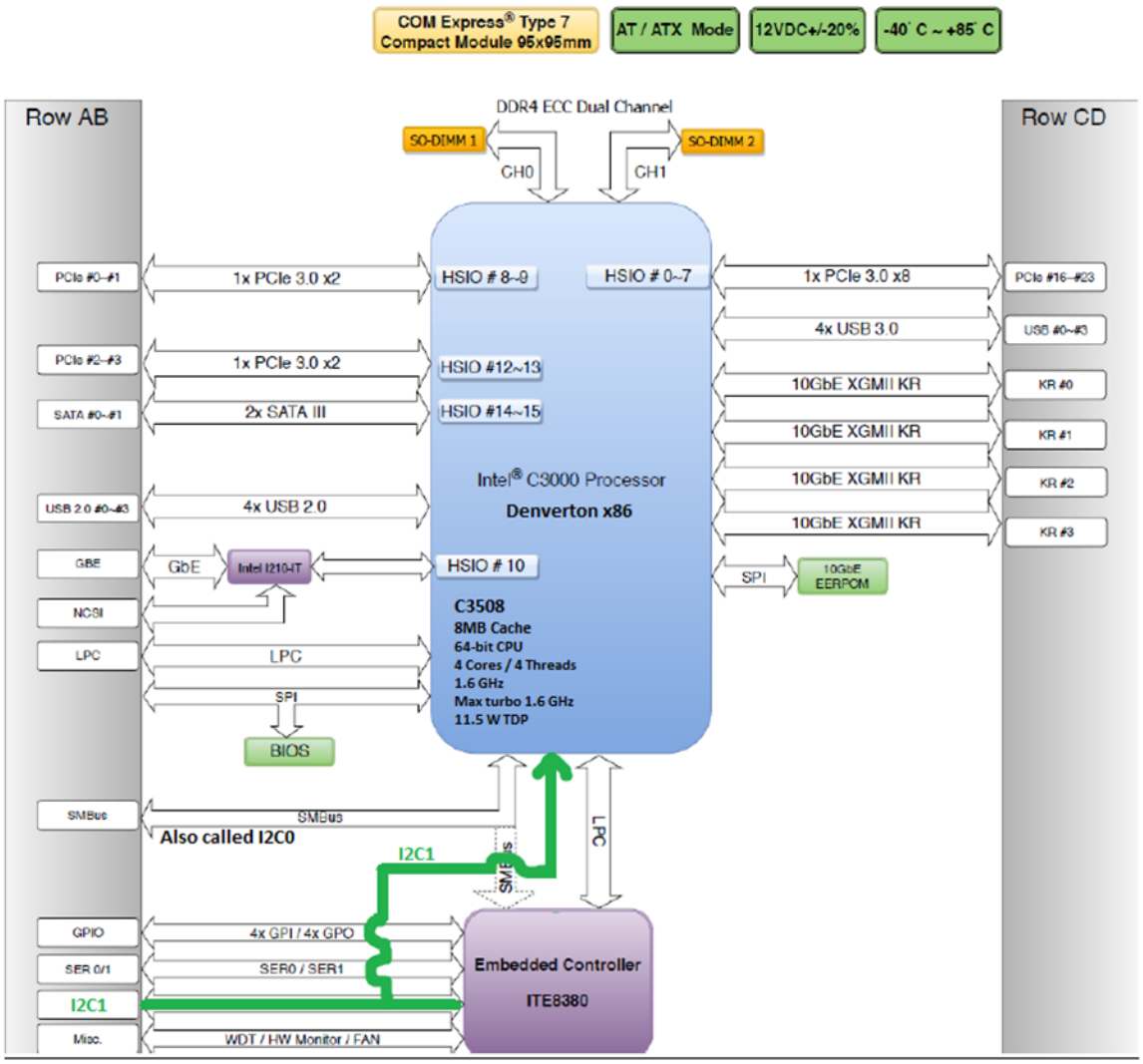
Pin number	Pin name	Pin number	Pin name
1	RTS	**2**	UART_TXD
3		**4**	
5	GND	**6**	UART_RxD
7		**8**	CTS

System Overview:

Main PCB Block Diagram



CPU Module block diagram



PCB Board Set

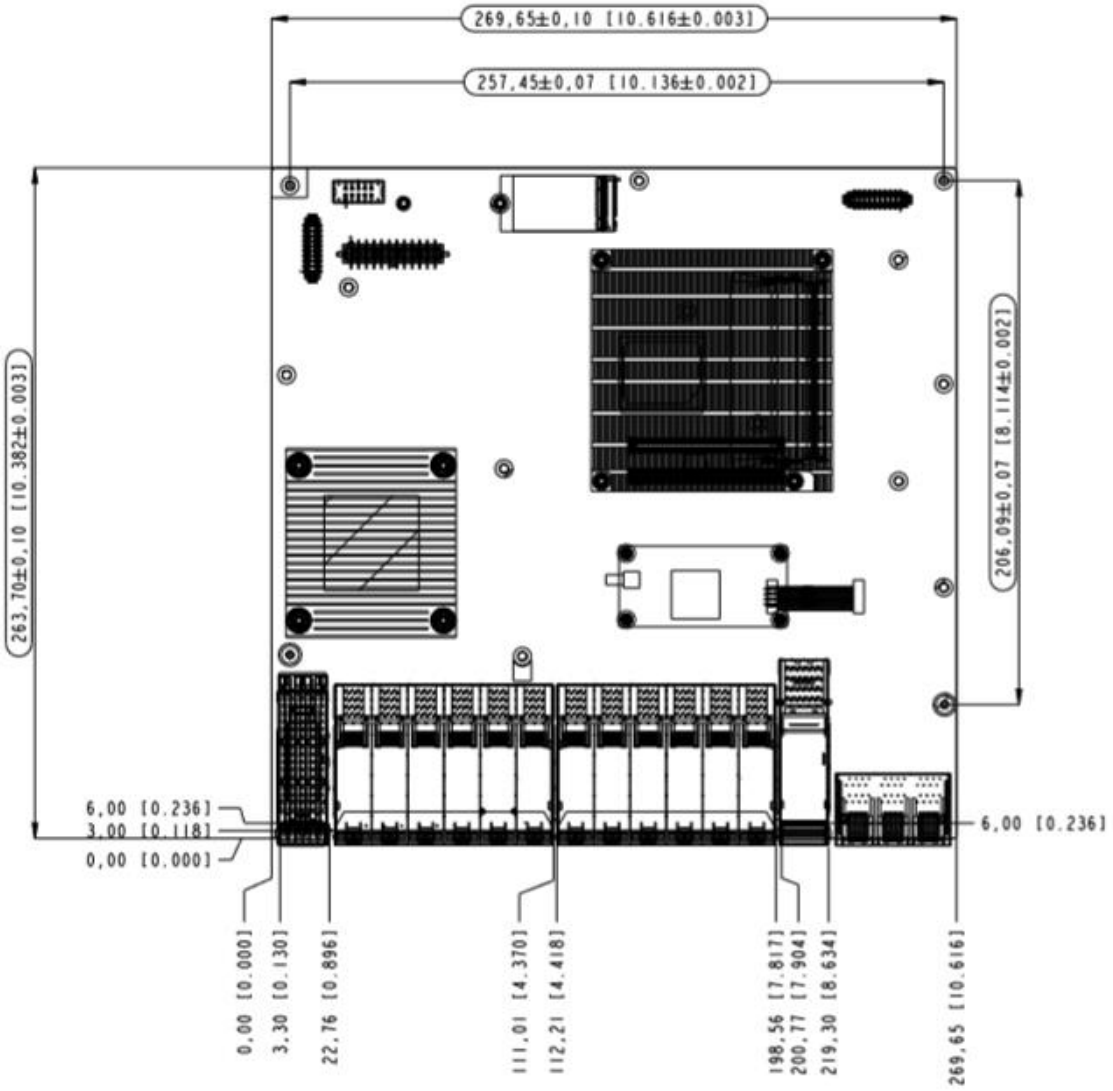
AS7315-27X is composed of five unique PCB assemblies as follows:

- Main switch PCB which supports the switching silicon and all front panel connections
- CPU module PCB (Type 7 Com Express) which provides the control processor and associated components. This CPU module is from Portwell part # PCOM-B702G
- Fan module PCB
- Power connection PCB
- Backplane PCB

PCB Dimensions

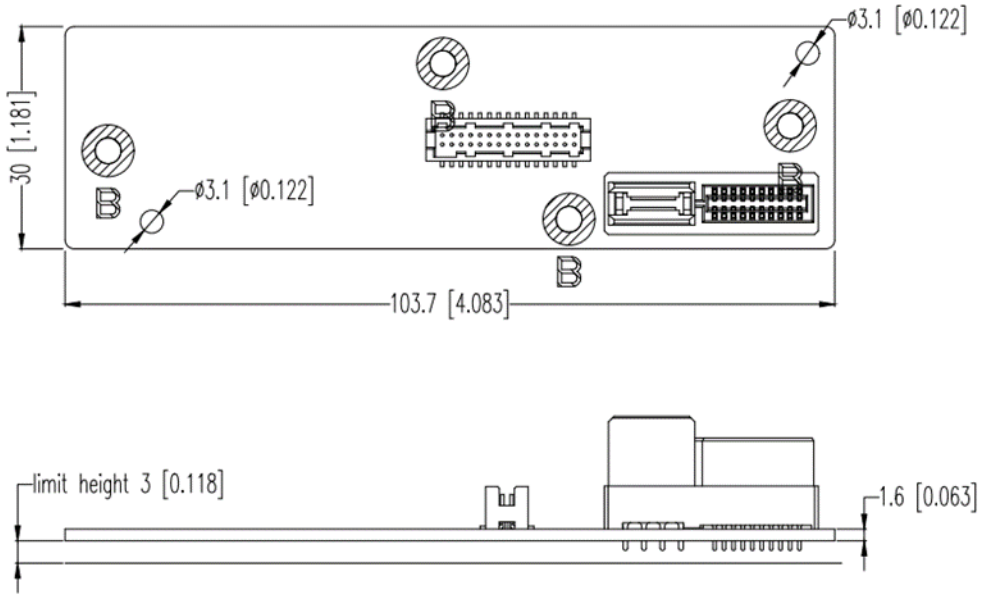
Main board PCB Dimension

Main_L x W = 263.7mm x 269.65mm



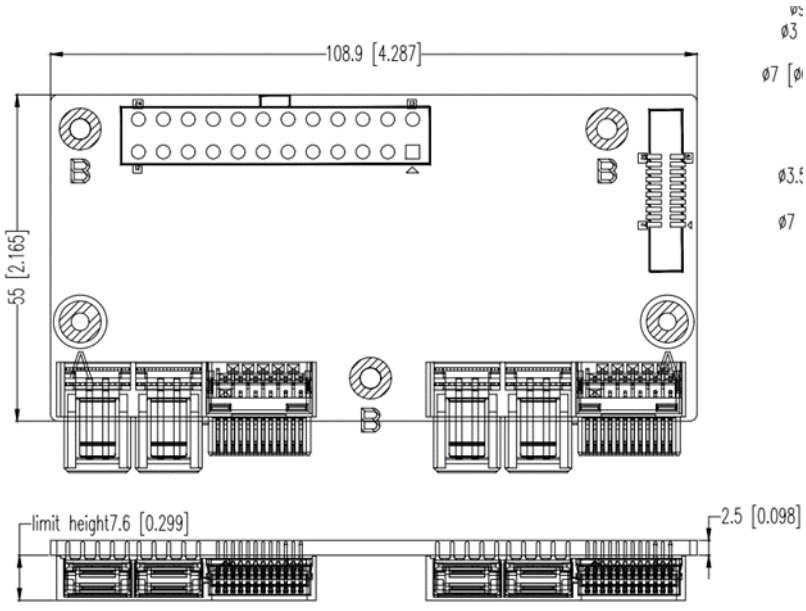
Backplane PCB

Backplane_L x W = 103.7mm x 30mm



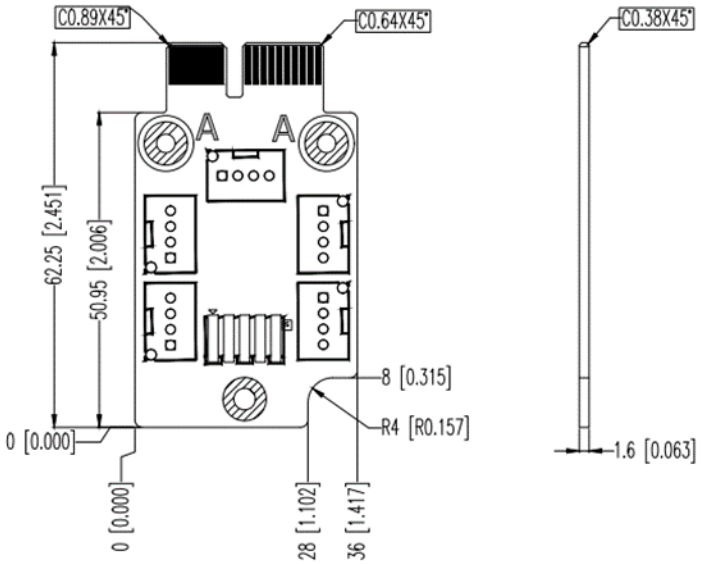
Connection PCB

Connection_L x W = 108.9mm x 55mm



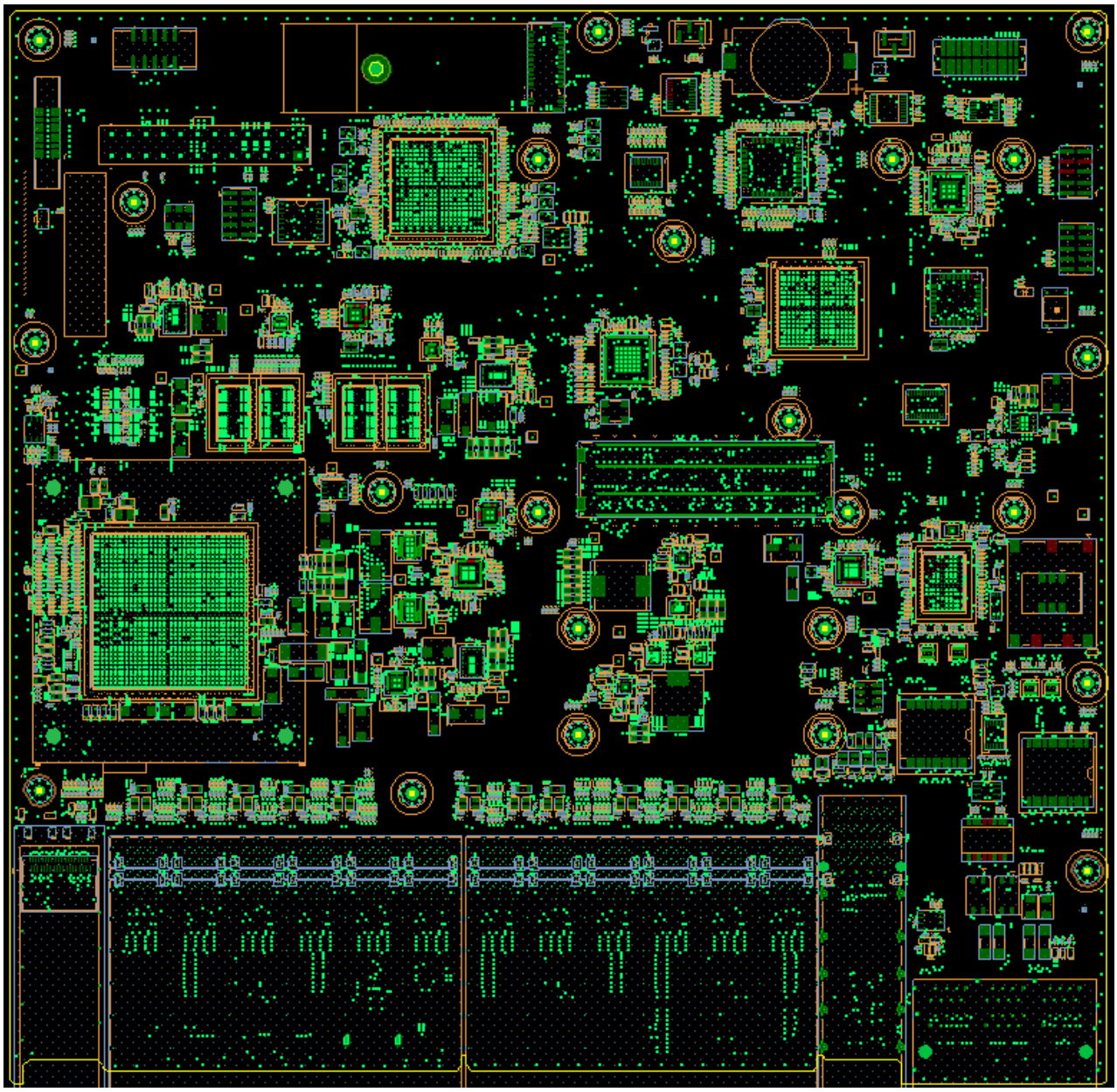
Fan PCB

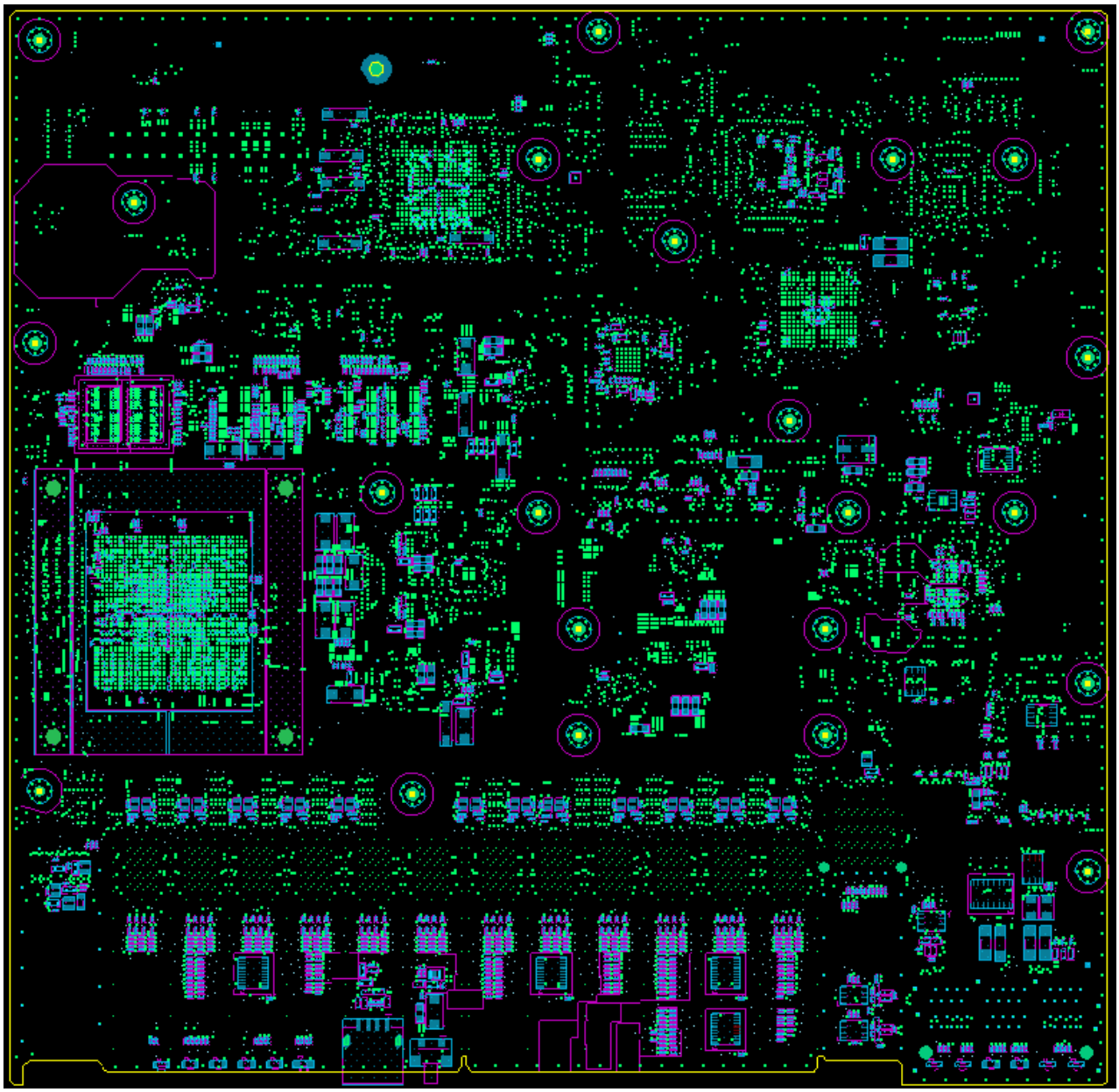
FAN_L x W = 36mm x 62.5mm



Placement

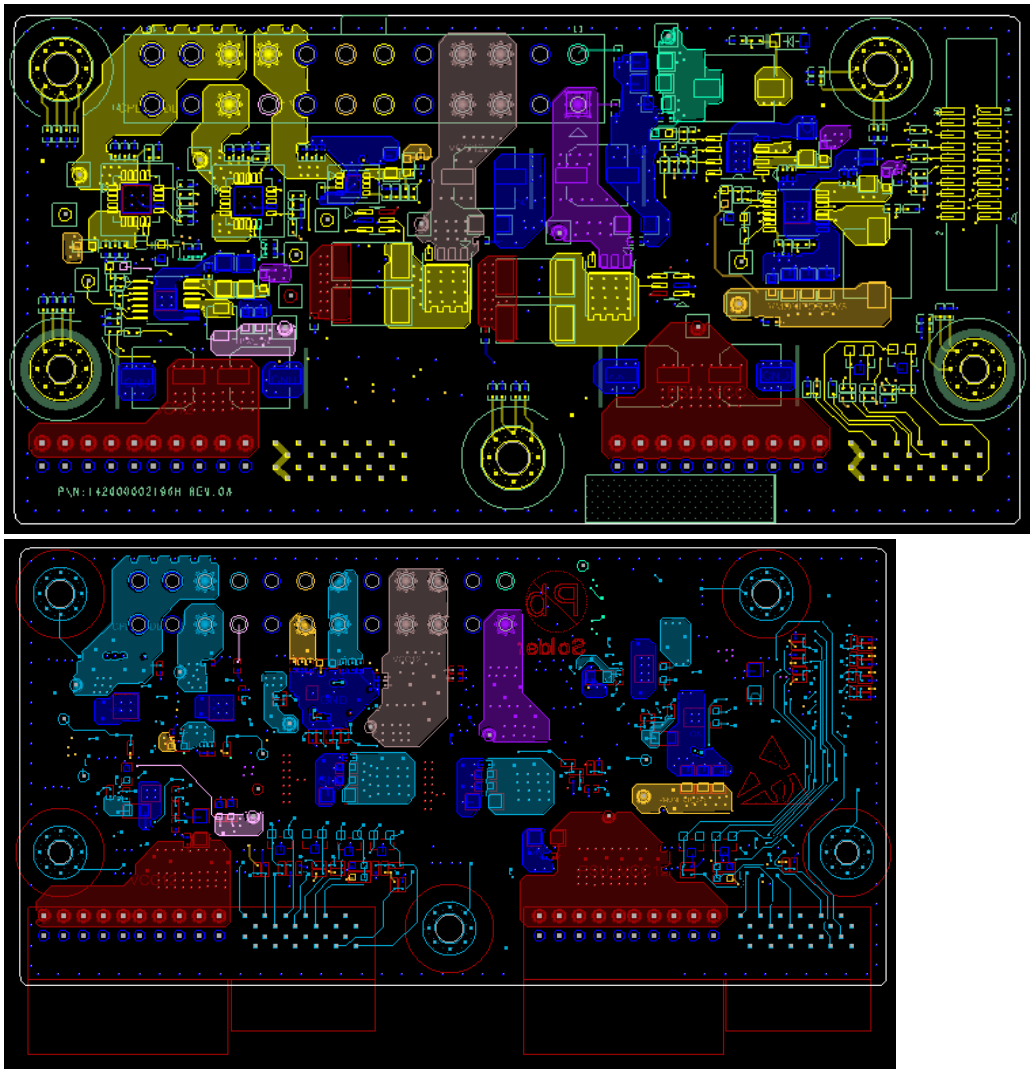
Main board:





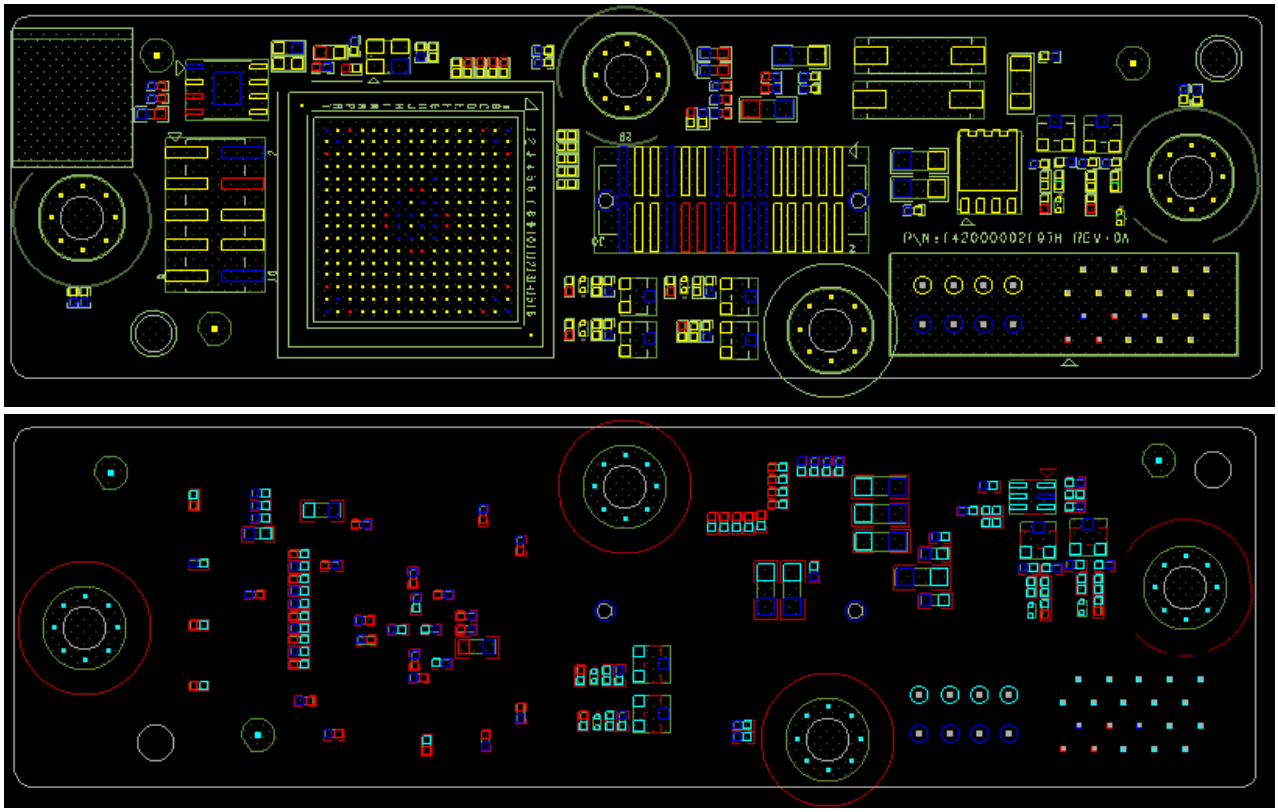
Mainboard TOP/Bottom PCB Placement

Connection board:

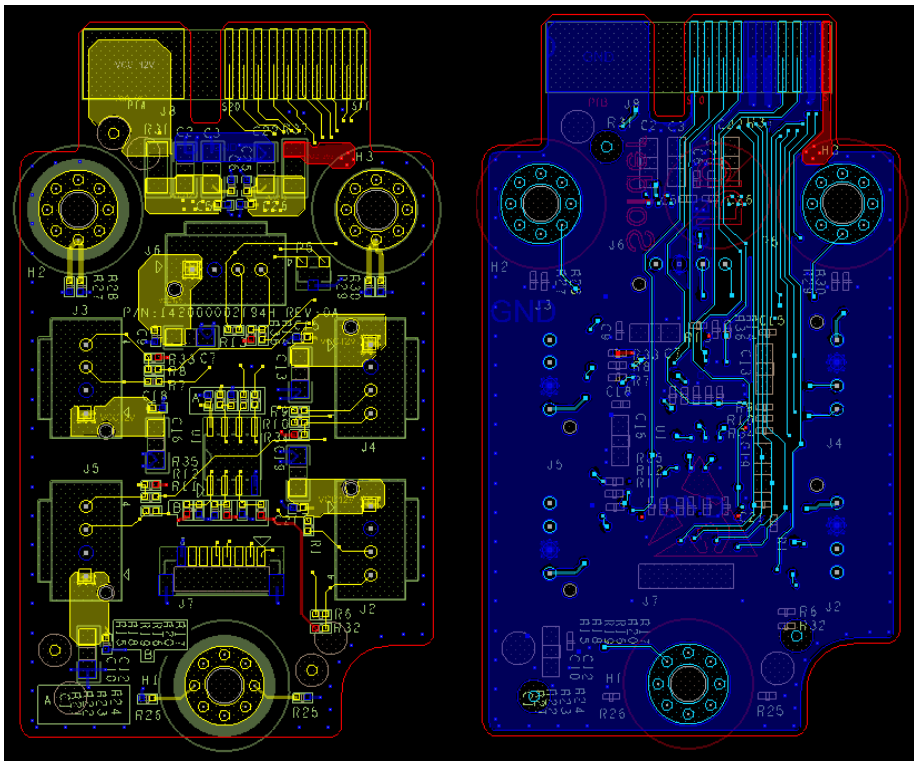


Connection board TOP/Bottom PCB Placement

Backplane board:



FAN board:



FAN board TOP/Bottom PCB Placement

Mechanical

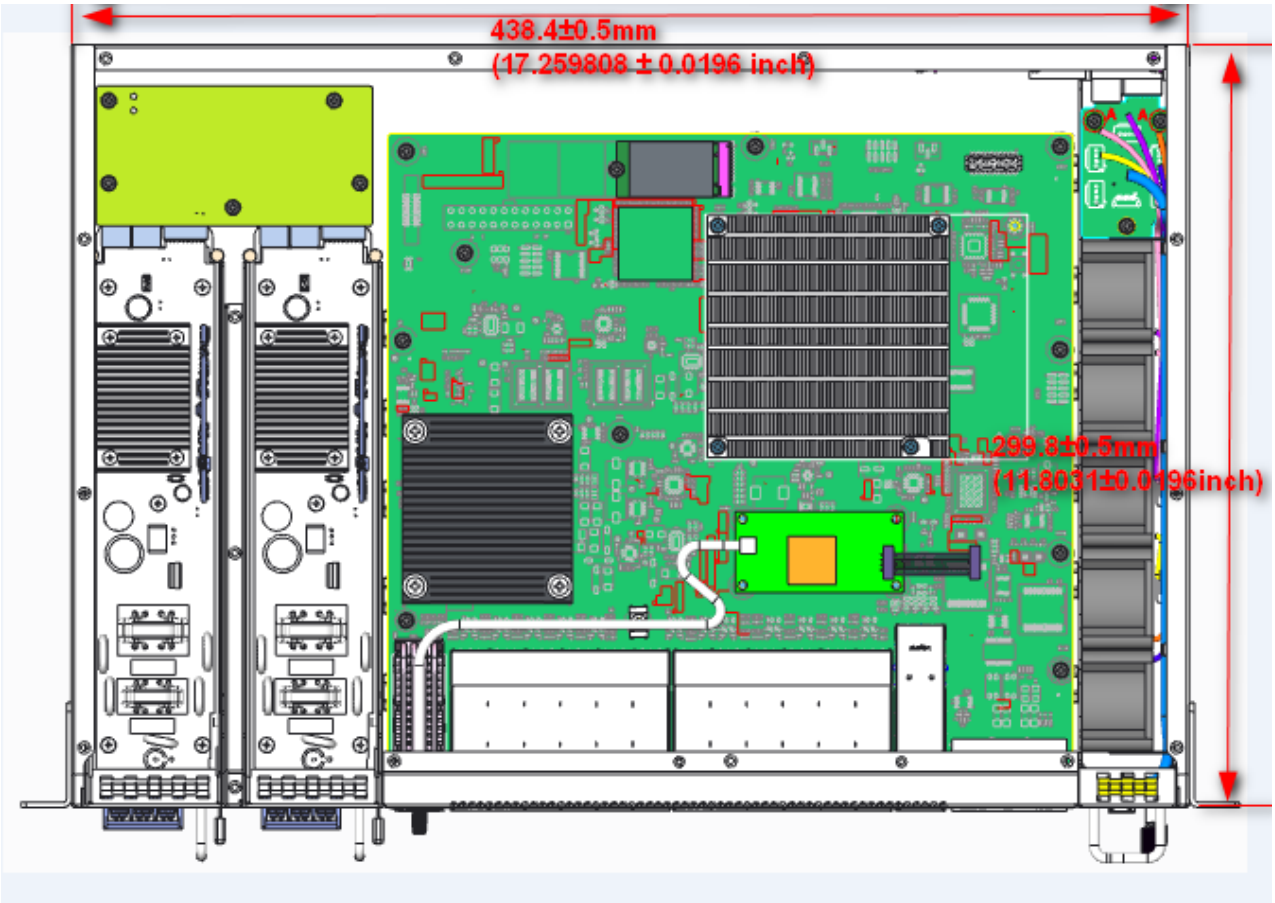
Dimension

The dimension is

Height: 43.25±0.5mm(1.7027±0.0196inch)

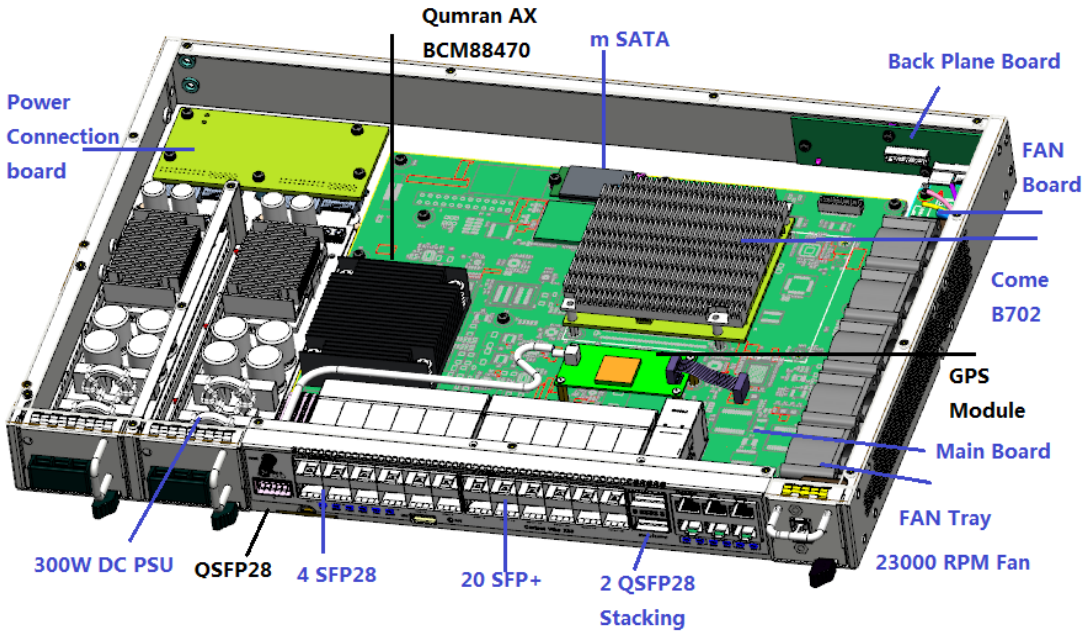
Width: 438.4±0.5mm(17.259808 ± 0.0196 inch)

Depth: 299.8±0.5mm(11.8031±0.0196inch)



Mechanical Dimension

Placement

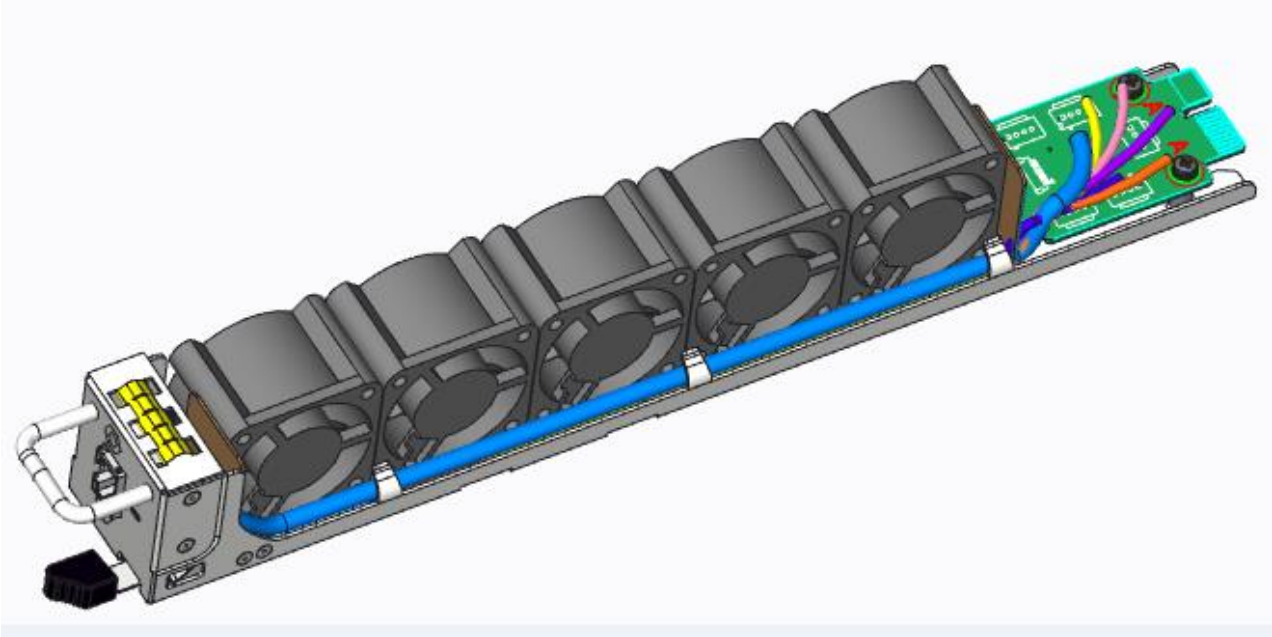


Mechanical Placement

Cooling Method

Fan module

AS7315-27X system supports one fan module with redundant fans. This fan module supports five fans and produces the side to side system airflow



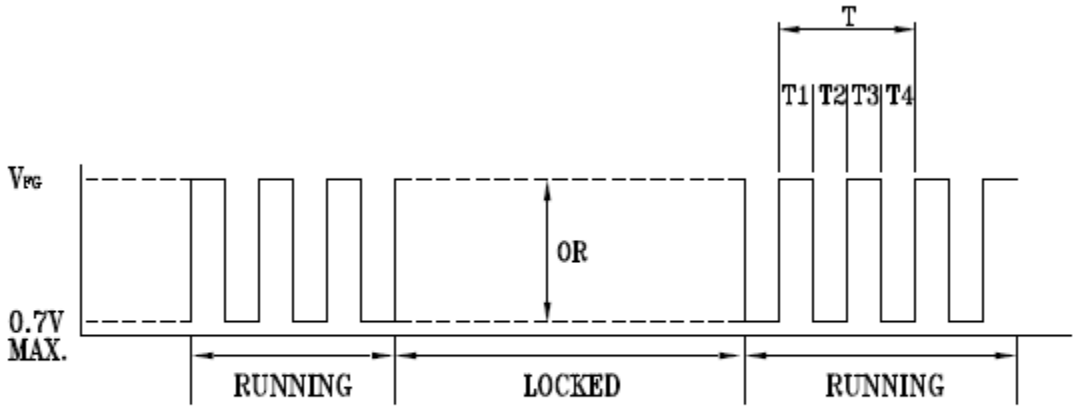
side to side fan tray

(AT Ta=25°C)

ITEM	SPEC.
RATED VOLTAGE	12 VDC
OPERATION VOLTAGE	7.0 ~ 13.2 VDC
RATED CURRENT (IN FREE AIR)	1.2 (1.44 MAX.) A (AVERAGE)
CURRENT ON LABEL	1.50 A
RATED POWER (IN FREE AIR)	14.4 (17.28MAX.) W
SPEED (IN FREE AIR)	23000±10% R.P.M
SPEED CONTROL TYPE	PWM CONTROLLER
SIGNAL OUTPUT	FREQUENCY GENERATOR (FG)
MAX. AIR FLOW (AT ZERO STATIC PRESSURE)	0.885 (0.797 MIN.) M^3/MIN 31.27 (28.14 MIN.) CFM
MAX. AIR PRESSURE (AT ZERO FLOW)	74.76 (60.56 MIN.) mm−H_2O 2.943 (2.384 MIN.) inch−H_2O
ACOUSTICAL NOISE	63.5 (67.5 MAX.) dB−A

FAN characteristics:

FREQUENCY GENERATOR WAVEFORM:

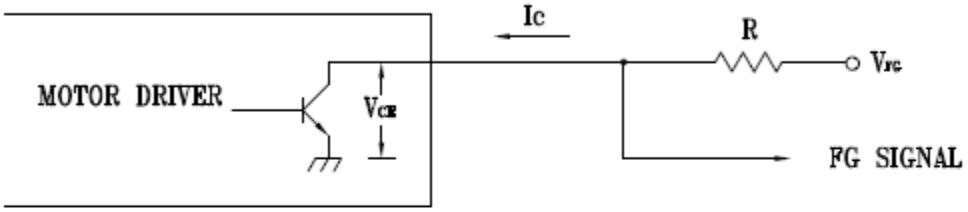


T=T1+T2+T3+T4=60/N (Sec) N: SPEED (RPM)

Fan Speed information

FREQUENCY GENERATOR (FG) SIGNAL

9-1. SCHEMATIC:



CAUTION:

THE LEAD WIRE OF FG SIGNAL CAN NOT TOUCH
THE LEAD WIRE OF POSITIVE OR NEGATIVE.

9-2. SIGNAL SPECIFICATION:

OUTPUT TYPE: OPEN COLLECTOR

V_{FG} MAXIMUM VOLTAGE = 13.2V

V_{FG} MINIMUM VOLTAGE = 2.8V

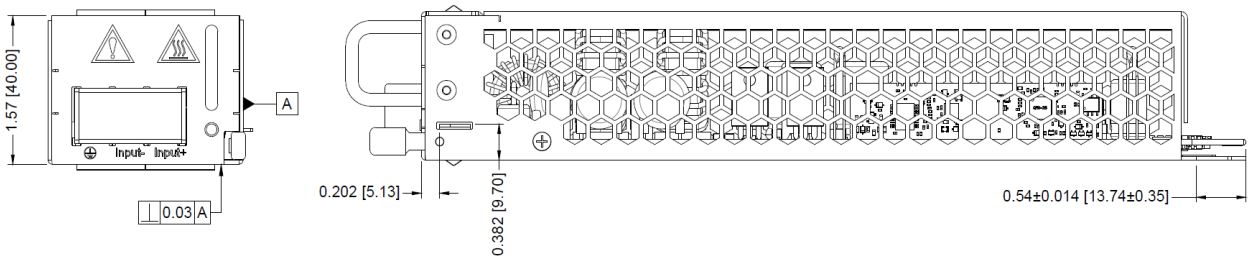
I_C MAXIMUM CURRENT =5mA

LOW LEVEL VOLTAGE = 0.7V MAX.

$R \geq V_{FG} / I_C$

Power Supplies

The AS7315-27X supports two redundant power supply modules. Power supply modules are offered that support AC input power or DC input power and both variants support 300W output power (each supply). If one unit fails or is replaced, the other unit can take over and can provide enough power to keep the AS7315 up and running.



PSU Dimension

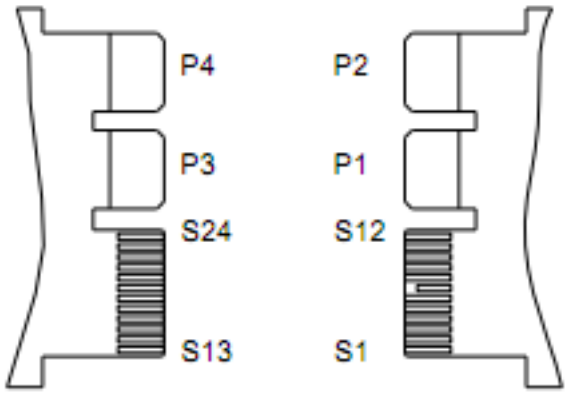
- **Model Number:** CRXT-T0T12AG
- **Vendor:** Bel
- **Input Voltage:** 36V to 72V DC
- **Output Voltage:** 12V
- **Max Output Current:** 25A
- **Max Power:** 300W
- **Typical Efficiency:**90%
- **Airflow Direction:** side to side

Pinout&DC inlet connector

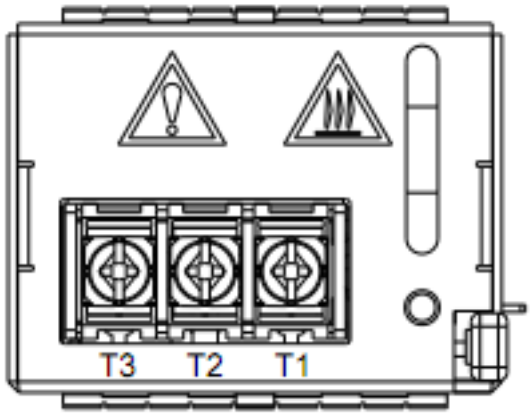
The power module pin definition is as below.

MECHANICAL DIMENSIONS(CONTINUED)

PIN DEFINITIONS



TOP VIEW BOTTOM VIEW



SIDE VIEW

PIN NO.	Condition
S1	NC
S2	NC
S3	NC
S4	Alert
S5	SDA
S6	SCL
S7	PS-KILL_H
S8	PS_ON_L
S9	PW_OK_H
S10	A1
S11	NC
S12	NC
S13	NC
S14	Present_L
S15	A0
S16	NC
S17	NC
S18	NC
S19	NC
S20	NC
S21	NC
S22	NC
S23	NC
S24	NC
P1	+12V
P2	+12V
P3	GND
P4	GND

PIN NO.	Condition
T1	Input+(+48V)
T2	Input-(RTN)
T3	Earth

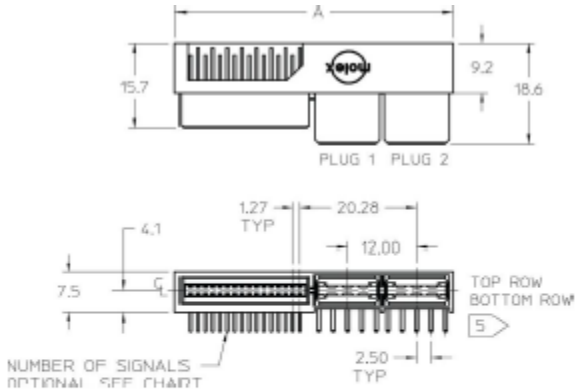


Figure 3 – PDB Mating Connector

Pin Assignment:

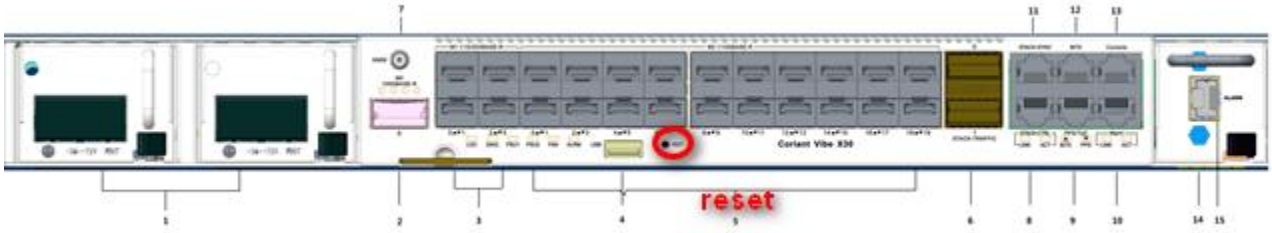
- **P1~4：Power Circuits**
- **S1 ~ S24：Signal Circuits**

MISC

Push Button

Main board has two Push Button, one shows front panel for manual H/W reset function used. This button is “recessed” and reset whole system. The system will restart.

The other one is for R&D debug purpose, and it connects to power monitor IC. The power sequence will restart when press this, and system will restart.



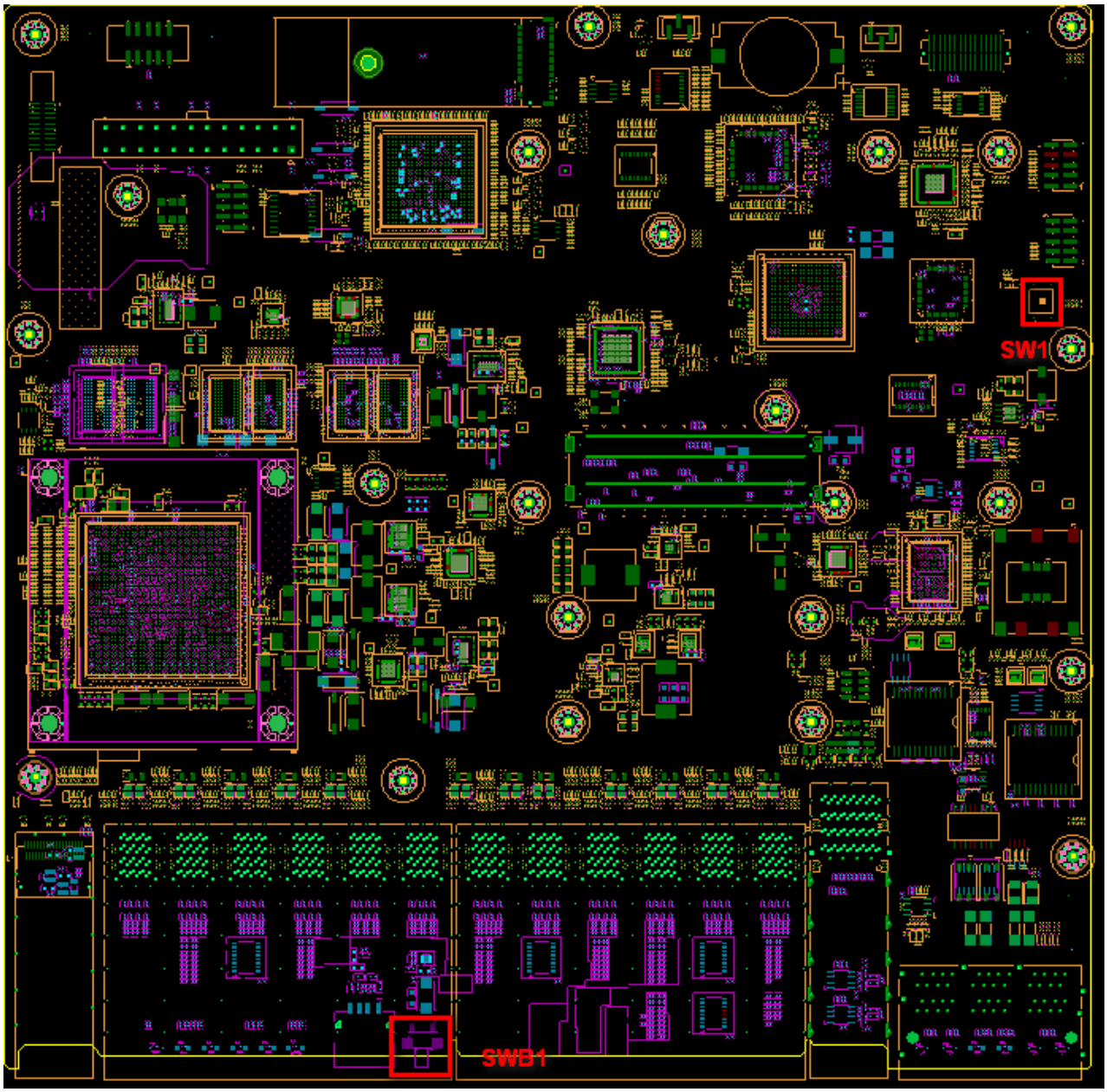
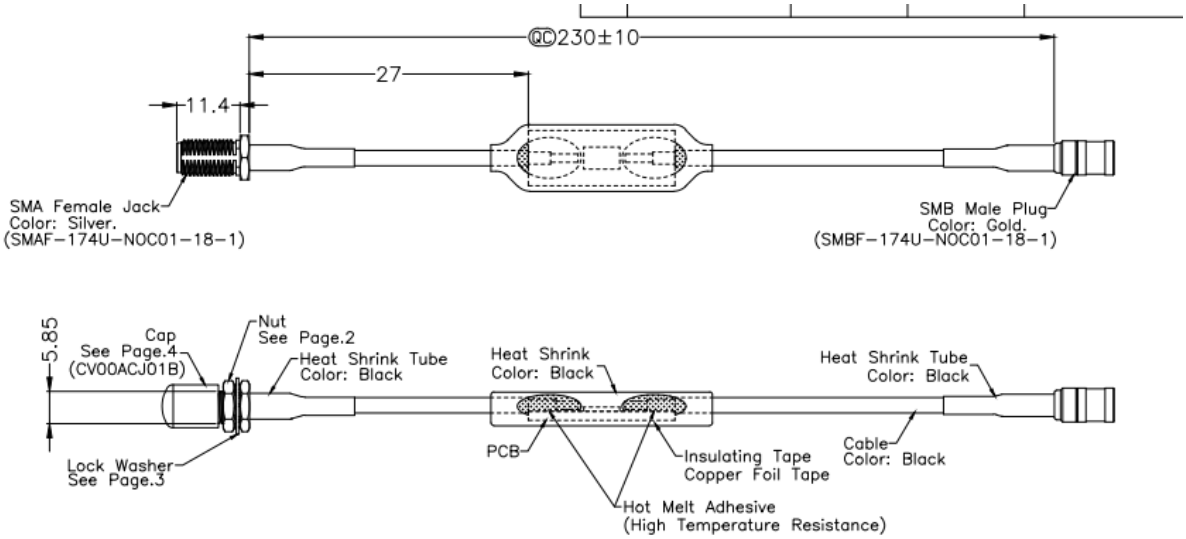


Figure 1 Push Button Dimension/Location

Cable

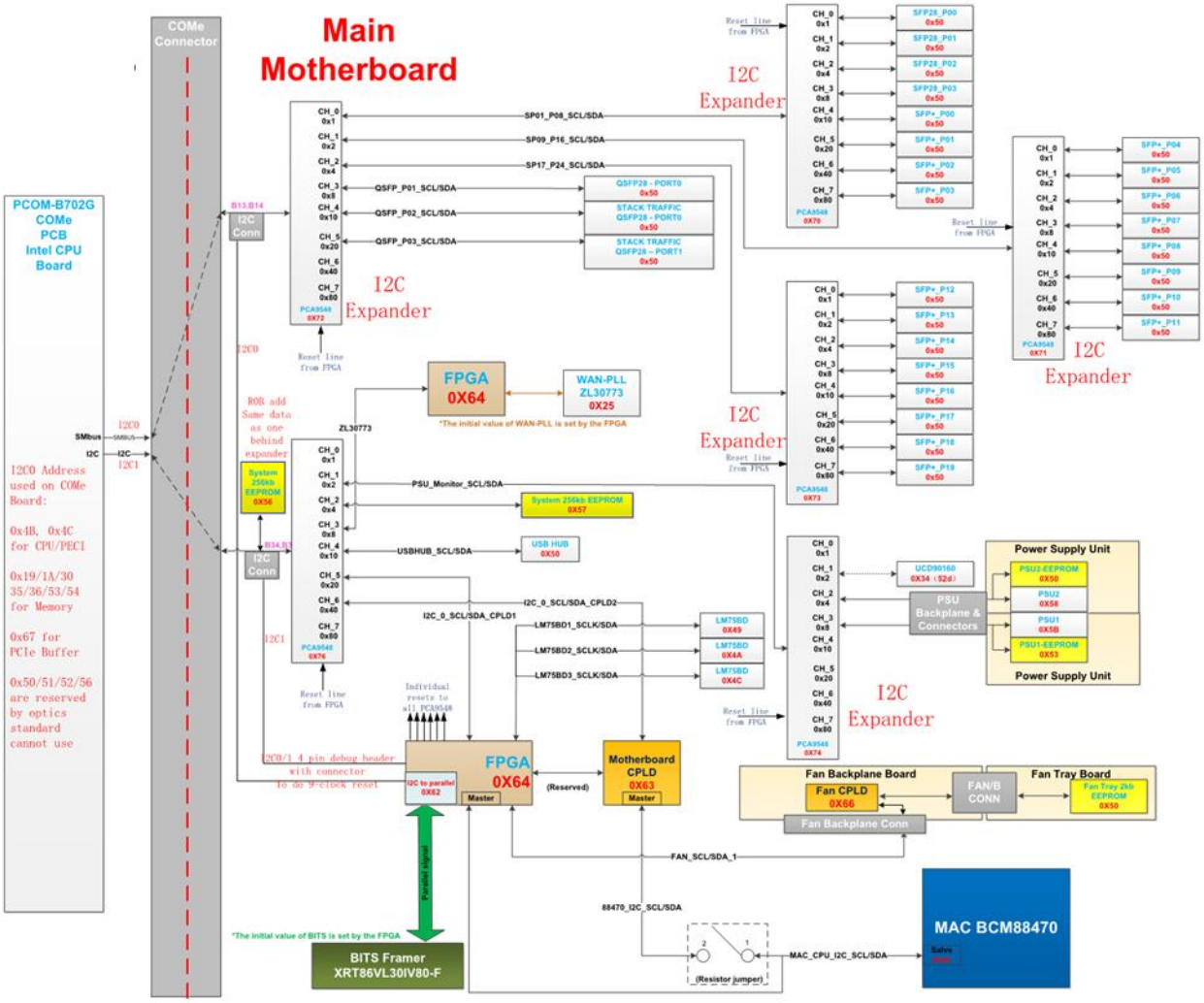
Cable	Part Number	UL94V-0	Note
GPS cable	ACFLA031	Yes	28AWG
RF cable	TM-09A-SMA-L230	Yes	RG-174

GPS Module to Main Board



SMA-FEMALE to SMB-PLUG

I2C Diagram


Main Motherboard
COMe Connector
PCOM-B702G COMe PCB Intel CPU Board
I2C0 Address used on COMe Board:
0x4B, 0x4C for CPU/PEC1
0x19/1A/30 35/36/53/54 for Memory
0x67 for PCIe Buffer
0x50/51/52/56 are reserved by optics standard cannot use
I2C Expander
FPGA 0X64
WAN-PLL ZL30773 0X25
BITS Framer XRT86VL30IV80-F
Motherboard CPLD 0X63
MAC BCM88470
Power Supply Unit
Fan Backplane Board
Fan CPLD 0X66
Fan Tray Board
PSU Backplane & Connectors
SP01_P08_SCL/SDA
SP09_P16_SCL/SDA
SP17_P24_SCL/SDA
QSFP_P01_SCL/SDA
QSFP_P02_SCL/SDA
QSFP_P03_SCL/SDA
PSU_Monitor_SCL/SDA
USBHUB_SCL/SDA
I2C_0_SCL/SDA_CPLD2
I2C_0_SCL/SDA_CPLD1
LM75BD1_SCLK/SDA
LM75BD2_SCLK/SDA
LM75BD3_SCLK/SDA
FAN_SCL/SDA_1
88470_I2C_SCL/SDA
MAC_CPU_I2C_SCL/SDA
Parallel Signal
(Resistor jumper)

BCM88470 Serdes Mapping

The AS7315-27X design allocates the BCM88470 Network Interface block in the following manner below.PM25-0/1/2 is running at 100G per port and design for three of uplink port that connects to QSFP28 connectors. The PM25-3 runs at 25G per port and connects to 4 SFP28 connector. Other NIFe SerDes is configuring as 10GbE that connects to SFP+ connector.

NIF/NIFE mapping Table

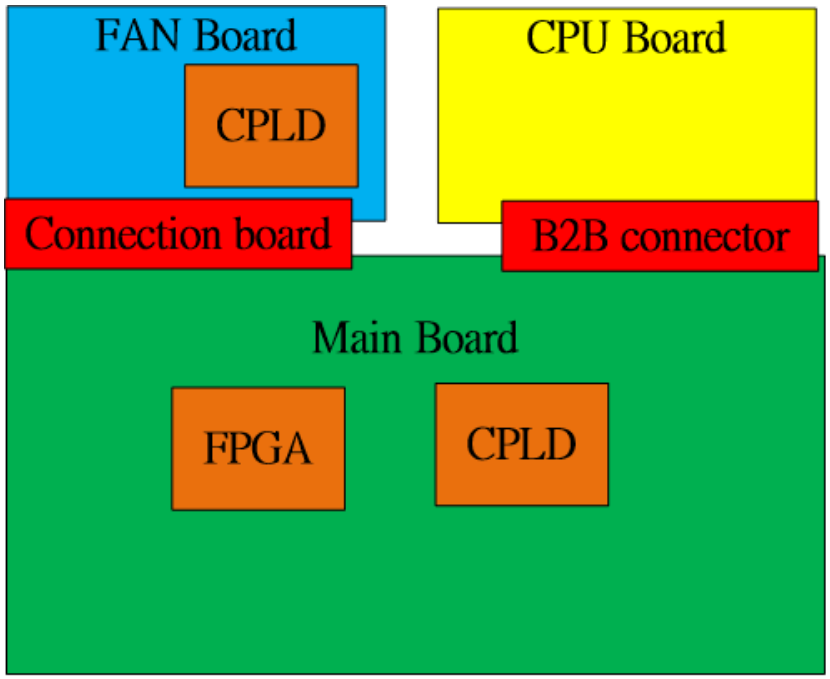
PM#	Interface	SFP+/QSFP28/SFP28	Physical Port	Logical Port	MAC			
					Device	Lane	Interface	P/N Polarity Inversion
PM25-2	SerDes	SFP28	9	xe1	BCM88470	2	NIF_TX[10]_P/N	
							NIF_RX[10]_P/N	Y
	SerDes	SFP28	10	xe2	BCM88470	3	NIF_TX[11]_P/N	Y
							NIF_RX[11]_P/N	Y
	SerDes	SFP28	11	xe3	BCM88470	0	NIF_TX[08]_P/N	
							NIF_RX[08]_P/N	
	SerDes	SFP28	12	xe4	BCM88470	1	NIF_TX[09]_P/N	Y
							NIF_RX[09]_P/N	Y
PM10Q-6	SerDes	SFP+	0	xe5	BCM88470	1	NIFE_TX[25]_P/N	
							NIFE_RX[25]_P/N	
PM10Q-6	SerDes	SFP+	1	xe6	BCM88470	0	NIFE_TX[24]_P/N	Y
							NIFE_RX[24]_P/N	Y
PM10Q-6	SerDes	SFP+	2	xe7	BCM88470	3	NIFE_TX[27]_P/N	
							NIFE_RX[27]_P/N	
PM10Q-6	SerDes	SFP+	3	xe8	BCM88470	2	NIFE_TX[26]_P/N	Y
							NIFE_RX[26]_P/N	Y
PM10Q-5	SerDes	SFP+	4	xe9	BCM88470	2	NIFE_TX[22]_P/N	
							NIFE_RX[22]_P/N	Y
PM10Q-5	SerDes	SFP+	5	xe10	BCM88470	3	NIFE_TX[23]_P/N	
							NIFE_RX[23]_P/N	
PM10Q-5	SerDes	SFP+	6	xe11	BCM88470	0	NIFE_TX[20]_P/N	
							NIFE_RX[20]_P/N	Y
PM10Q-5	SerDes	SFP+	7	xe12	BCM88470	1	NIFE_TX[21]_P/N	Y
							NIFE_RX[21]_P/N	
PM10Q-4	SerDes	SFP+	8	xe13	BCM88470	2	NIFE_TX[18]_P/N	
							NIFE_RX[18]_P/N	
PM10Q-4	SerDes	SFP+	9	xe14	BCM88470	3	NIFE_TX[19]_P/N	Y
							NIFE_RX[19]_P/N	
PM10Q-4	SerDes	SFP+	10	xe15	BCM88470	0	NIFE_TX[16]_P/N	
							NIFE_RX[16]_P/N	
PM10Q-4	SerDes	SFP+	11	xe16	BCM88470	1	NIFE_TX[17]_P/N	Y
							NIFE_RX[17]_P/N	Y

PM10Q-8	SerDes	SFP+	12	xe17	BCM88470	1	NIFE_TX[33]_P/N	Y
							NIFE_RX[33]_P/N	
PM10Q-8	SerDes	SFP+	13	xe18	BCM88470	0	NIFE_TX[32]_P/N	
							NIFE_RX[32]_P/N	Y
PM10Q-8	SerDes	SFP+	14	xe19	BCM88470	3	NIFE_TX[35]_P/N	
							NIFE_RX[35]_P/N	
PM10Q-8	SerDes	SFP+	15	xe20	BCM88470	2	NIFE_TX[34]_P/N	
							NIFE_RX[34]_P/N	Y
PM10Q-9	SerDes	SFP+	16	xe21	BCM88470	1	NIFE_TX[37]_P/N	
							NIFE_RX[37]_P/N	
PM10Q-9	SerDes	SFP+	17	xe22	BCM88470	0	NIFE_TX[36]_P/N	Y
							NIFE_RX[36]_P/N	Y
PM10Q-9	SerDes	SFP+	18	xe23	BCM88470	3	NIFE_TX[39]_P/N	
							NIFE_RX[39]_P/N	
PM10Q-9	SerDes	SFP+	19	xe24	BCM88470	2	NIFE_TX[38]_P/N	Y
							NIFE_RX[38]_P/N	Y
PM25-3	SerDes	QSFP28	0	ce25	BCM88470	0	NIF_TX[12]_P/N	Y
							NIF_RX[12]_P/N	
						2	NIF_TX[14]_P/N	Y
							NIF_RX[14]_P/N	
						1	NIF_TX[13]_P/N	
							NIF_RX[13]_P/N	
						3	NIF_TX[15]_P/N	
							NIF_RX[15]_P/N	
PM25-0	SerDes	QSFP28	1	ce26	BCM88470	3	NIF_P/N_TX[03]	
							NIF_P/N_RX[03]	
						2	NIF_P/N_TX[02]	
							NIF_P/N_RX[02]	
						1	NIF_P/N_TX[01]	
							NIF_P/N_RX[01]	
						0	NIF_P/N_TX[00]	Y
							NIF_P/N_RX[00]	Y
PM25-1	SerDes	QSFP28	2	ce27	BCM88470	3	NIF_P/N_TX[07]	
							NIF_P/N_RX[07]	
						1	NIF_P/N_TX[05]	
							NIF_P/N_RX[05]	
						2	NIF_P/N_TX[06]	
							NIF_P/N_RX[06]	
						0	NIF_P/N_TX[04]	
							NIF_P/N_RX[04]	Y

System CPLDs and FPGA

This AS7315-27X system has 2x CPLDs and 1x FPGA. Both CPLDs and the FPGA can be updated from the CPU.

1. The CPLD on main board shows network port LEDs and detects transceiver status.
2. The CPLD on backplane handles fan speed adjustment and detects fan status.
3. The FPGA on main board handles initialization of various devices such as Zarlink PLL and BITS FRAMER. It can also pull reset lines on I2C busses. The FPGA has PCIe access to the CPU for configuration options. The FPGA is also responsible for controlling the timing system and various clocks go into and out of the FPGA.



CPLD and FPGA

For specific information consult the appropriate CPLD/FPGA design specifications included in this contribution

Specifications and Standards

- Reference Documents
  1) ATT-TP-76200
  2) SIAD-whitebox-Specification112017-v4.pdf

Safety

- UL (CAN/CSA 22.2 No 60950-1 & UL60950-1)
- CB (IEC/EN60950-1)
- CCC (GB4943.1-2011)
- BSMI (CNS14336-1)

Electromagnetic Compatibility

- CE Mark
  - EN55032 Class A
  - EN55024(Immunity) for Information Technology Equipment
  - EN 61000-3-3
  - EN 61000-3-2
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CNS 13438 (BSMI)
- CCC (GB9254-2008)

Environmental

- Low-Temperature Exposure and Thermal Shock (packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.1
- High Relative Humidity Exposure (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.2
- High-Temperature Exposure and Thermal Shock (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.3
- Operating Temperature and Relative Humidity : NEBS GR63-CORE ISSUE 4 , Section 4.1.2
- Altitude : NEBS GR63-CORE ISSUE 4 , Section 4.1.3
- Handling Drop Tests -Packaged Equipment : NEBS GR63-CORE ISSUE 4 , Section 4.3.1.1
- Unpackaged Equipment -Drop Tests (All Equipment) : NEBS GR63-CORE ISSUE 4 , Section 4.3.2
- Earthquake (10U Rack) : NEBS GR63-CORE ISSUE 4 , Section 4.4.1 (Zone4)
- Office Vibration Test Procedure; 90 minutes/axis (Stand & 42U Rack) : NEBS GR63-CORE ISSUE 4 , section 4.4.4
- Transportation Vibration-Packaged Equipment : NEBS GR63-CORE ISSUE 4 , section 4.4.5
- Acoustic noise : NEBS GR63-CORE ISSUE 4 , section 4.6
- Bump : IEC60068-2-29- packaged
- Shock : ETSI EN 300 019-2-3 -Operational Tests, Class T3.2 op

ROHS (6/6) Requirement

Restriction of Hazardous Substances (6/6):

Compliance with Environmental procedure 020499-00, primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste Electrical and Electronic Equipment (WEEE Directive 2002/96/EC).

Software Support

AS7315-27X supports a base software package composed of the following components:

BIOS support

AS7315-27X Supports AMI AptioV BIOS version A01 or greater with the x86 CPU module

ONIE

See https://github.com/opencomputeproject/onie/tree/master/machine/accton for the latest supported version

Open Network Linux

See http://opennetlinux.org/ for latest supported version