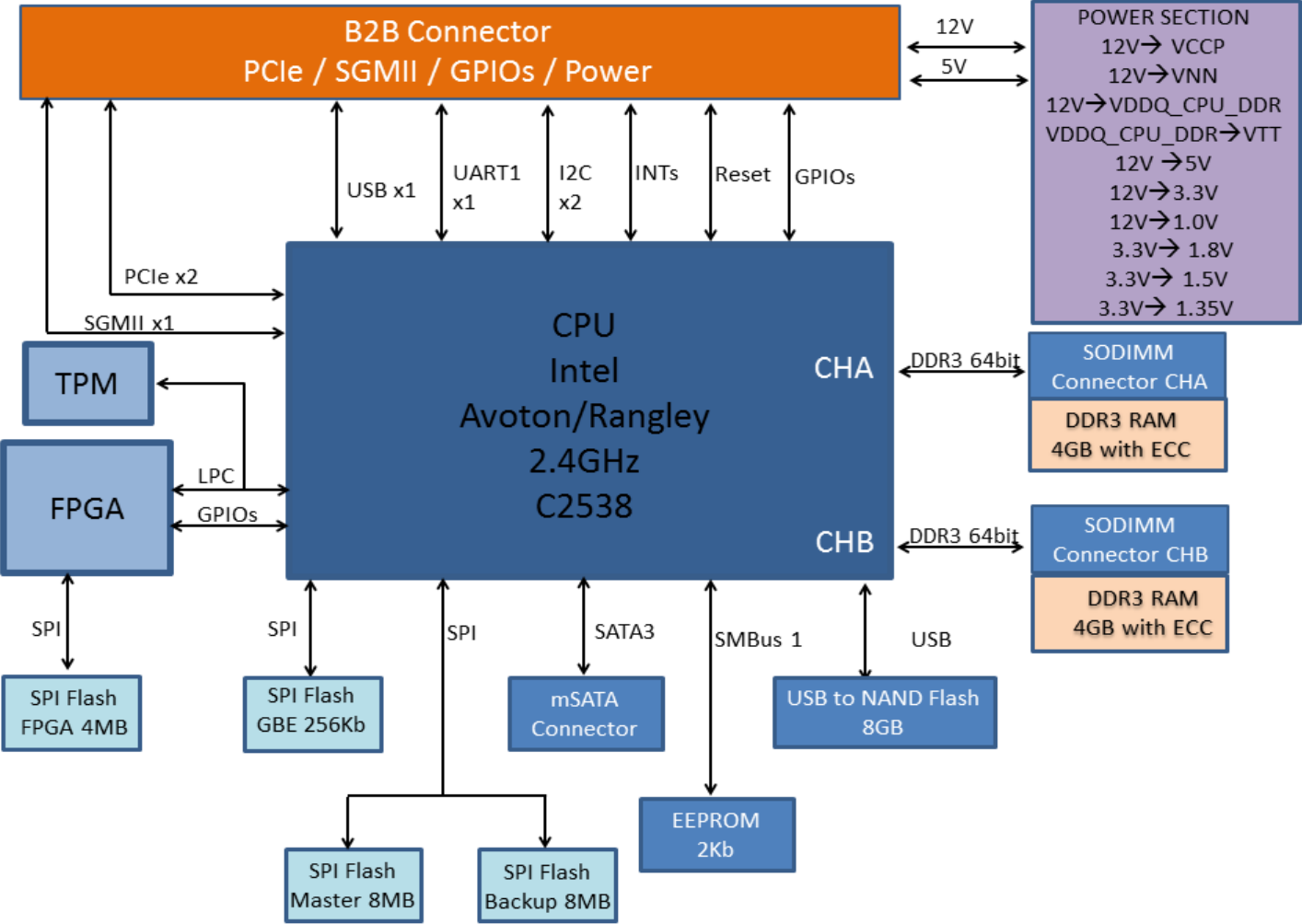


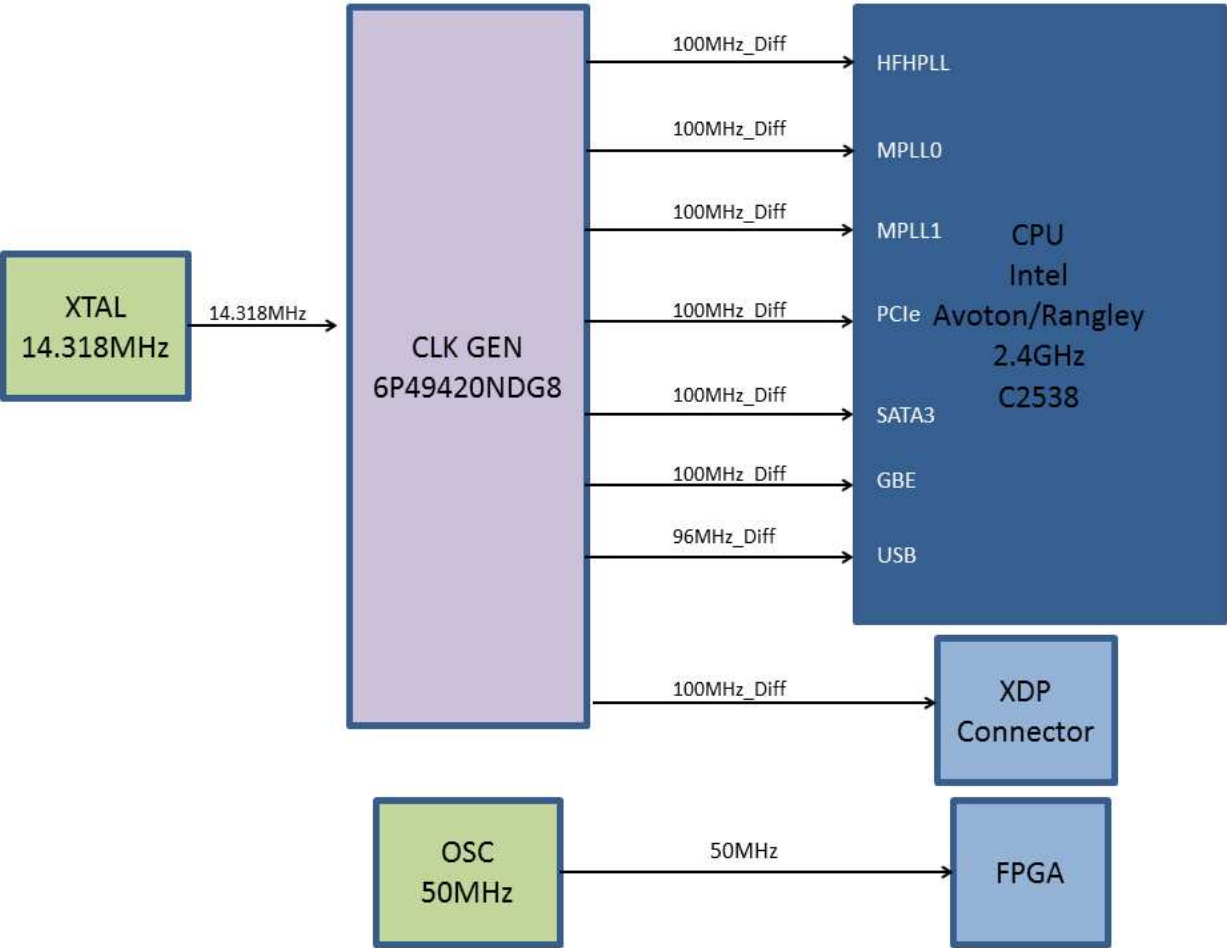
Table of Contents

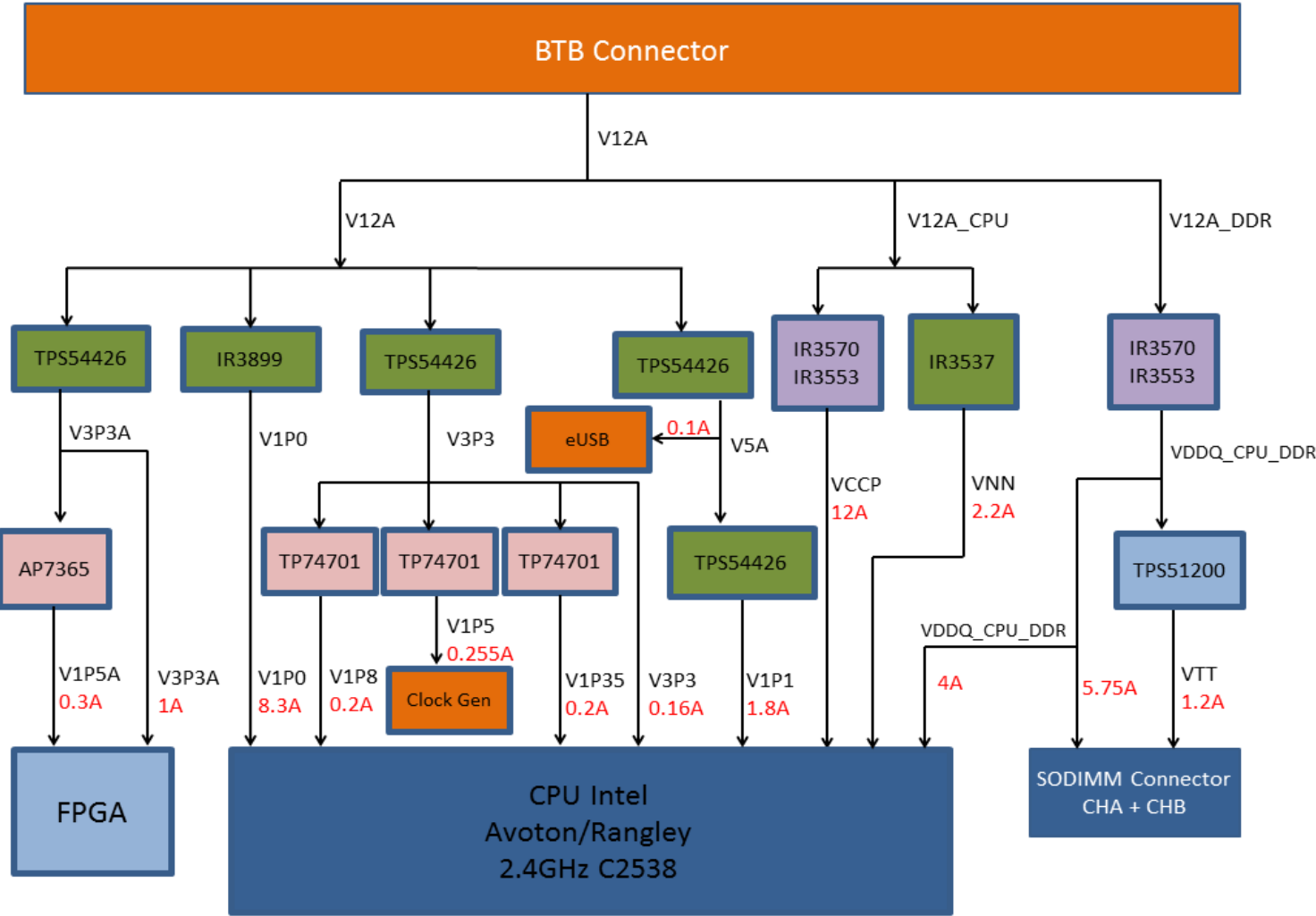
1	Cover Page	18	Clocks
2	History	19	DDR3 SODIMM_CH0
3	Block Diagram	20	DDR3 SODIMM_CH1
4	Clock Tree	21	XDP_PORT80 Debug
5	Power Tree	22	SPI_SCREW_HS_RPCAP
6	SMBus Tree	23	FPGA_Management
7	Reset Tree	24	FPGA_POWER
8	Power Sequence	25	B2B & SATA Connectors
9	GPIO Table	26	VCCP_VNN_PWM
10	JTAG Tree	27	VCCP_VNN_MOS
11	Rangeley_DDRIII_CH0	28	VDDQ_VTT
12	Rangeley_DDRIII_CH1	29	V1P0
13	Rangeley_PCIE, GBE	30	V3P3A_V1P1
14	Rangeley SATA,USB,MISC	31	V5A_V3P3
15	Rangeley Power	32	LD0_V1P8_V1P5_V1P35_V1P5A
16	Rangeley Power	33	Debug LED
17	Rangeley Power_GND		

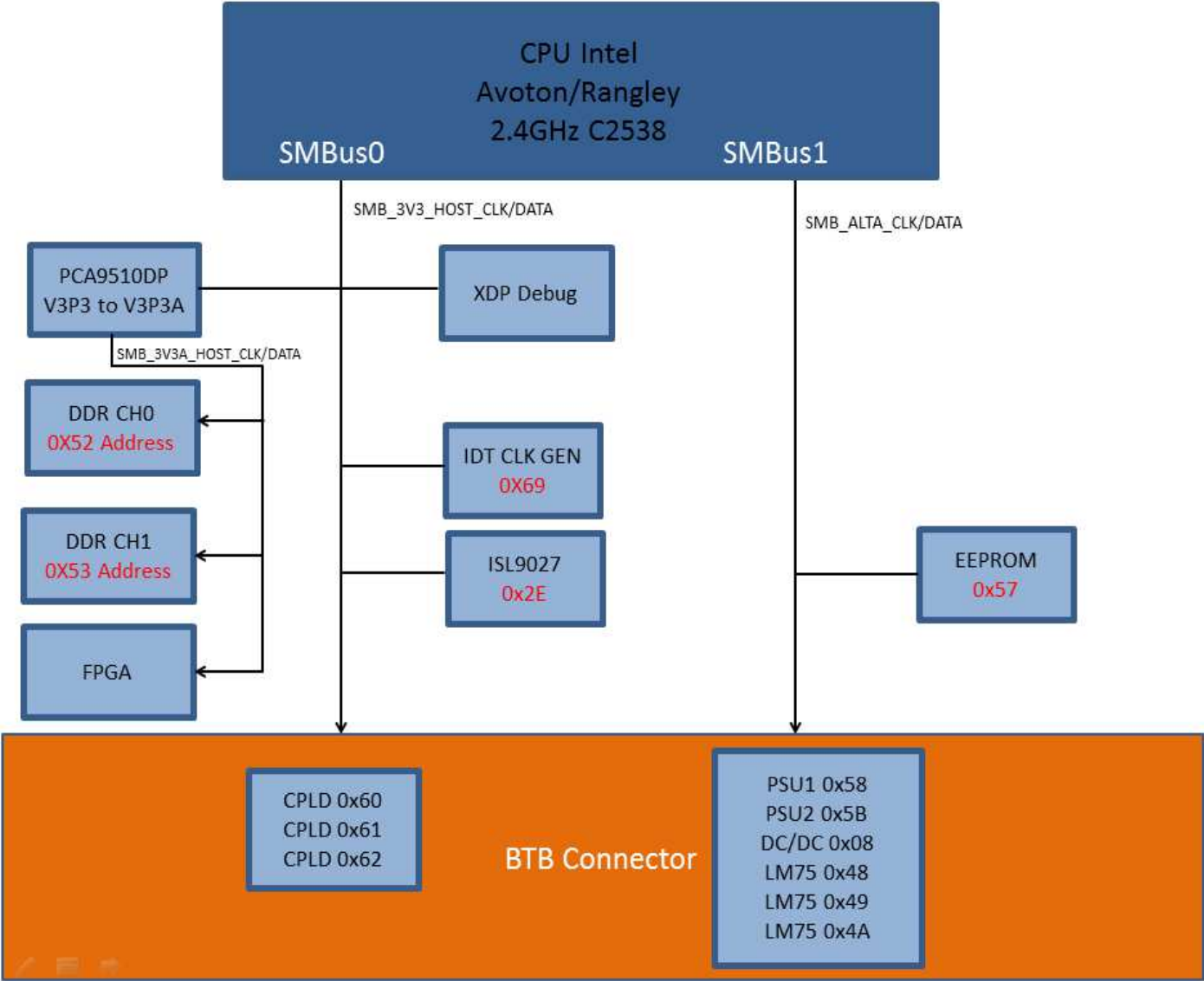
History

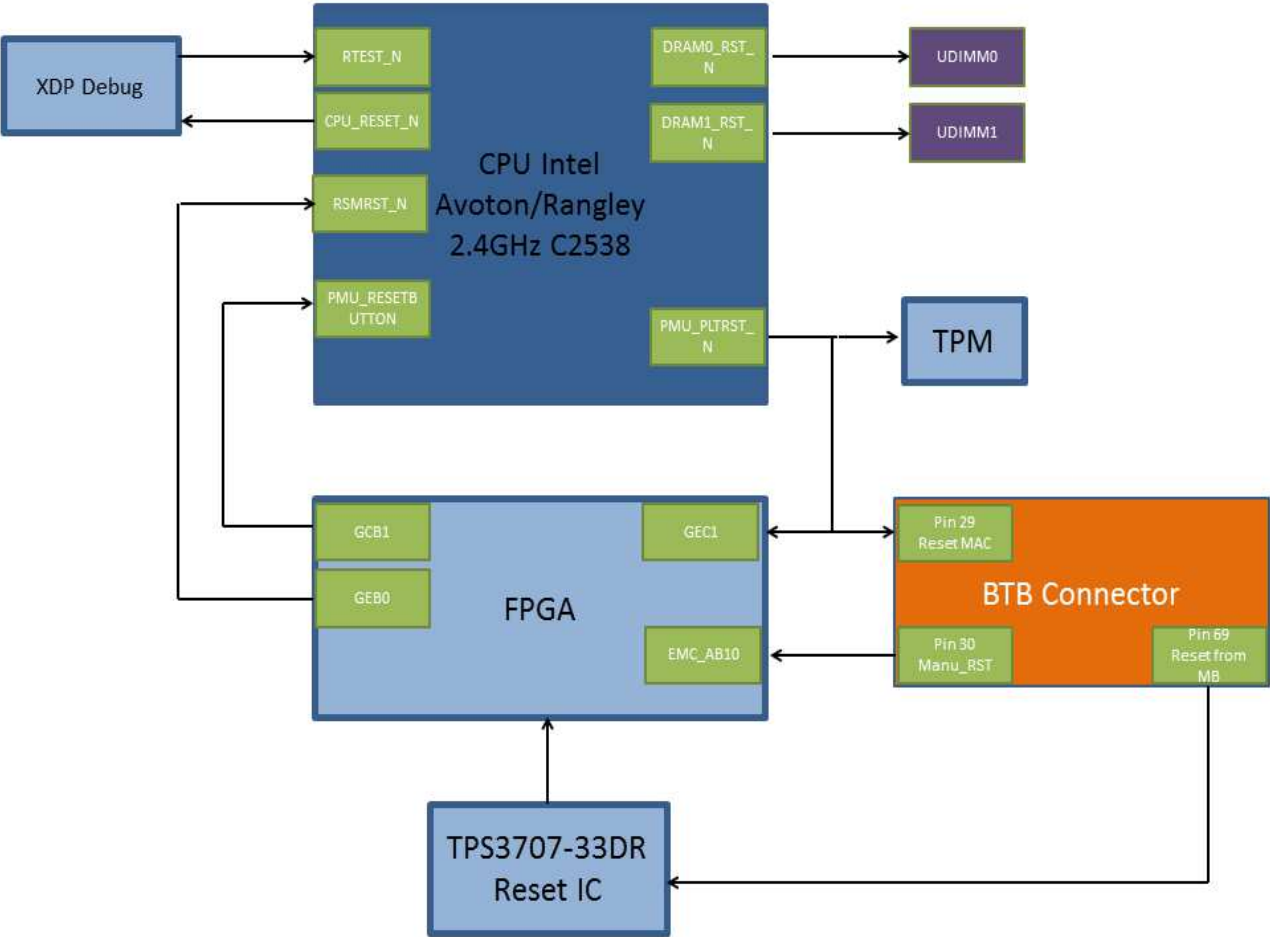
SCH Version	Date	Description
R0A	2014/03/05	Initial Version
R01	2014/06/30	Release to MP

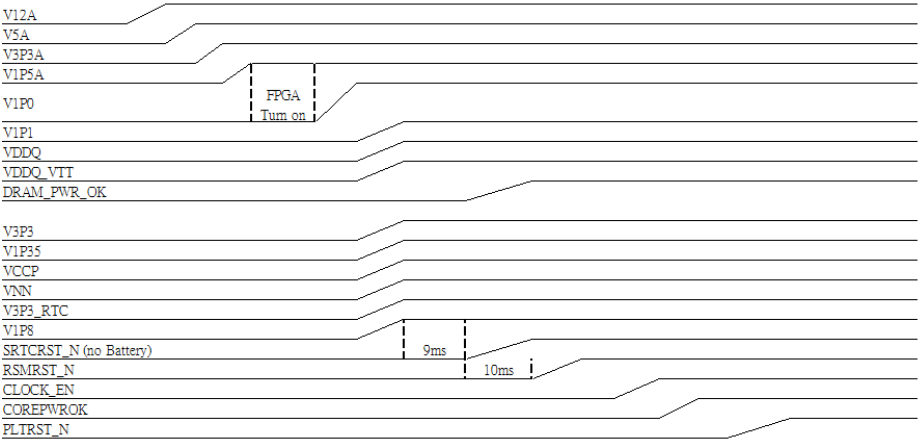






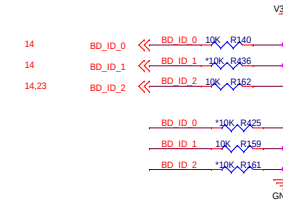






GPIOs	Pin#	Alternate Function	Rangeley Configuration
GPIO_0	AL56	NMI	Alternate Function
GPIO_1	AL63	ERROR2_B	Alternate Function
GPIO_2	AL62	ERROR1_B	Alternate Function
GPIO_3	AL65	ERROR0_B	Alternate Function
GPIO_4	AM52	IRERR_B	Alternate Function
GPIO_5	AL52	MCERR_B	Alternate Function
GPIO_6	AG50	UART1_RXD	Alternate Function
GPIO_7	AH50	UART1_TXD	Alternate Function
GPIO_8	AN62	SMB_CLK0	Alternate Function
GPIO_9	AP62	SMB_DATA0	Alternate Function
GPIO_10	AL58	SMB_ALRT_NO	Alternate Function
GPIO_11	AN63	SMB_DATA1	Goes to Mainboard
GPIO_12	AR63	SMB_CLK1	Goes to Mainboard
GPIO_13	AN65	SMB_DATA2	UART0_TXD
GPIO_14	AR65	SMB_CLK2	UART0_RXD
GPIO_15	AT63	SATA_GPO	BD_ID_0
GPIO_16	AL49	SATA_LEDN	N/A
GPIO_17	AH51	SATA3_GPO	BD_ID_1
GPIO_18	AH54	SATA3_LEDN	Alternate Function
GPIO_19	AH59	FLEX_CLK_SB0	Alternate Function
GPIO_20	AG56	FLEX_CLK_SE1	Alternate Function
GPIO_21	AG54	LPC_LAD0	Alternate Function
GPIO_22	AM53	LPC_LAD1	Alternate Function
GPIO_23	AL53	LPC_LAD2	Alternate Function
GPIO_24	AG59	LPC_LAD3	Alternate Function
GPIO_25	AH56	LPC_FRAMEB	Alternate Function
GPIO_26	AG51	LPC_CLKOUT0	Alternate Function
GPIO_27	AM49	LPC_CLKOUT1	Alternate Function
GPIO_28	AH48	LPC_CLKRUNB	Alternate Function
GPIO_29	AT50	ILB_SERIRQ	Alternate Function
GPIO_30	AM58	PMU_RESETBUTTON_B	Alternate Function

GPIOs	Pin#	Alternate Function	Rangeley Configuration
GPIO_SUS0	V66	N/A	ALTA_CPLD_TCK
GPIO_SUS1	W54	N/A	ALTA_CPLD_TDI
GPIO_SUS2	T53	N/A	BD_ID_2
GPIO_SUS3	V63	CPU_RESET_B	Alternate Function
GPIO_SUS4	Y57	SUSPWRDNACK	N/A ; pull up
GPIO_SUS5	AD58	PMU_SUSCLK	N/A
GPIO_SUS6	AC52	PMU_SLP_DDRVTT_B	Goes to FPGA, Output
GPIO_SUS7	Y50	PMU_SLP_LAN_B	Goes to FPGA, Output
GPIO_SUS8	AD66	PMU_WAKE_B	Alternate Function
GPIO_SUS9	AC49	PMU_PWRBTN_B	Alternate Function
GPIO_SUS10	AB65	SUS_STAT_B	N/A, pull down
GPIO_SUS11	AD63	USB_OC0_B	Alternate Function
GPIO_SUS12	AC58	SPL_CS1_B	Alternate Function
GPIO_SUS13	W51	GBE_EE_DI	Alternate Function
GPIO_SUS14	W60	GBE_EE_DO	Alternate Function
GPIO_SUS15	T50	GBE_EE_SK	Alternate Function
GPIO_SUS16	R59	GBE_EE_CS	Alternate Function
GPIO_SUS17	T58	GBE_SDP0_0	CPLD_INT_L
GPIO_SUS18	T48	GBE_SDP0_1	CPLD2_INT_L
GPIO_SUS19	P46	GBE_LED0	N/A, pull down
GPIO_SUS20	W50	GBE_LED1	N/A, pull down
GPIO_SUS21	P48	GBE_LED2	N/A, pull down
GPIO_SUS22	R58	GBE_LED3	N/A, pull down
GPIO_SUS23	V63	GBE_WOL	N/A, pull down
GPIO_SUS24	W56	GBE_MDIO0_LXC_CLK	MDIO0_CLK
GPIO_SUS25	W59	GBE_MDIO0_LXC_DATA	MDIO0_DATA
GPIO_SUS26	Y54	GBE_MDIO1_LXC_CLK	ALTA_CPLD_TDO
GPIO_SUS27	Y53	GBE_MDIO1_LXC_DATA	ALTA_CPLD_TMS



Board assignments			
BD_ID_2	BD_ID_1	BD_ID_0	Board Type
0	0	0	Lyon Peak SV
0	0	1	Lyon Peak BDV
0	1	0	Lyon Peak PPV
1	0	0	Mohon Peak
1	0	1	Intel Project 2
1	1	0	Tiger Cove

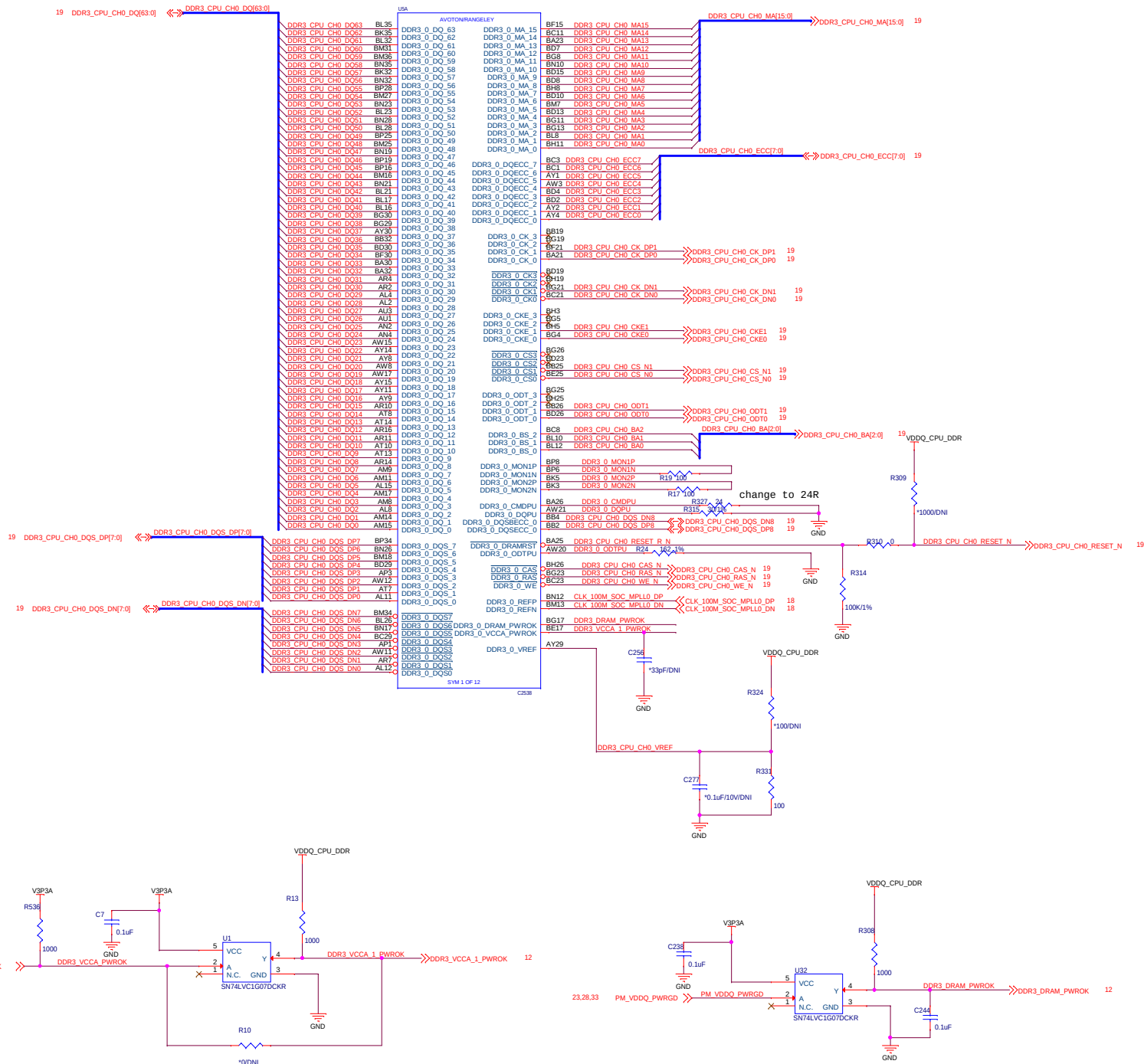


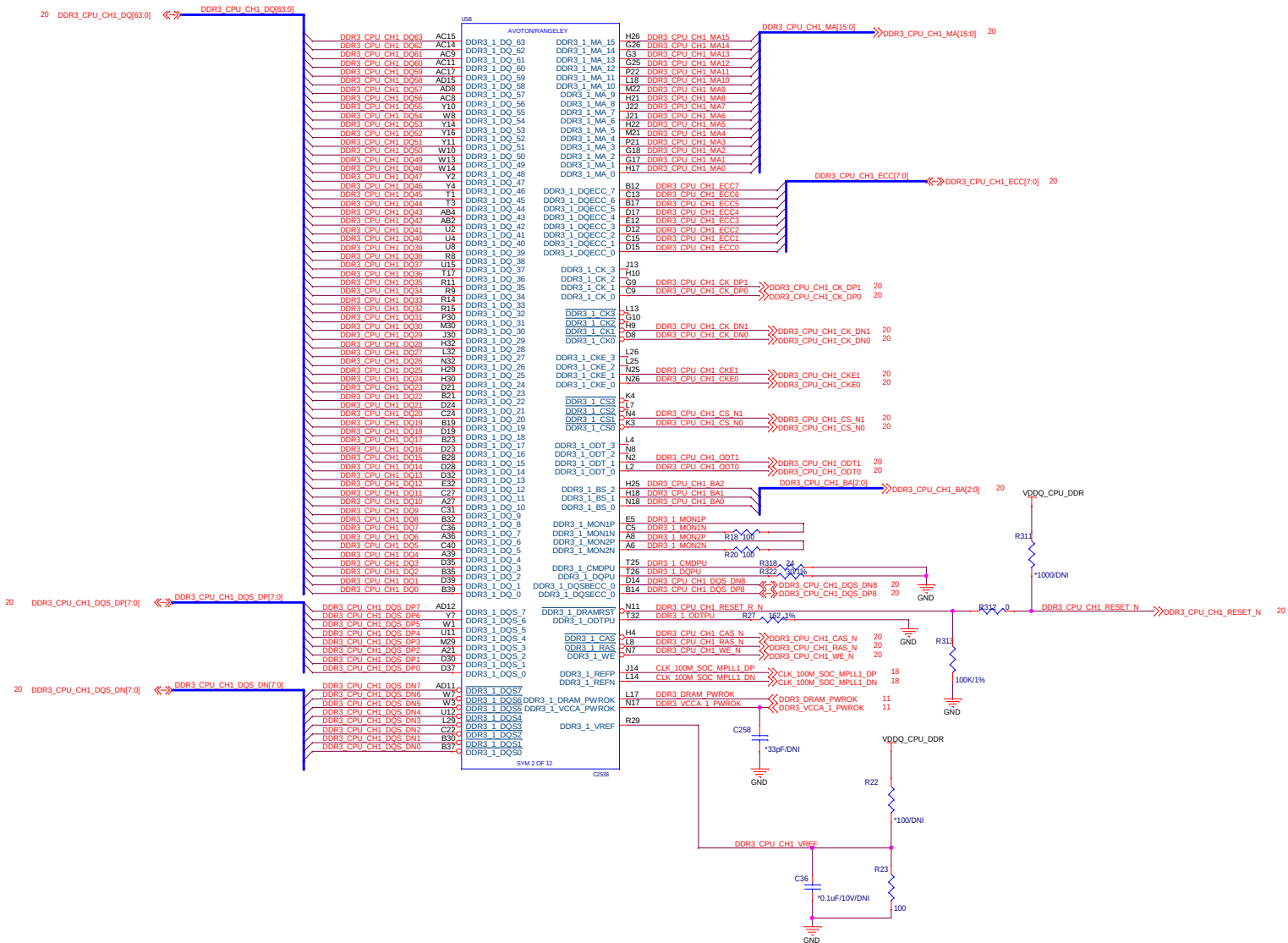
Accton Inc.

Making Partnership Work

Model Name		ES5654BT2-CPU-FLF-ZZ	Rev R02
Size C	Page Name	P09_GPIO TABLE	Engineer Jimmy_Huang
Date:	Tuesday, January 27, 2015	Sheet	9 of 33

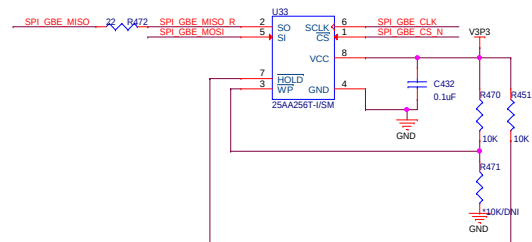
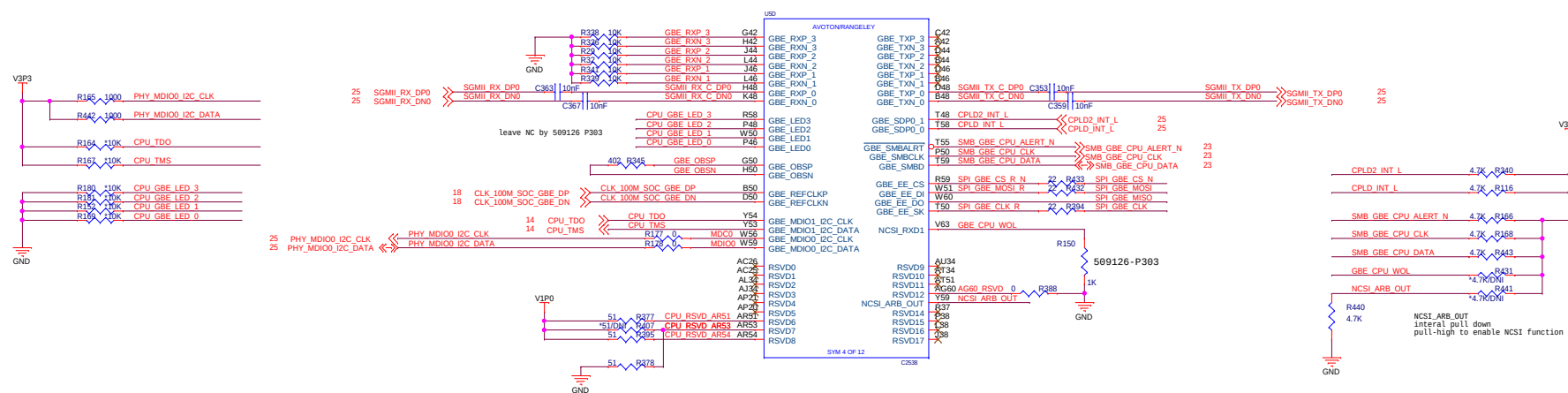
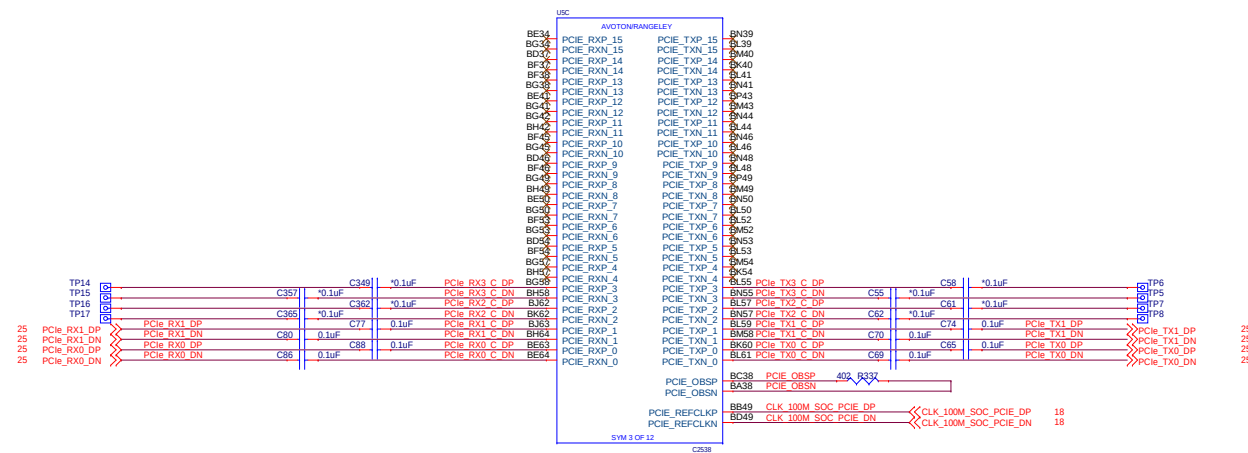
BLANK PAGE

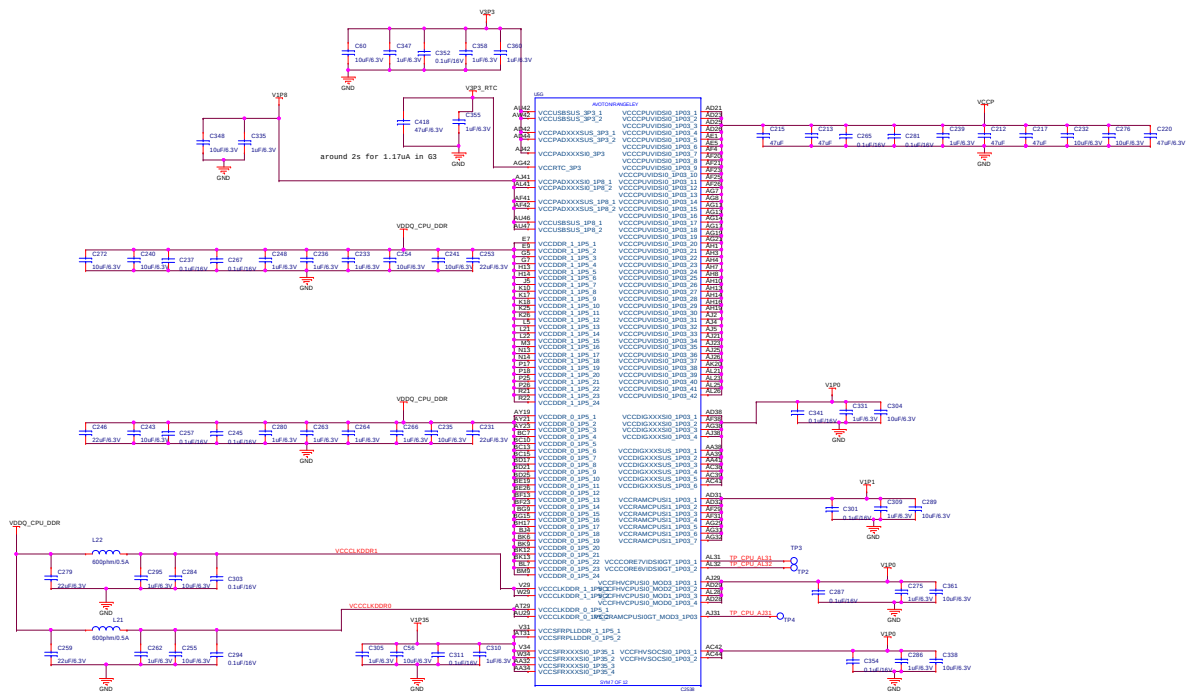


**Accton Inc.**

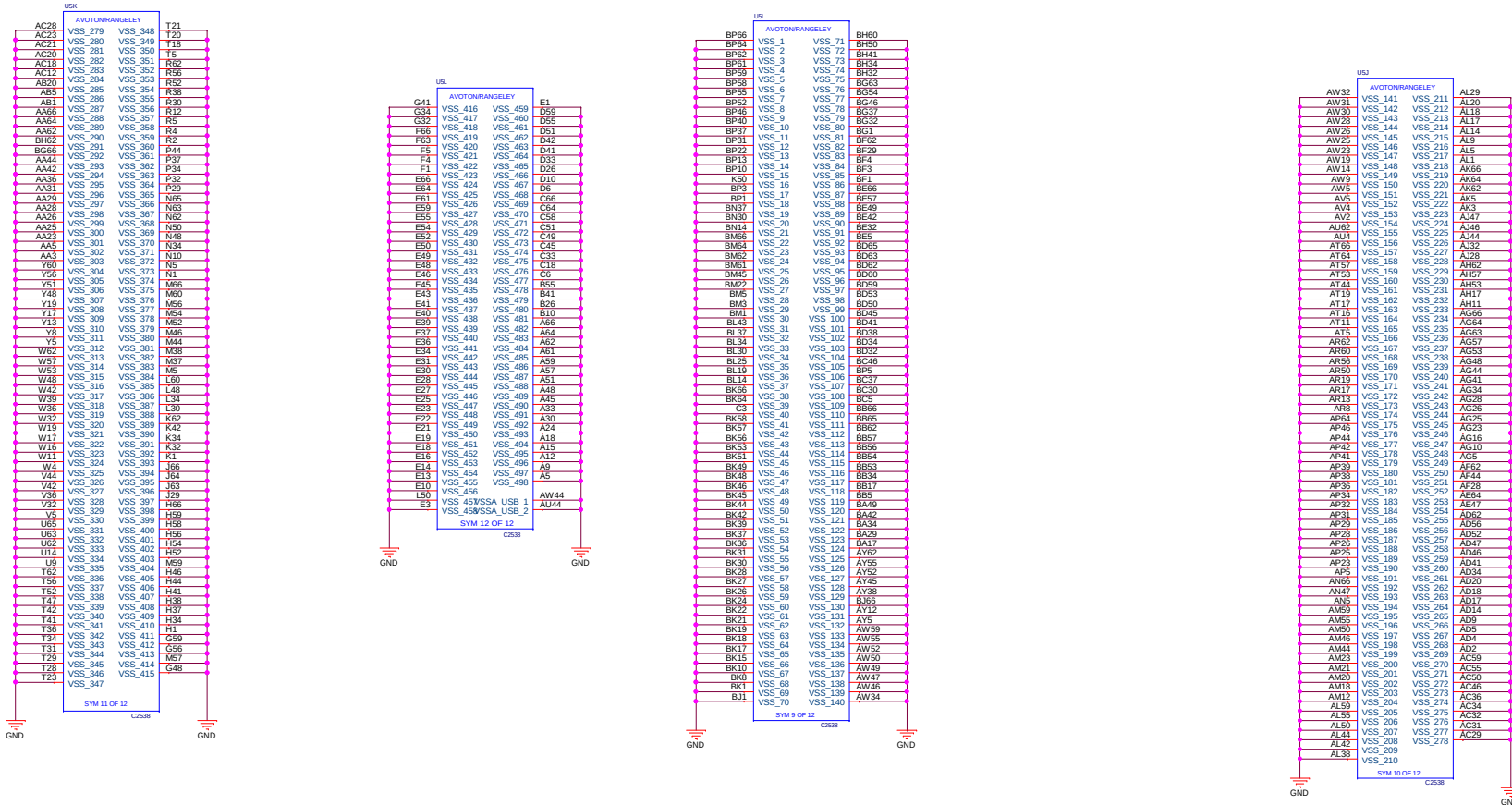
Making Partnership Work

Model Name		ES5654BT2-CPU-FLF-ZZ	Rev	R02
Size	Page Name	Engineer		
C	P12_Rangeley_DDRIII_CH1	Jummy_Huang		
Date:	Tuesday, January 27, 2015	Sheet	12	of 33



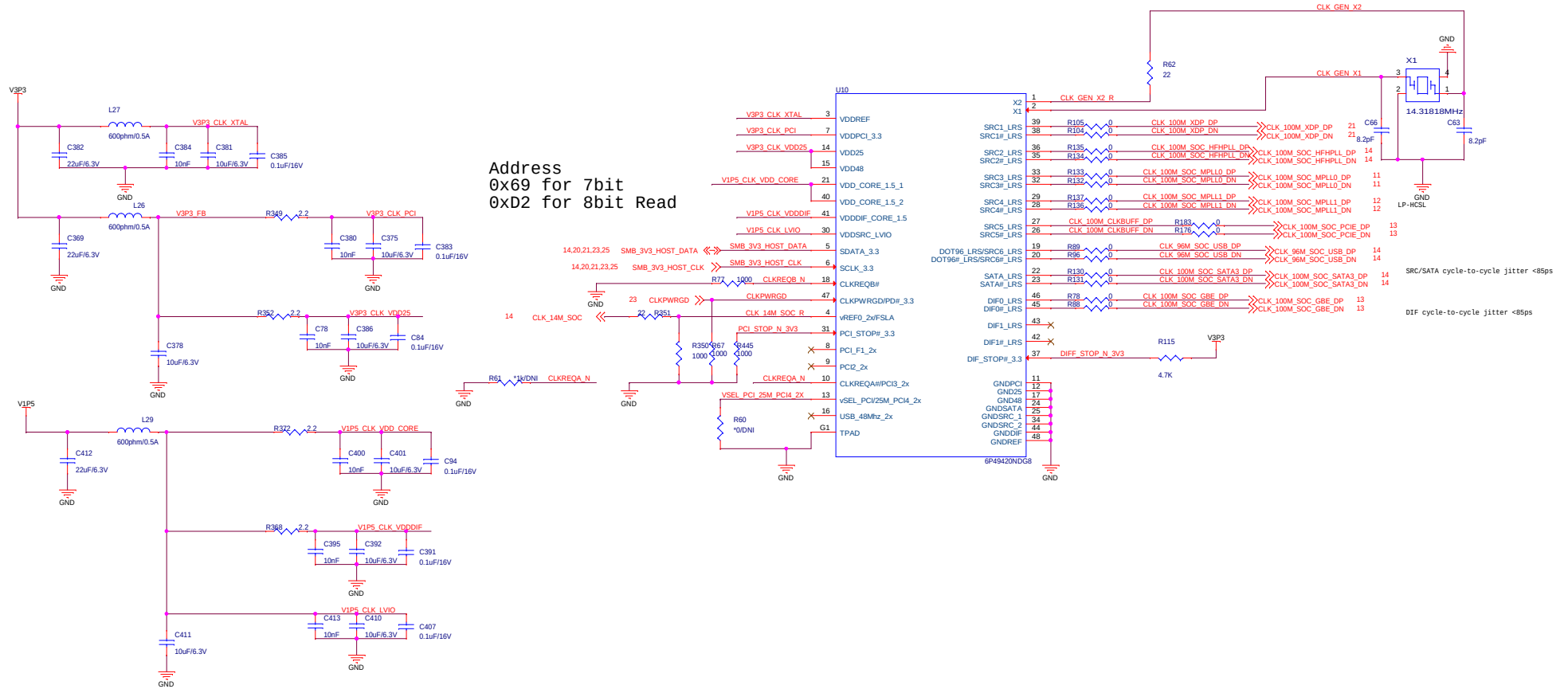




**Accton Inc.**

Making Partnership Work

Model Name		ES5654BT2-CPU-FLF-ZZ		Rev R02	
Size	C	Page Name P17_Rangeley Power_GND		Engineer Jummy_Huang	
Date:	Tuesdav, January 27, 2015		Sheet	17	of 33

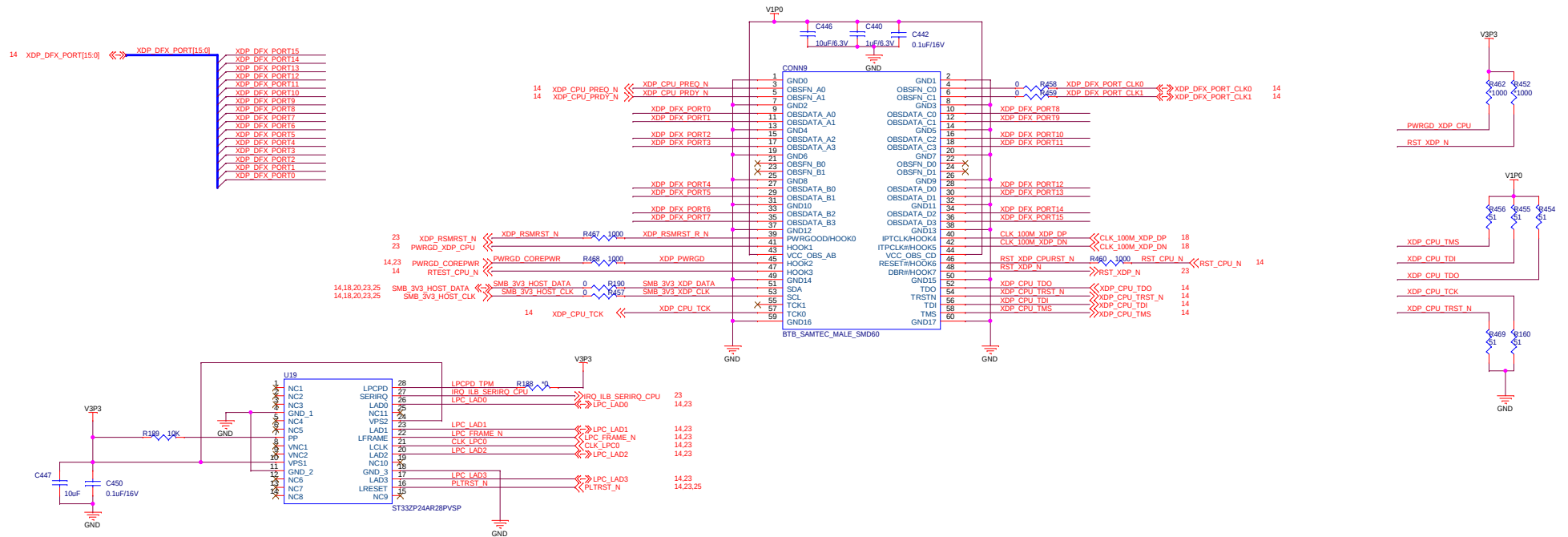


H=9.2mm

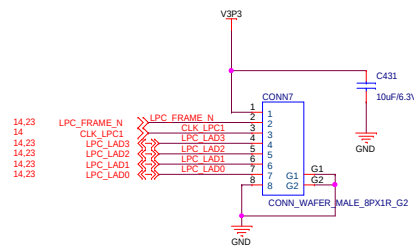


H = 5.2mm

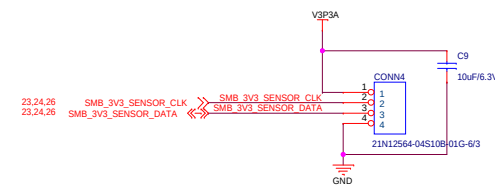


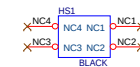
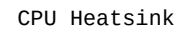
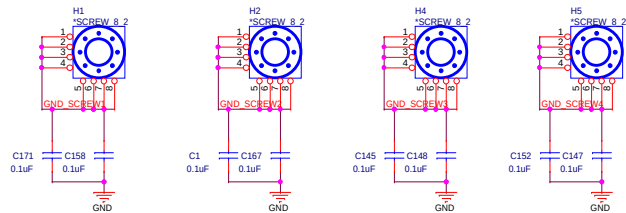
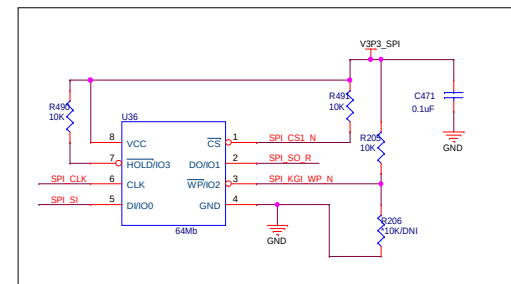
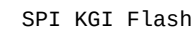
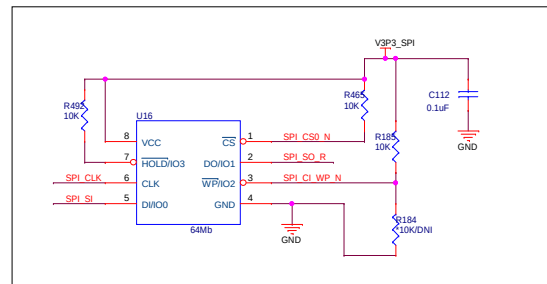
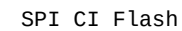
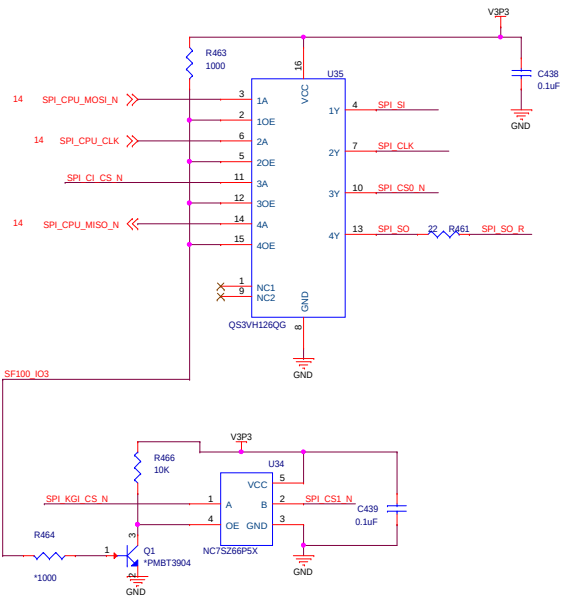
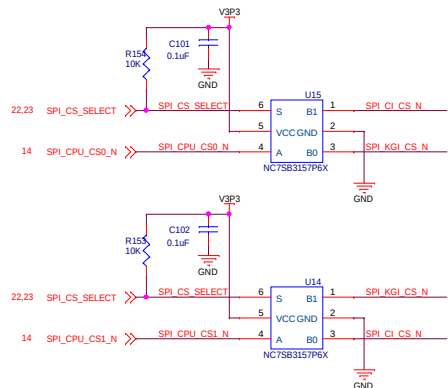
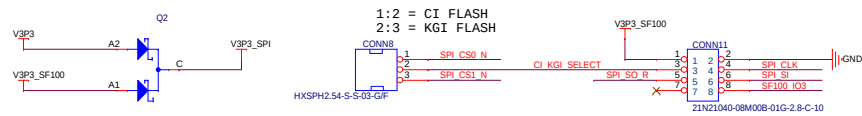


```
Port 80 Debug Header
Use LPC decoder board
```

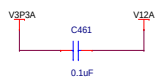
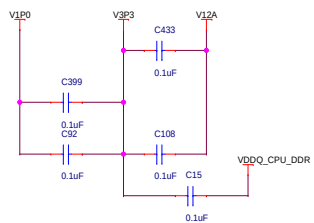


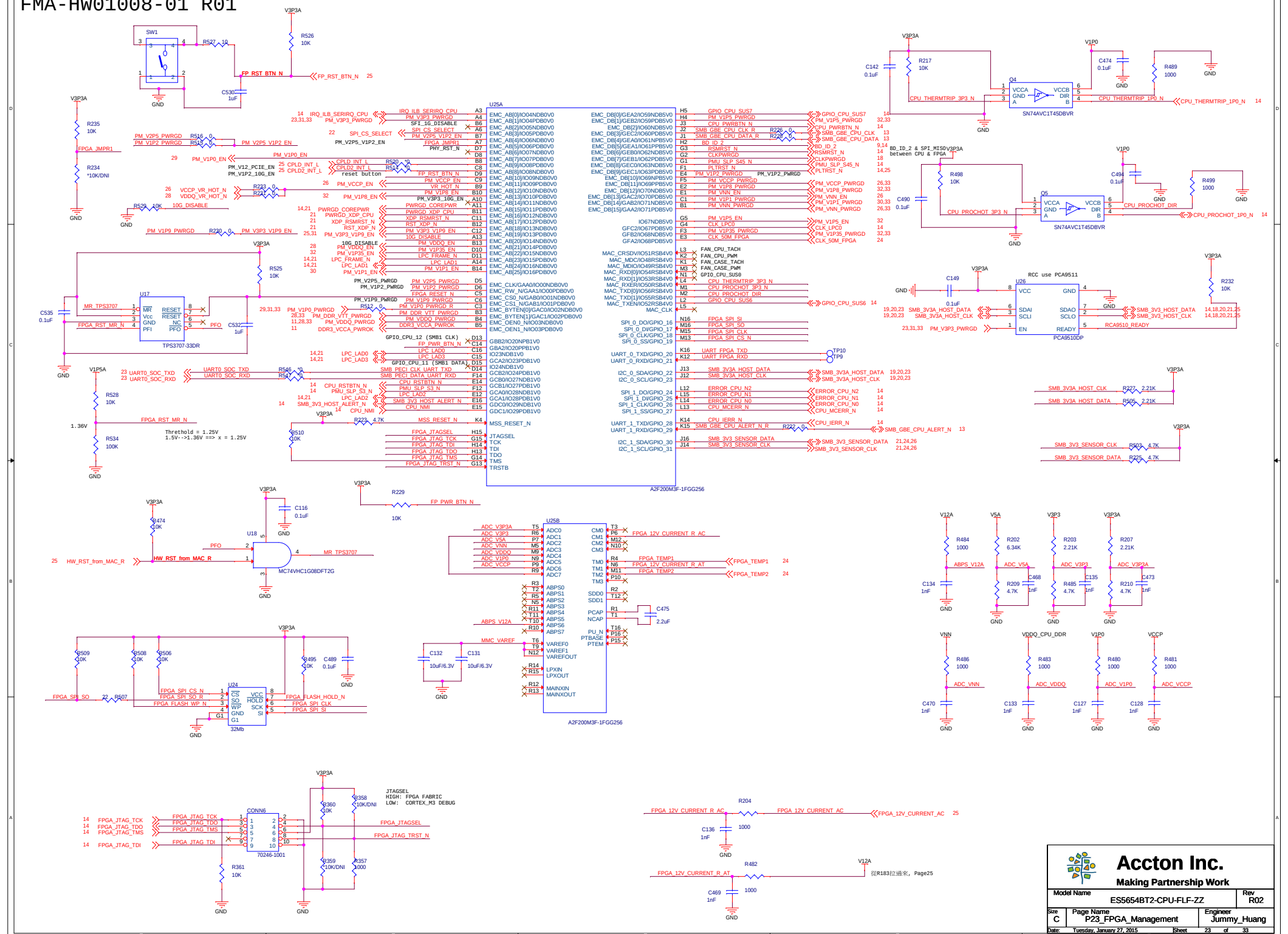
```
Port 80 Debug Header
Use I2C bus to connector HW debug board
```





Change to 50mmx50mmx14mm





Accton Inc.
Making Partnership Work

Model Name	ES5654BT2-CPU-FL-ZZ	Rev	R02
Size	Page Name	Engineer	
C	P23_FPGA_Management	Jummy_Huang	
Date:	Tuesday, January 27, 2015	Sheet	23 of 33

A vertical number line with four points labeled A, B, C, and D from bottom to top. An arrow points from point B to point C.



P13_Rangeley_PCIE, GBE

13	SGMII_TX_DP0	SGMII_TX_DP0
13	SGMII_TX_DN0	SGMII_TX_DN0
13	SGMII_RX_DP0	SGMII_RX_DP0
13	SGMII_RX_DN0	SGMII_RX_DN0
13	PCIE_TX1_DP	PCIE_TX1_DP
13	PCIE_TX1_DN	PCIE_TX1_DN
13	PCIE_TX0_DP	PCIE_TX0_DP
13	PCIE_TX0_DN	PCIE_TX0_DN
13	PCIE_RX1_DP	PCIE_RX1_DP
13	PCIE_RX1_DN	PCIE_RX1_DN
13	PCIE_RX0_DP	PCIE_RX0_DP
13	PCIE_RX0_DN	PCIE_RX0_DN
13	PHY_MDIO0_I2C_CLK	PHY_MDIO0_I2C_CLK
13	PHY_MDIO0_I2C_DATA	PHY_MDIO0_I2C_DATA
13	CPLD_INT_L	CPLD_INT_L
13	CPLD2_INT_L	CPLD2_INT_L

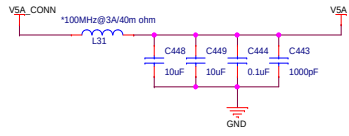
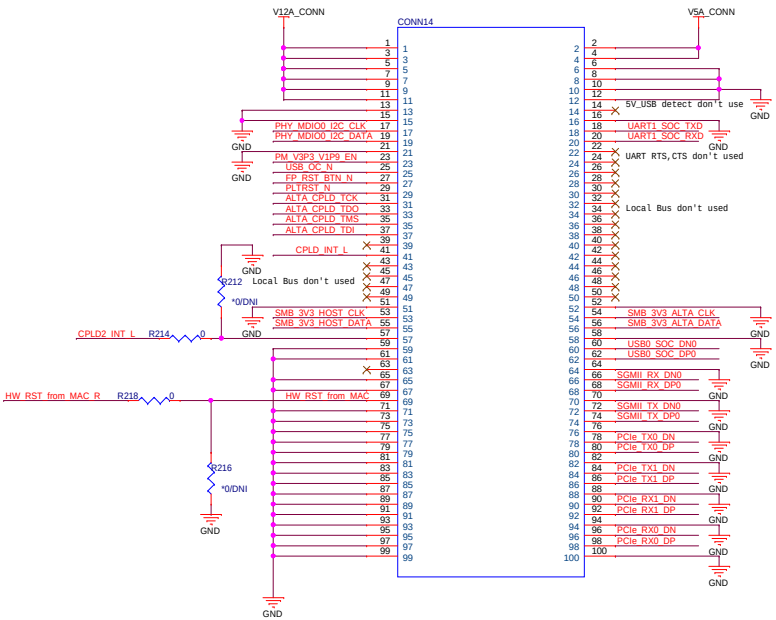
P14_Rangeley SATA,USB,MISC

14,18,20,21,23	SMB_3V3_HOST_CLK	SMB_3V3_HOST_CLK
14,18,20,21,23	SMB_3V3_HOST_DATA	SMB_3V3_HOST_DATA
14	SMB_3V3_ALTA_CLK	SMB_3V3_ALTA_CLK
14	SMB_3V3_ALTA_DATA	SMB_3V3_ALTA_DATA
14	USB0_SOC_DP0	USB0_SOC_DP0
14	USB0_SOC_DN0	USB0_SOC_DN0
14	UART1_SOC_TXD	UART1_SOC_TXD
14	UART1_SOC_RXD	UART1_SOC_RXD
14	ALTA_CPLD_TDI	ALTA_CPLD_TDI
14	ALTA_CPLD_TCK	ALTA_CPLD_TCK
14	ALTA_CPLD_TDO	ALTA_CPLD_TDO
14	ALTA_CPLD_TMS	ALTA_CPLD_TMS
14,23	PLTRST_N	PLTRST_N
14	USB_OC_N	USB_OC_N

P24_FPGA_Management

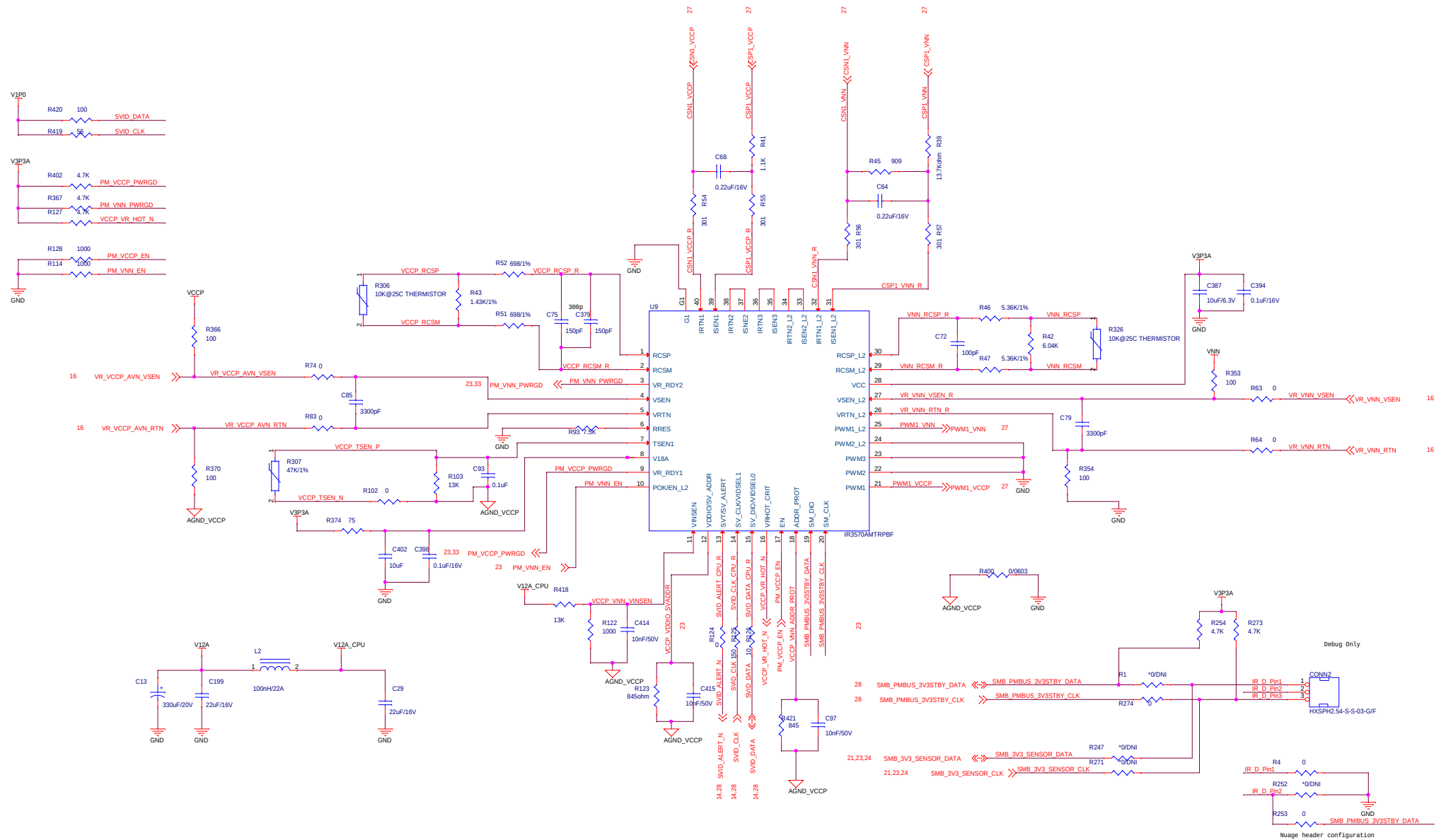
23,31	PM_V3P3_VIP9_EN	PM_V3P3_VIP9_EN
23	HW_RST_from_MAC_R	HW_RST_from_MAC_R
23	FP_RST_BTN_N	FP_RST_BTN_N

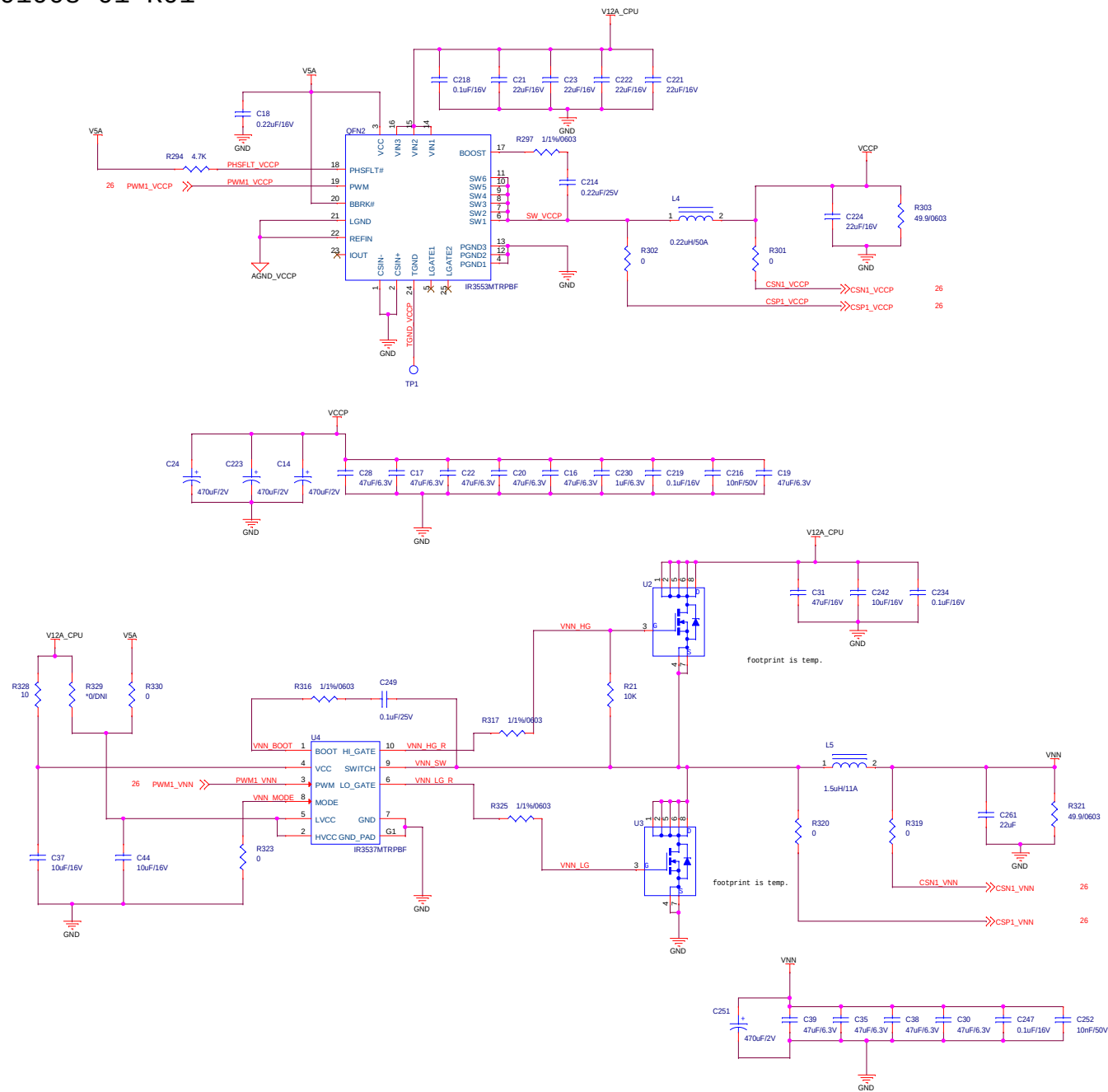
Resistor	96+8	96+8	48+6	32x48
R467	DI (Yes)	DNI (NO)	DNI (NO)	DNI (NO)
R495	DI (Yes)	DNI (NO)	DNI (NO)	DNI (NO)
R476	DNI (NO)	DI (Yes)	DI (Yes)	DI (Yes)
R477	DNI (NO)	DI (Yes)	DI (Yes)	DI (Yes)



Accton Inc.
Making Partnership Work

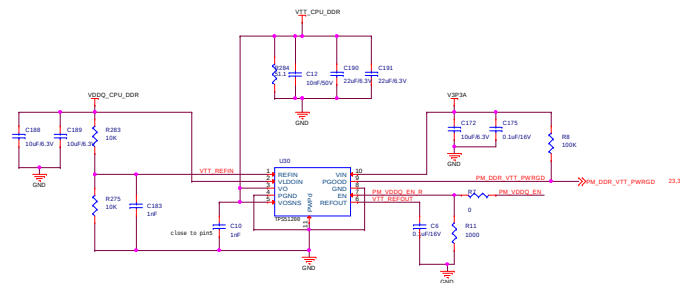
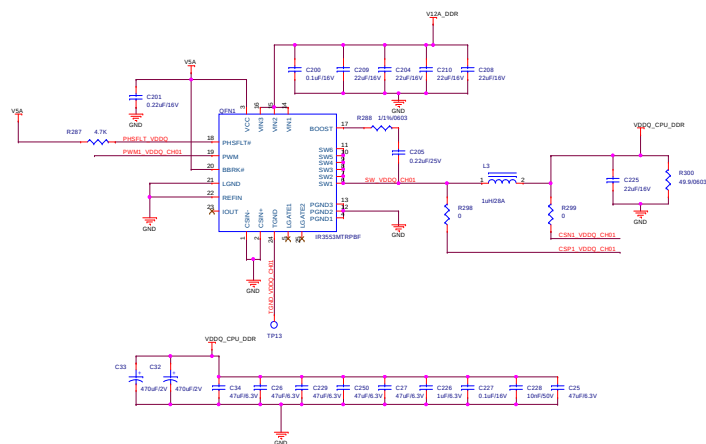
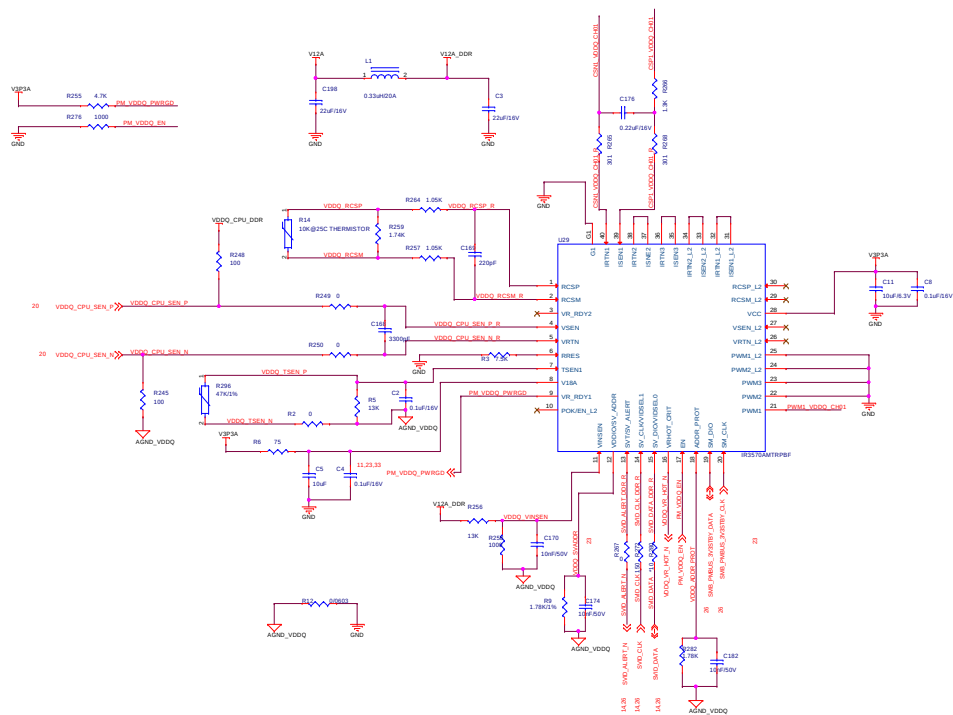
Model Name	ES5654BT2-CPU-FLF-ZZ	Rev	R02
Size	Page Name P25_B2B & SATA Connector	Engineer	Jummy_Huang
Date:	Tuesday, January 27, 2015	Sheet	25 of 33



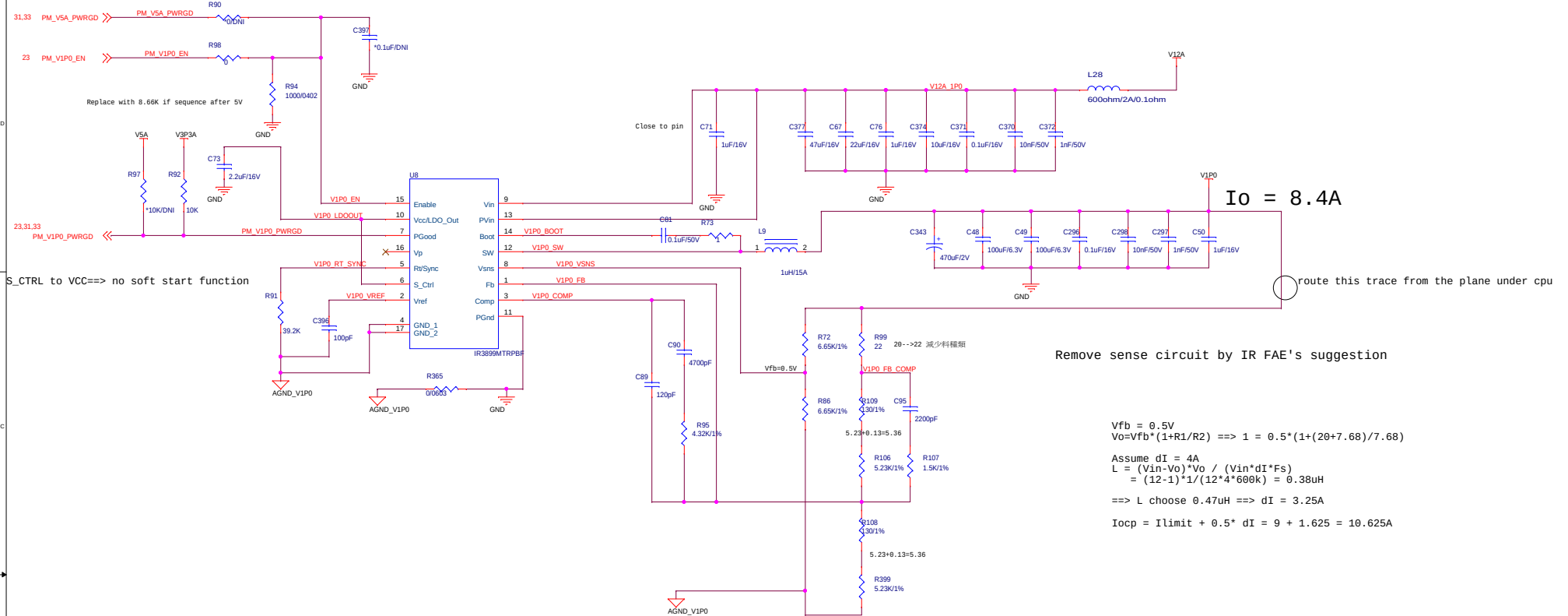


Accton Inc.
Making Partnership Work

Model Name		ES5654BT2-CPU-FLF-ZZ	Rev	R02
Size	Page Name	P27_VCCP_VNN_MOS	Engineer	Jummy_Huang
C	Date:	Tuesday, January 27, 2015	Sheet	27 of 33



FMA-HW01008-01 R01



$I_o = 8.4A$

$$V_{fb} = 0.5V$$

$$V_o = V_{fb} * (1 + R1/R2) \Rightarrow 1 = 0.5 * (1 + (20 + 7.68) / 7.68)$$

Assume $dI = 4A$

$$L = \frac{(V_{in} - V_o) * V_o}{(V_{in} * dI * F_s)}$$

$$= \frac{(12 - 1) * 1}{(12 * 4 * 600k)} = 0.38uH$$

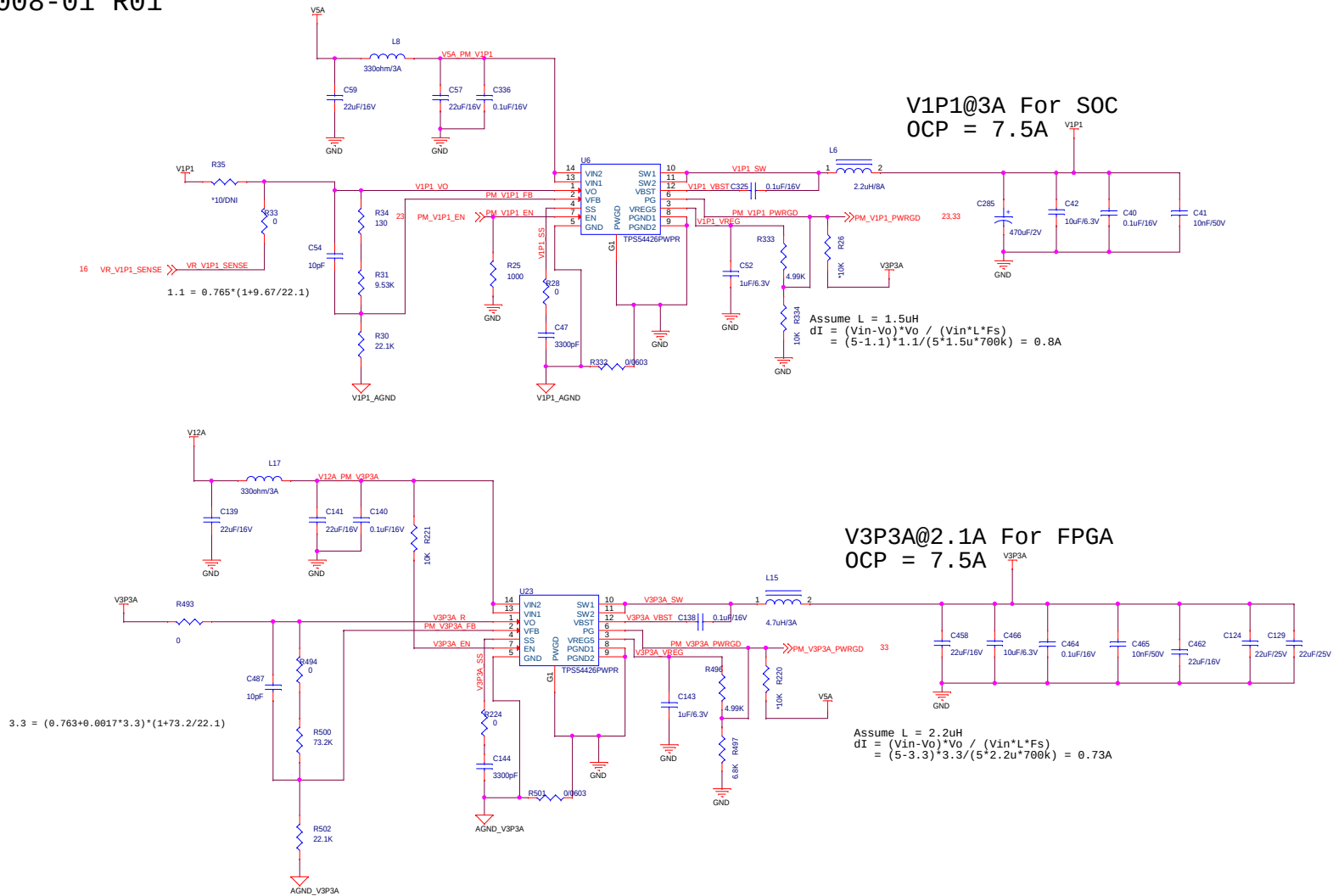
$$\Rightarrow L \text{ choose } 0.47uH \Rightarrow dI = 3.25A$$

$$I_{ocp} = I_{limit} + 0.5 * dI = 9 + 1.625 = 10.625A$$



Accton Inc.
Making Partnership Work

Model Name			ES5654BT2-CPU-FLF-ZZ		Rev R02	
Size	Page Name			Engineer		
C	P29_V1P0			Jummy_Huang		
Date:	Tuesday, January 27, 2015			Sheet	29	of 33

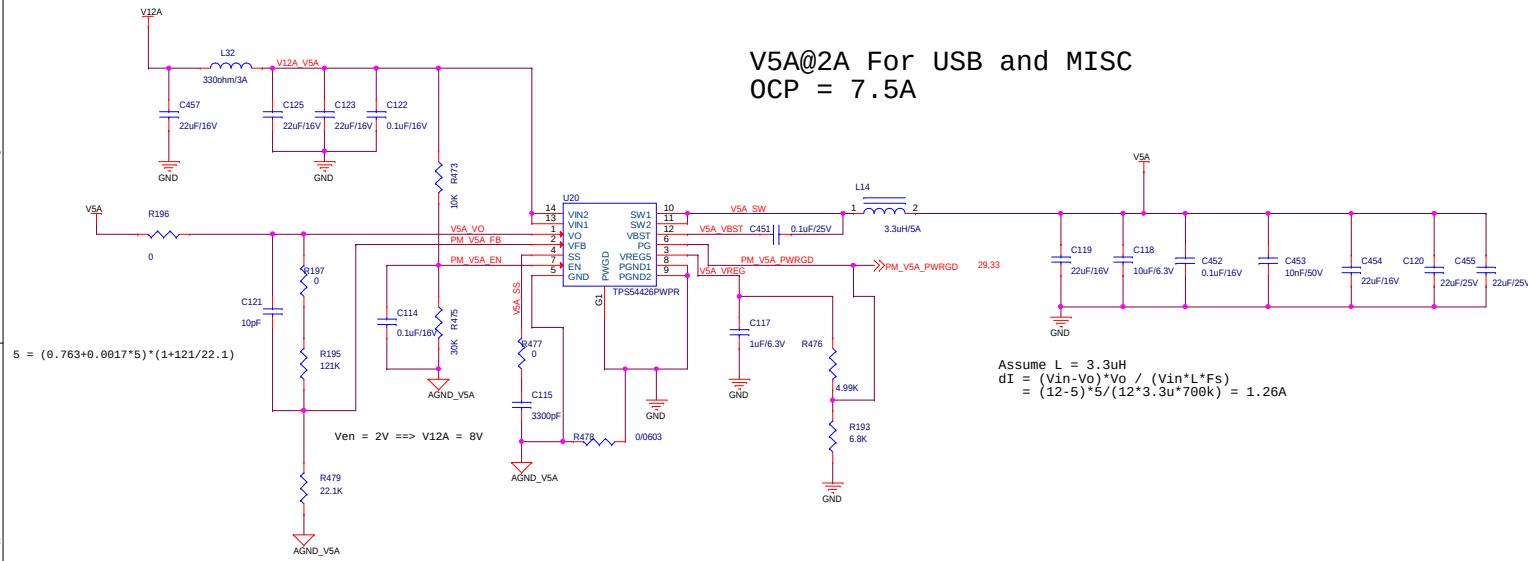


Accton Inc.

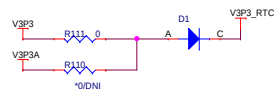
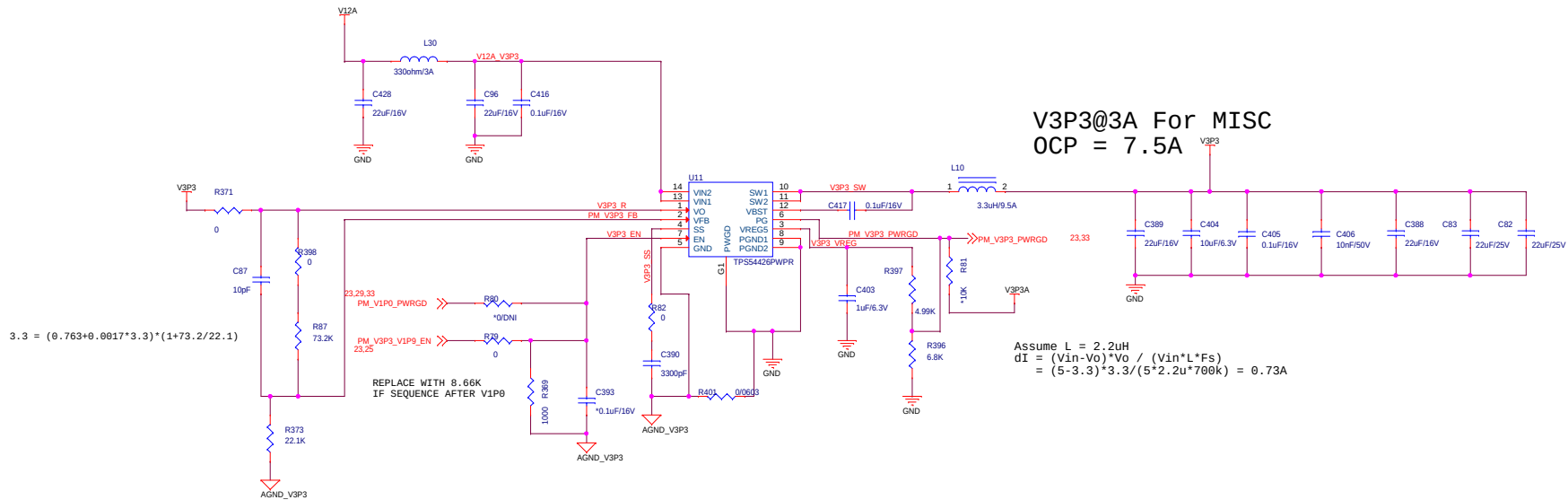
Making Partnership Work

Model Name		ES5654BT2-CPU-FLF-ZZ	Rev	R02
Size	Page Name	P30_V3P3A_V1P1	Engineer	
C			Jummy_Huang	
Date:	Tuesday, January 27, 2015	Sheet	30	of 33

V5A@2A For USB and MISC
OCP = 7.5A

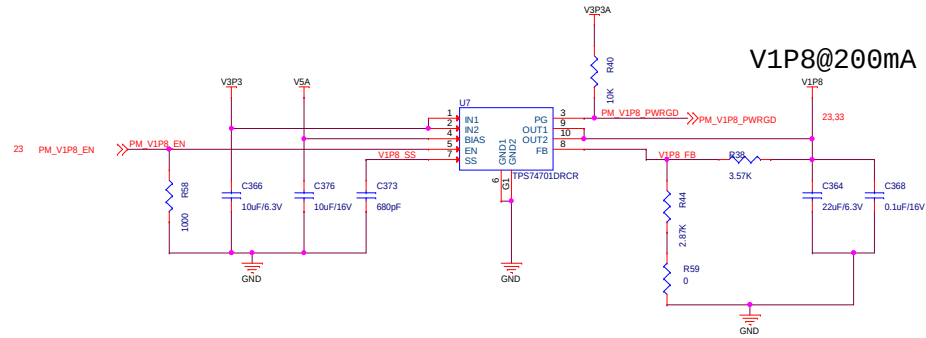


V3P3@3A For MISC
OCP = 7.5A

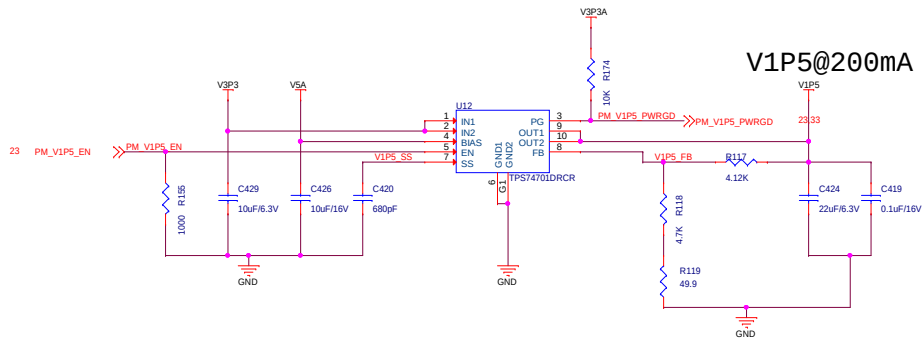


Accton Inc.
Making Partnership Work

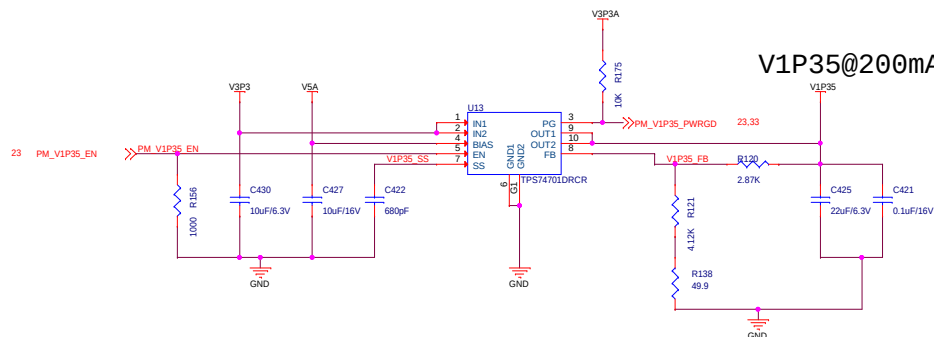
Model Name	ES56548T2-CPU-FLF-ZZ	Rev	R02
Page Name	P31_V5A_V3P3	Engineer	Jummy_Huang
Date	Tuesday, January 27, 2015	Sheet	31 of 33



$$1.8 = 0.8 * (1 + 3.57 / 2.87)$$

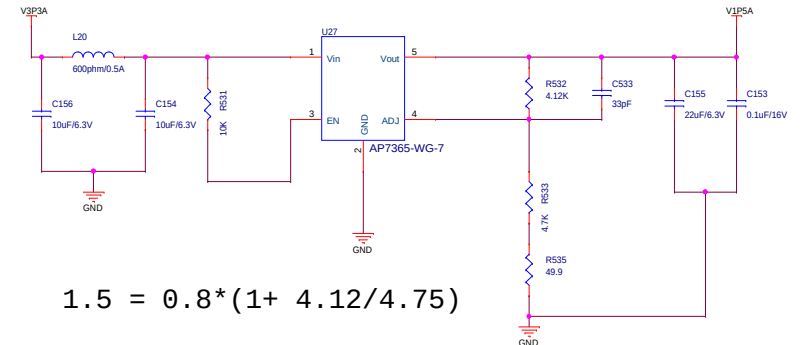


$$1.5 = 0.8 * (1 + 4.12 / 4.75)$$



$$1.35 = 0.8 * (1 + 2.87 / 4.12)$$

V1P5A@300mA for FPGA



$$1.5 = 0.8 * (1 + 4.12 / 4.75)$$



Accton Inc.
Making Partnership Work

Model Name			ES5654BT2-CPU-FLF-ZZ		Rev R02	
Size	C	Page Name P32_LDO			Engineer Jummy_Huang	
Date:	Tuesday, January 27, 2015			Sheet	32	of 33

Sequence

1. V5A / V3P3A
2. V1P5A
3. V1P0
4. V1P1 / VDDQ/VTT...else power

