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History

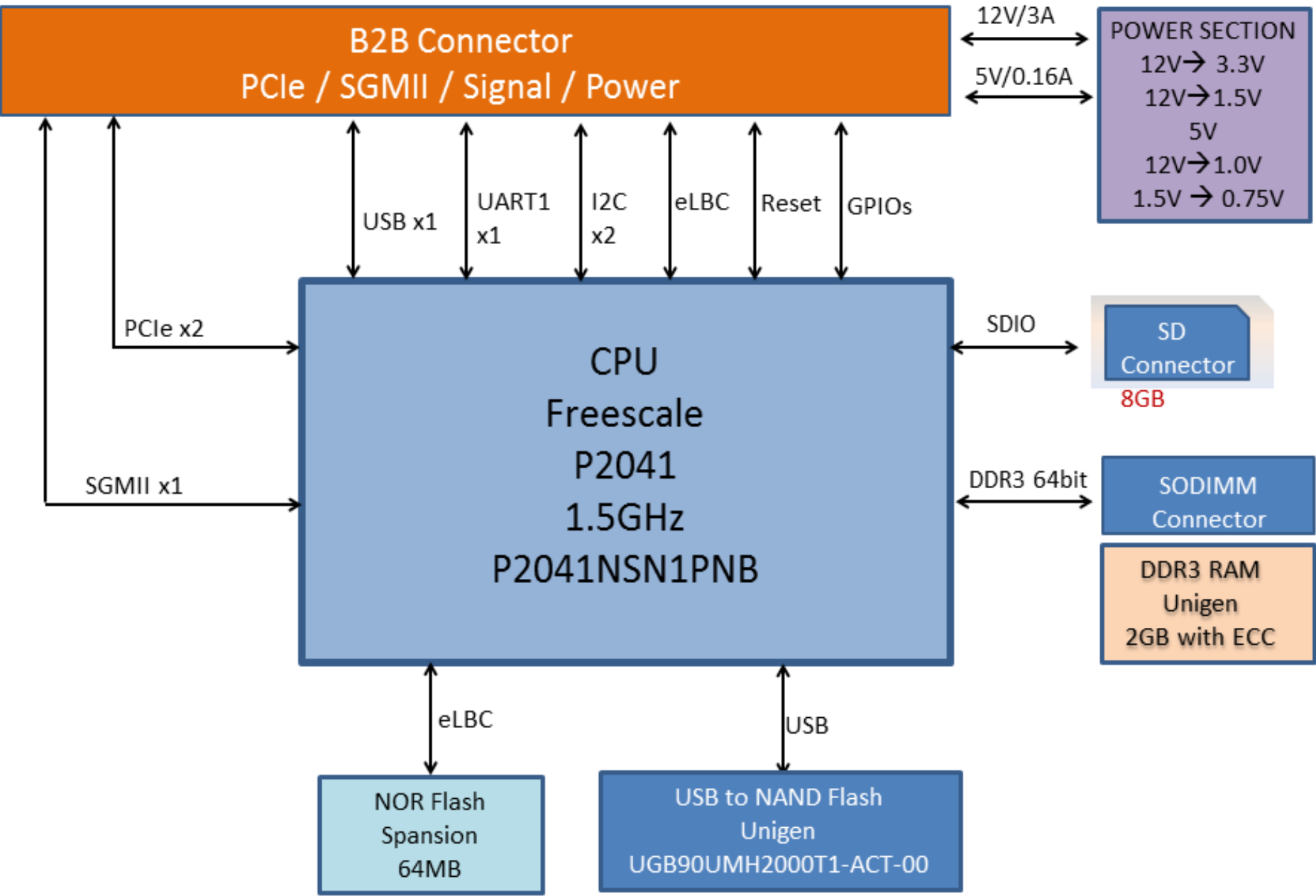
SCH Version	Date	Description
P1A	2013/03/21	Initial Version

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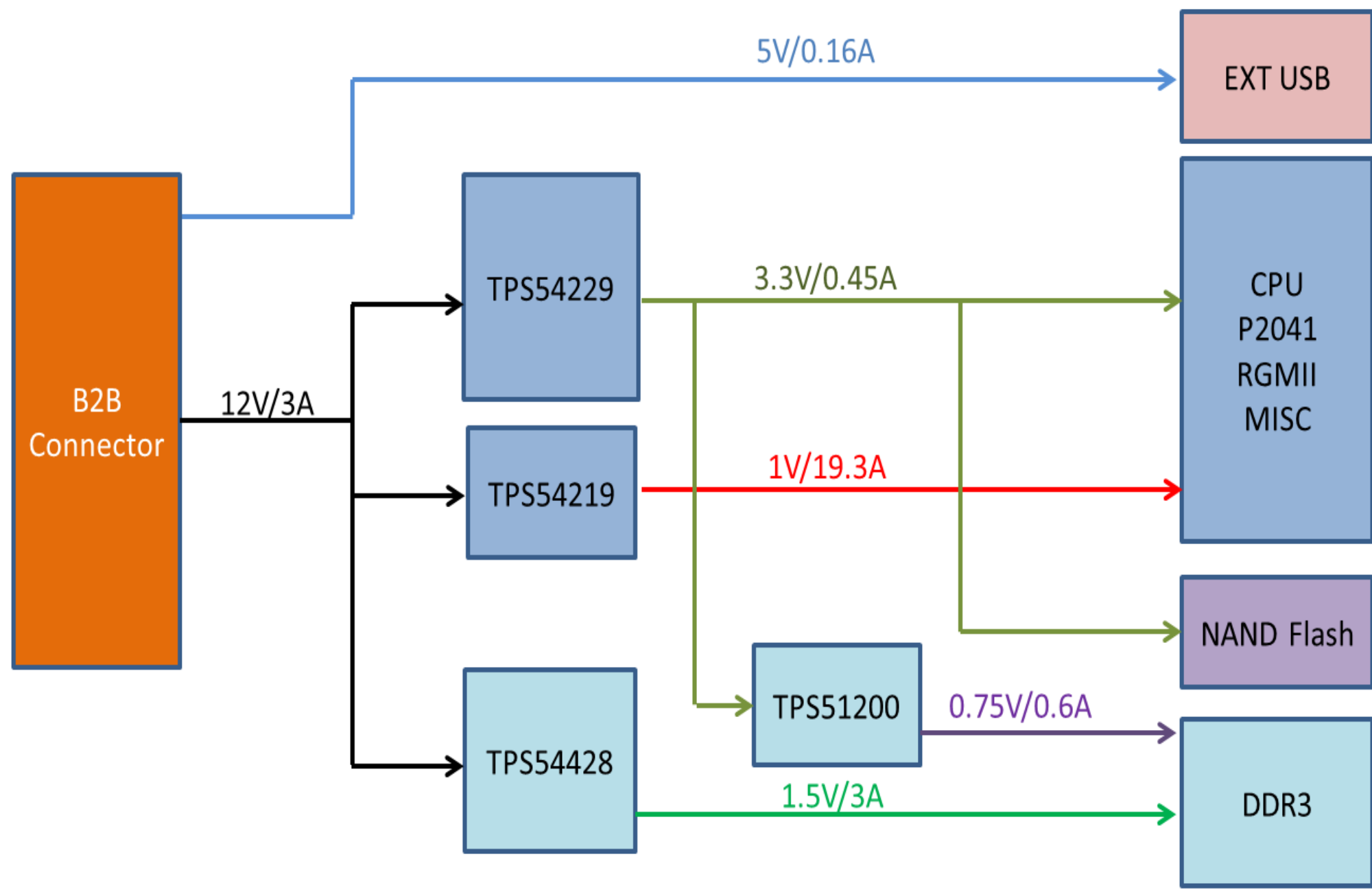


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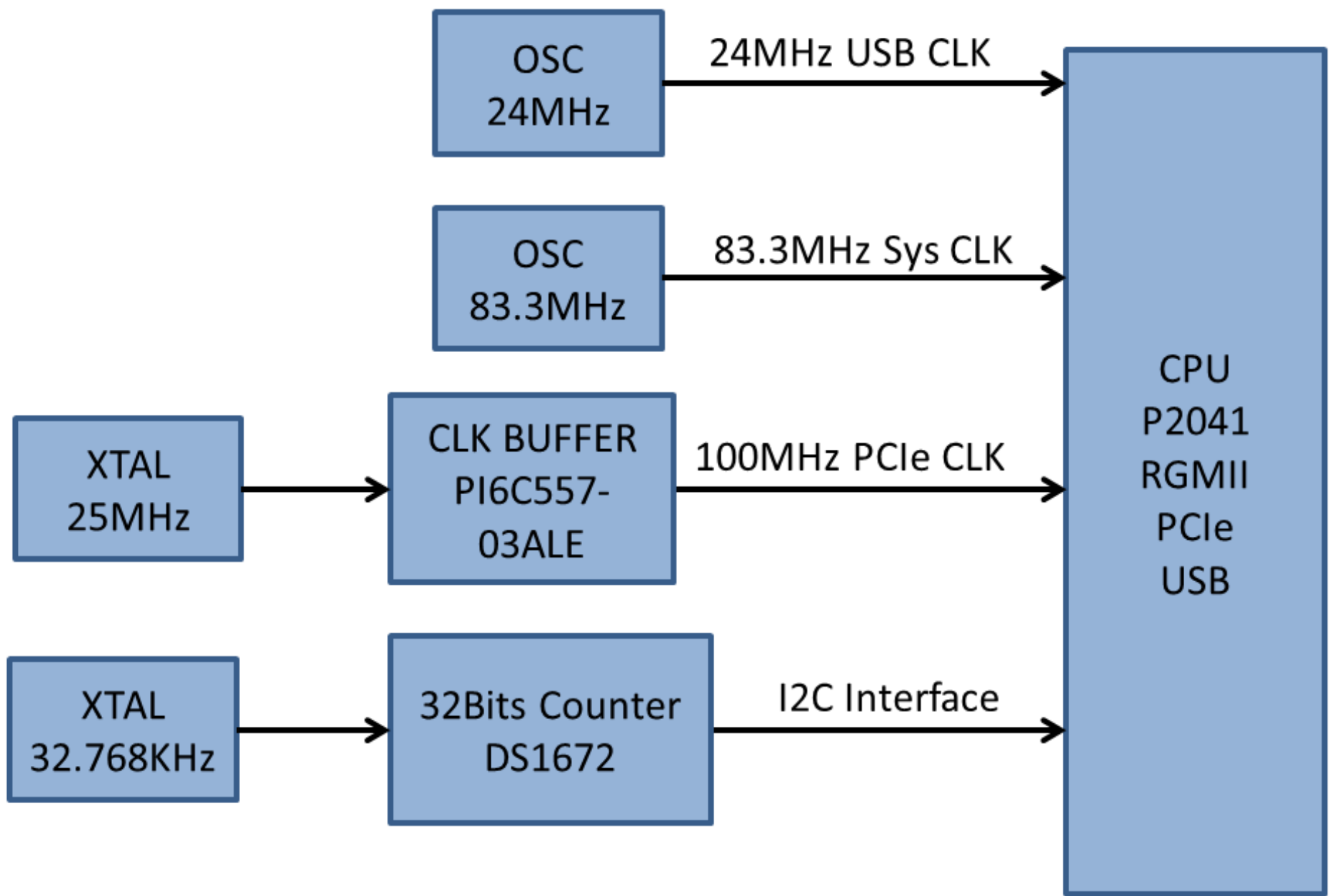
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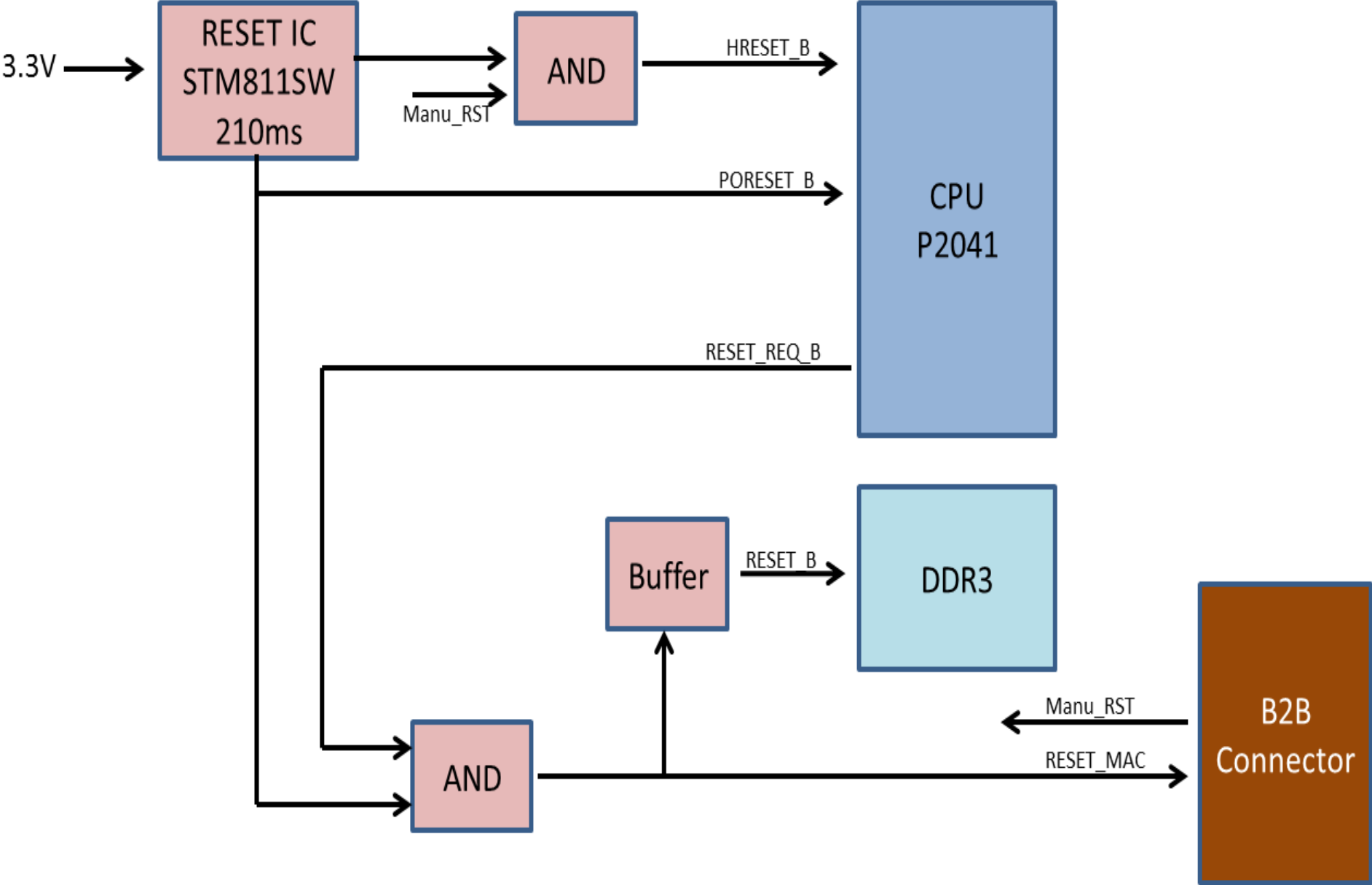
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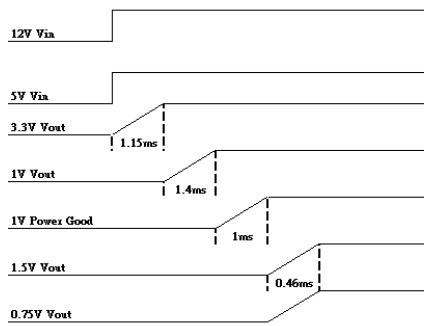
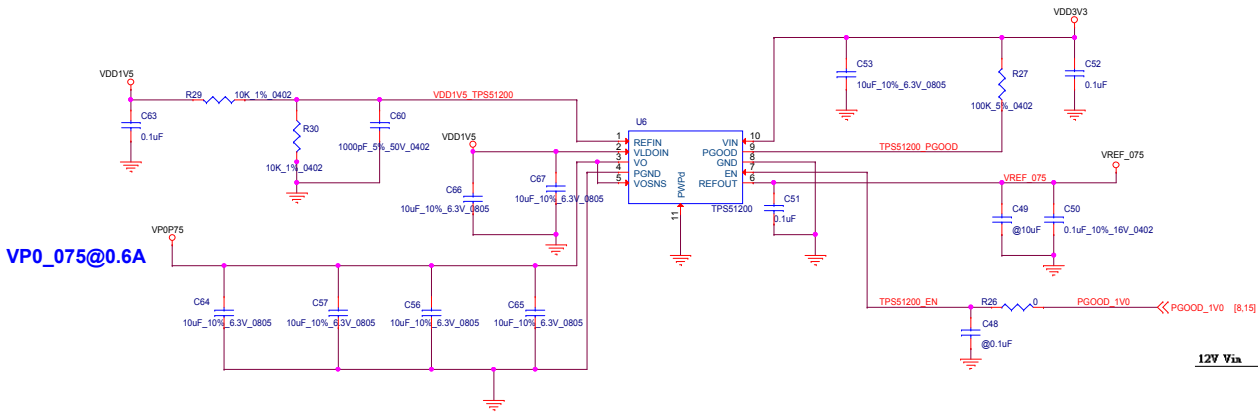
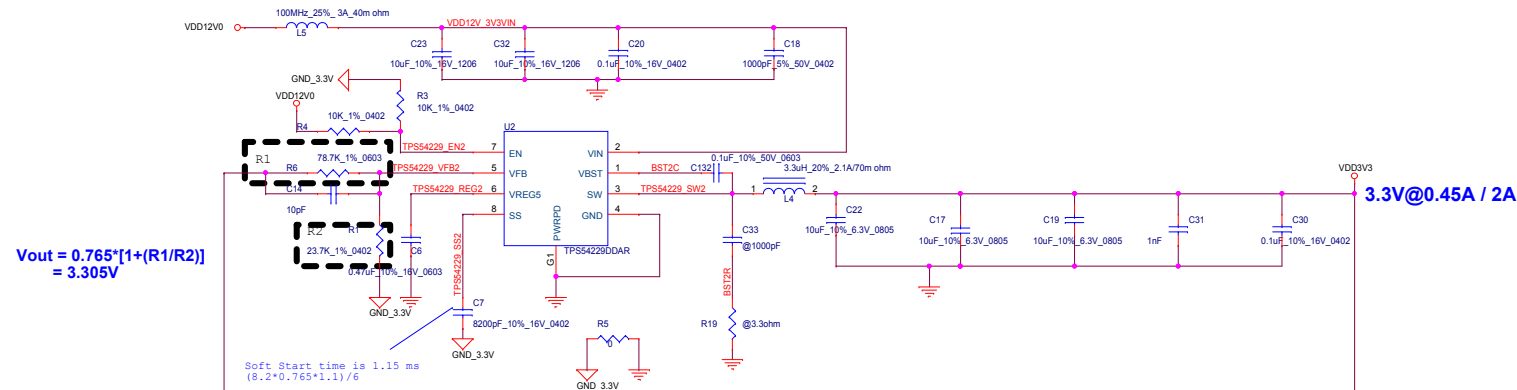
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- Power Up Sequency
1. Bring up OVDD, LVDD, BVDD, CVDD, and USB_VDD_3P3.

<< 3.3V
2. Bring up VDD_CA_CB_PL, SVDD, AVDD, and USB_VDD_1P0.

<< 1.0V
3. Bring up GVDD(DDR) and XVDD.

<< 1.5V



2.2 Power Up Sequencing

The device requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

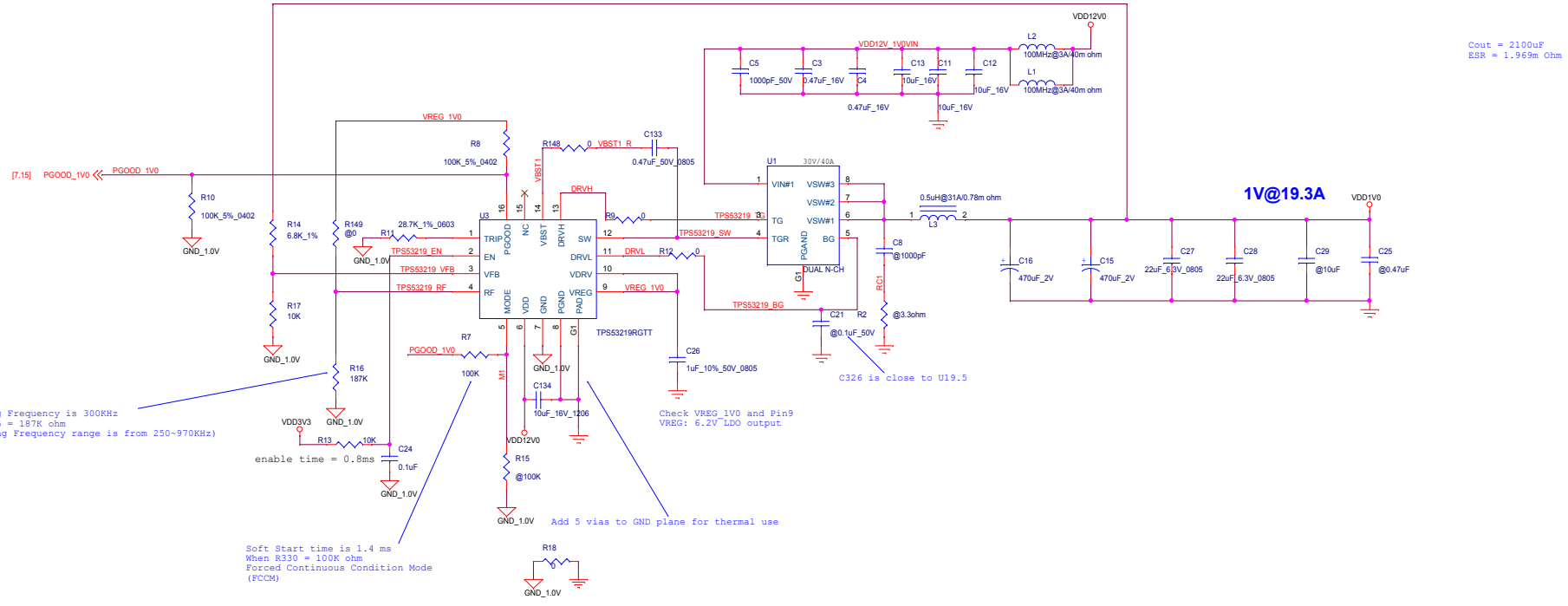
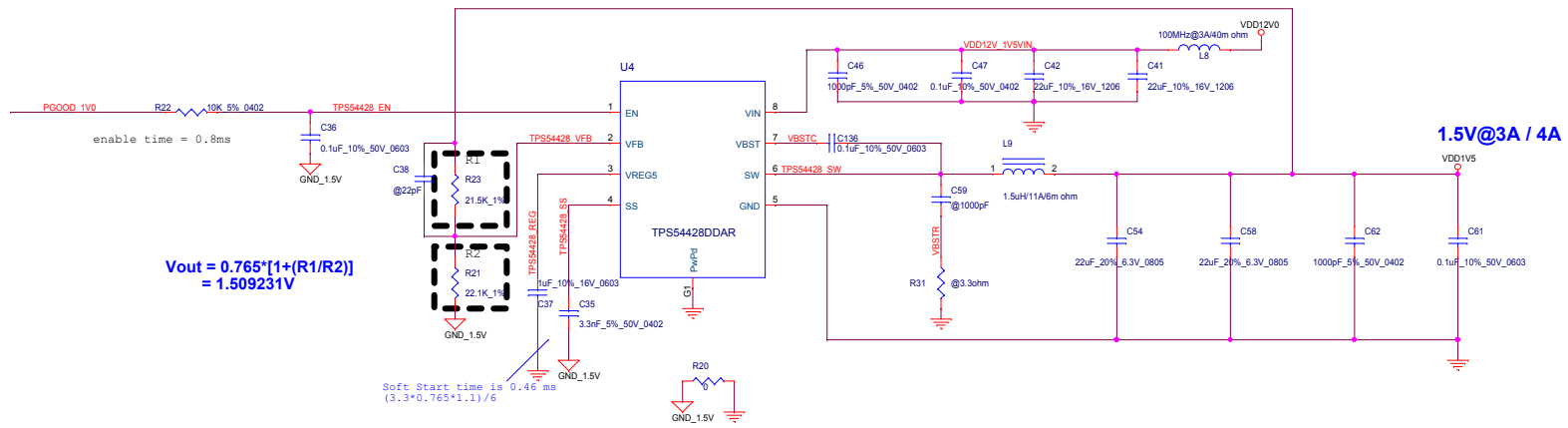
1. Bring up OV_{DD}, LV_{DD}, BV_{DD}, CV_{DD}, and USB_V_{DD}_3P3. Drive POV_{DD} = GND.

— PORESET input must be driven asserted and held during this step.

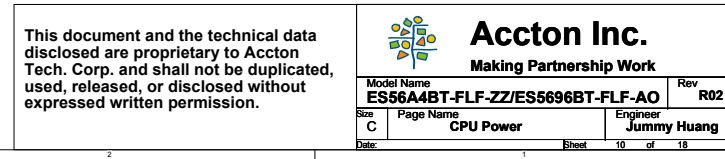
— IO_VSEL inputs must be driven during this step and held stable during normal operation.

— USB_V_{DD}_3P3 rise time (10% to 90%) has a minimum of 350 μs.
2. Bring up V_{DD}_CA_CB_PL, SV_{DD}, AV_{DD} (cores, platform, SerDes) and USB_V_{DD}_1P0. V_{DD}_CA_CB_PL and USB_V_{DD}_1P0 must be ramped up simultaneously.
3. Bring up GV_{DD} (DDR) and XV_{DD}.
4. Negate PORESET input as long as the required assertion/hold time has been met per Table 16.

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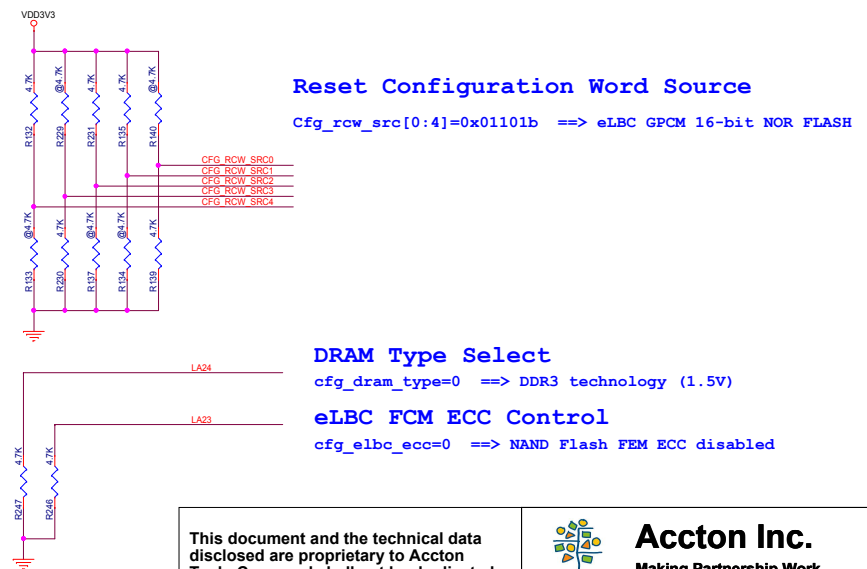
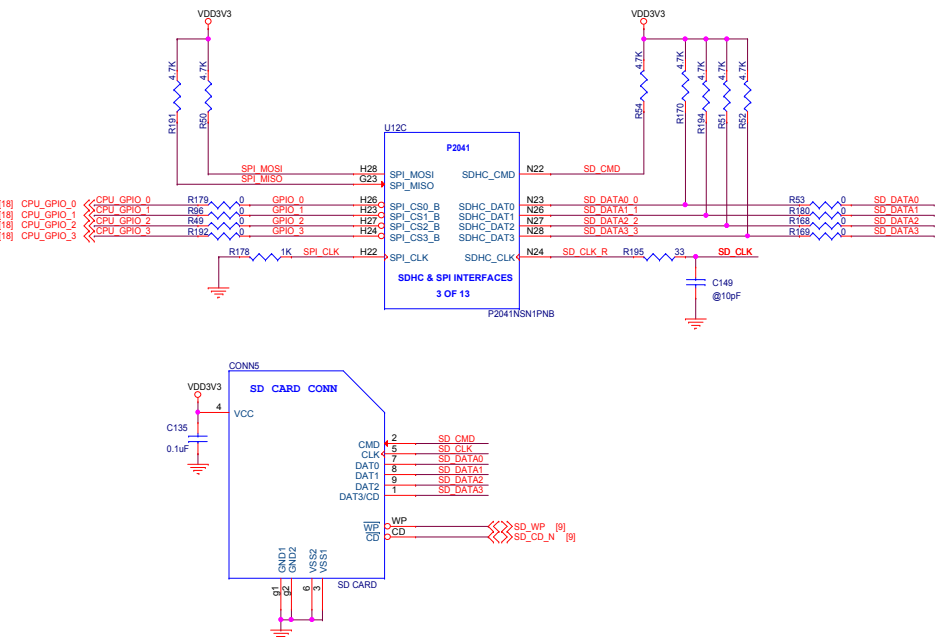
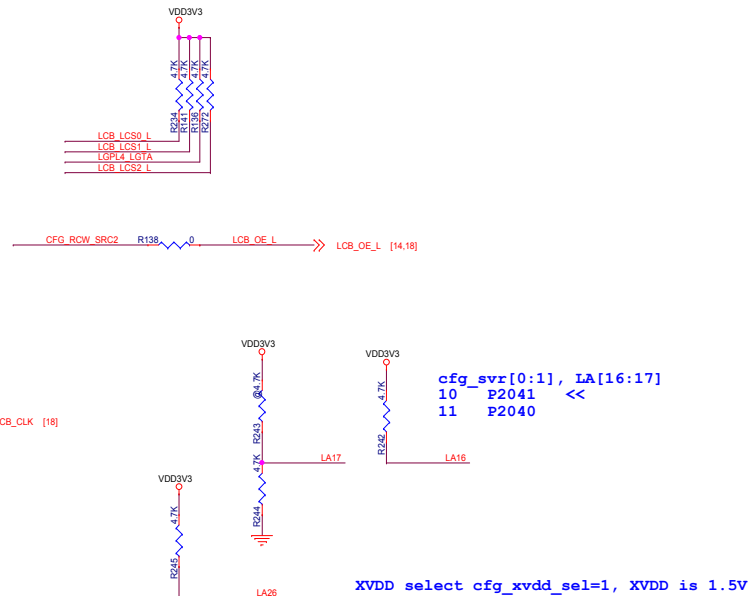
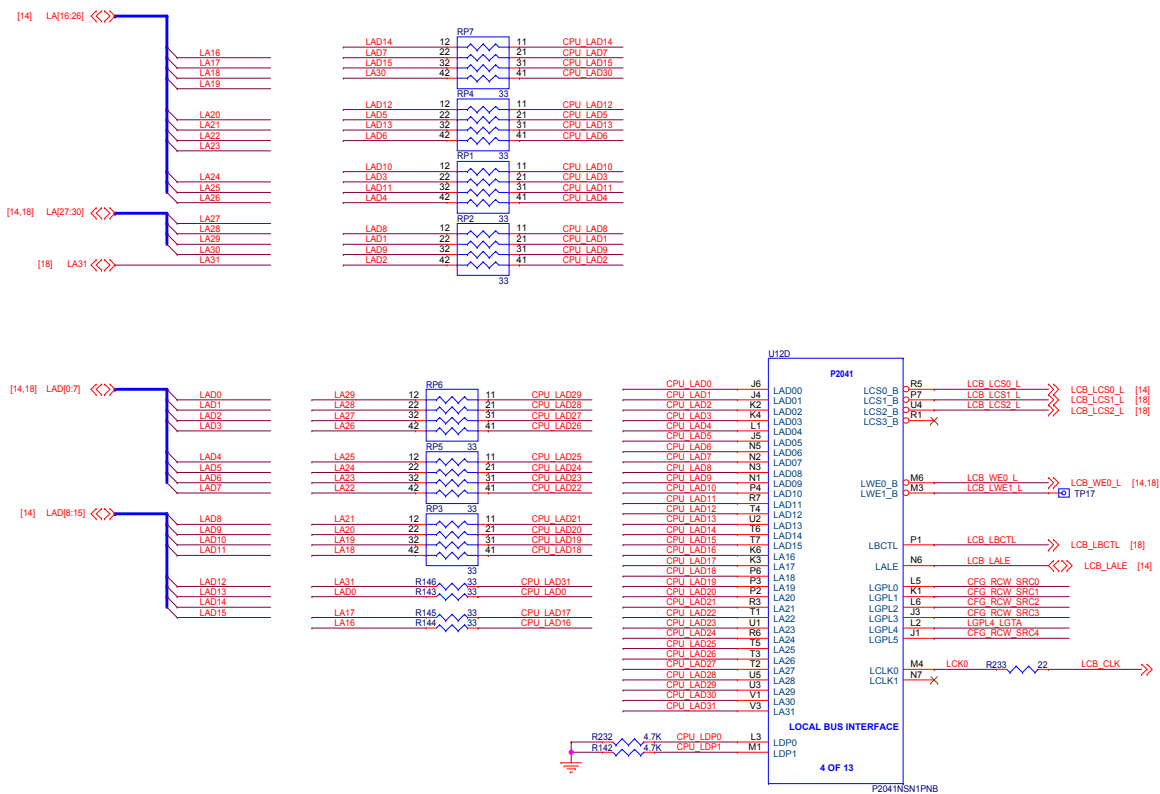


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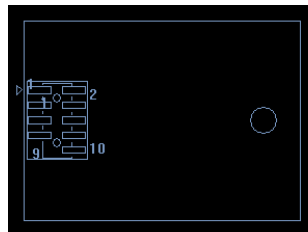




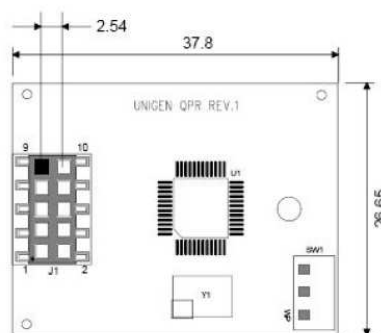
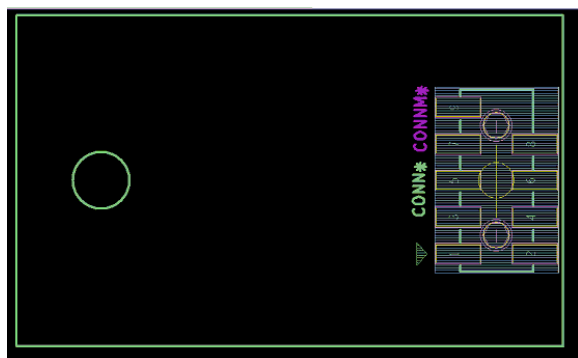
5	4	3	2	1
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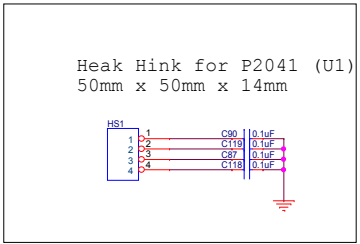
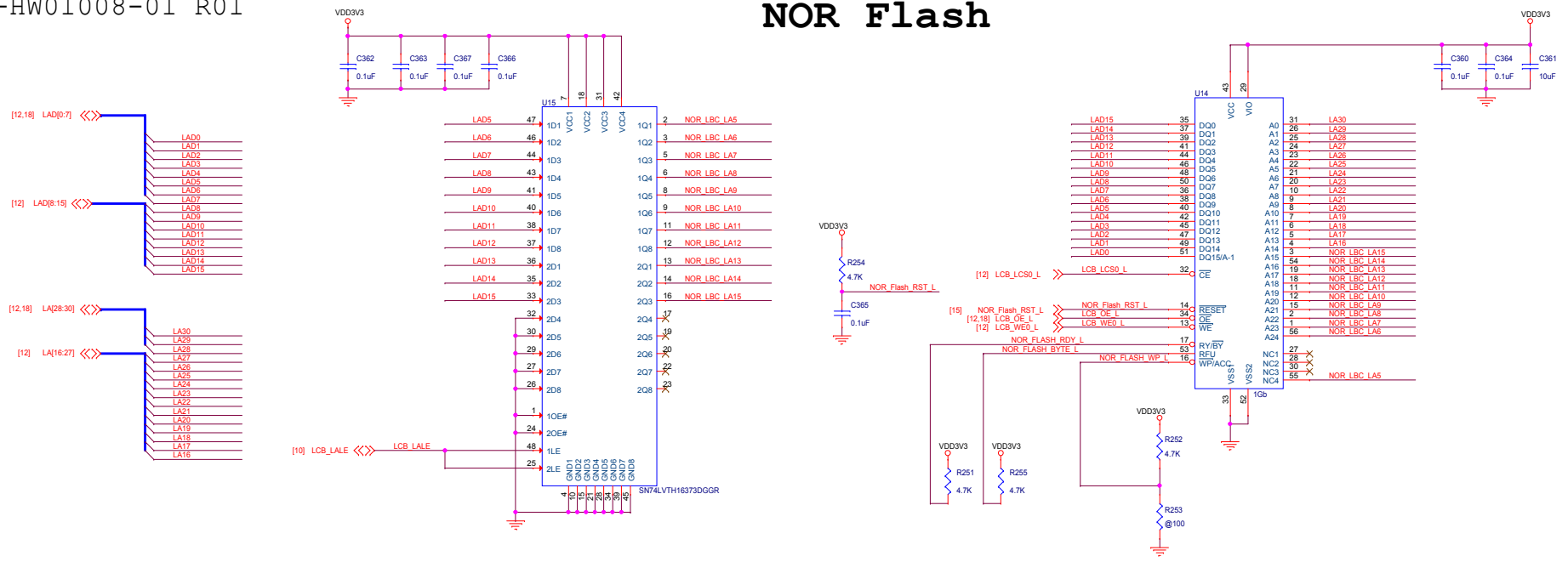


Pin No.	Signal	Signal Types	Function
1	VCC	PWR	Input Power
3	D-	I/O	Differential Signal
5	D+	I/O	Differential Signal
7	VSS	GND	Ground
9			Key
2, 4, 6, 8		NC	No Connect
10	LED	I/O	Activity



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NOR Flash



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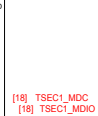


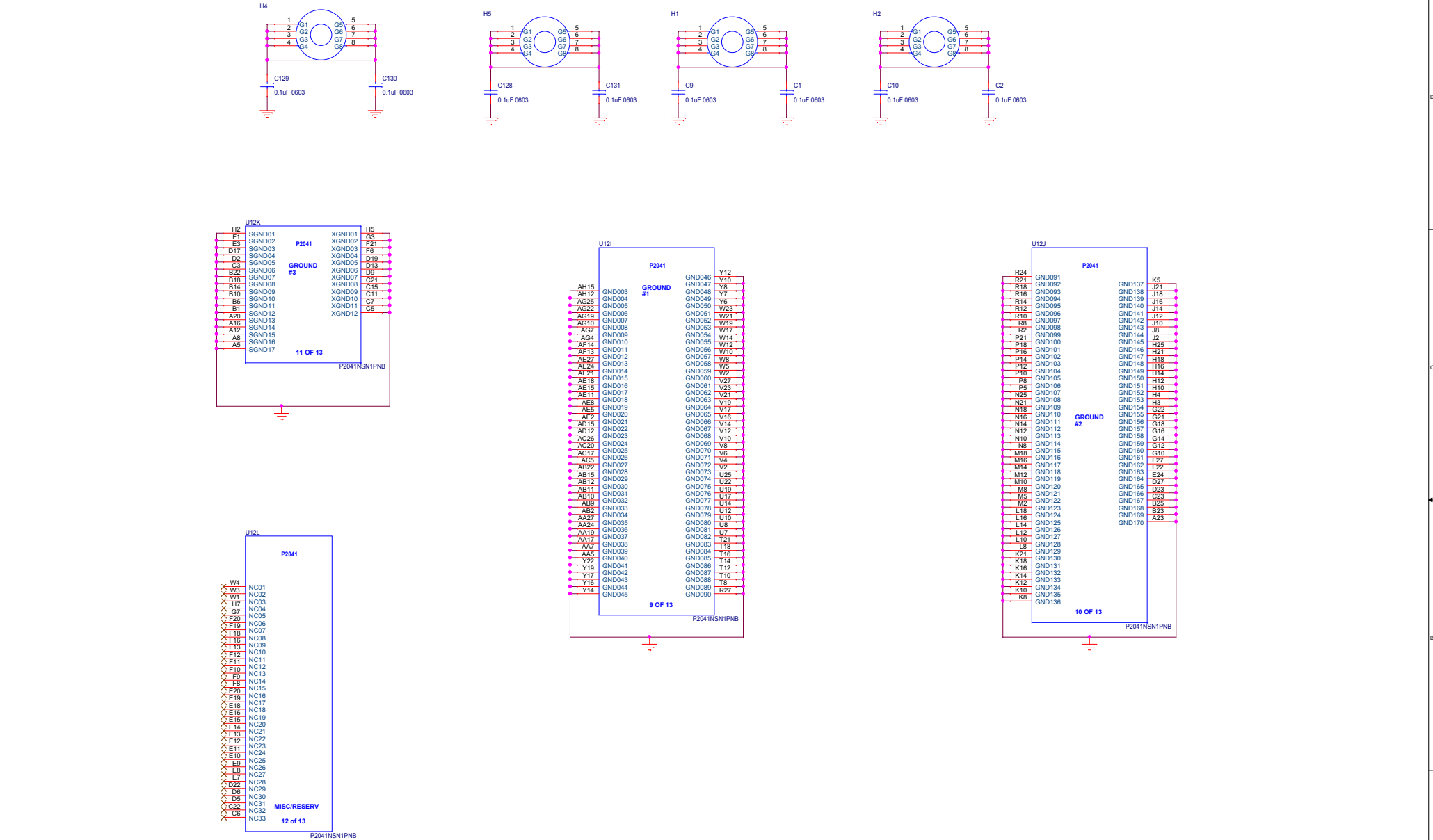
Figure 4-22. Power-On Reset Sequence

Table 16. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit ¹	Note
Required assertion time of PORESET	1	—	ms	3
Required input assertion time of HRESET	32	—	SYCLKs	1, 2
Input setup time for POR configs with respect to negation of PORESET	4	—	SYCLKs	1
Input hold time for all POR configs with respect to negation of PORESET	2	—	SYCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET	—	5	SYCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.
2. The device asserts HRESET as an output when PORESET is asserted to initiate the power-on reset process. The device releases HRESET sometime after PORESET is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1, "Power-On Reset Sequence," in the chip reference manual.
3. PORESET must be driven asserted before the core and platform power supplies are powered up. Refer to [Section 2.2, "Power Up Sequencing."](#)



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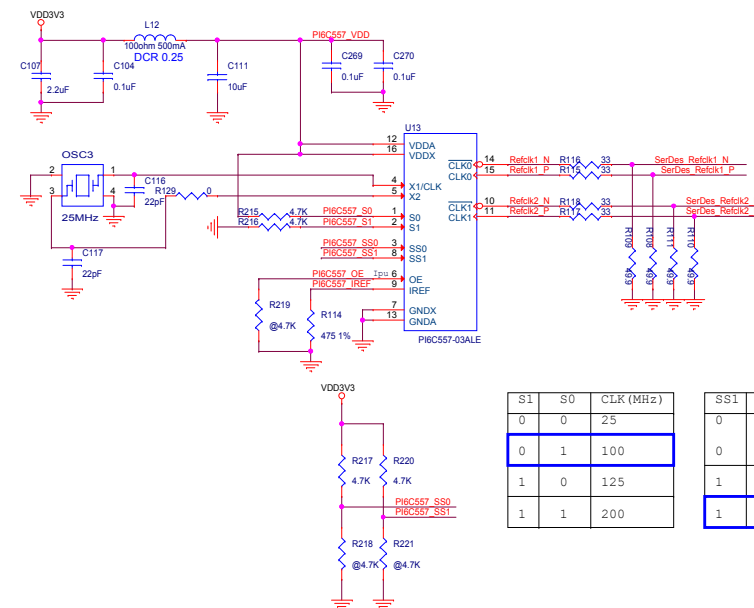
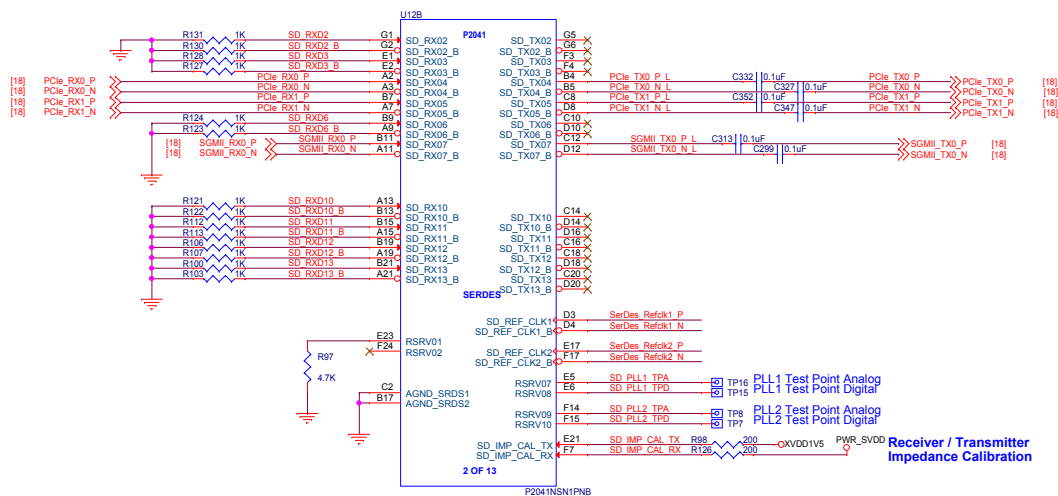


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Table 4. P2040/P2041 SerDes lane multiplexing/configuration (continued)

SRDS. PRCTL	Bank 1						Bank 2			
	C	D	E	F	G	H	A	B	C	D
0x14	SGMII1 (1.25G)	SGMII2 (1.25G)	PCIE2 (5/2.5G)		sRIO1 (5/2.5G)		Debug (5/3.125/ 2.5G)	SGMII5 (1.25G or 3.125G) †	SGMII3 1.25G or 3.125G) †	SGMII4 1.25G 3.125G
0x15	SGMII1 (1.25G)	SGMII2 (1.25G)	PCIE2 (5/2.5G)	sRIO2 (5/2.5G)	sRIO1 (5/2.5G)				SATA1 (3/1.5G)	SATA2 (3/1.5G)
0x16	PCIE1 (5/2.5G)	PCIE3 (5/2.5G)	PCIE2 (5/2.5G)		SGMII3 (1.25G)	SGMII4 (1.25G)			SATA1 (3/1.5G)	SATA2 (3/1.5G)
0x17	PCIE1 (5/2.5G)	PCIE3 (5/2.5G)	PCIE2 (5/2.5G)		SGMII3 (1.25G)	SGMII4 (1.25G)	XAUI 10GEC (P2041 only, P2040 does not support 10GEC)			
0x18	PCIE1 (5/2.5G)	PCIE3 (5/2.5G)	sRIO2 (5/2.5G)		SGMII3 (1.25G)	SGMII4 (1.25G)			SATA1 (3/1.5G)	SATA2 (3/1.5G)



S1	S0	CLK (MHz)	SS1	SS0	Spread
0	0	25	0	0	Center +/- 0.2
0	1	100	0	1	Down -0.5
1	0	125	1	0	Down -0.75
1	1	200	1	1	No Spread

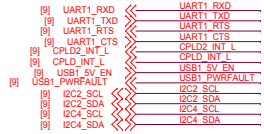
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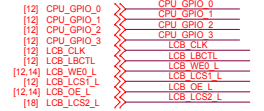
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P09_CPU_MISC



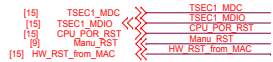
P12_CPU_LOCAL_BUS



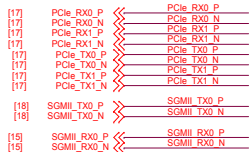
P13_CPU USB & NAND FLASH



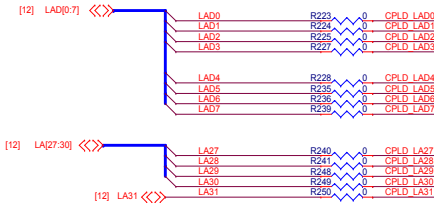
P15_CPU Ethernet & Reset



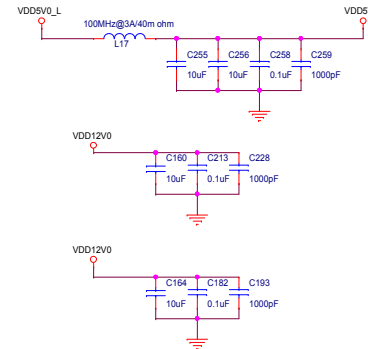
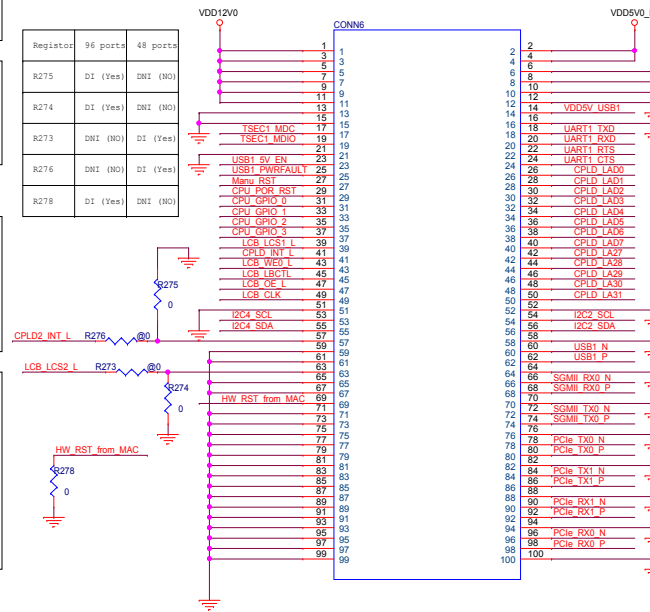
P17_CPU_PCIE



P12_CPU_LOCAL_BUS



Register	96 pins	48 pins
R275	DI (Yes)	DNI (NO)
R274	DI (Yes)	DNI (NO)
R273	DNI (NO)	DI (Yes)
R276	DNI (NO)	DI (Yes)
R278	DI (Yes)	DNI (NO)



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