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Size	Page Name	Engineer
B	Table of Content	Chaohua_Chung

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Rev	Date	Author	Revision Description
R0A	2015/01/29	Chaohua_Chung	1. Initial Draft
	2015/02/17	Chaohua_Chung	1. Add PoE capacitance : Add C437, C457 (47uF) into BOM
R0B	2015/02/17	Chaohua_Chung	1. Modify BCM59121 PG schematic : Modify entire net name from CPLD_BCM_RST_L to CPLD_BCM_PoE_PG1 signal and connect to BCM59121 PGOOD1 Add photo coupler U139 schematic for connecting CPLD_BCM_PoE_PG0 signal
	2015/03/24	Chaohua_Chung	1. Change X'FMR : From TAG(115500000068H) to M-TEK(115500000051A) 2. Remove fan 2 connector : Marked CONN2 3. Change micro-USB connector : From 119000000080A to 119000000103A
	2015/04/22	Chaohua_Chung	1. Change X'FMR : From M-TEK(115500000051A) to TAG(115500000068H) 2. VCC33_TPS53353 schematic : Change L16, L17(102100000049A) to R1596, R1597 (20000000JM40A)(0ohm 0603) Add R1598 (20000000JM40A)(0ohm 0603) between 12V and chip VDD pin
	2015/04/29	Chaohua_Chung	1. Modify BCM59121 PG schematic : Remove photo coupler U139 schematic
	2015/05/05	Chaohua_Chung	1. Modify 2x6 1G cage footprint for DIP process: Change from "rj45_2x6x8dp_28d5w87d13l_pip" to "rj45_2x6x8dp_28d5w87d13l_kin"
	2015/05/07	Chaohua_Chung	1. Change component : C1488, C1657, C1478, C1460, C1384, C1385, C1386, C1458, C1383, C1457, C1461, C1489 change from 2041029KF301J to 204000000533A
	2015/05/18	Chaohua_Chung	1. Modify VCC10_PHY voltage : R225 change from 200500000168A(14.3K ohm, 0402) to 20013020FN60E(13K ohm, 0402)
	2015/06/01	Chaohua_Chung	1. VCC33_TPS53353 schematic : Add R1599, R1600 placed on top(20000000JM40A)(0ohm 0603) 2. Remove switch that select boot from SPI or NAND : Remove SW2 (116300000031A) 3. Force to boot from SPI flash : Add R84 (20000000JN60A) 4. Remove CPU board connector : Remove CONN4 (119B00000080A) 5. Remove RESET button : Remove SW1, SW3 (116400000062A) 6. Remove NAND flash : Remove U4 (107300000034A)
R01A	2015/07/08	Chaohua_Chung	1. Modify eUSB description : From 114300000015A MODULE BOARD MTEDCAE002SAJ-1M2 eUSB NAND FLASH Micron to 114300000027A MODULE BOARD R4.7AC AF8GSSGH-AC3 8G eUSB SSD LT ATP
	2015/08/05	Chaohua_Chung	1.Update Block diagram 2. Change components : -C1383, -C1386, -C1457, -C1458, -C1461, -C1489 change from 204000000533A to 204000000554A 3. Change components : -C932, -C935, -C936, -C937, -C938, -C939, -C940, -C962, -C963, -C1141, -C1142 change from 204000000086A to 204000000555A

Rev	Date	Author	Revision Description

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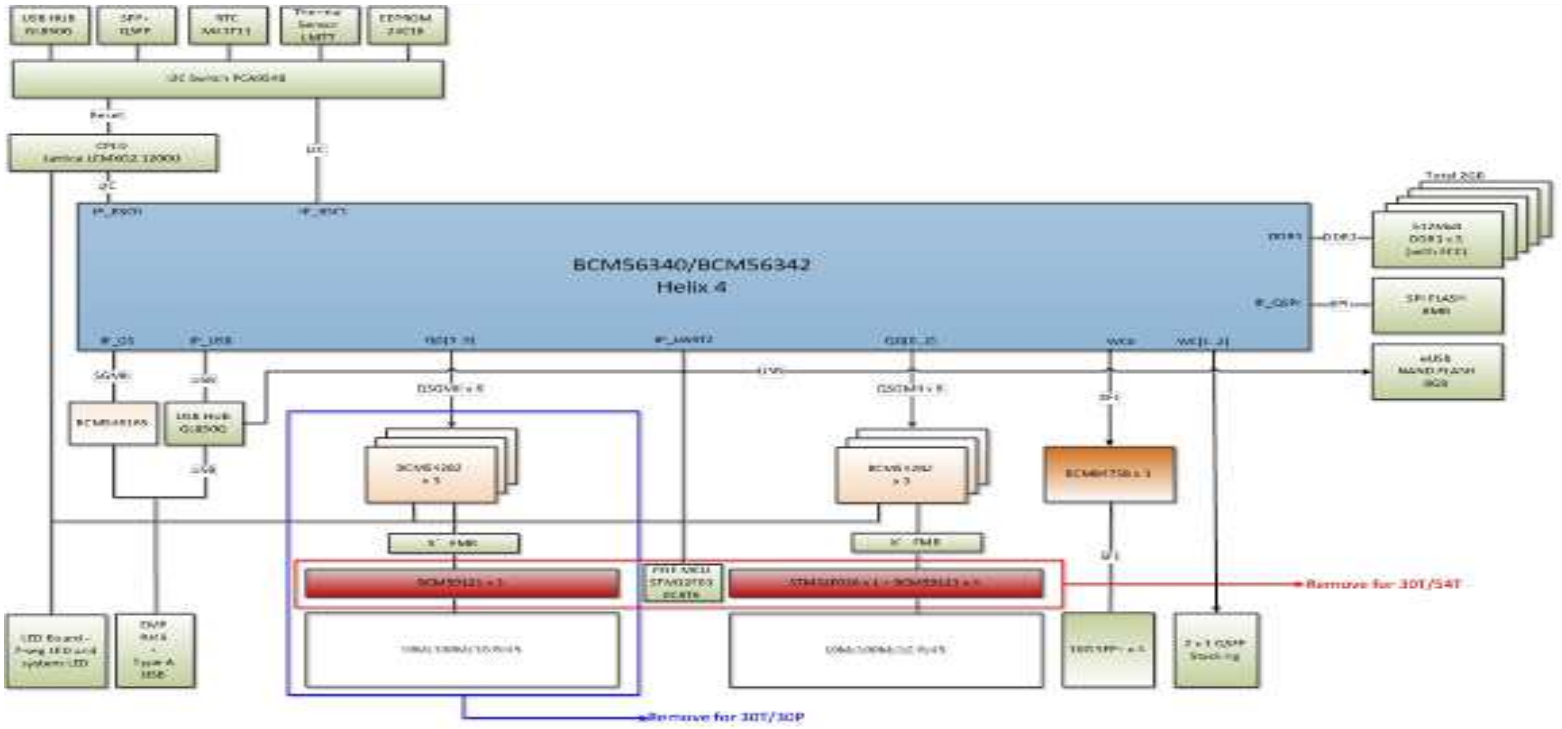
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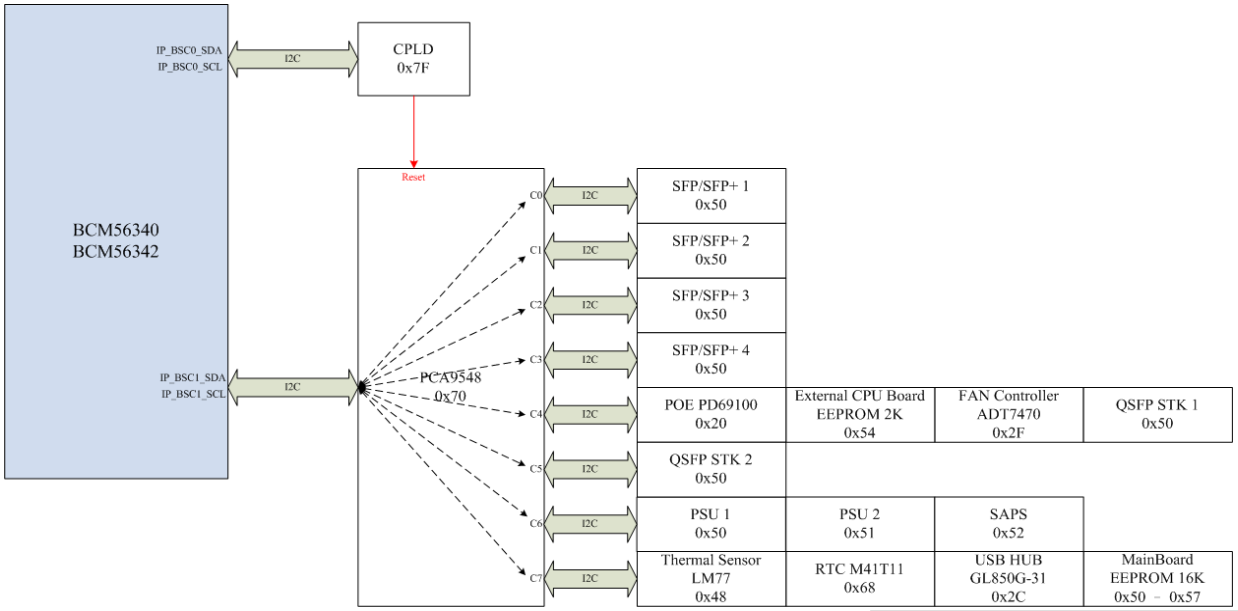
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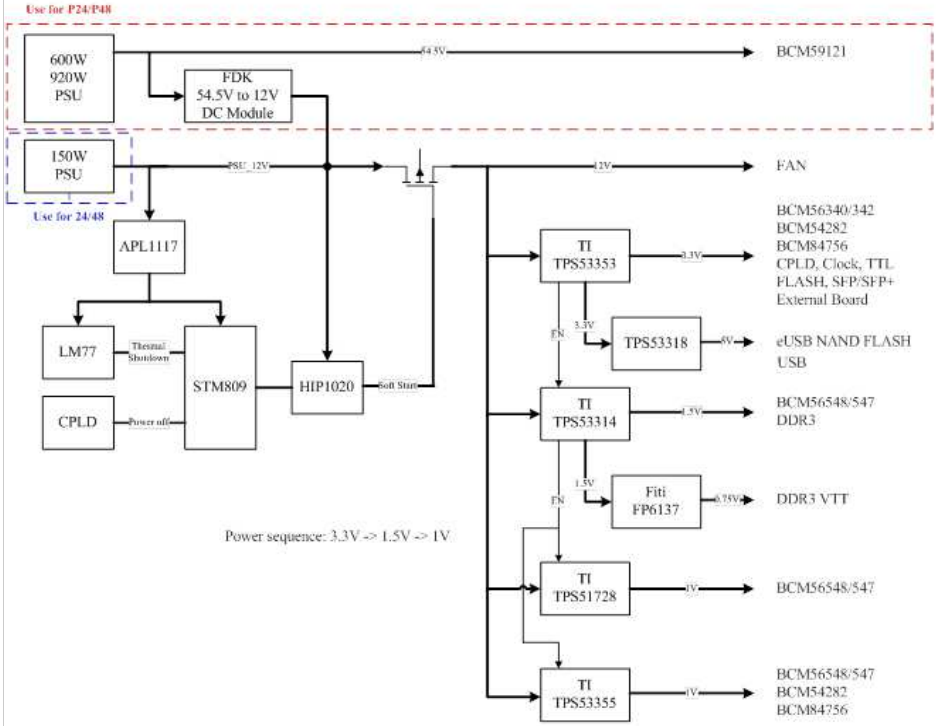
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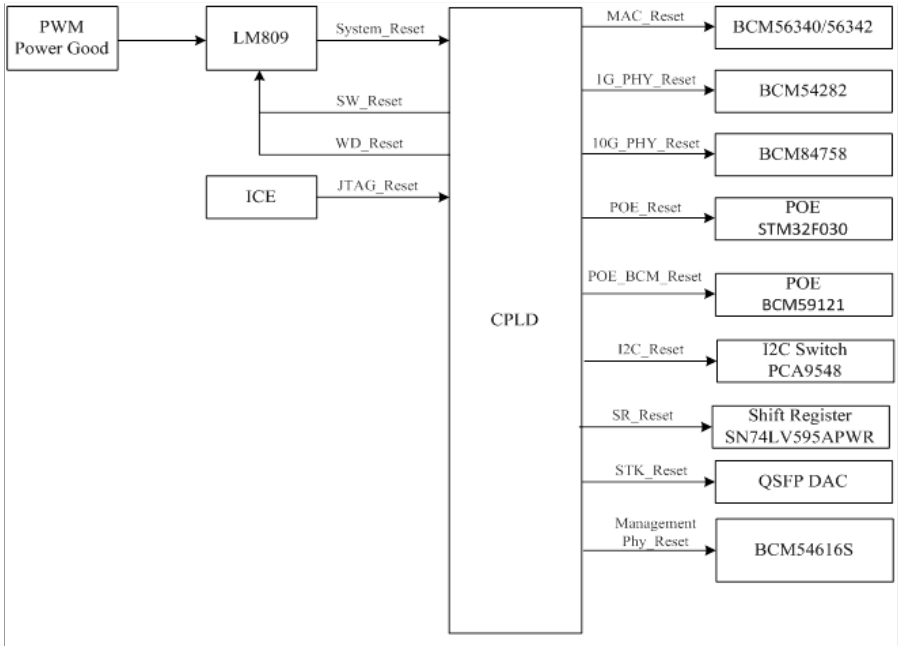
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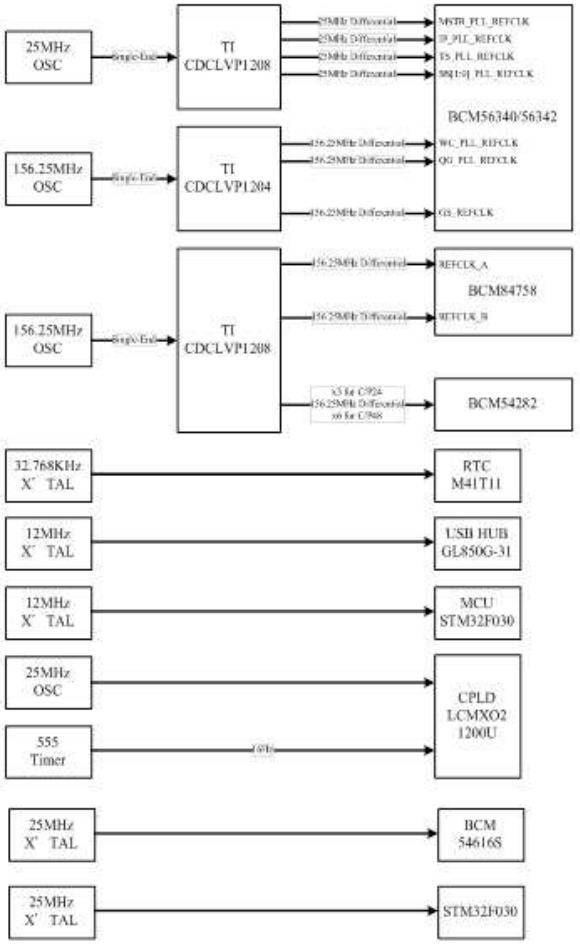
Model Name	Rev
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Size	Page Name	Engineer
C	Block_Diagram & I2C Mapping	Chaohua_Chung

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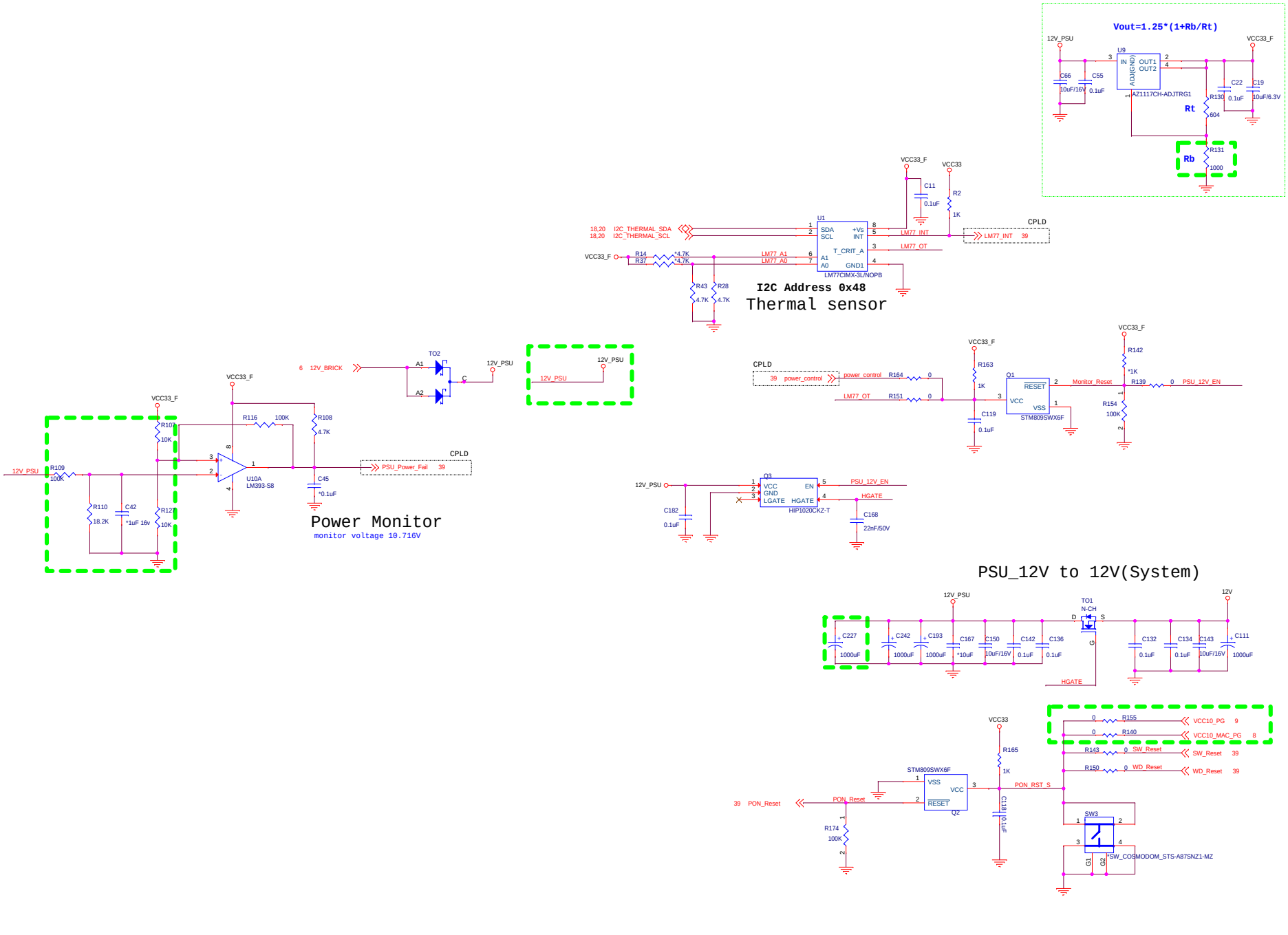
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Model Name	Rev
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C	Power/Clock/Reset_Tree	Chaohua_Chung

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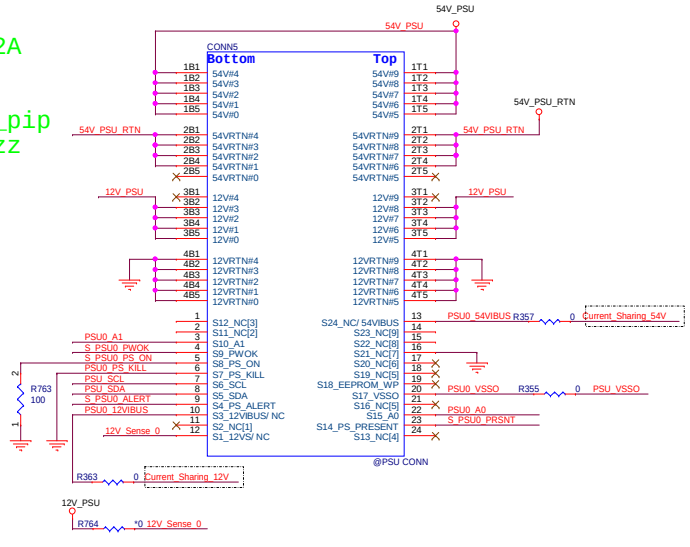
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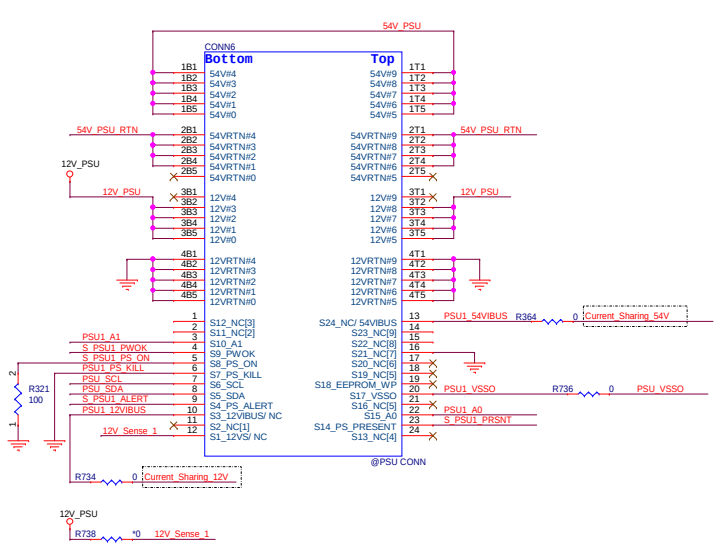
Size	Page Name	Engineer
C	12V_Power_Input	Chaohua_Chung

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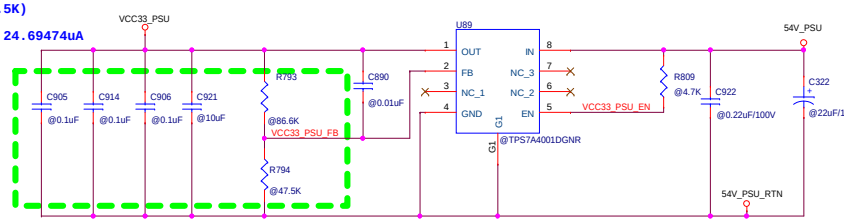
POE PSU connecter:118500000163A
Non-POE PSU connecter: 118500000162A

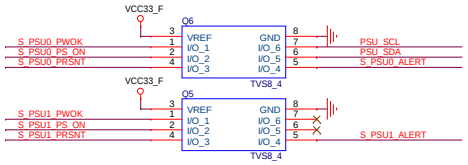
Special footprint for HI-POT :
original:conn_2d5_2d54_64dp_68d38w_pip
special:conn_2d5_2d54_64dp_68d38w_zz

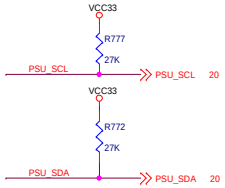


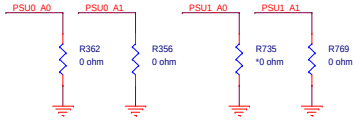


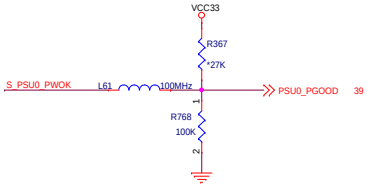
Vout=1.173*(1+R1/R2)
3.31156V=1.173*(1+86.6K/47.5K)
Vout / (R1+R2) > 10uA
3.31156V / (86.6K+47.5K) = 24.69474uA

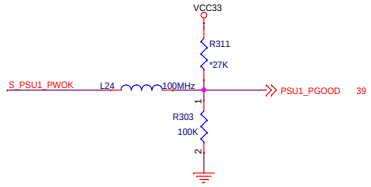








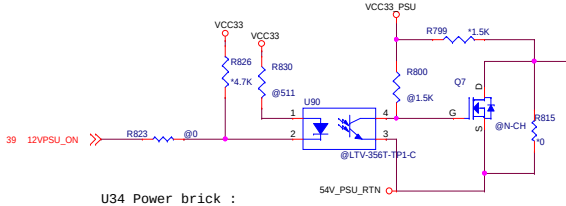




PWOK (Active high)
High -> PSU is Good
Low -> PSU is Fail

PS_ALERT (Active High)
High -> PSU Good
Low -> PSU Alert

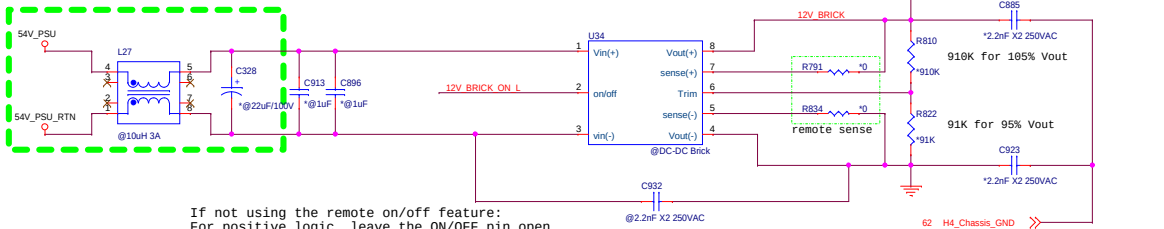
PS_ON (Active High)
High -> Power supply off
Low -> Power supply on



12VPSU_ON:
LOW --> 12V_BRICK_ON_L Open --> Turn off DC module
HIGH --> 12V_BRICK_ON_L LOW --> Turn on DC module

U34 Power brick :
main : 131400000036A
2nd : 131400000037A

Its footprint is different from database, it is for special PIPI process



If not using the remote on/off feature:
For positive logic, leave the ON/OFF pin open.
For negative logic, short the ON/OFF pin to VIN(-).

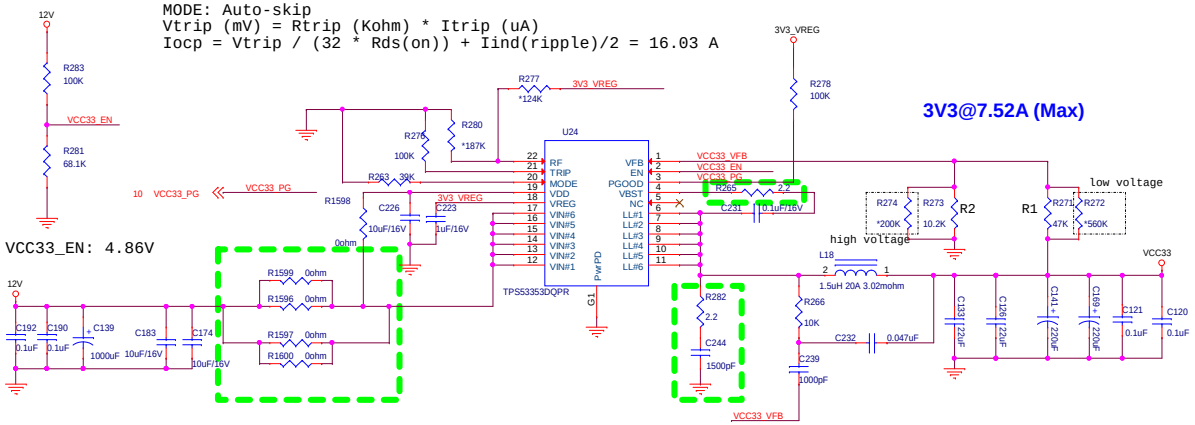
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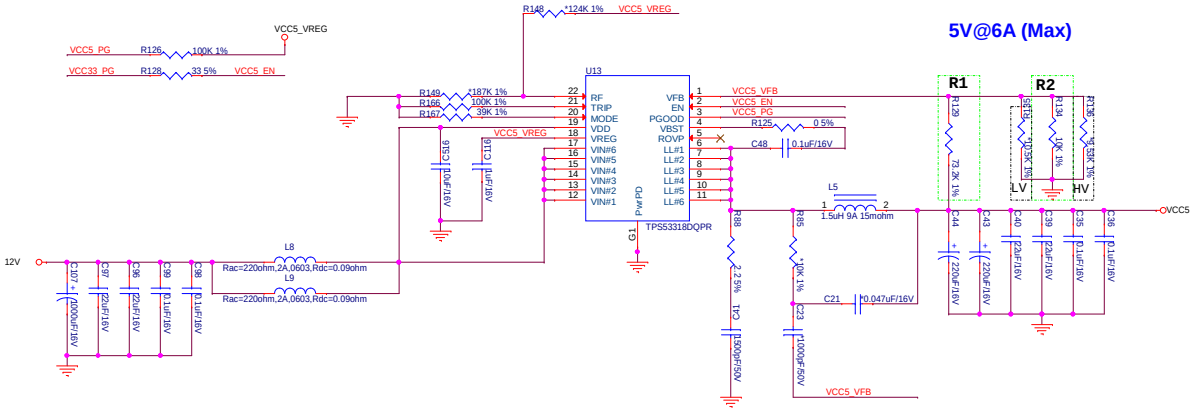
Model Name	AS4610	Rev	R01
Size	C	Page Name	54V_Power_Input
Engineer	Chaohua_Chung		
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Vout=0.6(1+R1/R2)
RF open, Switching frequency = 500 KHz
RF = 187 Kohm to GND, Switching frequency = 300KHz
MODE: Auto-skip
Vtrip (mV) = Rtrip (Kohm) * Itrip (uA)
Iocp = Vtrip / (32 * Rds(on)) + Iind(ripple)/2 = 16.03 A



R1	R2	Vout
73.2	10	4.992
73.2	9.53	5.208604
73.2	10.5	4.782857

Vout=0.6(1+R1/R2)
RF open, Switching frequency = 500 KHz
RF = 187 Kohm to GND, Switching frequency = 300KHz
MODE: Auto-skip
Vtrip (mV) = Rtrip (Kohm) * Itrip (uA)
Iocp = Vtrip / (32 * Rds(on)) + Iind(ripple)/2 =



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Model Name	Rev
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Size	Page Name	Engineer
C	VCC33 & VCC5	Chaohua_Chung

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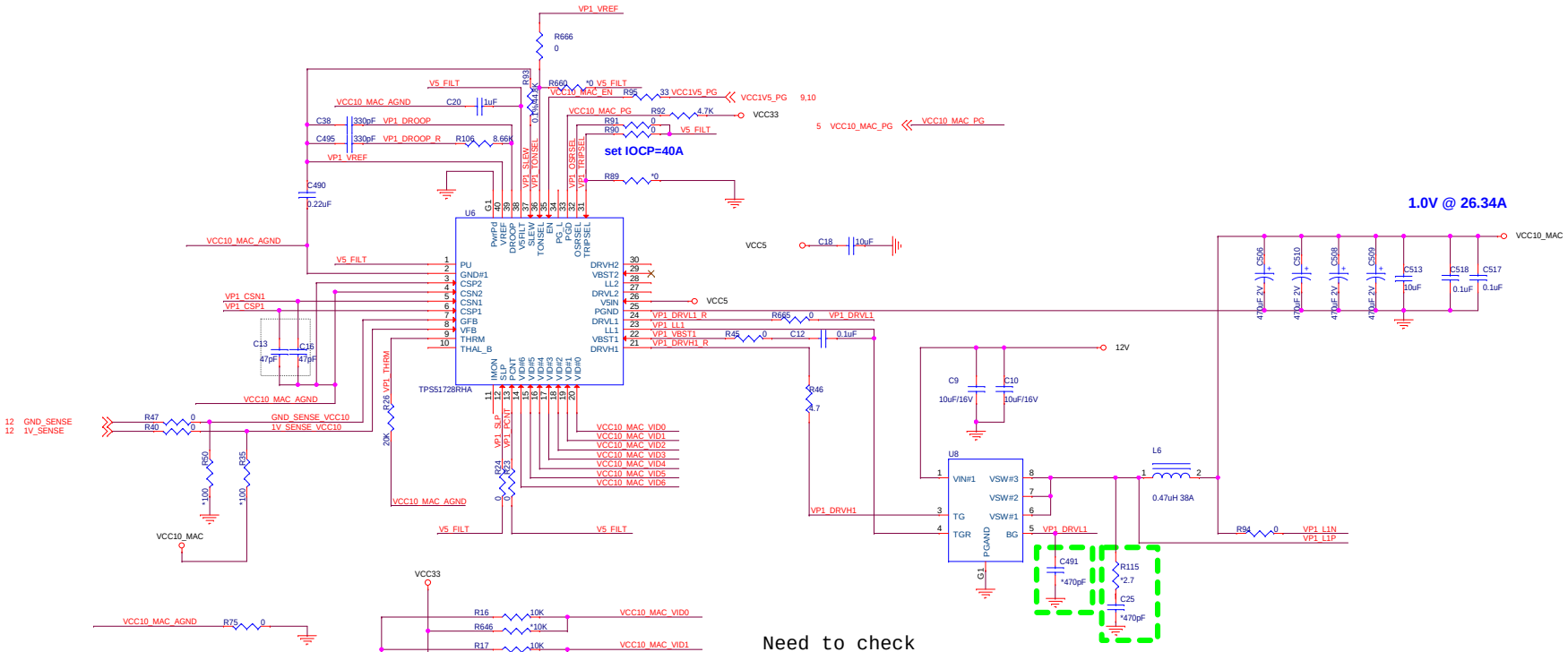


Table 5. VID Table

VID							V_{DAC} (V)
6	5	4	3	2	1	0	
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375

Table 26: Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
1.00V ±2%, Core Voltage	–	0.980	1.00	1.020	V
0.95V ±2%, Core Voltage (ROV)	–	0.931	0.95	0.969	V
1.025V ±2%, Core Voltage (BCM56344)	–	1.005	1.025	1.045	V
1.00V ±3%, Analog Voltage	–	0.970	1.00	1.030	V
1.20V ±3%, MIIM Voltage	–	1.164	1.20	1.236	V
1.50V ±3%, DDR3 Voltage	–	1.455	1.50	1.545[a]	V
1.80V ±3%, DDR2 Voltage	–	1.746	1.80	1.854	V
3.30V ±3%, I/O Voltage	–	3.201	3.30	3.399	V
Ambient Temperature	T_A	0	–	70	°C
Ambient Temperature (Industrial Temperature)	T_A	–40	–	+85	°C
Junction Temperature	T_J	–	–	110	°C

Note: 1.00V Core Voltage allows the use of ROV. Refer to the *Hardware Design Guidelines Application Note* for detailed implementation (see "References" on page 25).

a. Implementations that were originally designed for 1.525V DDR3 voltage can have a maximum input voltage of 1.571V.

PRELIMINARY INFORMATION

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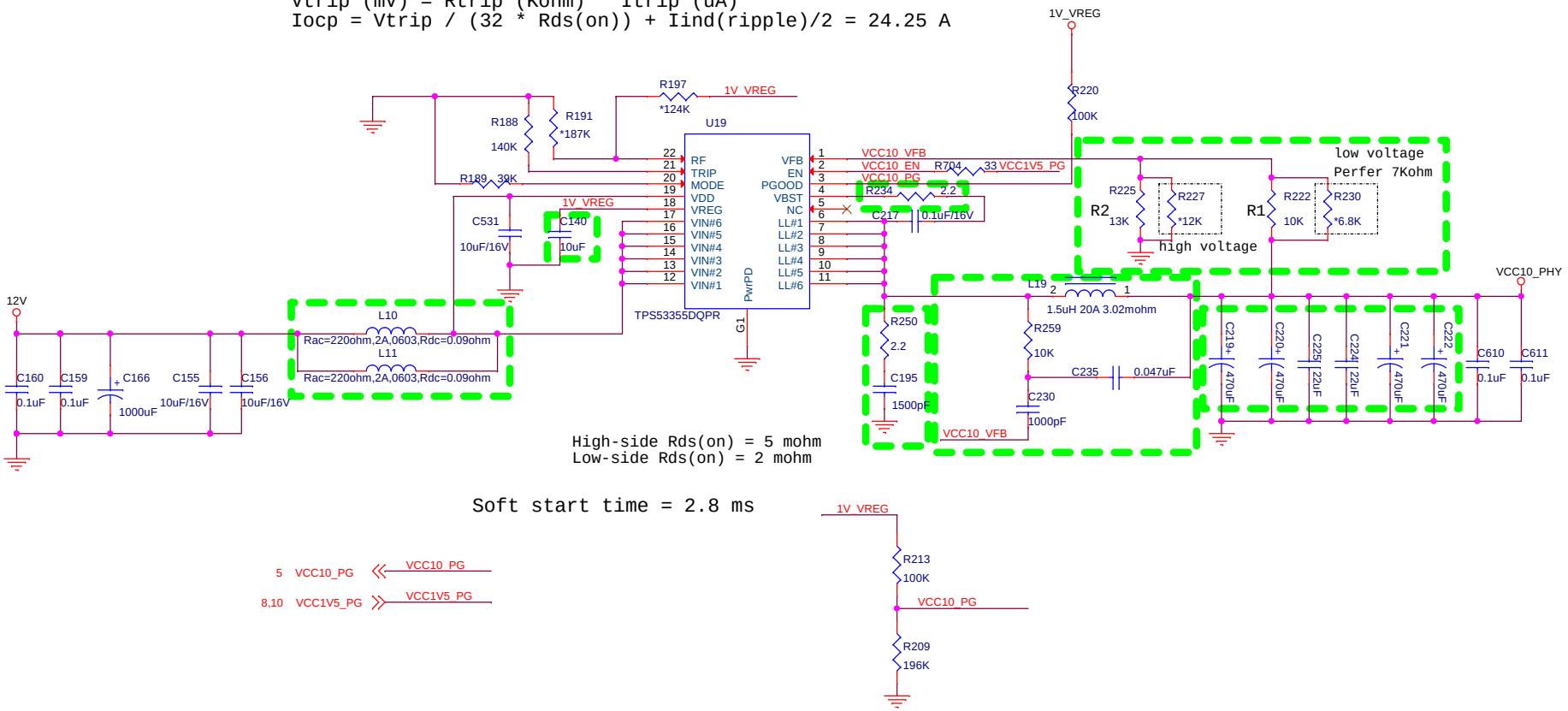
Model Name	Rev
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Size	Page Name	Engineer
C	VCC10_MAC	Chaohua_Chung

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Vout=0.6(1+R1/R2)
1.05 = 0.6 * (1+1K/1.33K)
RF open, Switching frequency = 500 KHz
RF = 187 Kohm to GND, Switching frequency = 300KHz
MODE: Auto-skip
Vtrip (mV) = Rtrip (Kohm) * Itrip (uA)
Iocp = Vtrip / (32 * Rds(on)) + Iind(ripple)/2 = 24.25 A

1V@18.62A (Max)



High-side Rds(on) = 5 mohm
Low-side Rds(on) = 2 mohm

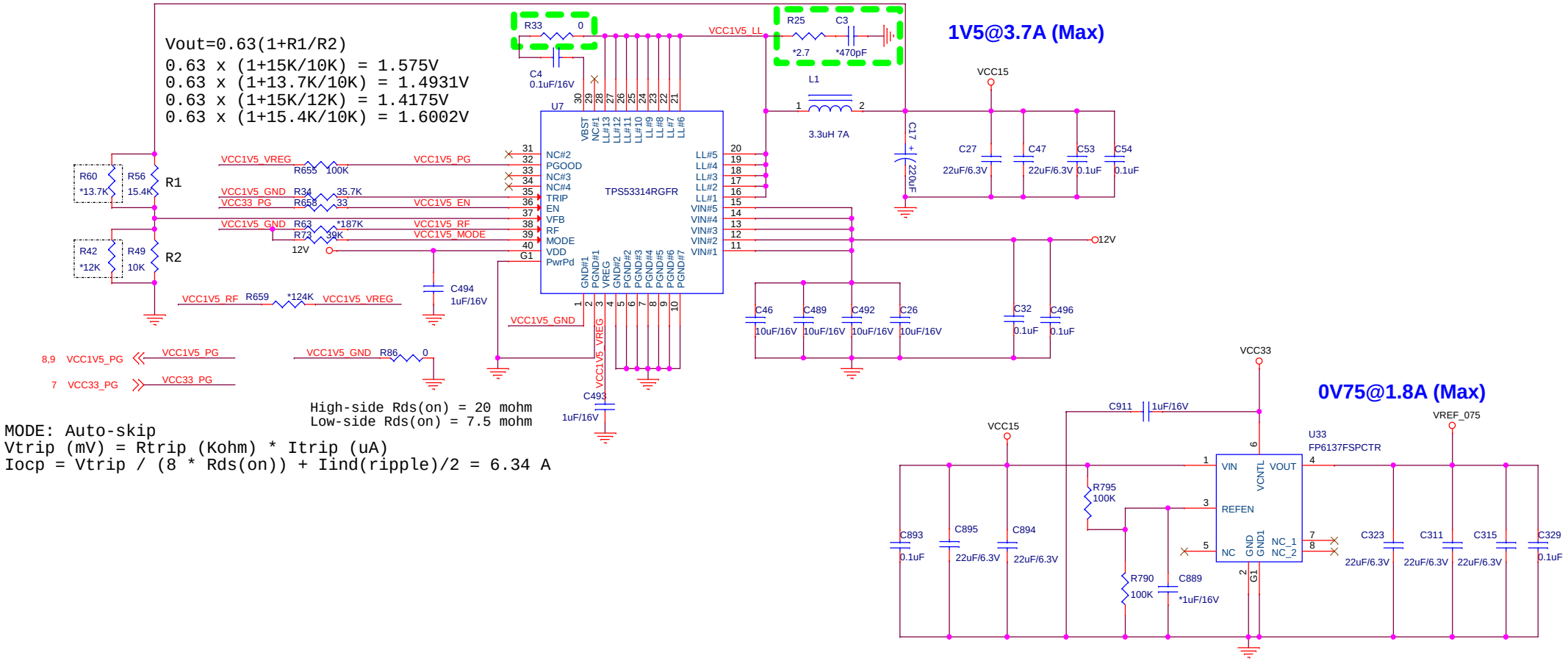
Soft start time = 2.8 ms

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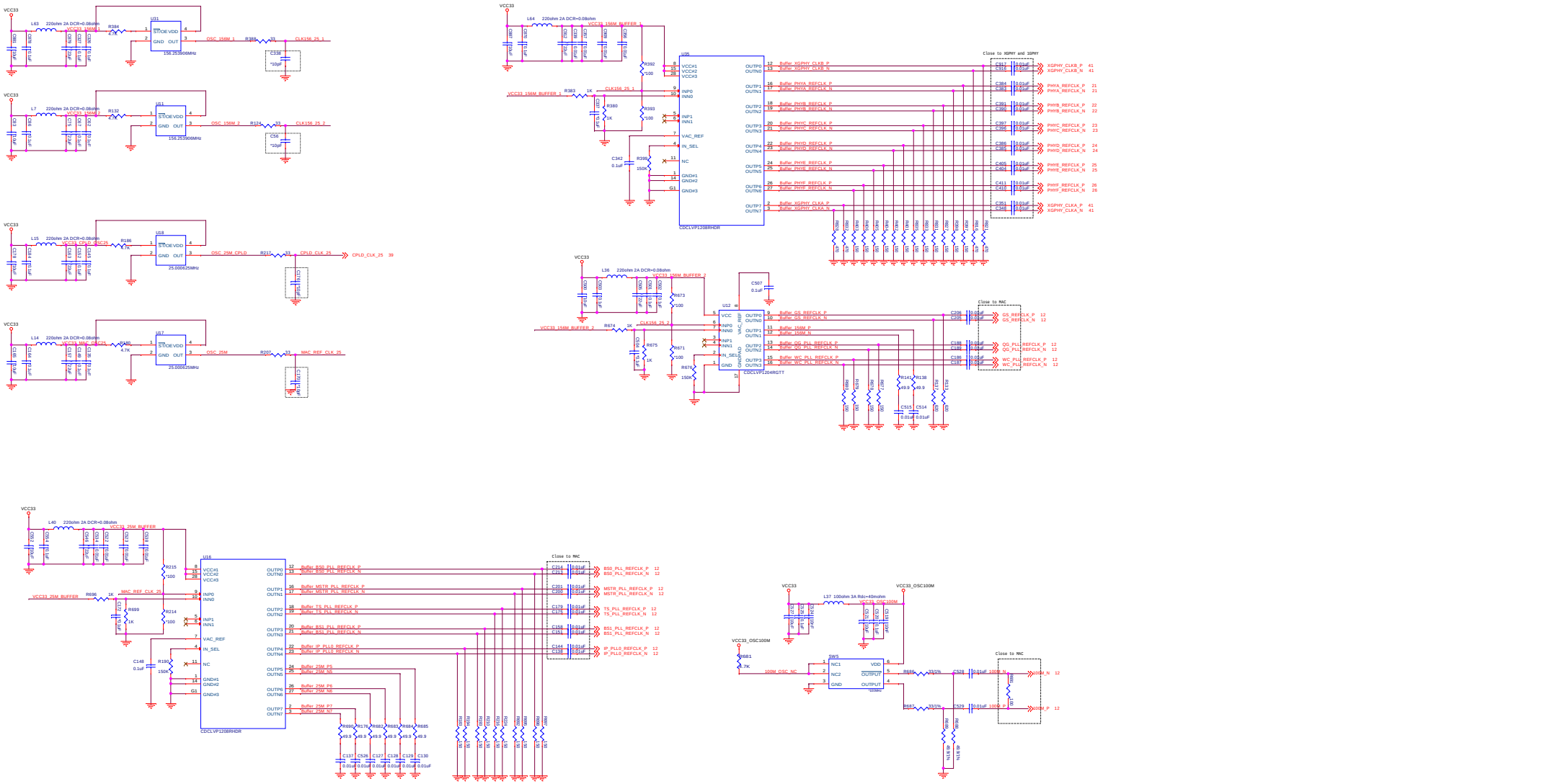
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Size	Page Name	Engineer
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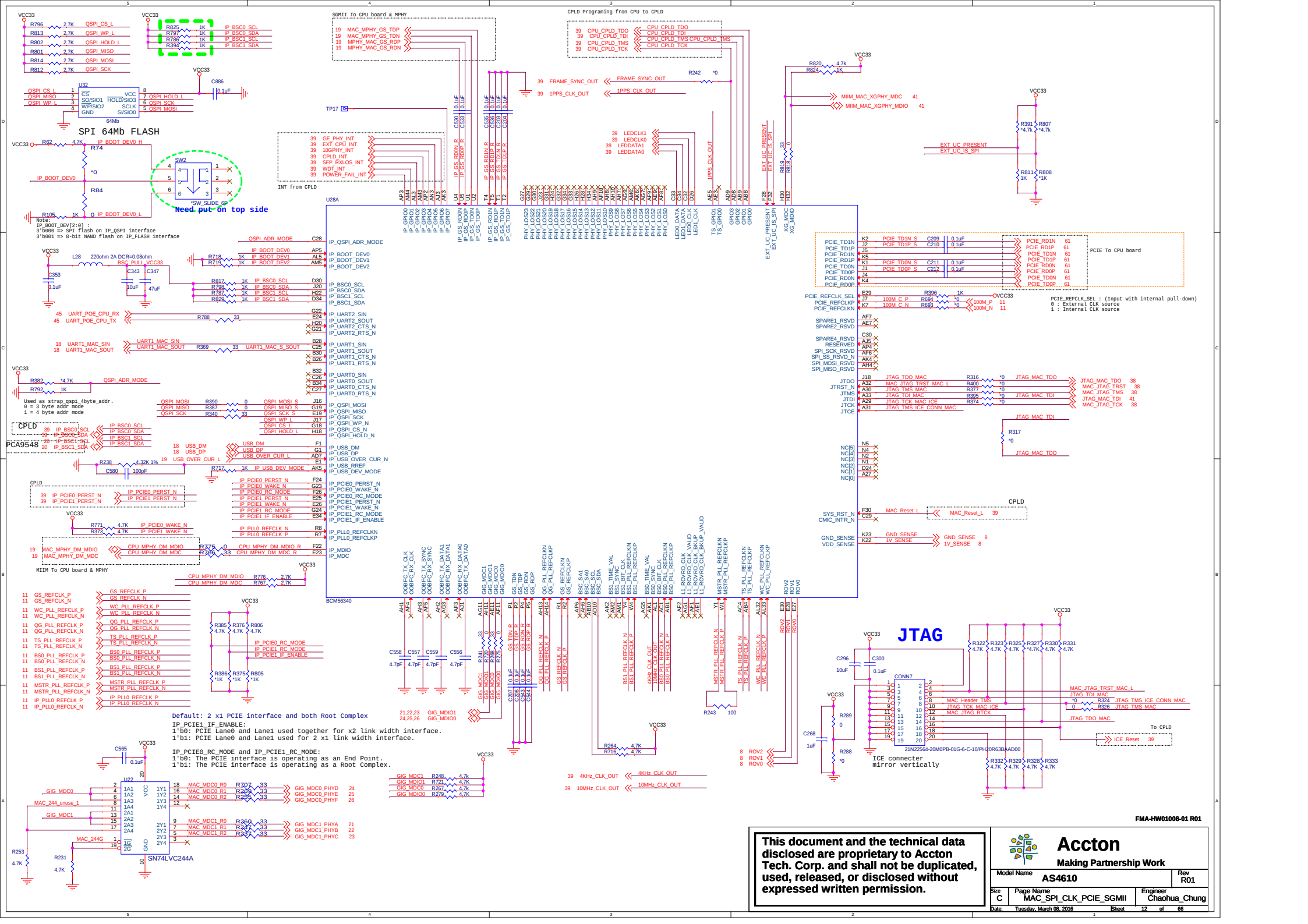


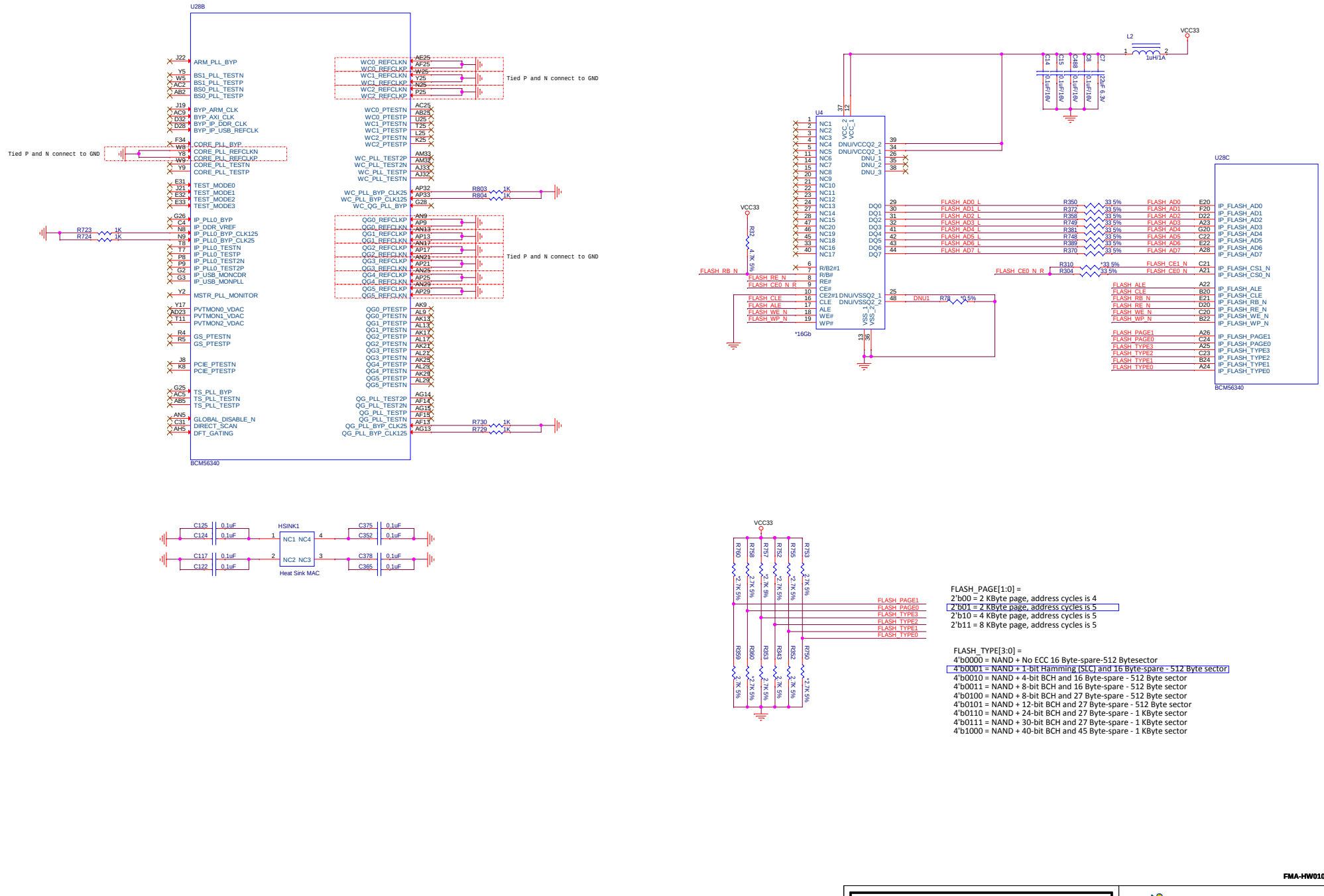
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Model Name	AS4610	Rev	R01
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SPI 64Mb FLASH
Need put on top side
JTAG
Default: 2 x1 PCIE interface and both Root Complex
IP_PCIE1_IF_ENABLE:
1'b0: PCIE Lane0 and Lane1 used together for x2 link width interface.
1'b1: PCIE Lane0 and Lane1 used for 2 x1 link width interface.
IP_PCIE0_RC_MODE and IP_PCIE1_RC_MODE:
1'b0: The PCIE interface is operating as an End Point.
1'b1: The PCIE interface is operating as a Root Complex.
ICE connecter
mirror vertically
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Model Name AS4610
Rev R01
Size C
Page Name MAC_SPI_CLK_PCIE_SGMII
Engineer Chaohua_Chung
Date: Tuesday, March 08, 2016
Sheet 12 of 66
FMA-HW01008-01 R01

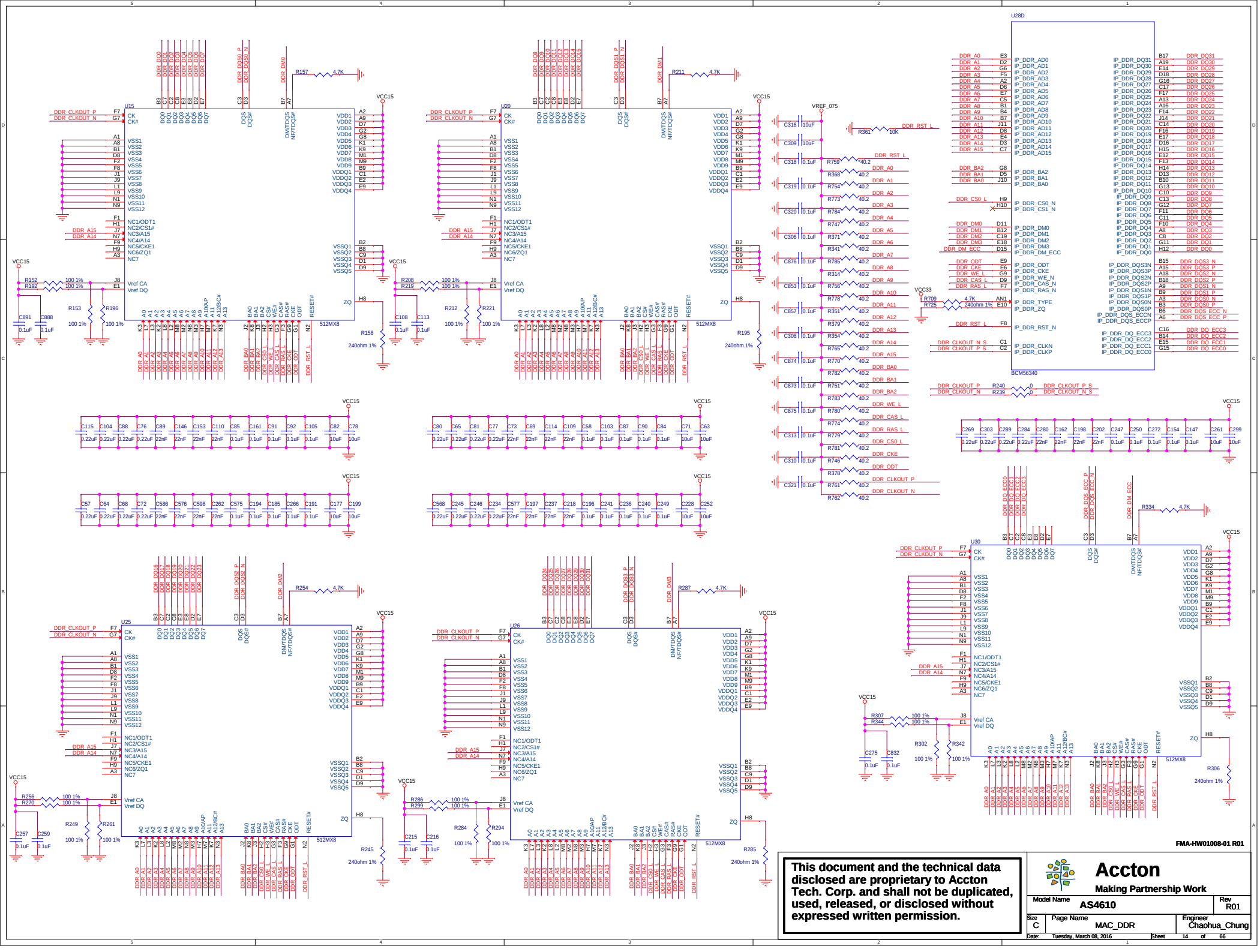


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Model Name	AS4610	Rev	R01
Size	C	Page Name	MAC_TEST & NAND
Engineer	Chaohua_Chung		
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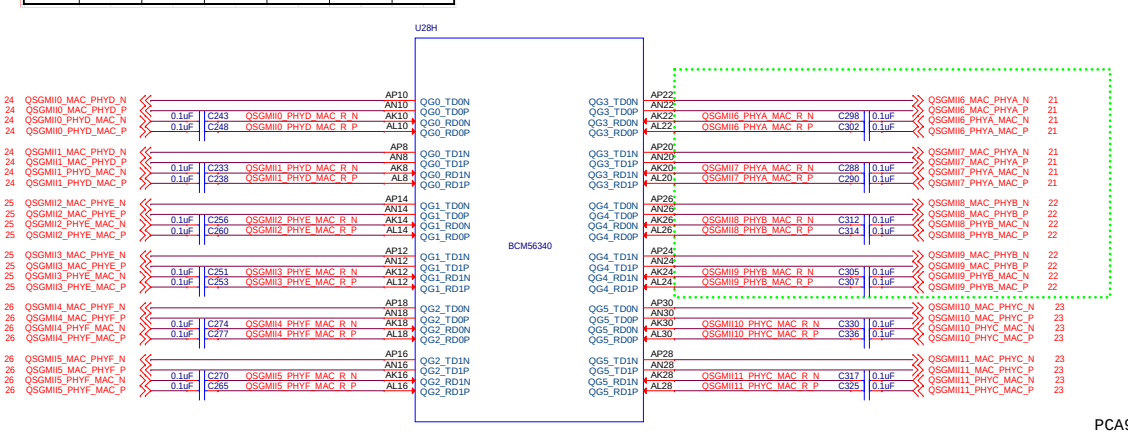
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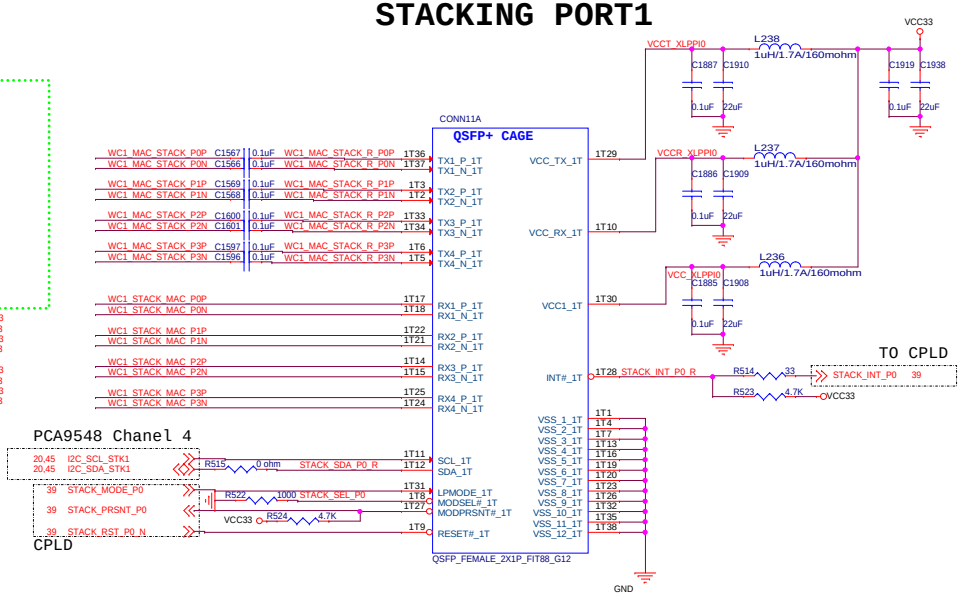
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Model Name	AS4610	Rev	R01
Size C	Page Name MAC_DDR	Engineer Chaohua_Chung	
Date: Tuesday, March 08, 2016	Sheet 14 of 66		

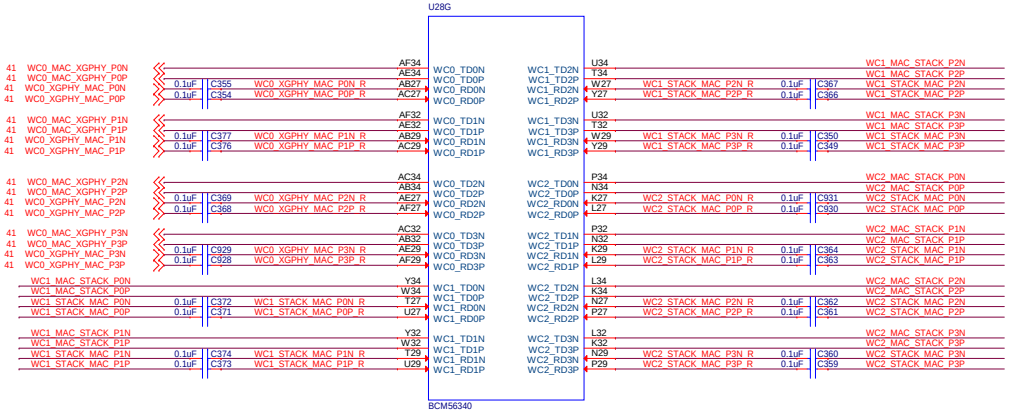
MAC_QSGMII	0-0	0-1	1-0	1-1	2-0	2-1	3-0	3-1	4-0	4-1	5-0	5-1
PHY#	4		5		6		1		2		3	

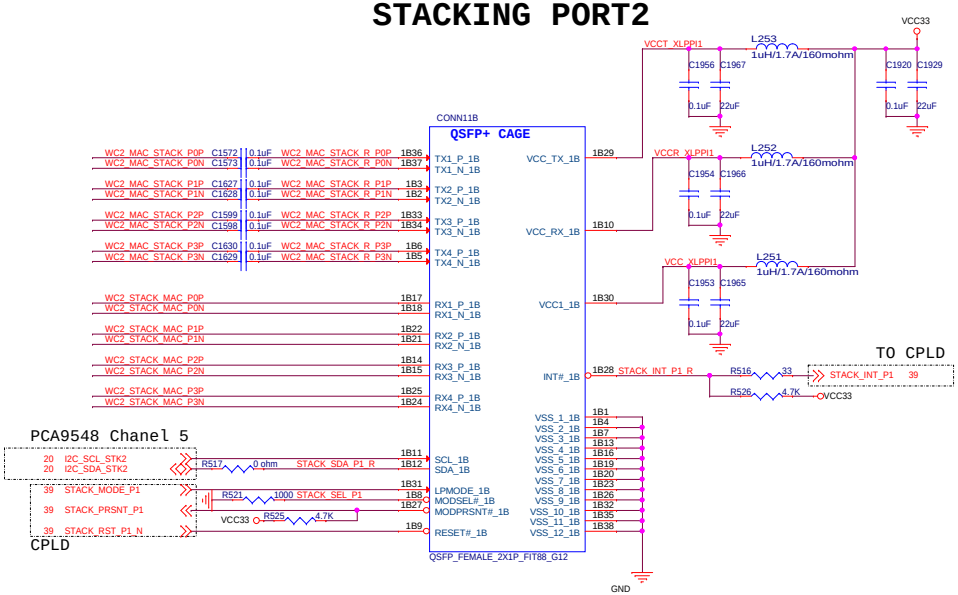
STACKING PORT1

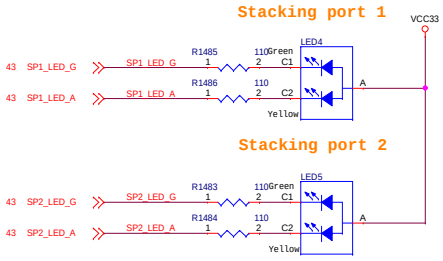


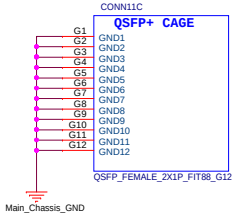


STACKING PORT2







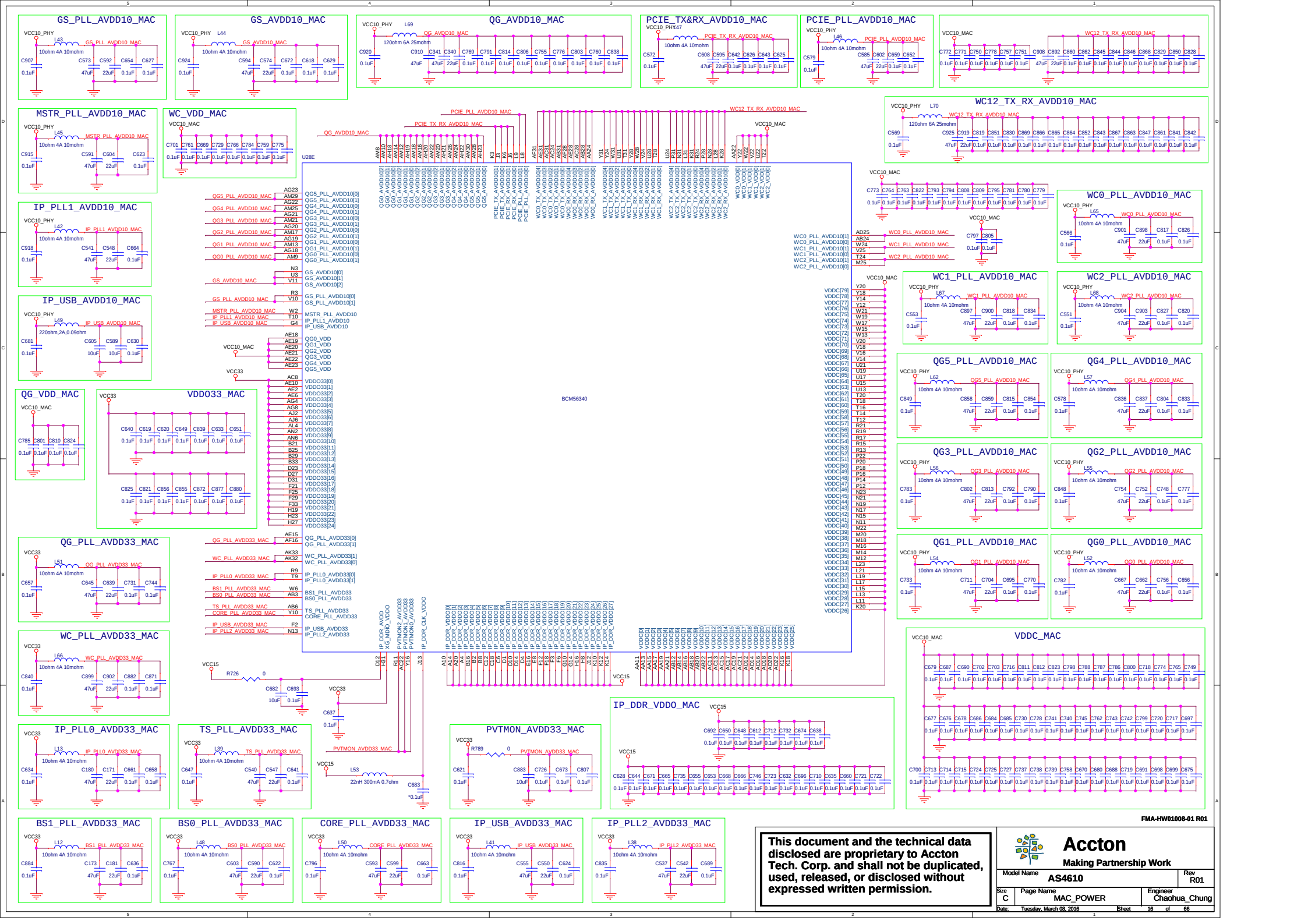


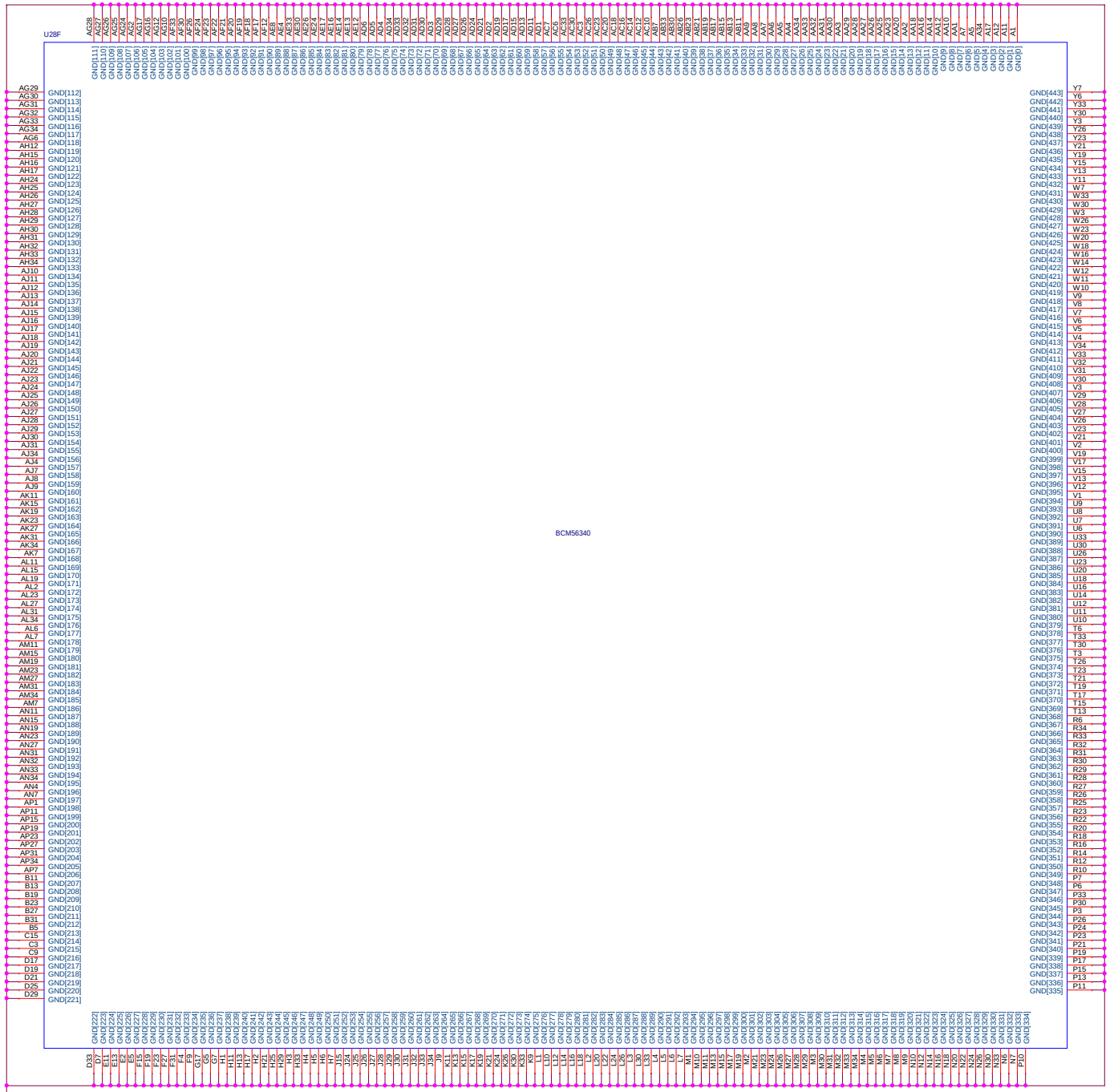
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Model Name	AS4610	Rev	R01
Size	C	Page Name	MAC_QSGMII_XFI_HG2+
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GS_PLL_AVDD10_MAC
GS_AVDD10_MAC
QG_AVDD10_MAC
PCIE_TX&RX_AVDD10_MAC
PCIE_PLL_AVDD10_MAC
WC12_TX_RX_AVDD10_MAC
MSTR_PLL_AVDD10_MAC
WC_VDD_MAC
IP_PLL1_AVDD10_MAC
IP_USB_AVDD10_MAC
WC0_PLL_AVDD10_MAC
WC1_PLL_AVDD10_MAC
WC2_PLL_AVDD10_MAC
QG5_PLL_AVDD10_MAC
QG4_PLL_AVDD10_MAC
QG3_PLL_AVDD10_MAC
QG2_PLL_AVDD10_MAC
QG1_PLL_AVDD10_MAC
QG0_PLL_AVDD10_MAC
QG_VDD_MAC
VDDO33_MAC
QG_PLL_AVDD33_MAC
WC_PLL_AVDD33_MAC
VDDC_MAC
IP_PLL0_AVDD33_MAC
TS_PLL_AVDD33_MAC
PVTMON_AVDD33_MAC
IP_DDR_VDDO_MAC
BS1_PLL_AVDD33_MAC
BS0_PLL_AVDD33_MAC
CORE_PLL_AVDD33_MAC
IP_USB_AVDD33_MAC
IP_PLL2_AVDD33_MAC
BCM56340
U28E
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Model Name AS4610
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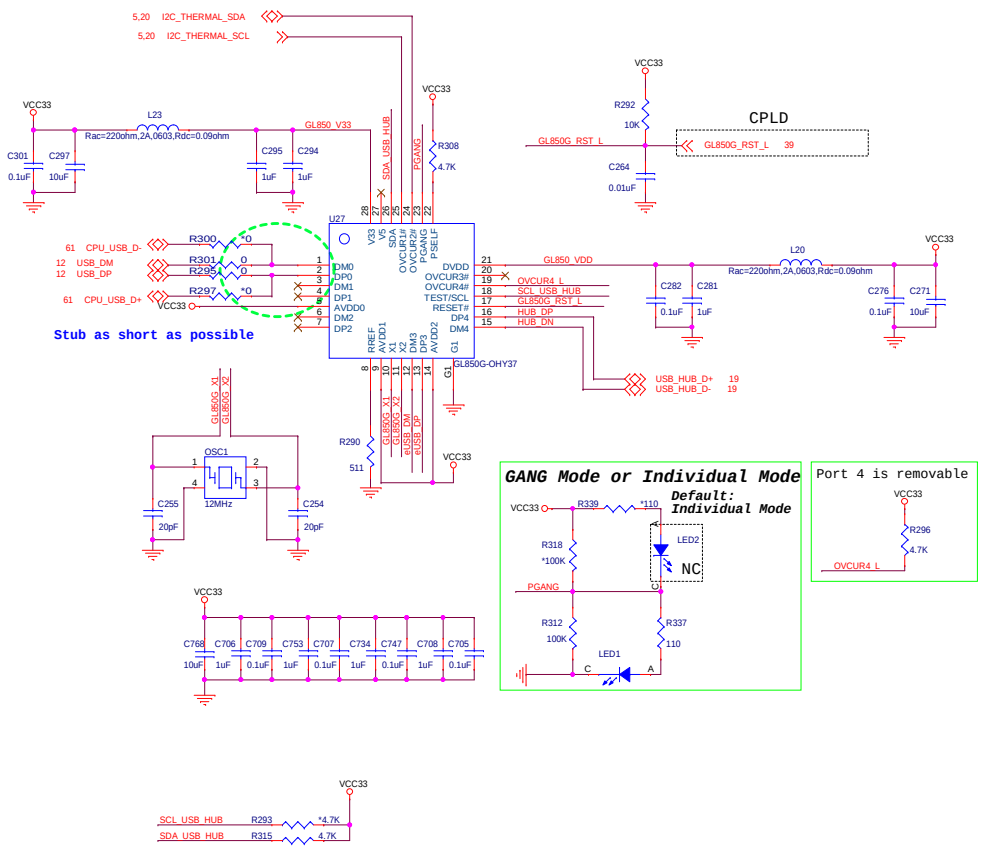
Accton

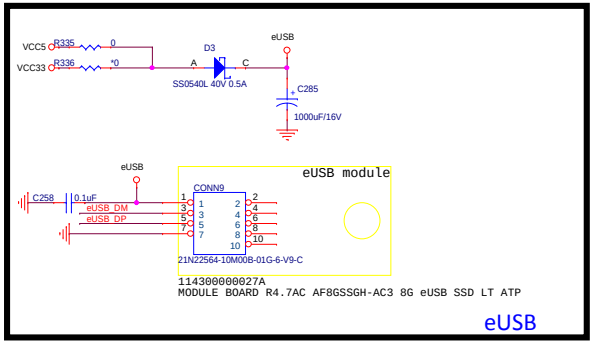
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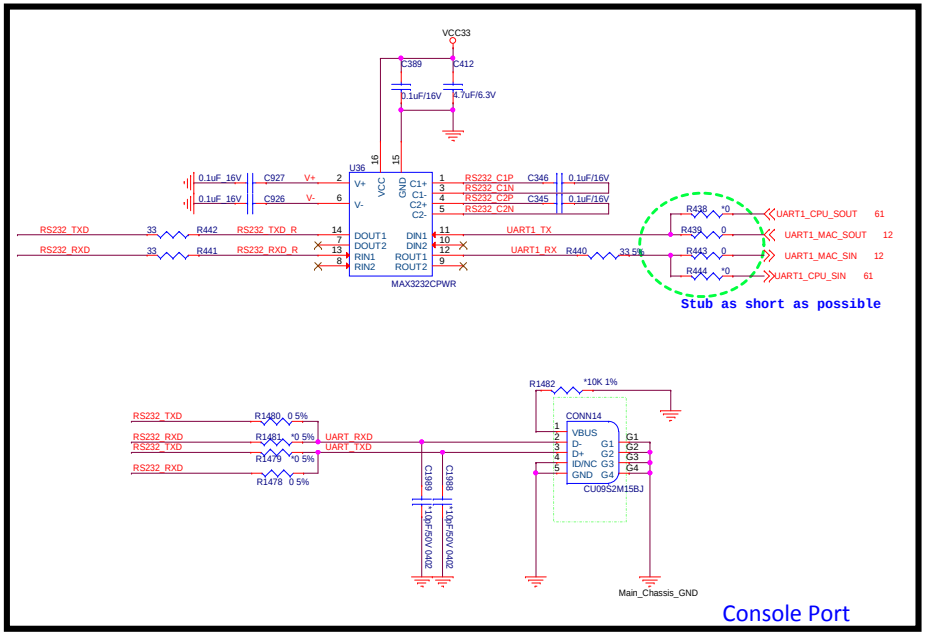
Model Name	Rev
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Size	Page Name	Engineer
C	MAC_GND	Chaohua_Chung

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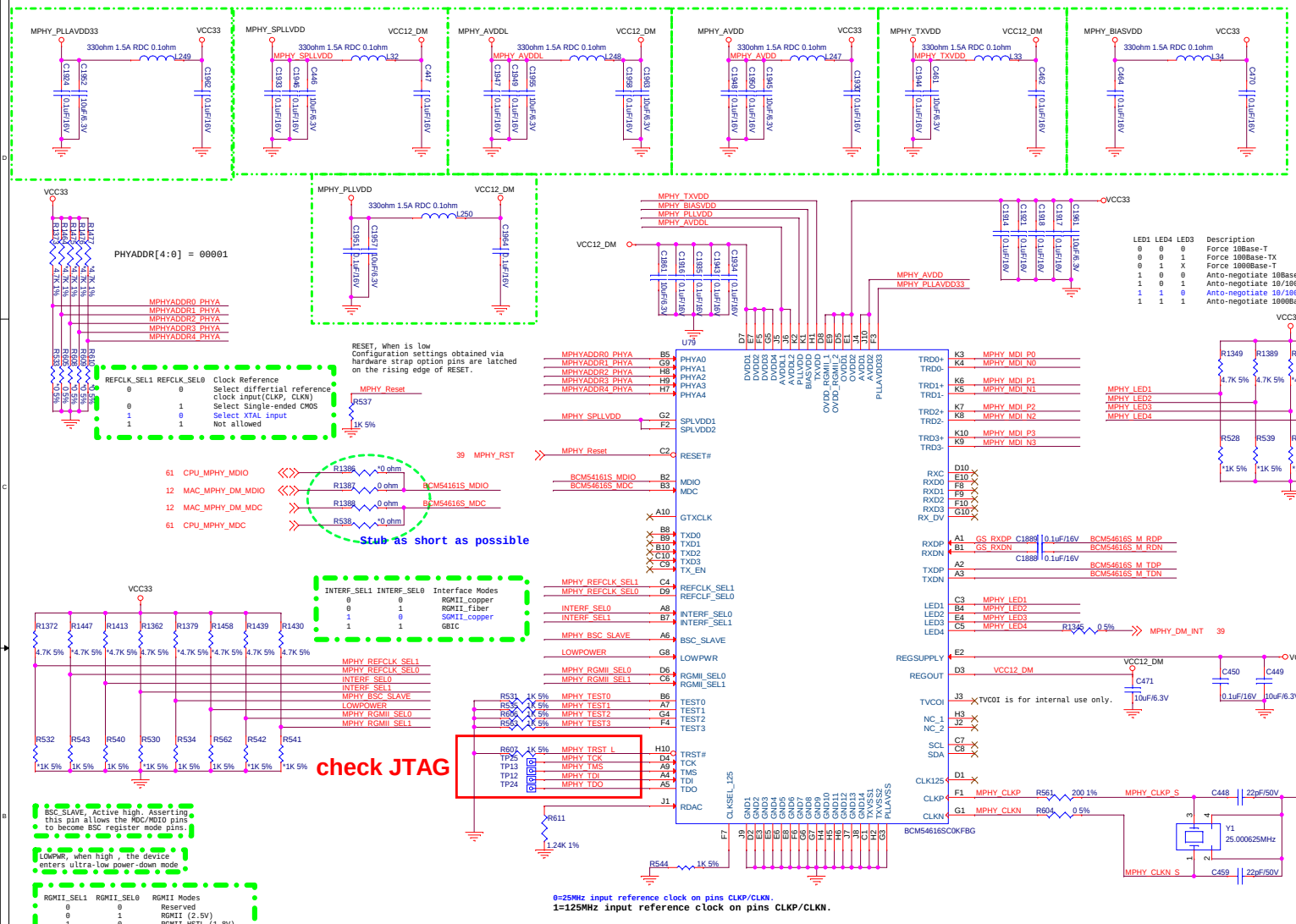
FMA-HW01008-01 R01

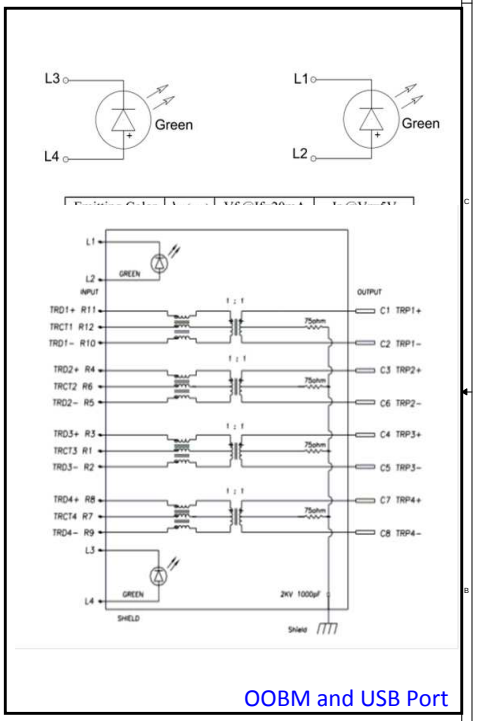
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Model Name	AS4610	Rev	R01
Size C	Page Name USB & eUSB & console	Engineer	Chaohua_Chung
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Power Name	Volt	Description
DVDD	1.2V	for digital core
OVDD	3.3V	for non RGMII pads
OVDD_RGMII	3.3V	In SGMII mode, 2.5V or 3.3V should be provided
AVDDL	1.2V	for analog core
AVDD	3.3V	for analog core
PLLVDD	1.2V	PLL supply
BIASVDD	3.3V	Bias VDD
TXVDD	1.2V	transmitter and receiver of the SerDes
SPLLVDD	1.2V	to the SerDer PLL
PLLAVDD33	3.3V	to the reference clock of SerDes PLL





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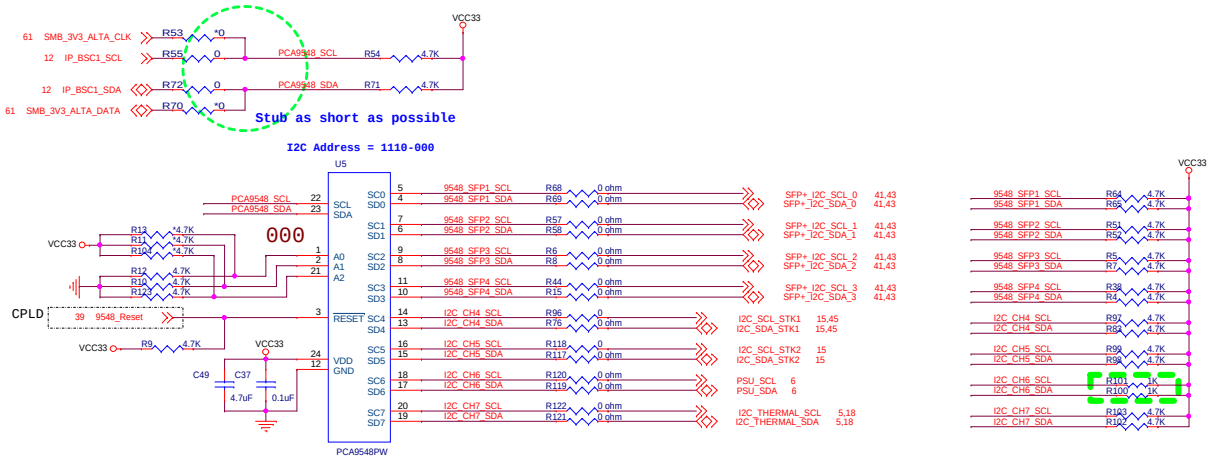
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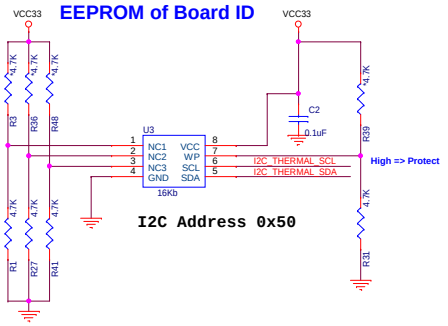
Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	PHY_BCM54616S	Ching_su

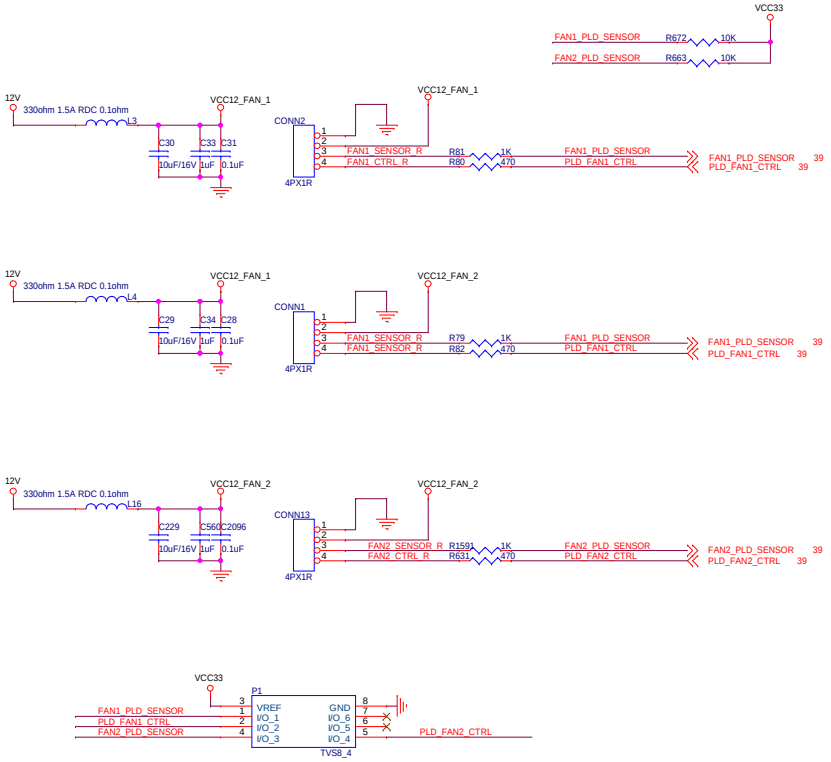
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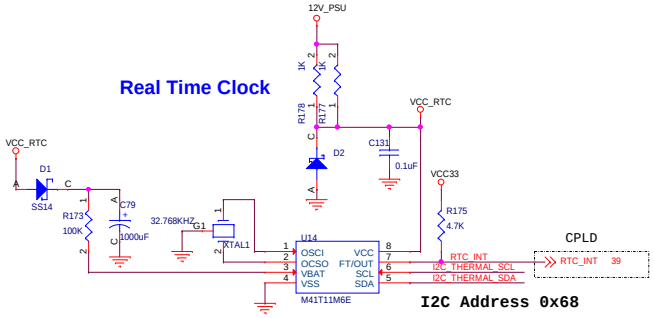
FMA-HW01008-01 R01





FAN Controller



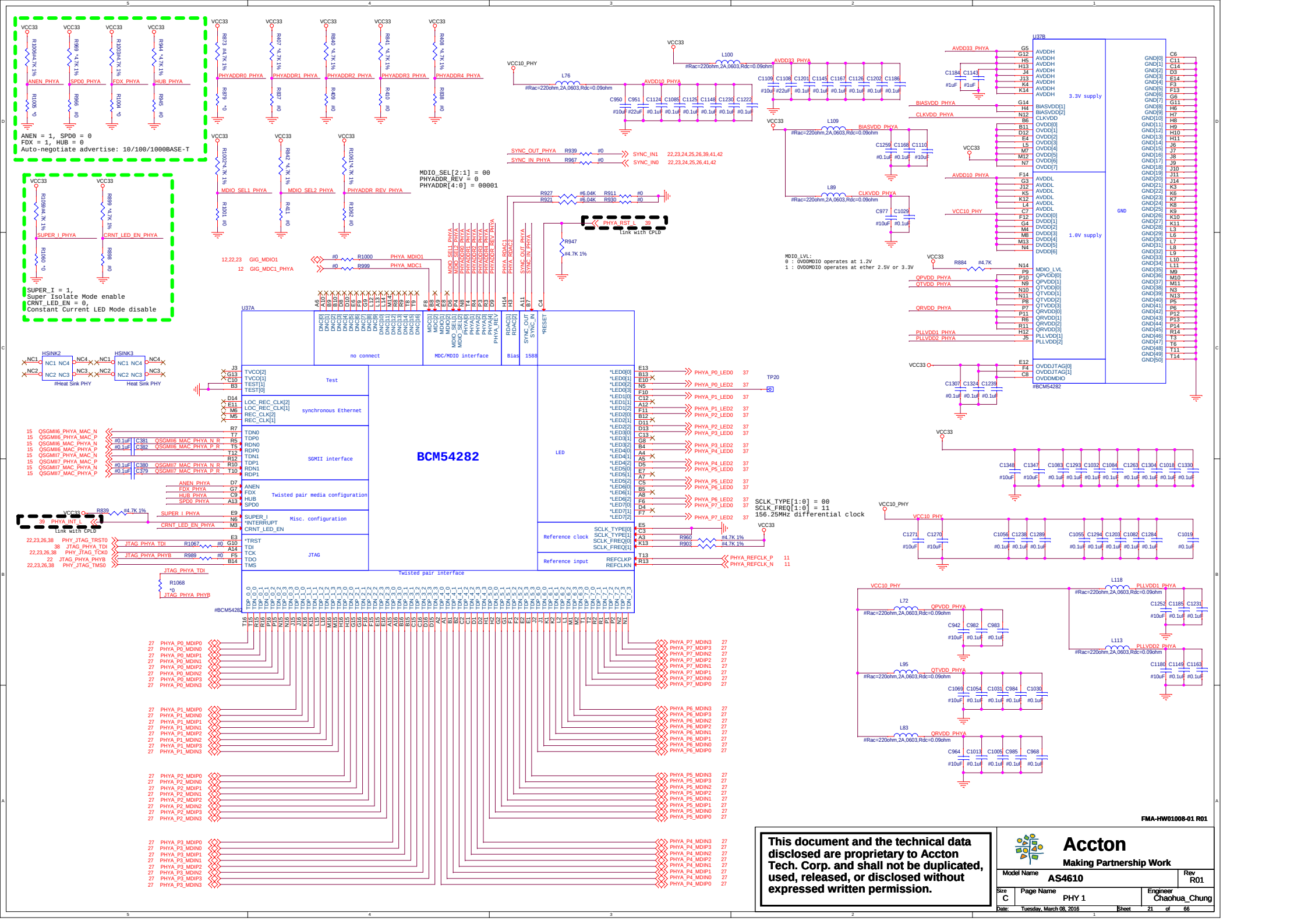


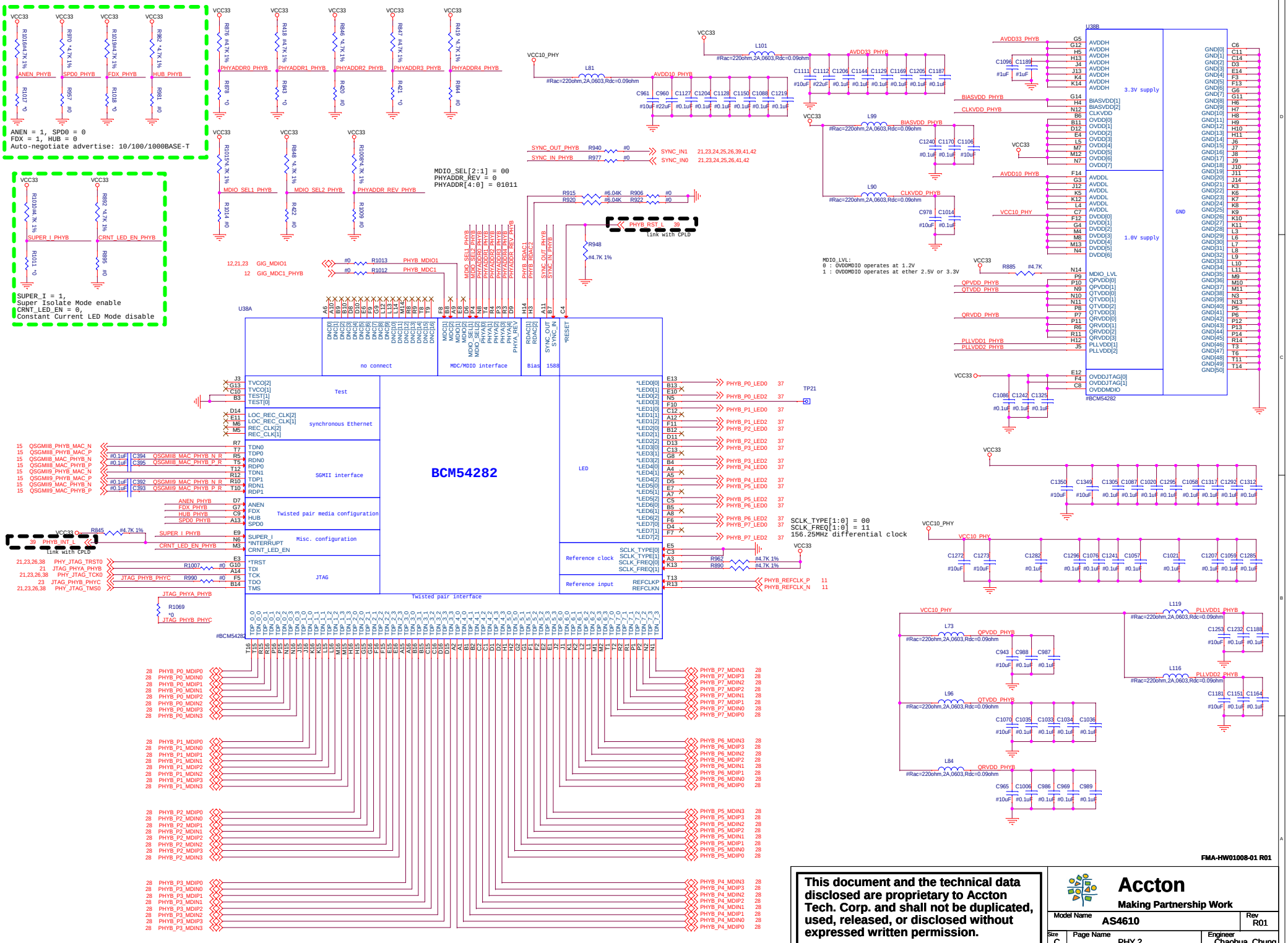
FMA-HW01008-01 R01

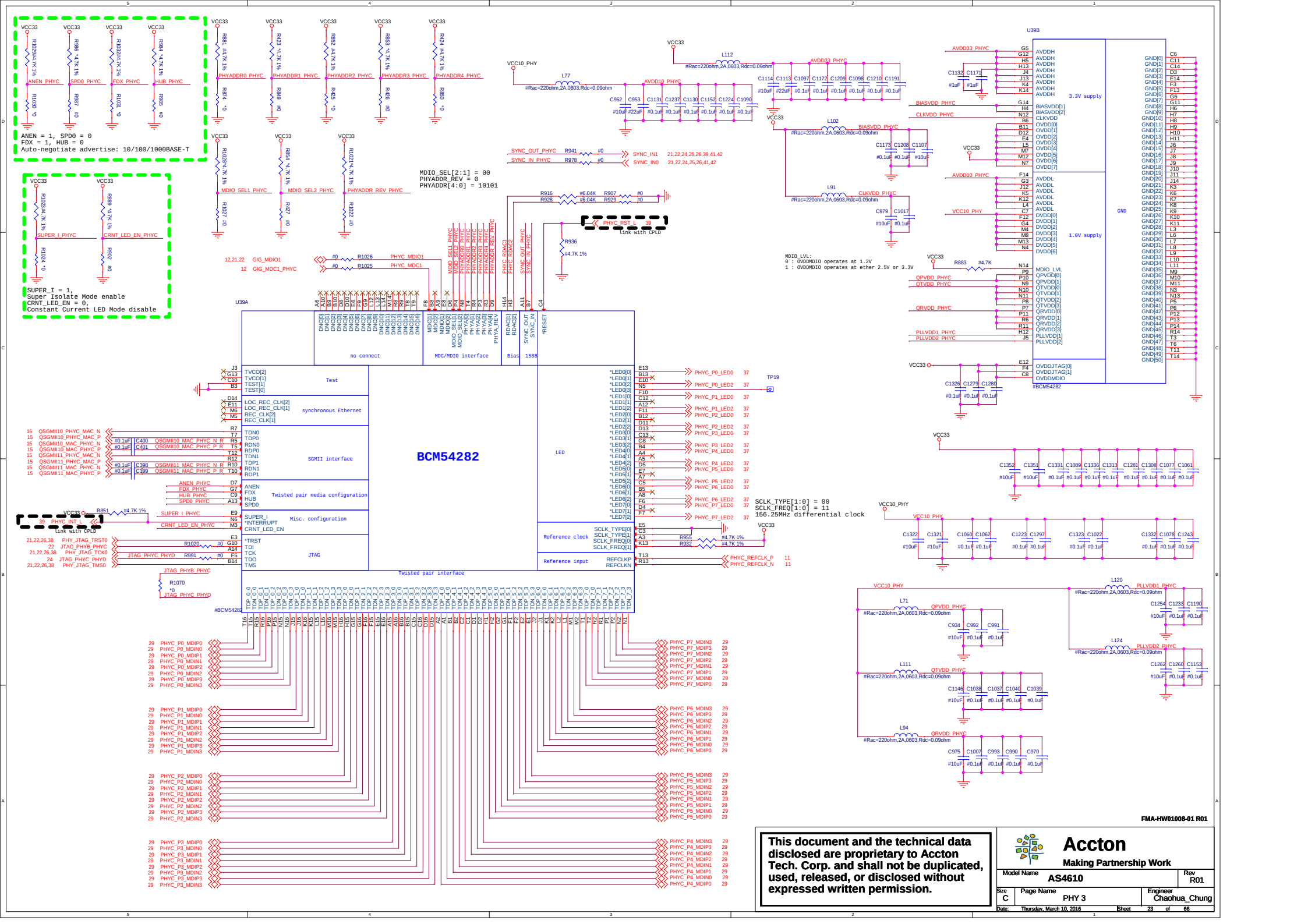
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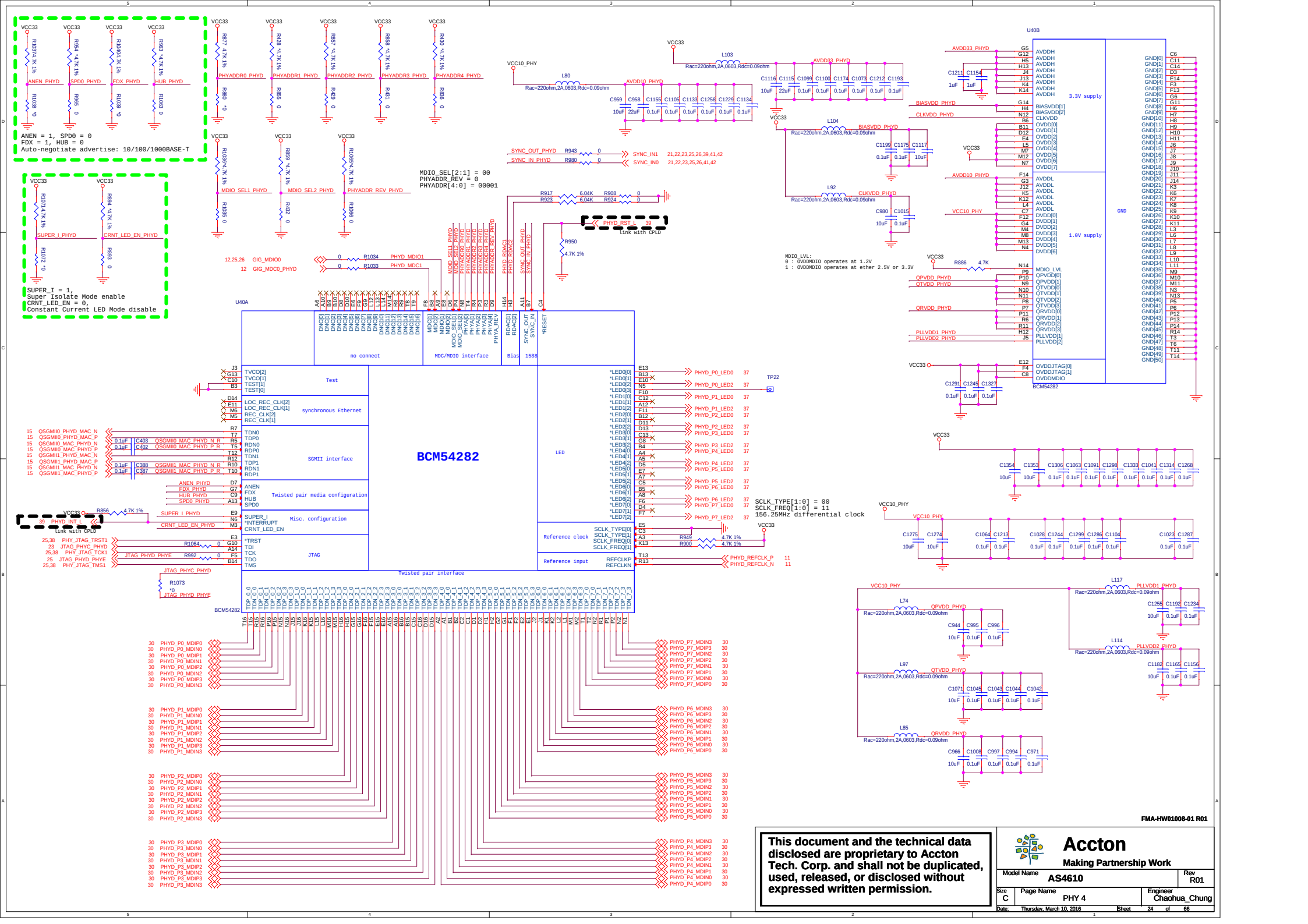
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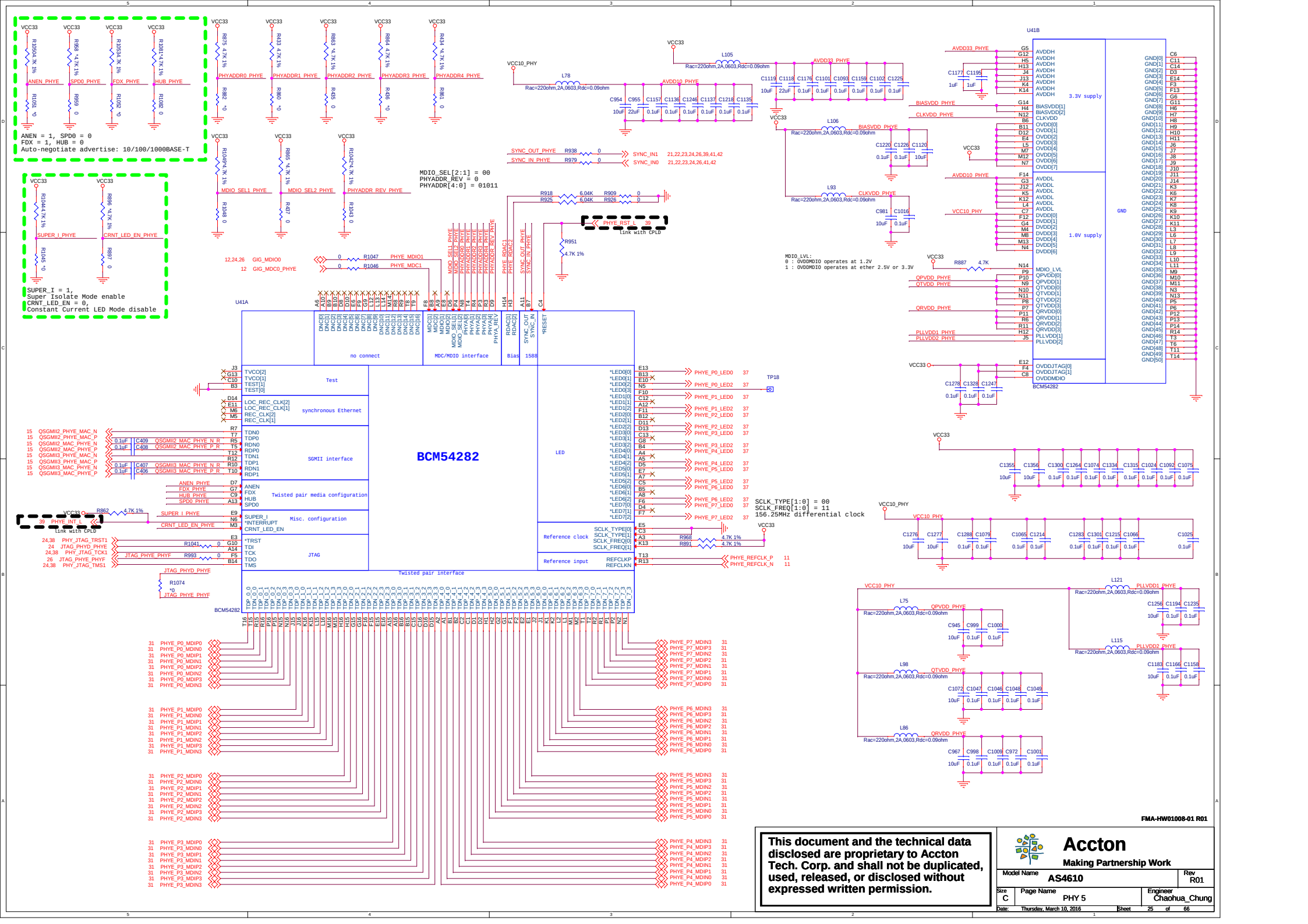
Model Name	AS4610	Rev	R01
Size C	Page Name I2C	Engineer	Chaohua_Chung
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ANEN = 1, SPD0 = 0
FDX = 1, HUB = 0
Auto-negotiate advertise: 10/100/1000BASE-T
SUPER_I = 1,
Super Isolate Mode enable
CRNT_LED_EN = 0,
Constant Current LED Mode disable
MDIO_SEL[2:1] = 00
PHYADDR_REV = 0
PHYADDR[4:0] = 00001
SCLK_TYPE[1:0] = 00
SCLK_FREQ[1:0] = 11
156.25MHz differential clock
MDIO_LVL:
0 : OVDDMDIO operates at 1.2V
1 : OVDDMDIO operates at ether 2.5V or 3.3V
BCM54282
U37A
U37B
Test
synchronous Ethernet
SGMII interface
Twisted pair media configuration
Misc. configuration
JTAG
LED
Reference clock
Reference input
Twisted pair interface
no connect
MDC/MDIO interface
Bias
3.3V supply
1.0V supply
GND
Heat Sink PHY
link with CPLD
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Model Name AS4610
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Size C
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Engineer Chaohua_Chung
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ANEN = 1, SPD0 = 0
FDX = 1, HUB = 0
Auto-negotiate advertise: 10/100/1000BASE-T
SUPER_I = 1,
Super Isolate Mode enable
CRNT_LED_EN = 0,
Constant Current LED Mode disable
MDIO_SEL[2:1] = 00
PHYADDR_REV = 0
PHYADDR[4:0] = 01011
BCM54282
SCLK_TYPE[1:0] = 00
SCLK_FREQ[1:0] = 11
156.25MHz differential clock
MDIO_LVL:
0 : OVDDMDIO operates at 1.2V
1 : OVDDMDIO operates at ether 2.5V or 3.3V
FMA-HW01008-01 R01
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Making Partnership Work
Model Name AS4610
Rev R01
Size C
Page Name PHY 2
Engineer Chaohua_Chung
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ANEN = 1, SPD0 = 0
FDX = 1, HUB = 0
Auto-negotiate advertise: 10/100/1000BASE-T
SUPER_I = 1,
Super Isolate Mode enable
CRNT_LED_EN = 0,
Constant Current LED Mode disable
MDIO_SEL[2:1] = 00
PHYADDR_REV = 0
PHYADDR[4:0] = 10101
BCM54282
SCLK_TYPE[1:0] = 00
SCLK_FREQ[1:0] = 11
156.25MHz differential clock
MDIO_LVL:
0 : OVDDMDIO operates at 1.2V
1 : OVDDMDIO operates at ether 2.5V or 3.3V
FMA-HW01008-01 R01
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Model Name AS4610
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ANEN = 1, SPD0 = 0
FDX = 1, HUB = 0
Auto-negotiate advertise: 10/100/1000BASE-T
SUPER_I = 1,
Super Isolate Mode enable
CRNT_LED_EN = 0,
Constant Current LED Mode disable
MDIO_SEL[2:1] = 00
PHYADDR_REV = 0
PHYADDR[4:0] = 00001
SCLK_TYPE[1:0] = 00
SCLK_FREQ[1:0] = 11
156.25MHz differential clock
MDIO_LVL:
0 : OVDDMDIO operates at 1.2V
1 : OVDDMDIO operates at ether 2.5V or 3.3V
BCM54282
U40A
U40B
Test
synchronous Ethernet
SGMII interface
Twisted pair media configuration
Misc. configuration
JTAG
LED
Reference clock
Reference input
Twisted pair interface
no connect
MDC/MDIO interface
Bias
3.3V supply
1.0V supply
GND
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Model Name AS4610
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ANEN = 1, SPD0 = 0
FDX = 1, HUB = 0
Auto-negotiate advertise: 10/100/1000BASE-T
SUPER_I = 1,
Super Isolate Mode enable
CRNT_LED_EN = 0,
Constant Current LED Mode disable
MDIO_SEL[2:1] = 00
PHYADDR_REV = 0
PHYADDR[4:0] = 01011
BCM54282
SCLK_TYPE[1:0] = 00
SCLK_FREQ[1:0] = 11
156.25MHz differential clock
MDIO_LVL:
0 : OVDDMDIO operates at 1.2V
1 : OVDDMDIO operates at ether 2.5V or 3.3V
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SUPER_I = 1,
Super Isolate Mode enable
CRNT_LED_EN = 0,
Constant Current LED Mode disable

ANEN = 1, SPD0 = 0
FDX = 1, HUB = 0
Auto-negotiate advertise: 10/100/1000BASE-T

MDIO_SEL[2:1] = 00
PHYADDR_REV = 0
PHYADDR[4:0] = 10101

BCM54282

SYNC_IN1 21,22,23,24,25,39,41,42
SYNC_IN0 21,22,23,24,25,41,42
PHYF_RST_L 39 link with CPLD

SCLK_TYPE[1:0] = 00
SCLK_FREQ[1:0] = 11
156.25MHz differential clock

MDIO_LVL:
0 : OVDDMDIO operates at 1.2V
1 : OVDDMDIO operates at ether 2.5V or 3.3V

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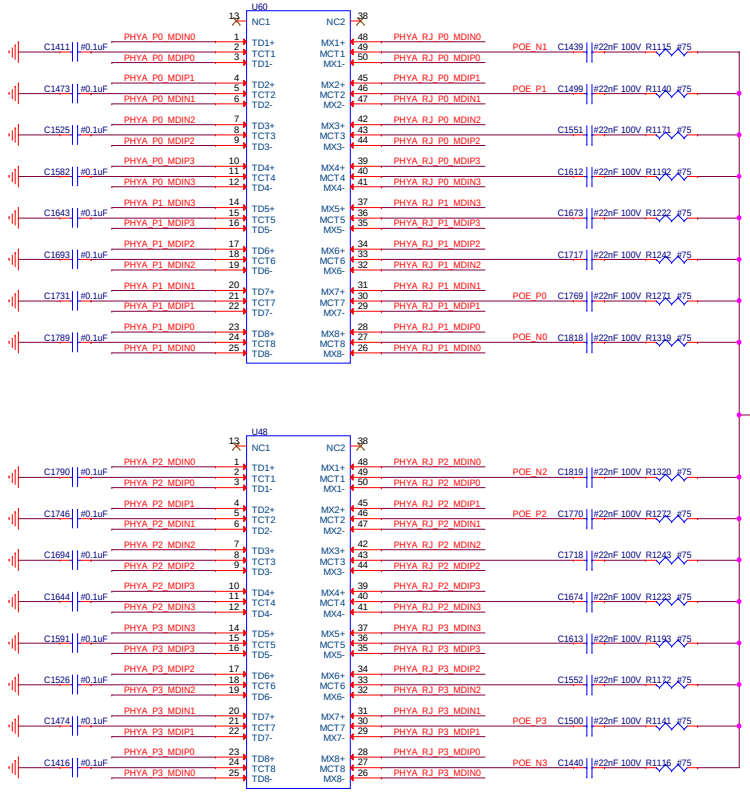
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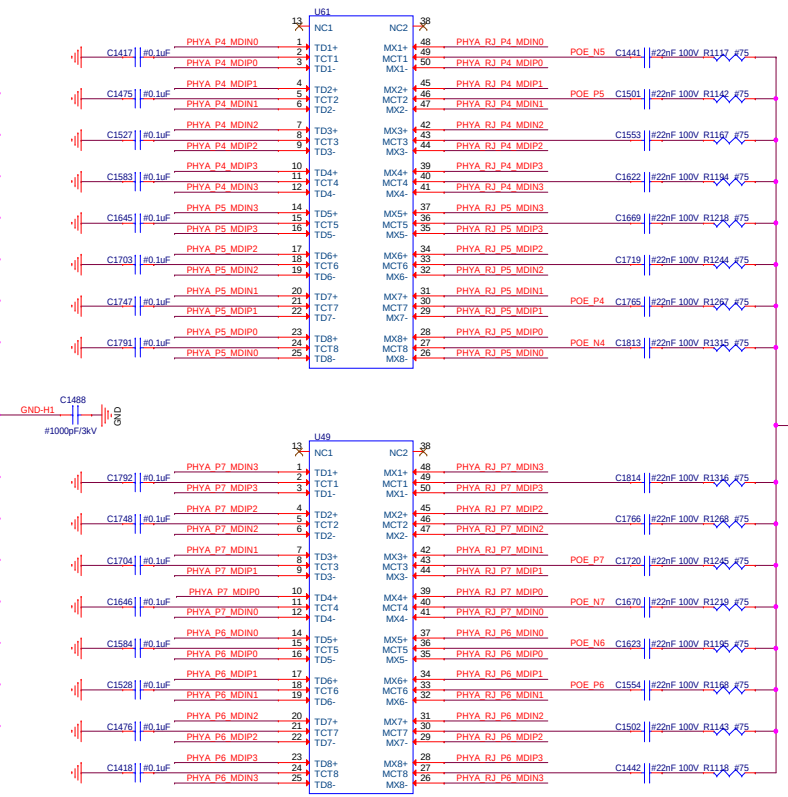
Model Name	AS4610	Rev R01
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PHY1

Front panel port	1	3	5	7
PHY phiscal port	P1	P2	P5	P6
Front panel port	2	4	6	8
PHY phiscal port	P0	P3	P4	P7

PHY1 port1~port4





PHY1 port5~port8

POE main source: 115500000051A M-TEK
2nd source: 115500000068H TAG

Non POE main source: 115500000085A FPE
2nd source: 115500000050A M-TEK

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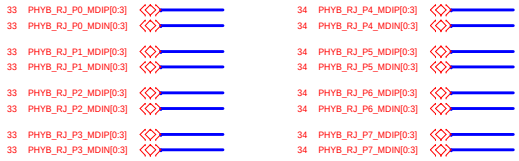
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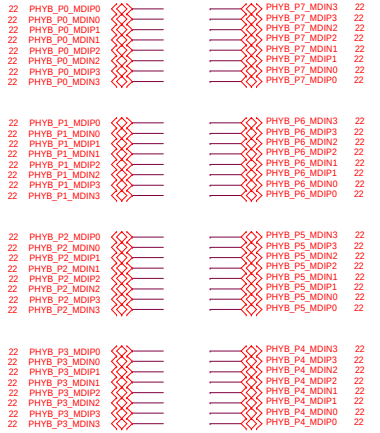
Model Name	AS4610	Rev	R01
Size	C	Page Name	Xfmr 1-8
Engineer	Chaohua_Chung		
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PHY2

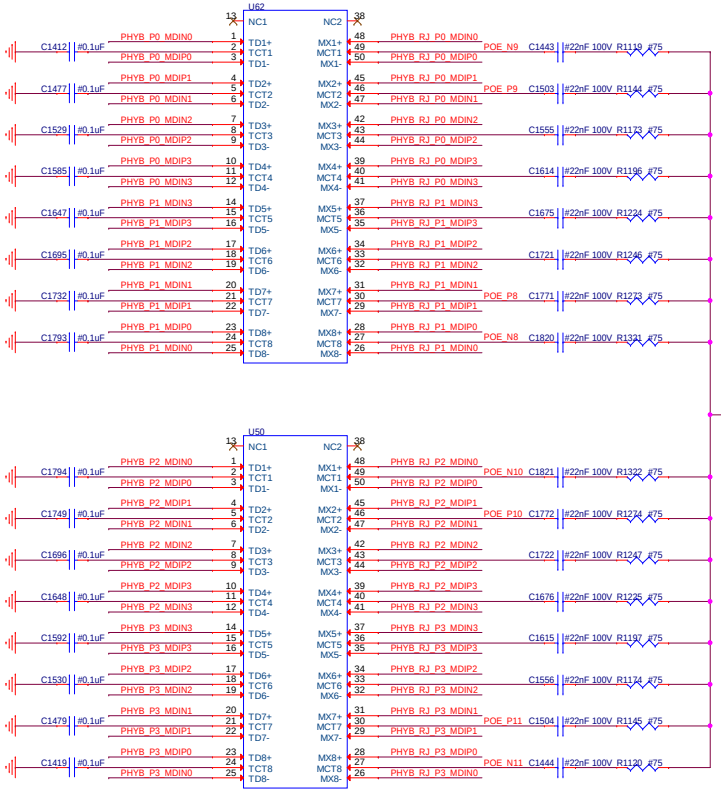
Front panel port	9	11	13	15
PHY phiscal port	P1	P2	P5	P6
Front panel port	10	12	14	16
PHY phiscal port	P0	P3	P4	P7







PHY2 port9~port12



PHY2 port13~port16



Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

POE main source: 115500000051A M-TEK
2nd source: 115500000068H TAG

Non POE main source: 115500000085A FPE
2nd source: 115500000050A M-TEK

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Model Name	Rev
AS4610	R01

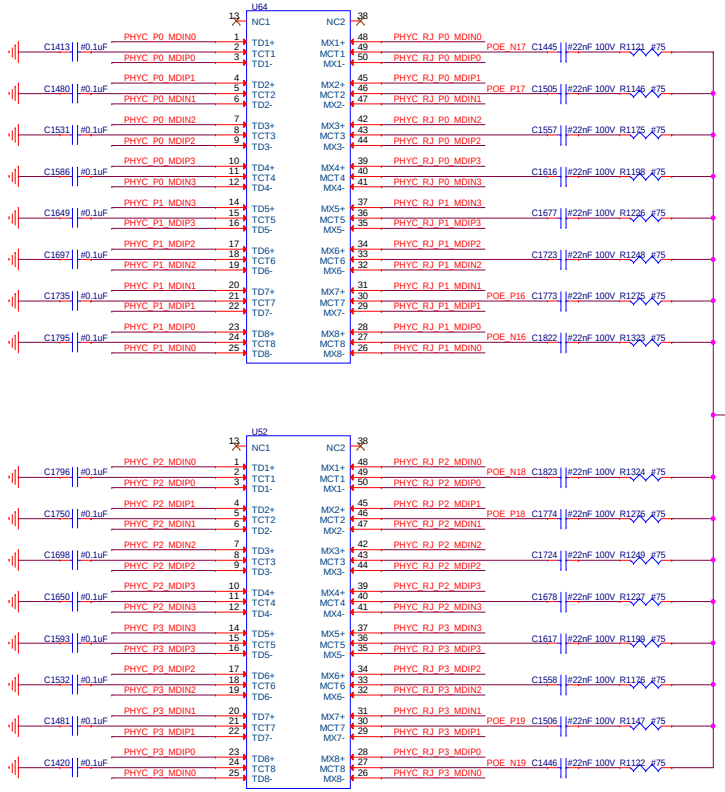
Size	Page Name	Engineer
C	Xfmr 9-16	Chaohua_Chung

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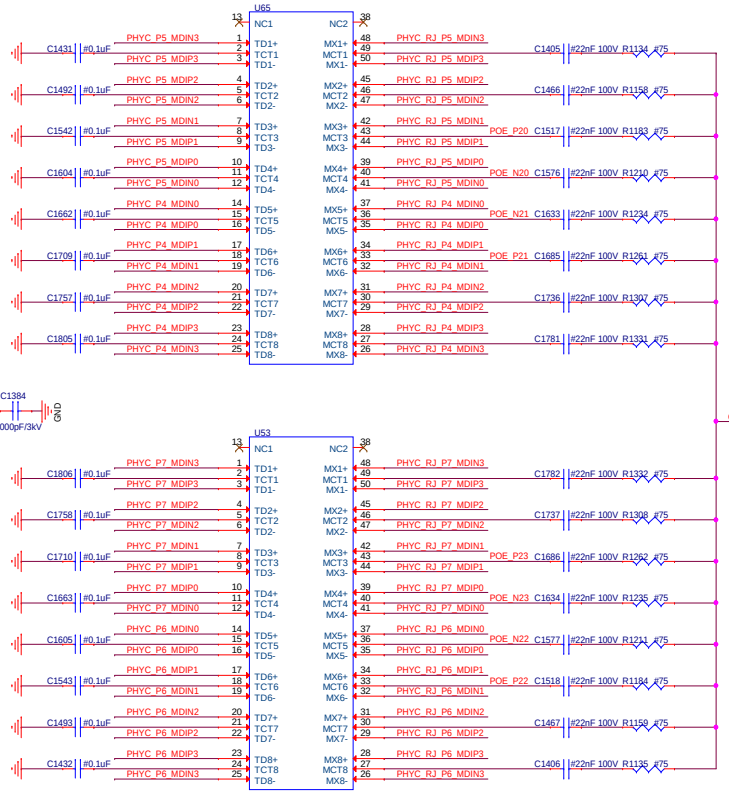
PHY3

Front panel port	17	19	21	23
PHY phiscal port	P1	P2	P5	P6
Front panel port	18	20	22	24
PHY phiscal port	P0	P3	P4	P7

PHY3 port17~port20



PHY3 port21~port24



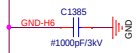


Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

POE main source: 115500000051A M-TEK
2nd source: 115500000068H TAG

Non POE main source: 115500000085A FPE
2nd source: 115500000050A M-TEK

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PHY4

Front panel port	25	27	29	31
PHY phiscal port	P1	P2	P5	P6
Front panel port	26	28	30	32
PHY phiscal port	P0	P3	P4	P7

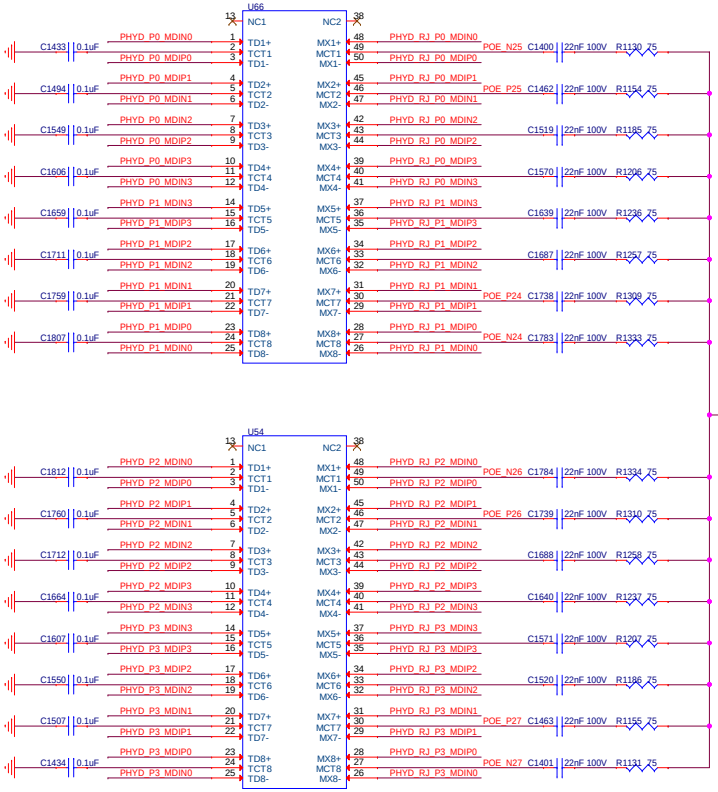
54 POE_P[24:31]
54 POE_N[24:31]

35 PHYD_RJ_P0_MDIP[0:3]
35 PHYD_RJ_P0_MDIN[0:3]
35 PHYD_RJ_P1_MDIP[0:3]
35 PHYD_RJ_P1_MDIN[0:3]
35 PHYD_RJ_P2_MDIP[0:3]
35 PHYD_RJ_P2_MDIN[0:3]
35 PHYD_RJ_P3_MDIP[0:3]
35 PHYD_RJ_P3_MDIN[0:3]

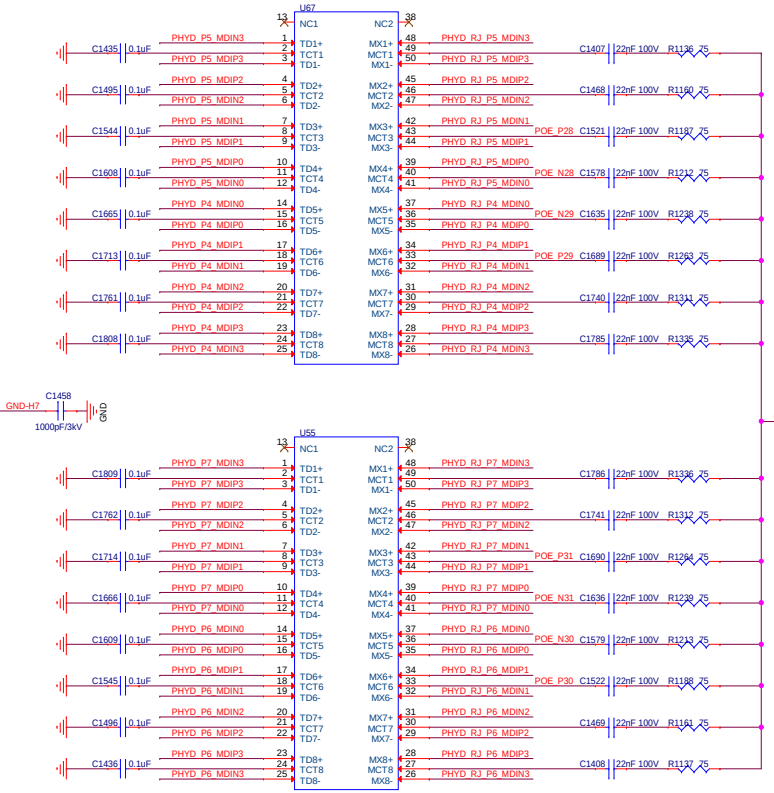
35 PHYD_RJ_P4_MDIP[0:3]
35 PHYD_RJ_P4_MDIN[0:3]
35 PHYD_RJ_P5_MDIP[0:3]
35 PHYD_RJ_P5_MDIN[0:3]
35 PHYD_RJ_P6_MDIP[0:3]
35 PHYD_RJ_P6_MDIN[0:3]
35 PHYD_RJ_P7_MDIP[0:3]
35 PHYD_RJ_P7_MDIN[0:3]

24 PHYD_P0_MDIP0 … PHYD_P0_MDIN3
24 PHYD_P1_MDIP0 … PHYD_P1_MDIN3
24 PHYD_P2_MDIP0 … PHYD_P2_MDIN3
24 PHYD_P3_MDIP0 … PHYD_P3_MDIN3
24 PHYD_P4_MDIP0 … PHYD_P4_MDIN3
24 PHYD_P5_MDIP0 … PHYD_P5_MDIN3
24 PHYD_P6_MDIP0 … PHYD_P6_MDIN3
24 PHYD_P7_MDIP0 … PHYD_P7_MDIN3

PHY4 port25~port28



PHY4 port29~port32



GND-H7 C1458 1000pF/3kV GND
GND-H8 C1386 1000pF/3kV GND

Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

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POE main source: 11550000051A M-TEK
2nd source: 11550000068H TAG

Non POE main source: 11550000085A FPE
2nd source: 11550000050A M-TEK

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PHY5

Front panel port	33	35	37	39
PHY phiscal port	P1	P2	P5	P6
Front panel port	34	36	38	40
PHY phiscal port	P0	P3	P4	P7

52 POE_P[32:39]
52 POE_N[32:39]

35 PHYE_RJ_P0_MDIP[0:3]
35 PHYE_RJ_P0_MDIN[0:3]
35 PHYE_RJ_P1_MDIP[0:3]
35 PHYE_RJ_P1_MDIN[0:3]
35 PHYE_RJ_P2_MDIP[0:3]
35 PHYE_RJ_P2_MDIN[0:3]
35 PHYE_RJ_P3_MDIP[0:3]
35 PHYE_RJ_P3_MDIN[0:3]

36 PHYE_RJ_P4_MDIP[0:3]
36 PHYE_RJ_P4_MDIN[0:3]
36 PHYE_RJ_P5_MDIP[0:3]
36 PHYE_RJ_P5_MDIN[0:3]
36 PHYE_RJ_P6_MDIP[0:3]
36 PHYE_RJ_P6_MDIN[0:3]
36 PHYE_RJ_P7_MDIP[0:3]
36 PHYE_RJ_P7_MDIN[0:3]

25 PHYE_P0_MDIP0
25 PHYE_P0_MDIN0
25 PHYE_P0_MDIP1
25 PHYE_P0_MDIN1
25 PHYE_P0_MDIP2
25 PHYE_P0_MDIN2
25 PHYE_P0_MDIP3
25 PHYE_P0_MDIN3

PHYE_P7_MDIN3 25
PHYE_P7_MDIP3 25
PHYE_P7_MDIN2 25
PHYE_P7_MDIP2 25
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PHYE_P7_MDIP1 25
PHYE_P7_MDIN0 25
PHYE_P7_MDIP0 25

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25 PHYE_P1_MDIN0
25 PHYE_P1_MDIP1
25 PHYE_P1_MDIN1
25 PHYE_P1_MDIP2
25 PHYE_P1_MDIN2
25 PHYE_P1_MDIP3
25 PHYE_P1_MDIN3

PHYE_P6_MDIN3 25
PHYE_P6_MDIP3 25
PHYE_P6_MDIN2 25
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PHYE_P6_MDIP0 25

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25 PHYE_P2_MDIN0
25 PHYE_P2_MDIP1
25 PHYE_P2_MDIN1
25 PHYE_P2_MDIP2
25 PHYE_P2_MDIN2
25 PHYE_P2_MDIP3
25 PHYE_P2_MDIN3

PHYE_P5_MDIN3 25
PHYE_P5_MDIP3 25
PHYE_P5_MDIN2 25
PHYE_P5_MDIP2 25
PHYE_P5_MDIN1 25
PHYE_P5_MDIP1 25
PHYE_P5_MDIN0 25
PHYE_P5_MDIP0 25

25 PHYE_P3_MDIP0
25 PHYE_P3_MDIN0
25 PHYE_P3_MDIP1
25 PHYE_P3_MDIN1
25 PHYE_P3_MDIP2
25 PHYE_P3_MDIN2
25 PHYE_P3_MDIP3
25 PHYE_P3_MDIN3

PHYE_P4_MDIN3 25
PHYE_P4_MDIP3 25
PHYE_P4_MDIN2 25
PHYE_P4_MDIP2 25
PHYE_P4_MDIN1 25
PHYE_P4_MDIP1 25
PHYE_P4_MDIN0 25
PHYE_P4_MDIP0 25

PHY5 port33~port36



PHY5 port37~port40

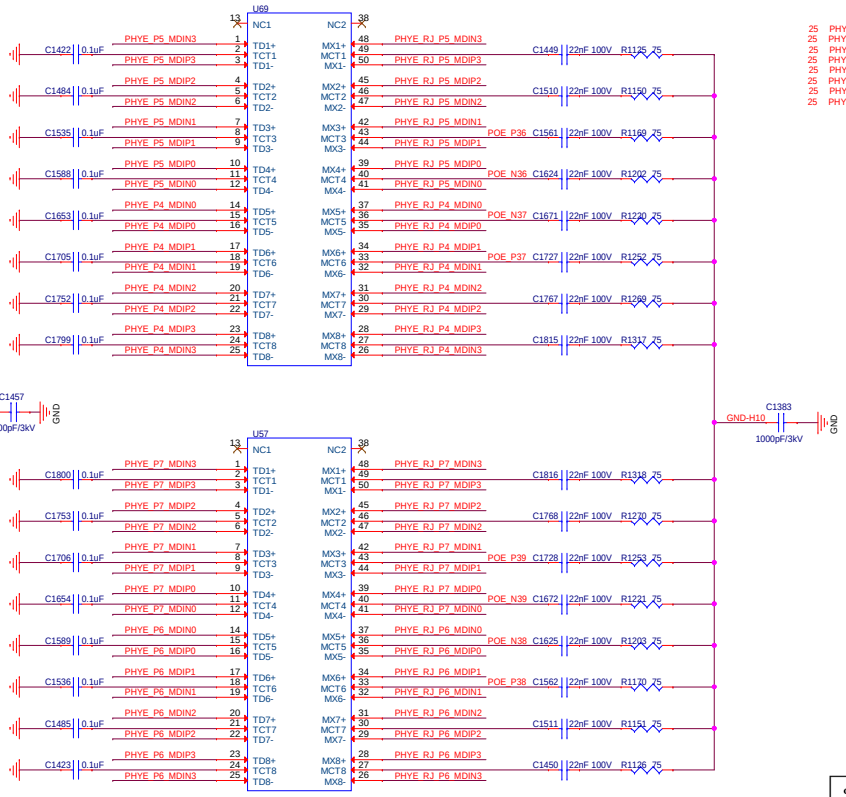


Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

POE main source: 115500000051A M-TEK
2nd source: 115500000068H TAG

Non POE main source: 115500000085A FPE
2nd source: 115500000050A M-TEK

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PHY6				
Front panel port	41	43	45	47
PHY phiscal port	P1	P2	P5	P6
Front panel port	42	44	46	48
PHY phiscal port	P0	P3	P4	P7

PHY6 port41~port44

PHY6 port45~port48

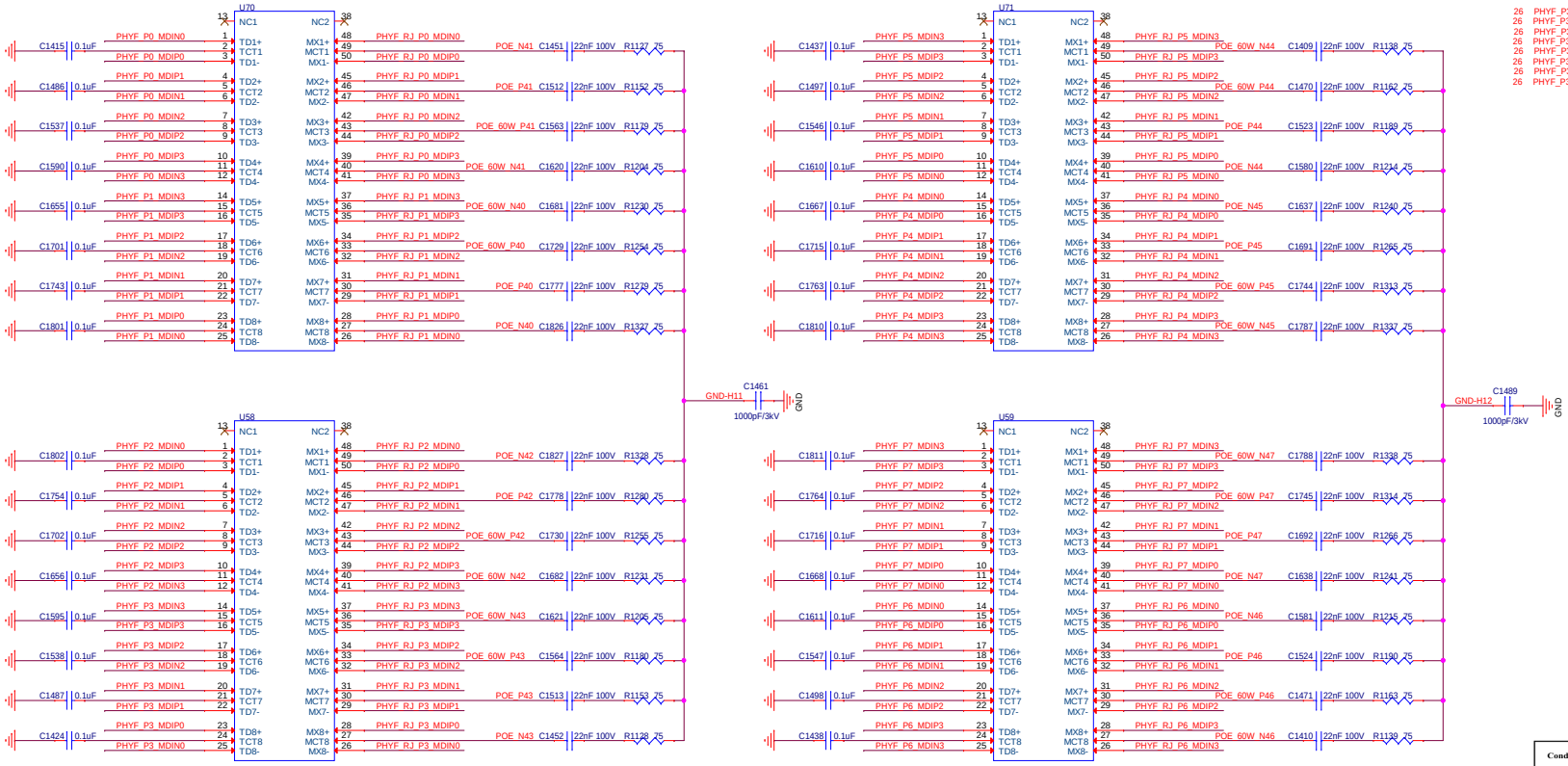


Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

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POE main source: 115500000051A M-TEK
2nd source: 115500000068H TAG

Non POE main source: 115500000085A FPE
2nd source: 115500000050A M-TEK

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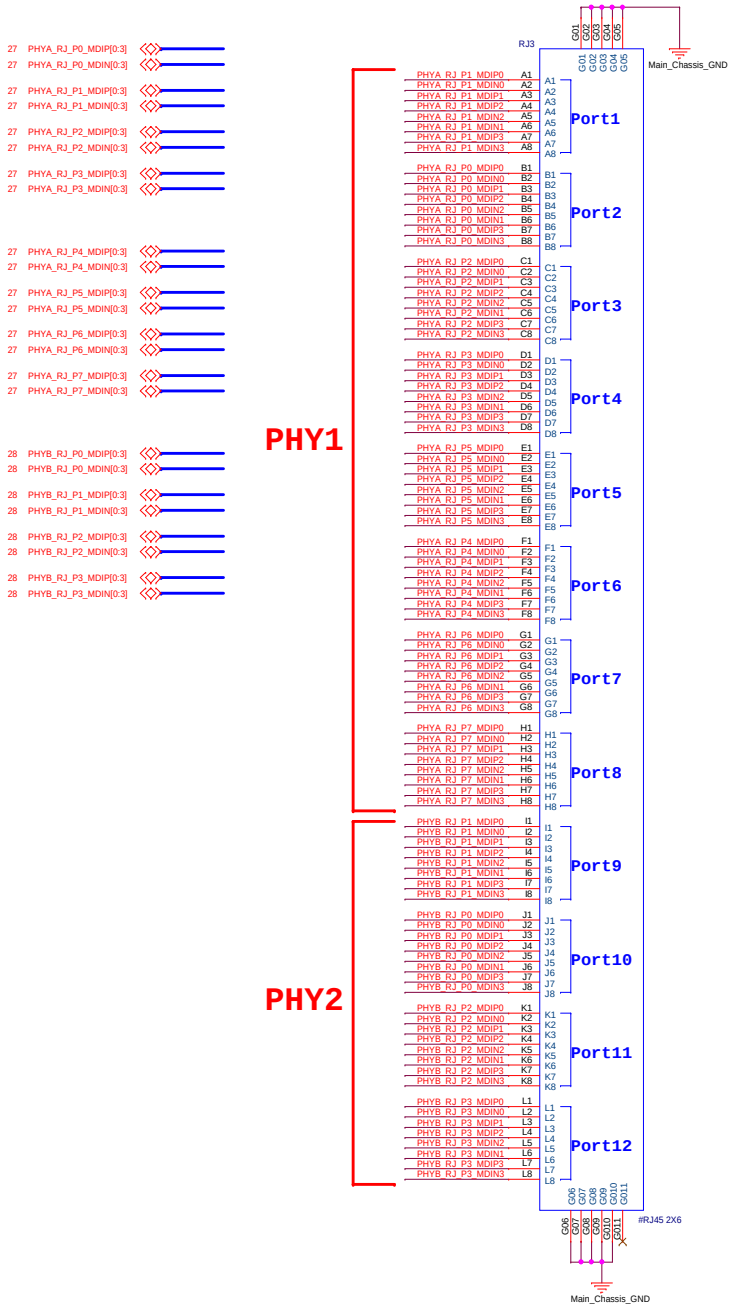
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	PHY1				PHY2				PHY3				PHY4				PHY5				PHY6			
Front panel port	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47
PHY phiscal port	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6
Front panel port	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48
PHY phiscal port	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7





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	PHY1				PHY2				PHY3				PHY4				PHY5				PHY6			
Front panel port	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47
PHY phiscal port	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6
Front panel port	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48
PHY phiscal port	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7

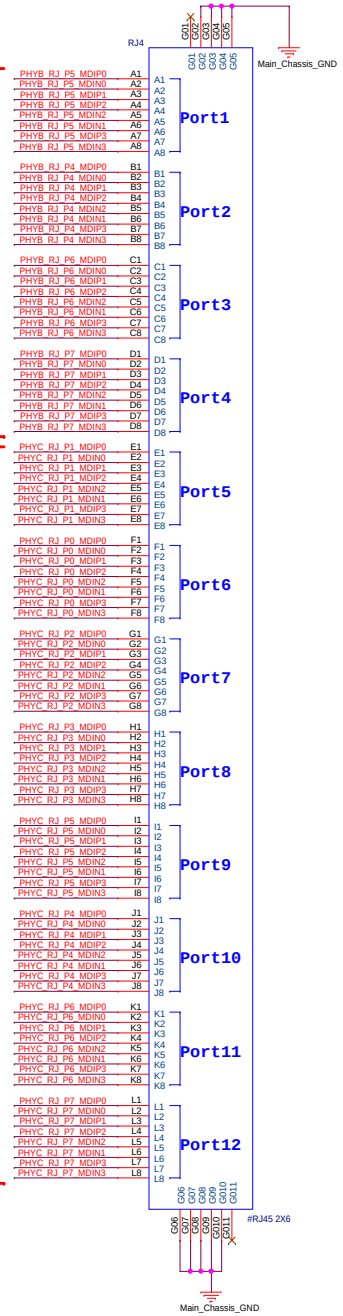
PHY2

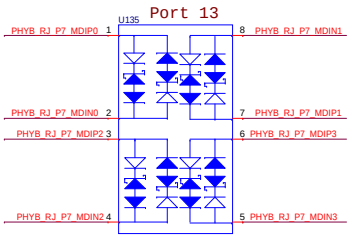
28 PHYB_RJ_P4_MDIP[0:3]
28 PHYB_RJ_P4_MDIN[0:3]
28 PHYB_RJ_P5_MDIP[0:3]
28 PHYB_RJ_P5_MDIN[0:3]
28 PHYB_RJ_P6_MDIP[0:3]
28 PHYB_RJ_P6_MDIN[0:3]
28 PHYB_RJ_P7_MDIP[0:3]
28 PHYB_RJ_P7_MDIN[0:3]

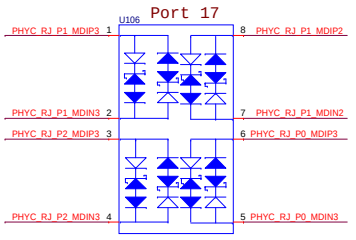
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29 PHYC_RJ_P0_MDIN[0:3]
29 PHYC_RJ_P1_MDIP[0:3]
29 PHYC_RJ_P1_MDIN[0:3]
29 PHYC_RJ_P2_MDIP[0:3]
29 PHYC_RJ_P2_MDIN[0:3]
29 PHYC_RJ_P3_MDIP[0:3]
29 PHYC_RJ_P3_MDIN[0:3]

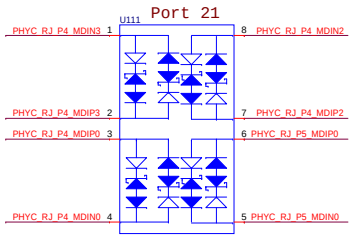
PHY3

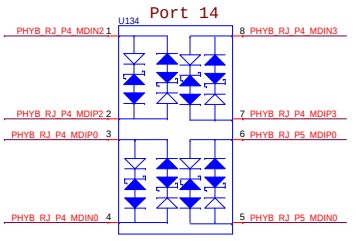
29 PHYC_RJ_P4_MDIP[0:3]
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29 PHYC_RJ_P5_MDIP[0:3]
29 PHYC_RJ_P5_MDIN[0:3]
29 PHYC_RJ_P6_MDIP[0:3]
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29 PHYC_RJ_P7_MDIN[0:3]

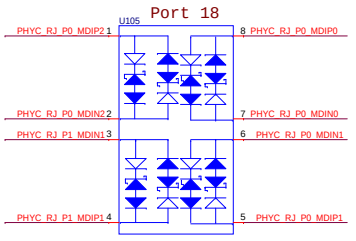


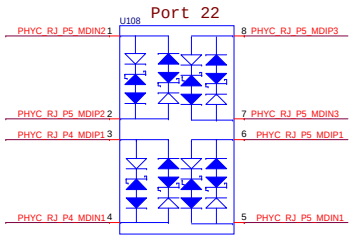


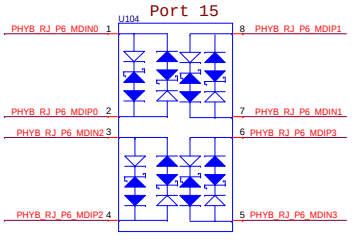


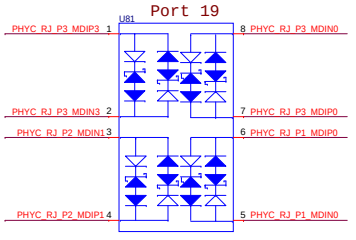


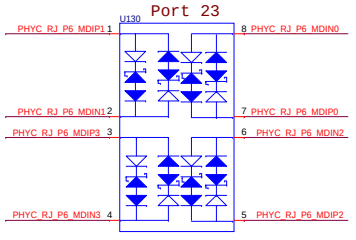


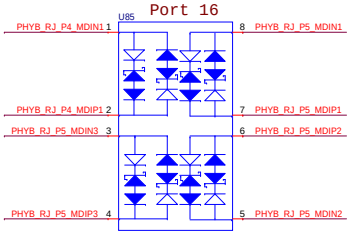


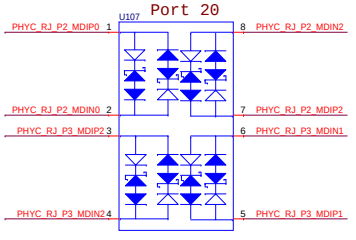


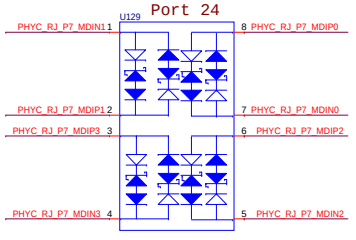












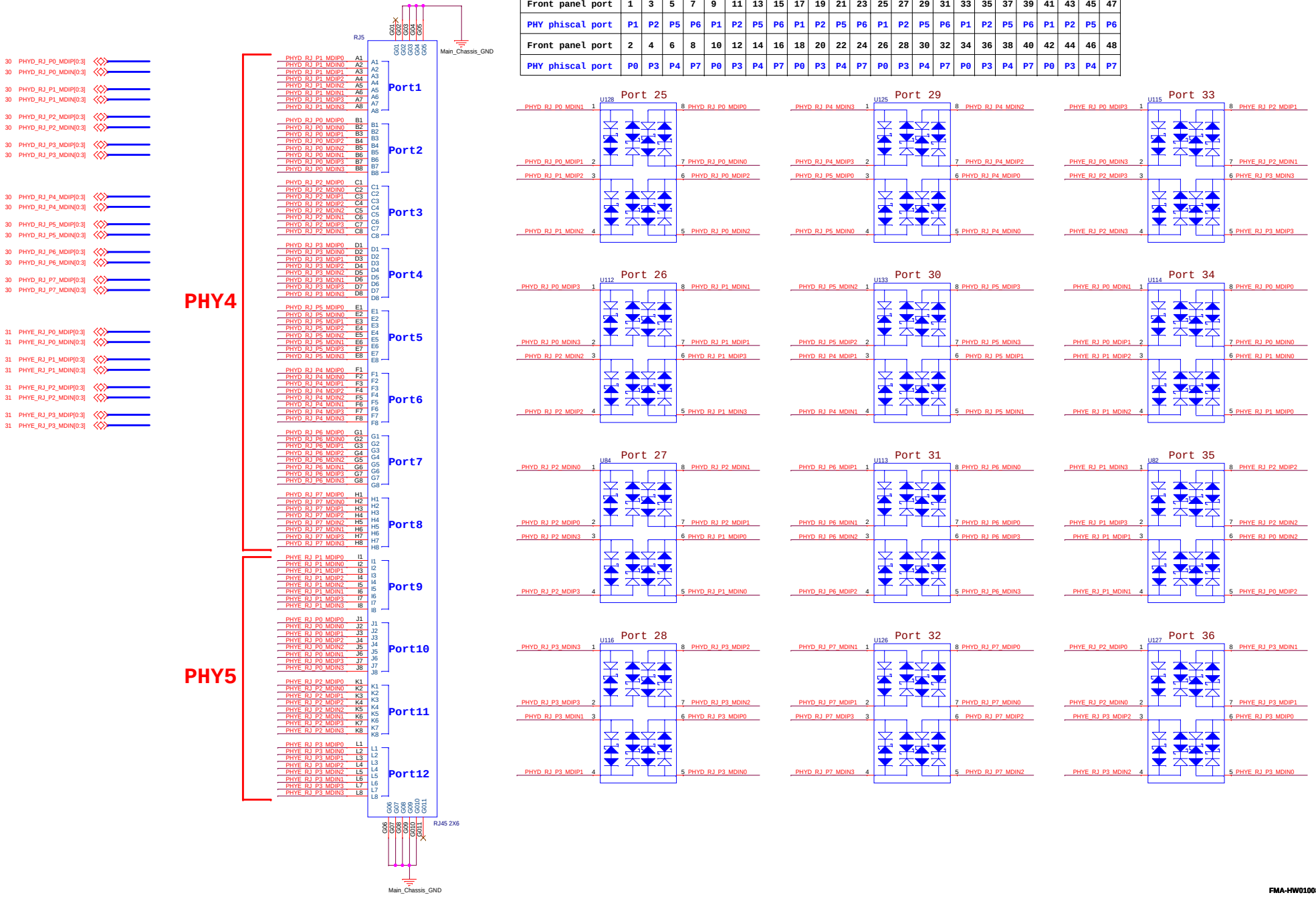
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	PHY1				PHY2				PHY3				PHY4				PHY5				PHY6			
Front panel port	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47
PHY phiscal port	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6
Front panel port	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48
PHY phiscal port	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7



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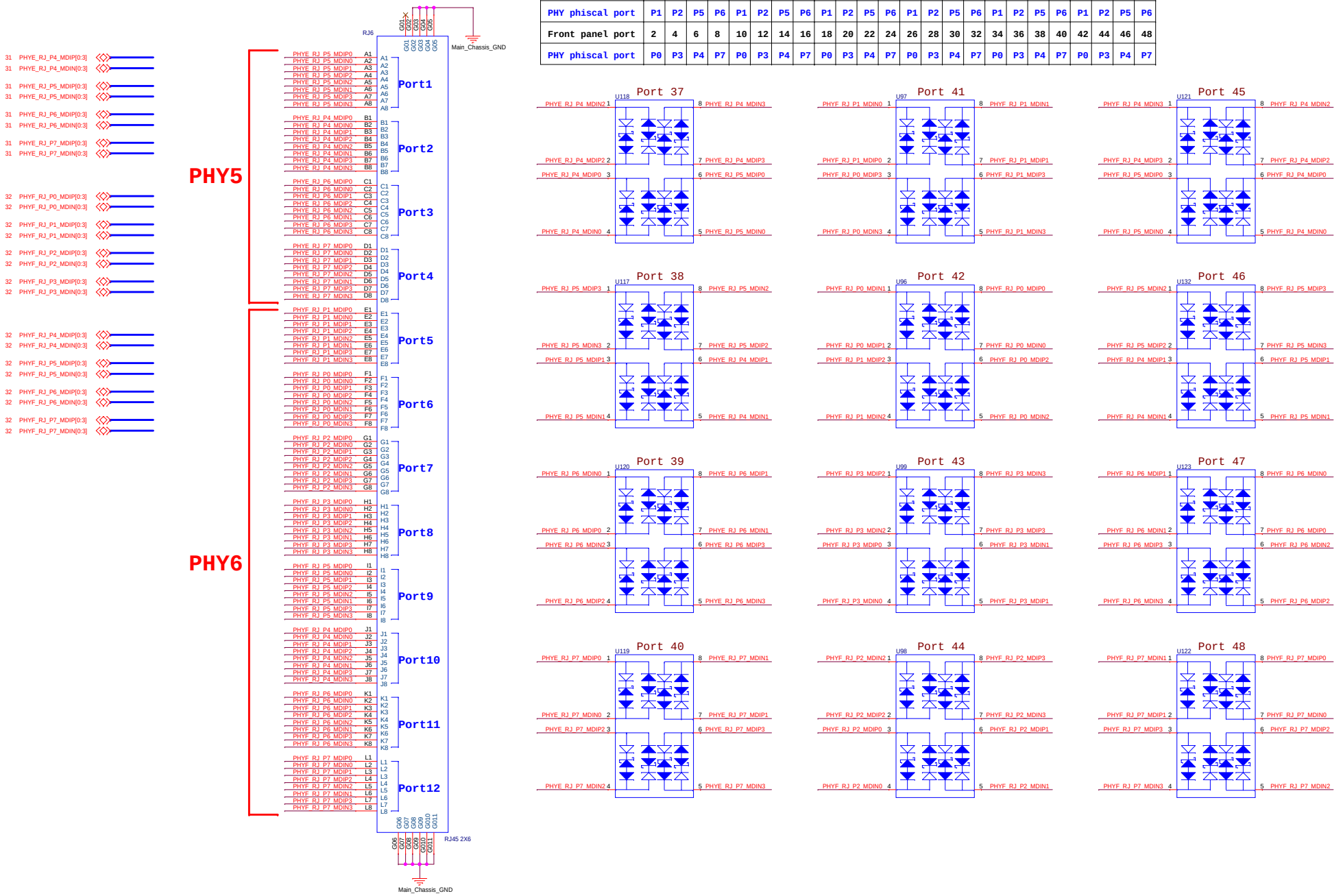
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	PHY1				PHY2				PHY3				PHY4				PHY5				PHY6			
Front panel port	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47
PHY phiscal port	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6	P1	P2	P5	P6
Front panel port	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48
PHY phiscal port	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7	P0	P3	P4	P7



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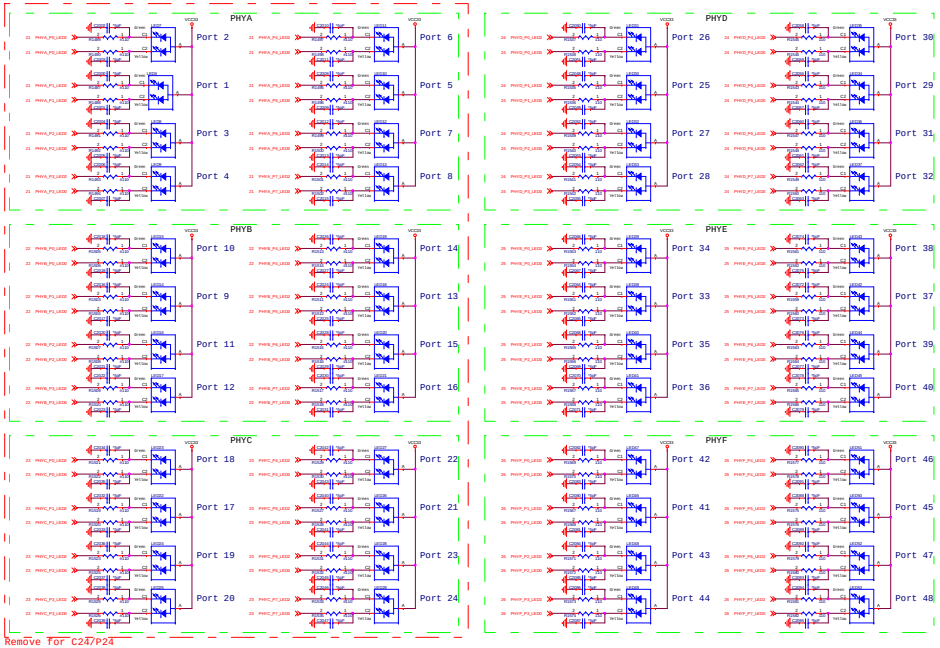
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Remove for C247P24

C48P48

PHY Chip #	PHY#1				PHY#2				PHY#3				PHY#4				PHY#5				PHY#6			
Front panel port	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47
PHY physic port	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Front panel port	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48
PHY physic port	8	7	6	5	4	3	2	1	16	15	14	13	12	11	10	9	24	23	22	21	20	19	18	17

C24P24

PHY Chip #	[redacted]	PHY#4				PHY#5				PHY#6			
Front panel port		1	3	5	7	9	11	13	15	17	19	21	23
PHY physic port		1	2	3	4	5	6	7	8	9	10	11	12
Front panel port		2	4	6	8	10	12	14	16	18	20	22	24
PHY physic port		8	7	6	5	4	3	2	1	12	11	10	9

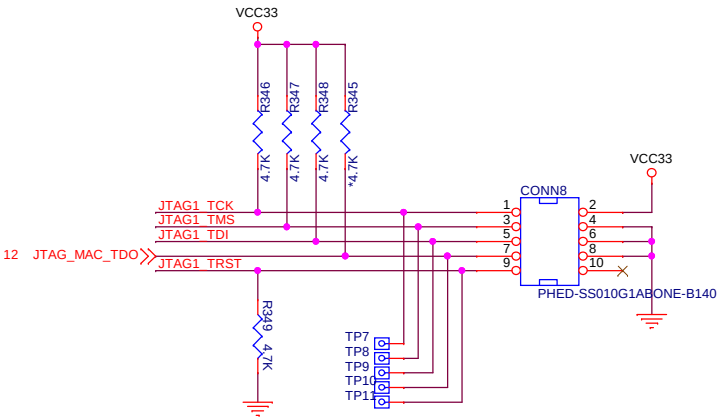
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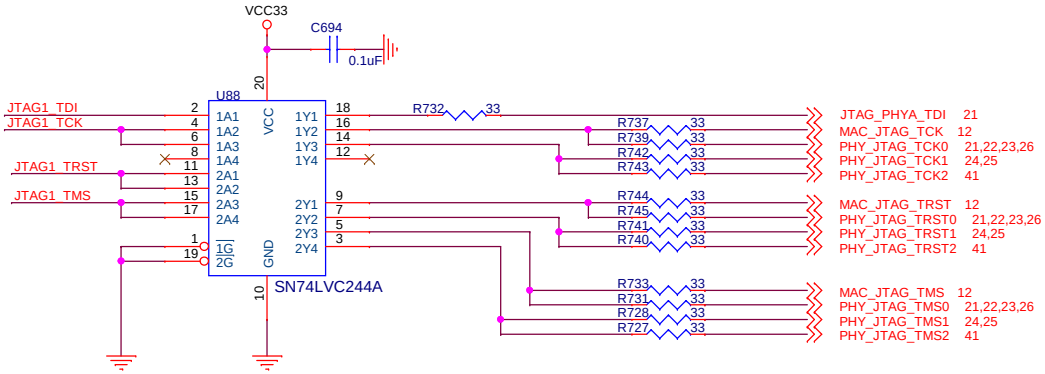
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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
E	1G PORT LED	Chaohua_Chang

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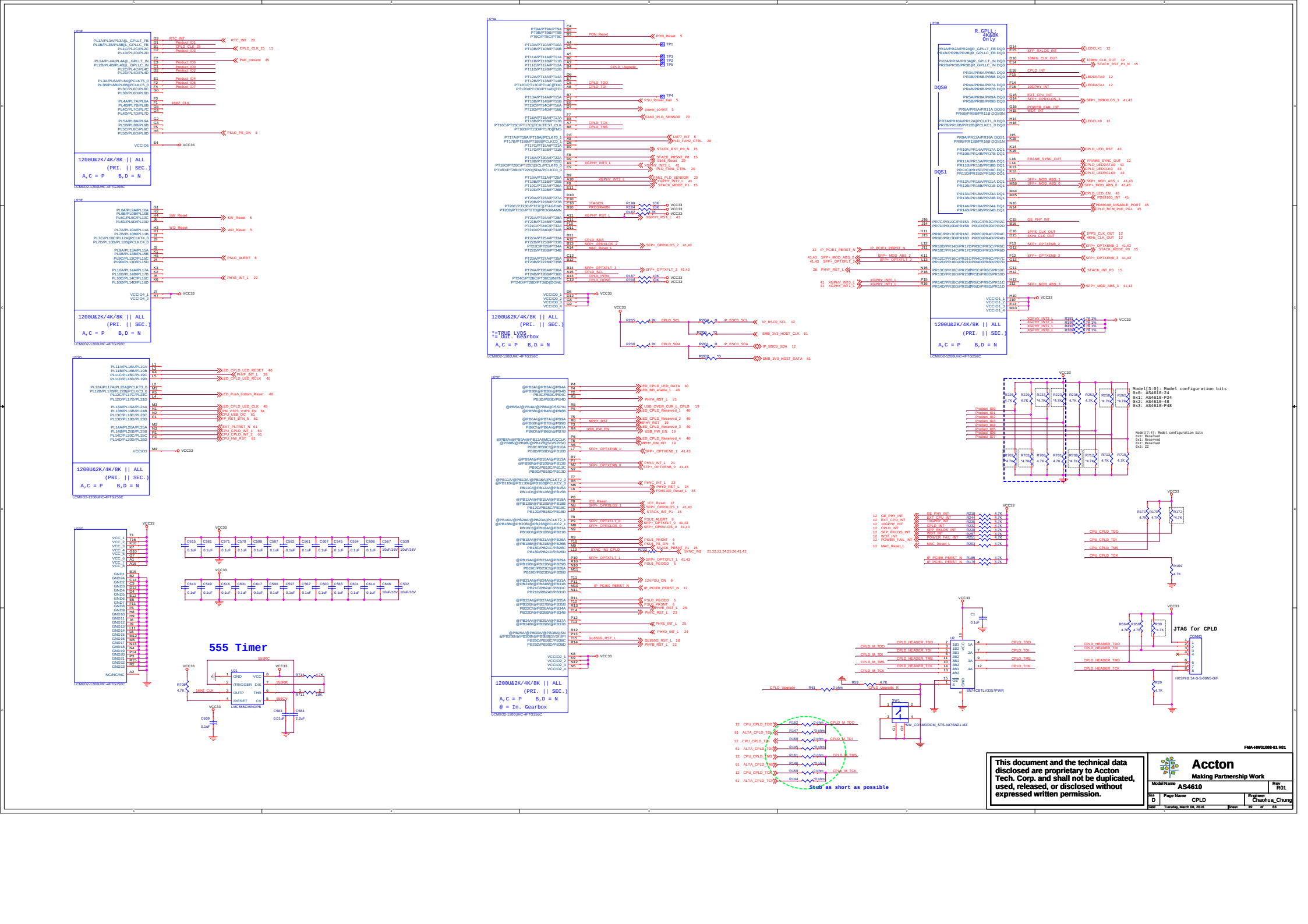
Accton

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Model Name	Rev
AS4610	R01

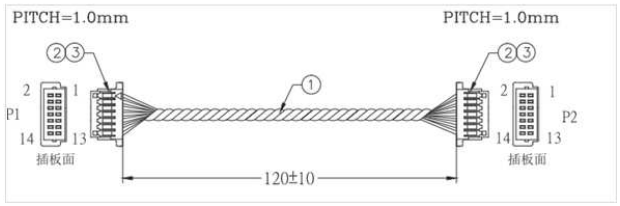
Size	Page Name	Engineer
B	JTAG	Chaohua_Chung

Date: Tuesday, March 08, 2016 Sheet 38 of 66


555 Timer
JTAG for CPLD
1200U&2K/4K/8K || ALL (PRI. || SEC.)
A,C = P B,D = N
*=TRUE LVDS
*= Out. Gearbox
@ = In. Gearbox
Stub as short as possible
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Accton
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Model Name AS4610
Rev R01
Size D
Page Name CPLD
Engineer Chaohua_Chung
Date: Tuesday, March 08, 2016
Sheet 39 of 66
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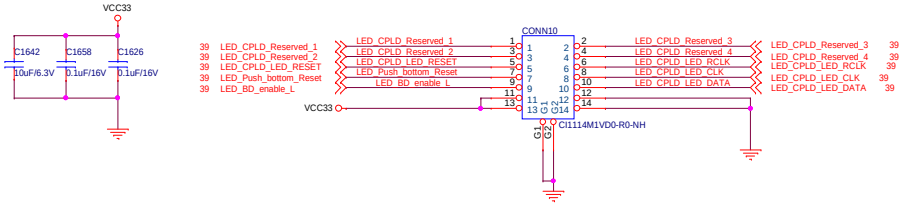
Mainboard-P1			
CPLD_Reserved_1	1	2	CPLD_Reserved_3
CPLD_Reserved_2	3	4	CPLD_Reserved_4
CPLD_LED_RESET	5	6	CPLD_LED_RCLK
Push_bottom_Reset	7	8	CPLD_LED_CLK
Register_Enable	9	10	CPLD_LED_DATA
VCC33	11	12	GND
VCC33	13	14	GND

Module-P2			
CPLD_Reserved_1	1	2	CPLD_Reserved_3
CPLD_Reserved_2	3	4	CPLD_Reserved_4
CPLD_LED_RESET	5	6	CPLD_LED_RCLK
Push_bottom_Reset	7	8	CPLD_LED_CLK
Register_Enable	9	10	CPLD_LED_DATA
VCC33	11	12	GND
VCC33	13	14	GND



WIRE LIST

P1	P2	
1	1	RED
2	2	BLACK
3	3	BLACK
4	4	BLACK
5	5	BLACK
6	6	BLACK
7	7	BLACK
8	8	BLACK
9	9	BLACK
10	10	BLACK
11	11	BLACK
12	12	BLACK
13	13	BLACK
14	14	BLACK



FMA-HW01008-01 R01

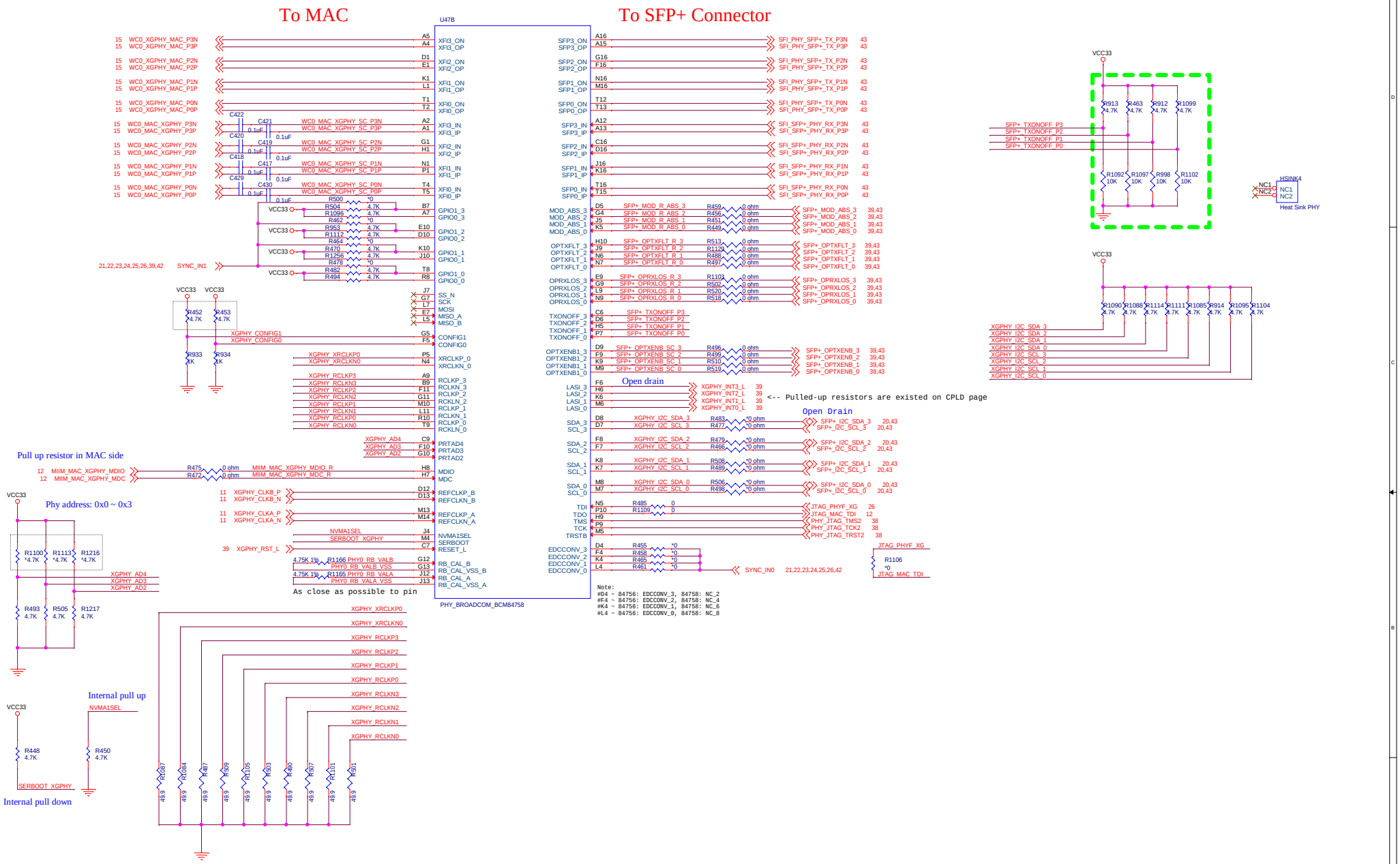
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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	LED Board Connector	Chaohua_Chung

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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	BCM84758_XGPHY_INTERFACE	Chaohua_Chung

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Note:
#C8 ~ 84756: VDDIOOPT, 84758: DVDD33_1
84756: can be 1.0V or 3.3V, 84758 should be 3.3V
#E6 ~ 84756: VDDIOI2C_1, 84758 : DVDD33_2
Both are 3.3V
#L10 ~ 84756: NC_4, 84758 : VSS_54
84756: should be floated, 84758 should be GND.
#L8 ~ 84756: VDDIOGPIO, 84758: DVDD33_3
84756: can be 1.0V or 3.3V, 84758 should be 3.3V
#N10 ~ 84756: NC_5, 84758: SYNC_OUT
84756 should be floated, 84758 is SYNC_OUT
#N8 ~ 84756: VDDIOI2C_2, 84758 : DVDD33_4
Both are 3.3V
#P6 ~ 84756: NC_6, 84758: SYNC_IN
84756 should be floated, 84758 is SYNC_IN

U47A

PHY_BROADCOM_BCM84758

BCM84758:
L8, N8 & C8 pin: DVDD33

VDDOLVL:1
VDDOSYS=2.5 ~ 3.3V

VDDOLVL: 0
VDDOSYS=1V

1V 268mA
1V 248mA
1V 268mA
1V 204mA
1V 520mA
1V 520mA
1V 520mA
1V 1880mA

BCM84758:
L10 pin: VSS
N10 pin: SYNC_OUT
P6 pin: SYNC_IN

As close as possible to pin

FMA-HW01008-01 R01

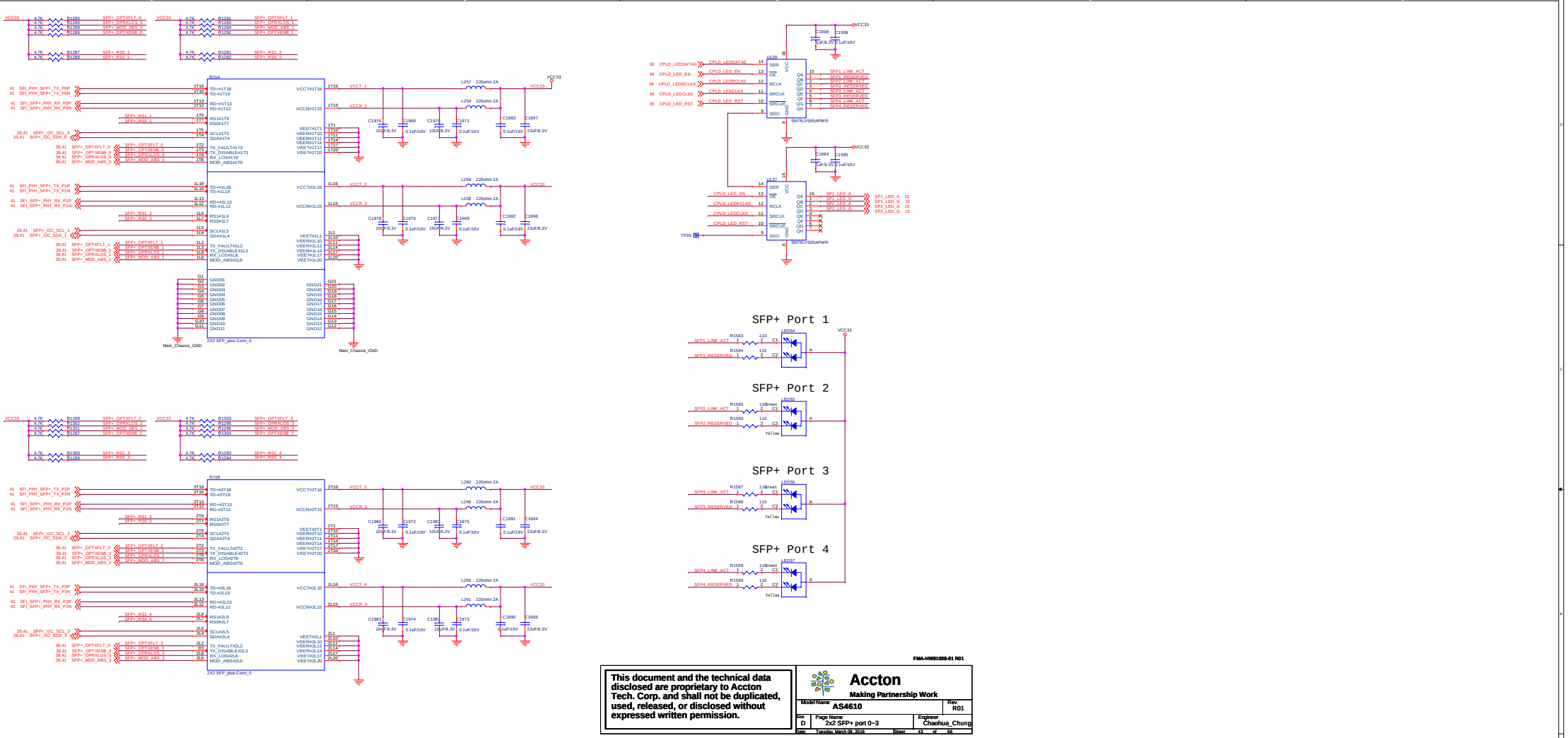
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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	BCM84758_XGPHY_PWR	Chaohua_Chung

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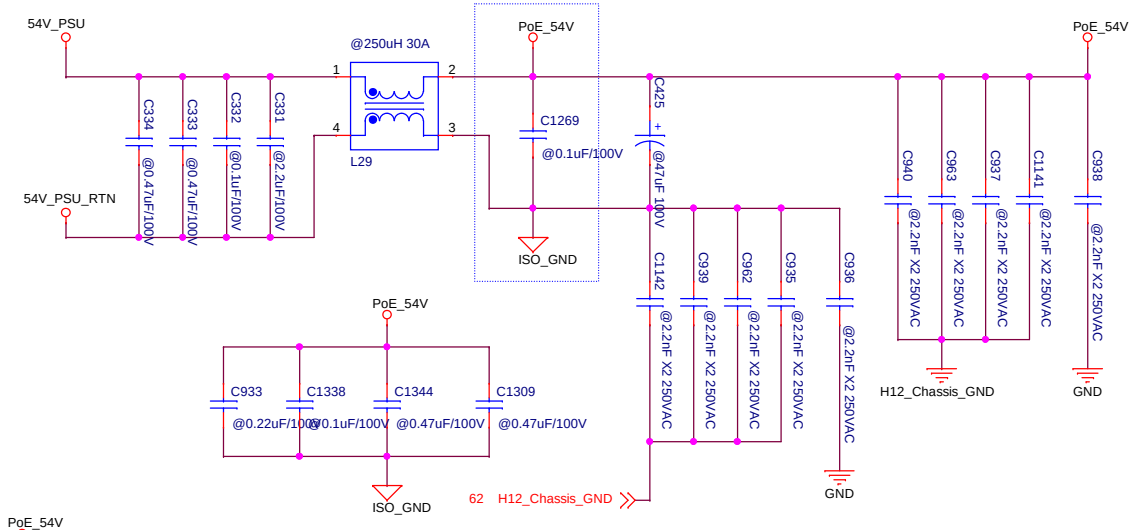


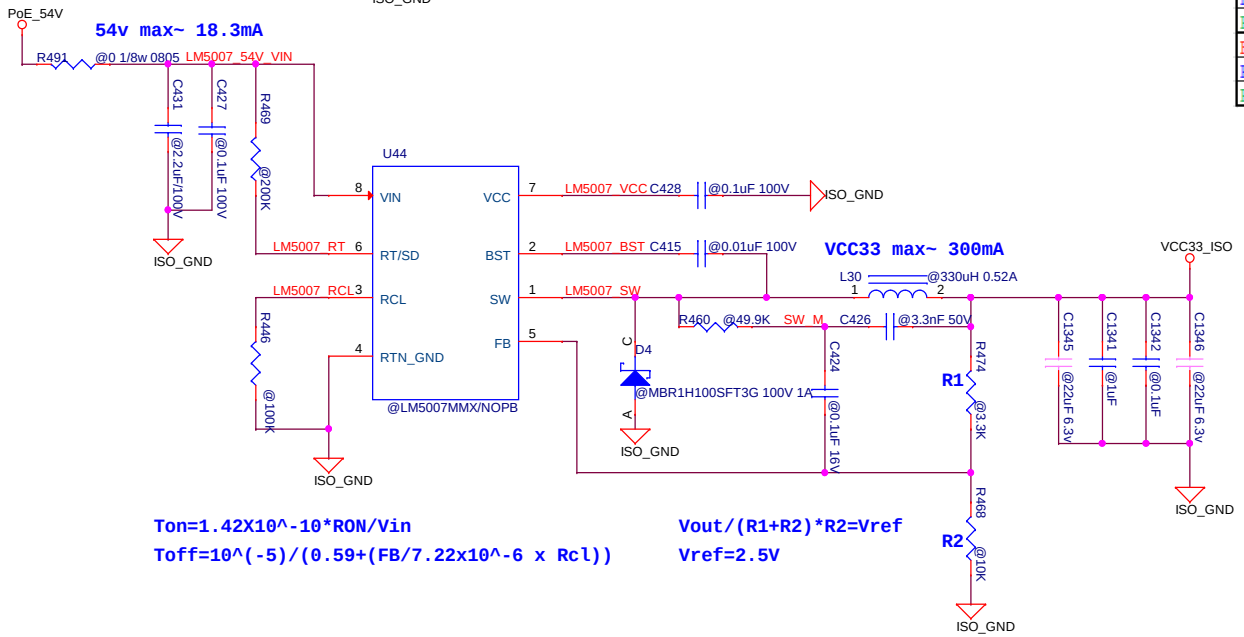
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Model Name	AS4610	Rev	R01
Size	D	Page Name	2x2 SFP+ port 0~3
Engineer	Chaohua_Chung		
Date:	Tuesday, March 08, 2016	Sheet	43 of 66





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MAC_QSGMII	QG3_0	QG3_1	QG4_0	QG4_1	QG5_0	QG5_1	QG0_0	GQ0_1	QG1_0	GQ1_1	QG2_0	QG2_1
PoE Chip #	PoE#7		PoE#6		PoE#5		PoE#4		PoE#3		PoE#2	PoE#1
PHY Chip #	PHY#1		PHY#2		PHY#3		PHY#4		PHY#5		PHY#6	
Front panel port	1 3 5 7		9 11 13 15		17 19 21 23		25 27 29 31		33 35 37 39		41 43 45 47	
PoE port	47 45 43 41		39 37 35 33		31 29 27 25		23 21 19 17		15 13 11 9		7 5 3 1	
PHY phiscal port	1 2 5 6		9 10 13 14		17 18 21 22		25 26 29 30		33 34 37 38		41 42 45 46	
Front panel port	2 4 6 8		10 12 14 16		18 20 22 24		26 28 30 32		34 36 38 40		42 44 46 48	
PoE port	48 46 44 42		40 38 36 34		32 30 28 26		24 22 20 18		16 14 12 10		8 6 4 2	
PHY phiscal port	0 3 4 7		8 11 12 15		16 19 20 23		24 27 28 31		32 35 36 39		40 43 44 47	

24

MAC_QSGMII	[redacted]	QG0_0	GQ0_1	QG1_0	GQ1_1	QG2_0	QG2_1
PoE Chip #		PoE#4		PoE#3		PoE#2	PoE#1
PHY Chip #		PHY#4		PHY#5		PHY#6	
Front panel port		1 3 5 7		9 11 13 15		17 19 21 23	
PoE port		23 21 19 17		15 13 11 9		7 5 3 1	
PHY phiscal port		1 2 5 6		9 10 13 14		17 18 21 22	
Front panel port		2 4 6 8		10 12 14 16		18 20 22 24	
PoE port		24 22 20 18		16 14 12 10		8 6 4 2	
PHY phiscal port		0 3 4 7		8 11 12 15		16 19 20 23	

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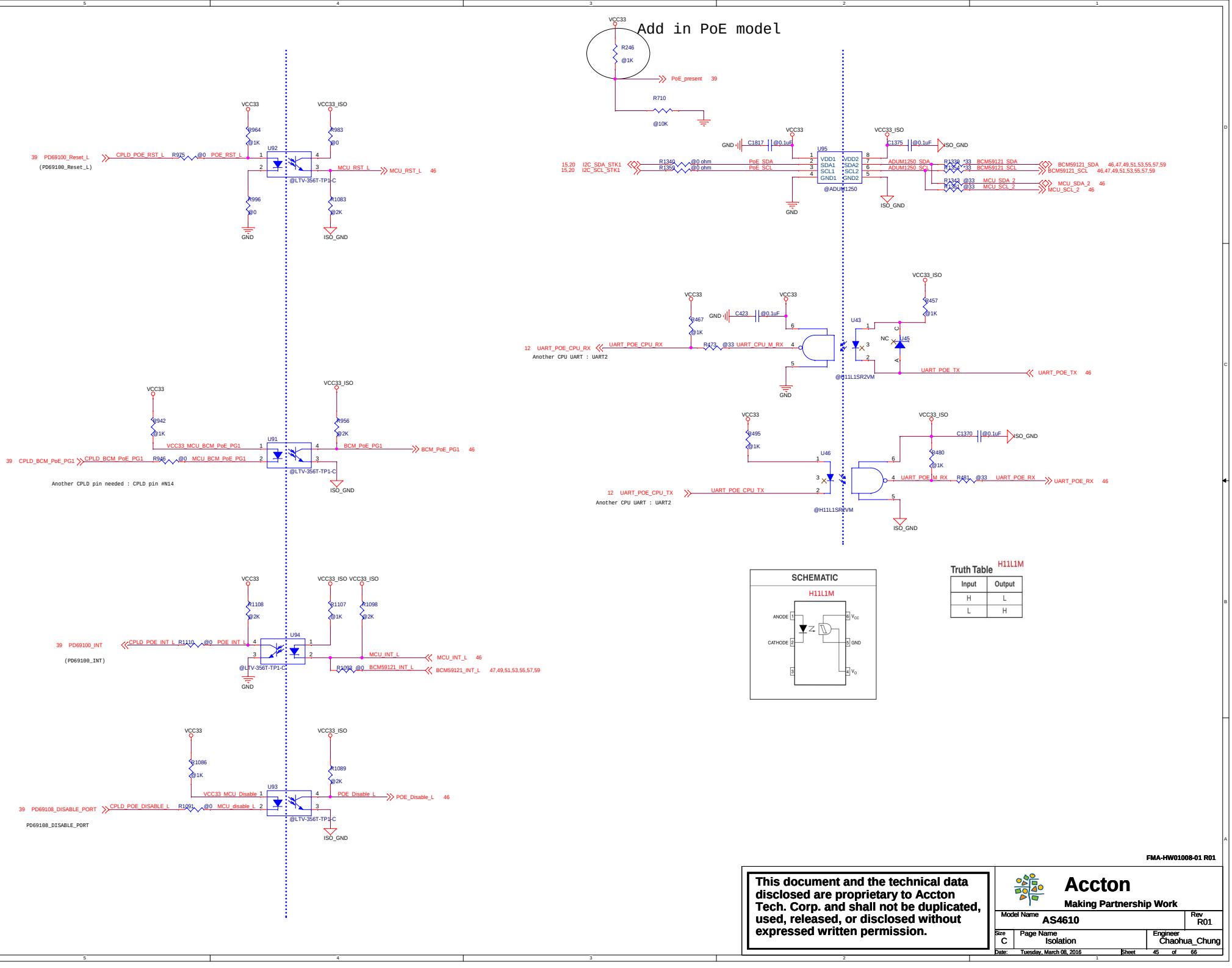
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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
B	POE POWER	Chaohua_Chung

Date: Tuesday, March 08, 2016 Sheet 44 of 66

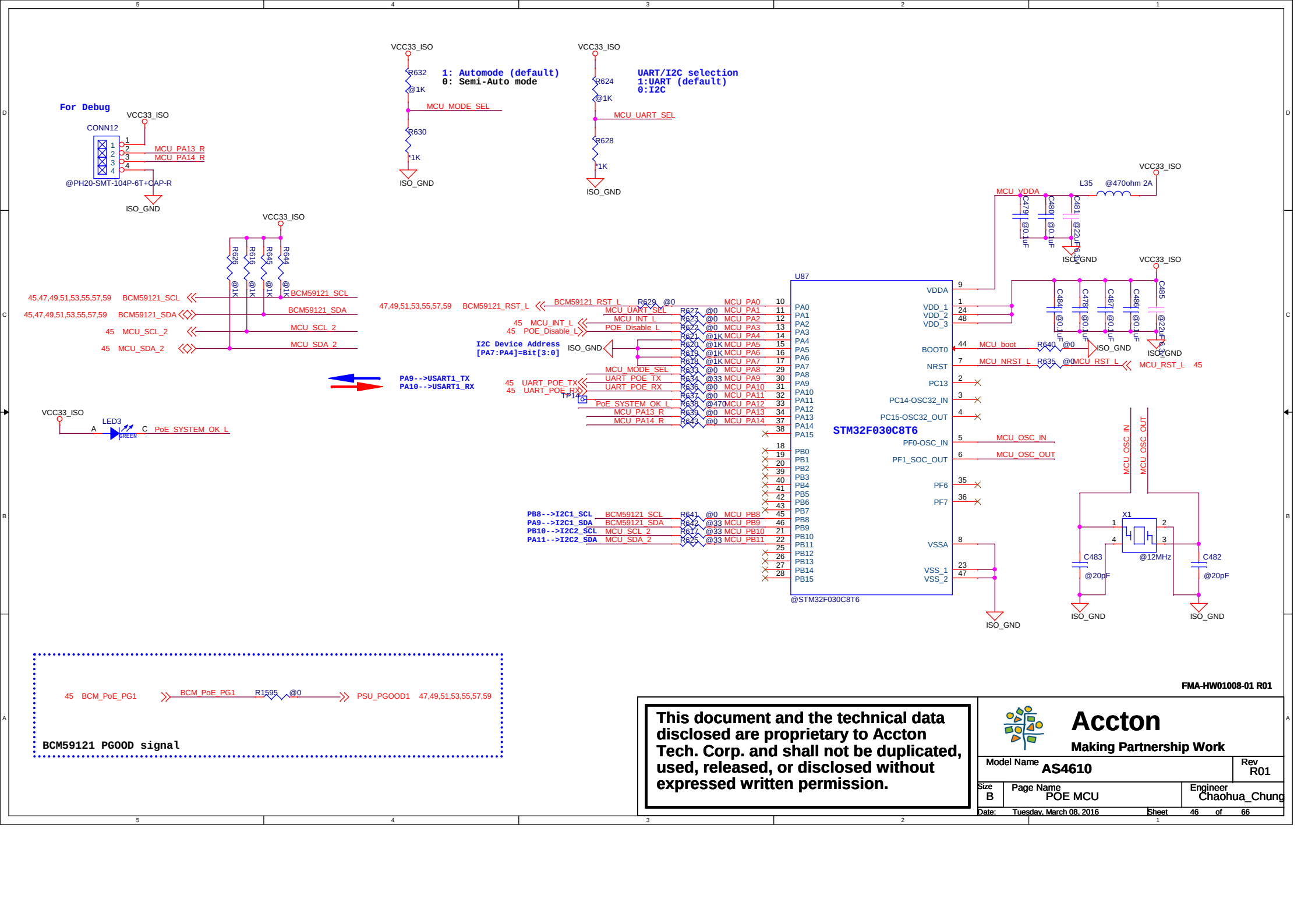


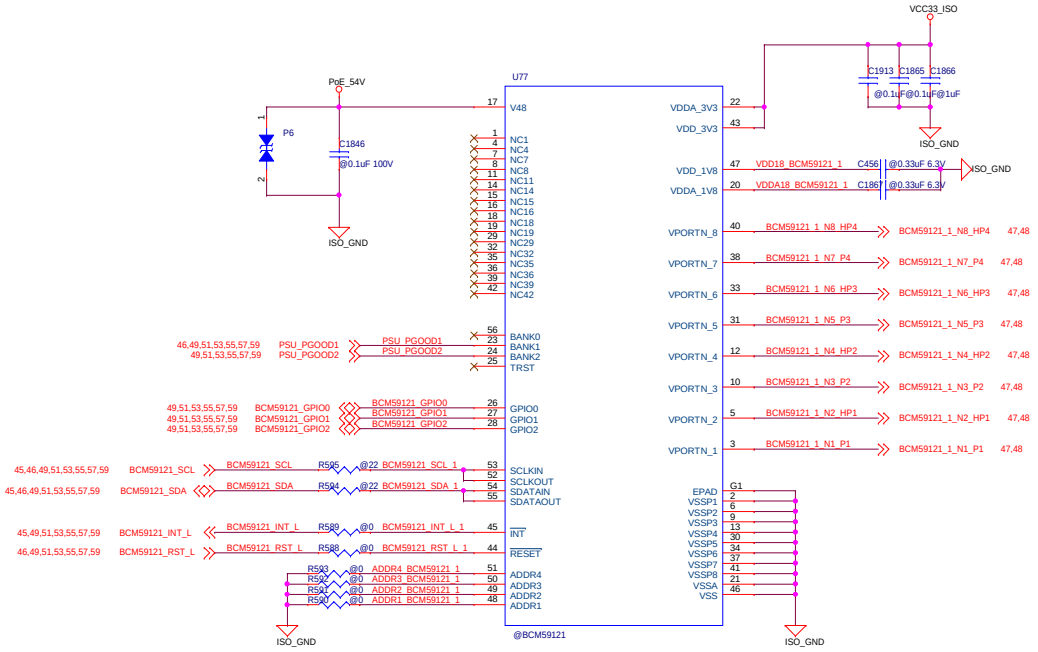
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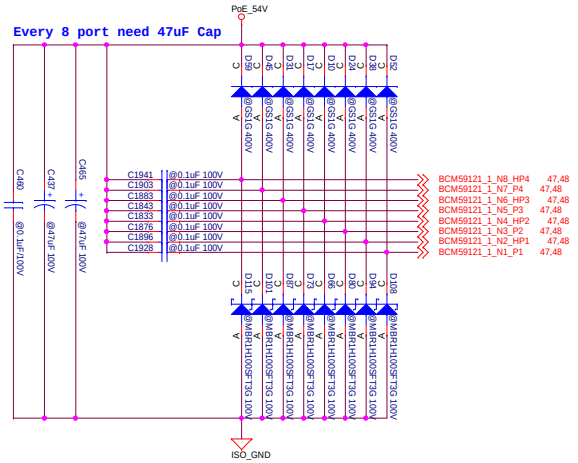
Model Name AS4610		Rev R01
Size C	Page Name Isolation	Engineer Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 45 of 66	


For Debug
CONN12
@PH20-SMT-104P-6T+CAP-R
MCU_PA13_R
MCU_PA14_R
VCC33_ISO
ISO_GND
R632 @1K
R630 *1K
MCU_MODE_SEL
1: Automode (default)
0: Semi-Auto mode
R624 @1K
R628 *1K
MCU_UART_SEL
UART/I2C selection
1:UART (default)
0:I2C
R626 @1K
R616 @1K
R645 @1K
R644 @1K
45,47,49,51,53,55,57,59 BCM59121_SCL
BCM59121_SDA
45 MCU_SCL_2
45 MCU_SDA_2
LED3
PoE_SYSTEM_OK_L
PA9-->USART1_TX
PA10-->USART1_RX
I2C Device Address
[PA7:PA4]=Bit[3:0]
U87
STM32F030C8T6
@STM32F030C8T6
BCM59121_RST_L
MCU_UART_SEL
MCU_INT_L
POE_Disable_L
UART_POE_TX
UART_POE_RX
TP14
PB8-->I2C1_SCL
PA9-->I2C1_SDA
PB10-->I2C2_SCL
PA11-->I2C2_SDA
MCU_VDDA
L35 @470ohm 2A
MCU_boot
MCU_NRST_L
MCU_RST_L
MCU_OSC_IN
MCU_OSC_OUT
X1 @12MHz
C483 @20pF
C482 @20pF
45 BCM_PoE_PG1
BCM_PoE_PG1
R1595 @0
PSU_PGOOD1
47,49,51,53,55,57,59
BCM59121 PGOOD signal
FMA-HW01008-01 R01
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Model Name AS4610
Rev R01
Size B
Page Name POE MCU
Engineer Chaohua_Chung
Date: Tuesday, March 08, 2016
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Device Address 0b0000

Internal Pull-Up or Pull-Down Resistor of Pins						
SCLKIN, SCLKOUT	–	R_{UP}	90	140	–	kΩ
SDATAIN, SDATAOUT	–	R_{UP}	90	140	–	kΩ
nINT	–	R_{UP}	90	140	–	kΩ
ADDR1, ADDR0, ADDR2, ADDR3, nRESET	–	R_{UP}	30	50	–	kΩ
Bank 0, Bank 1, Bank 2	–	R_{DOWN}	30	50	–	kΩ



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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	P04_BCM59121#1	Chaohua_Chung

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32 POE_P[44:47]
32 POE_N[44:47]
32 POE_60W_P[44:47]
32 POE_60W_N[44:47]

PoE_54V
L245 @3A 54V_P_P1 R1474 @0 POE_P46
47 BCM59121_1_N1_P1 BCM59121_1_N1_P1 L235 @3A PSE_59121_1_N1_P1 R1470 @0 POE_N46

PoE_54V
L186 @3A 54V_P_HP1 R1411 @0 POE_60W_P46
47 BCM59121_1_N2_HP1 BCM59121_1_N2_HP1 L193 @3A PSE_59121_1_N2_HP1 R1422 @0 POE_60W_N46

PoE_54V
L207 @3A 54V_P_P2 R1437 @0 POE_P47
47 BCM59121_1_N3_P2 BCM59121_1_N3_P2 L179 @3A PSE_59121_1_N3_P2 R1407 @0 POE_N47

PoE_54V
L165 @3A 54V_P_HP2 R1393 @0 POE_60W_P47
47 BCM59121_1_N4_HP2 BCM59121_1_N4_HP2 L137 @3A PSE_59121_1_N4_HP2 R1353 @0 POE_60W_N47

PoE_54V
L158 @3A 54V_P_P3 R1377 @0 POE_P44
47 BCM59121_1_N5_P3 BCM59121_1_N5_P3 L144 @3A PSE_59121_1_N5_P3 R1358 @0 POE_N44

PoE_54V
L221 @3A 54V_P_HP3 R1453 @0 POE_60W_P44
47 BCM59121_1_N6_HP3 BCM59121_1_N6_HP3 L172 @3A PSE_59121_1_N6_HP3 R1397 @0 POE_60W_N44

PoE_54V
L214 @3A 54V_P_P4 R1442 @0 POE_P45
47 BCM59121_1_N7_P4 BCM59121_1_N7_P4 L200 @3A PSE_59121_1_N7_P4 R1426 @0 POE_N45

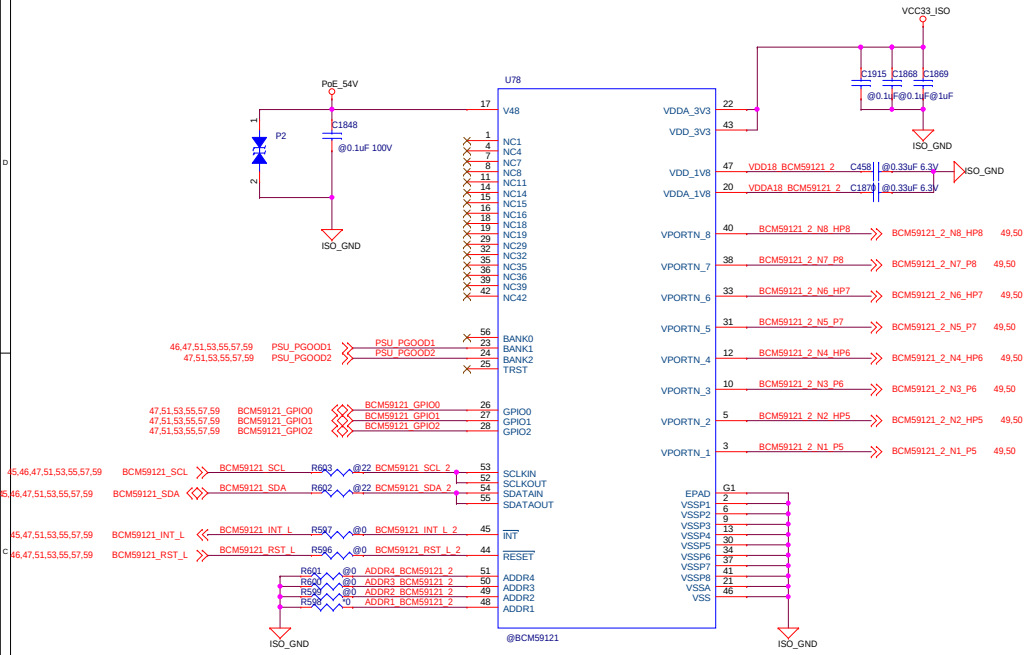
PoE_54V
L151 @3A 54V_P_HP4 R1371 @0 POE_60W_P45
47 BCM59121_1_N8_HP4 BCM59121_1_N8_HP4 L228 @3A PSE_59121_1_N8_HP4 R1457 @0 POE_60W_N45

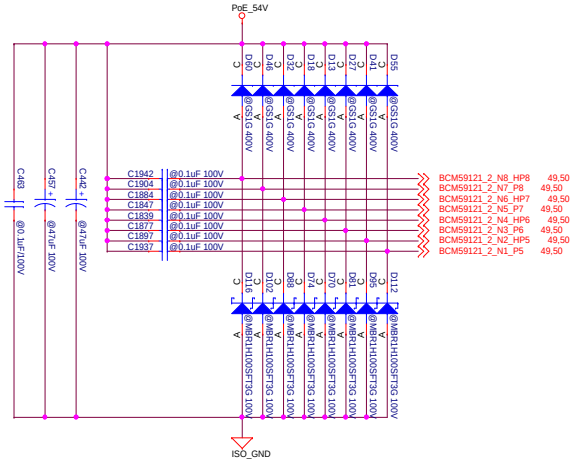
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Model Name: AS4610		Rev: R01
Size: B	Page Name: P05_EMI_Filter #1	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 48 of 66	





Device Address 0b0001

Internal Pull-Up or Pull-Down Resistor of Pins						
SCLKIN, SCLKOUT	–	R_{UP}	90	140	–	kΩ
SDATAIN, SDATAOUT	–	R_{UP}	90	140	–	kΩ
nINT	–	R_{UP}	90	140	–	kΩ
ADDR1, ADDR0, ADDR2, ADDR3, nRESET	–	R_{UP}	30	50	–	kΩ
Bank 0, Bank 1, Bank 2	–	R_{DOWN}	30	50	–	kΩ

PRELIMINARY

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Model Name	AS4610	Rev	R01
Size	C	Page Name	P06_BCM59121#2
Engineer	Chaohua_Chung		
Date:	Tuesday, March 08, 2016	Sheet	49 of 66

32 POE_P[40:43]
32 POE_N[40:43]
32 POE_60W_P[40:43]
32 POE_60W_N[40:43]



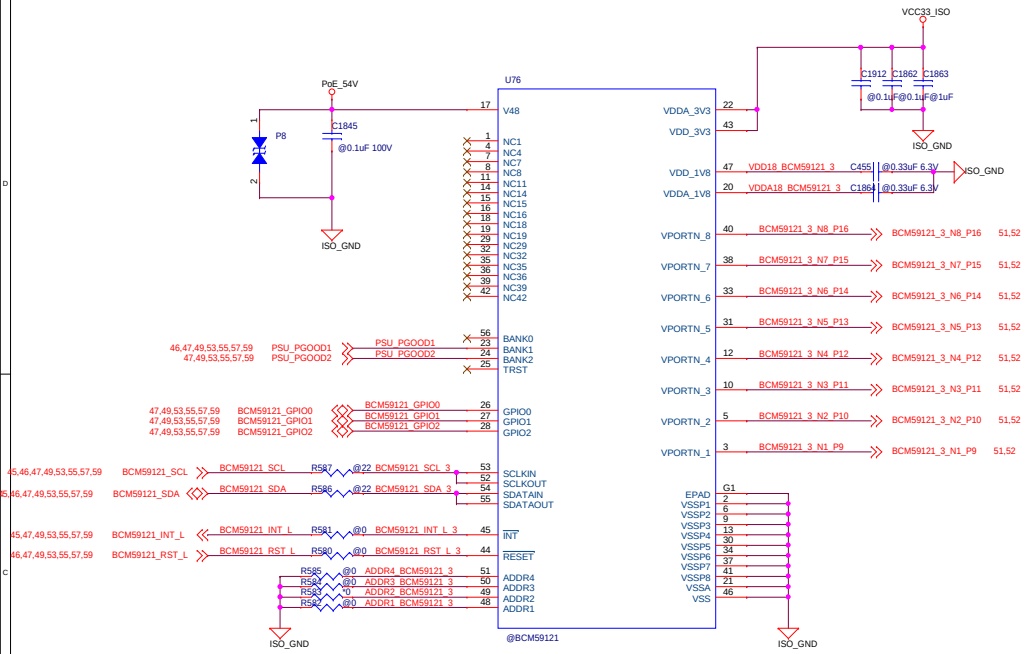


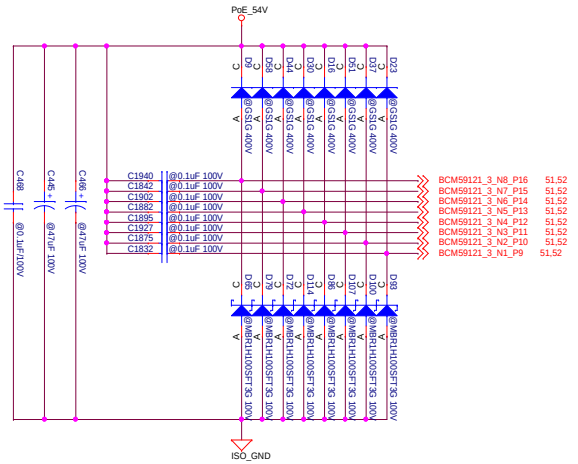
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Model Name: AS4610		Rev: R01
Size: B	Page Name: EMI_Filter #2	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 50 of 66	





Device Address 0b0010

Internal Pull-Up or Pull-Down Resistor of Pins						
SCLKIN, SCLKOUT	–	R_{UP}	90	140	–	kΩ
SDATAIN, SDATAOUT	–	R_{UP}	90	140	–	kΩ
nINT	–	R_{UP}	90	140	–	kΩ
ADDR1, ADDR0, ADDR2, ADDR3, nRESET	–	R_{UP}	30	50	–	kΩ
Bank 0, Bank 1, Bank 2	–	R_{DOWN}	30	50	–	kΩ

HNLOGY

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Model Name: AS4610		Rev: R01
Size: C	Page Name: BCM59121#3	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 51 of 66	

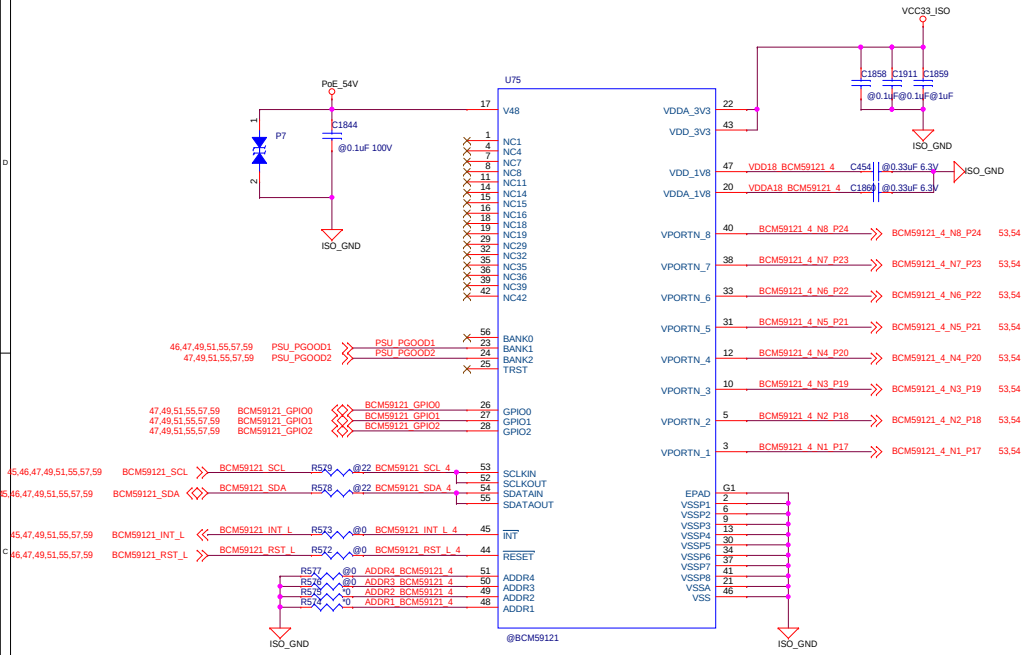


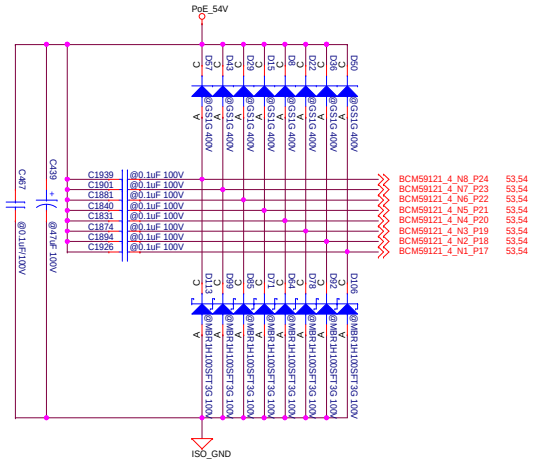
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Model Name AS4610		Rev R01
Size B	Page Name EMI_Filter #3	Engineer Chaohua_Chung
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Device Address 0b0011

Internal Pull-Up or Pull-Down Resistor of Pins						
SCLKIN, SCLKOUT	–	R_{UP}	90	140	–	kΩ
SDATAIN, SDATAOUT	–	R_{UP}	90	140	–	kΩ
nINT	–	R_{UP}	90	140	–	kΩ
ADDR1, ADDR0, ADDR2, ADDR3, nRESET	–	R_{UP}	30	50	–	kΩ
Bank 0, Bank 1, Bank 2	–	R_{DOWN}	30	50	–	kΩ

PRELIMINARY

FMA-HW01008-01 R01

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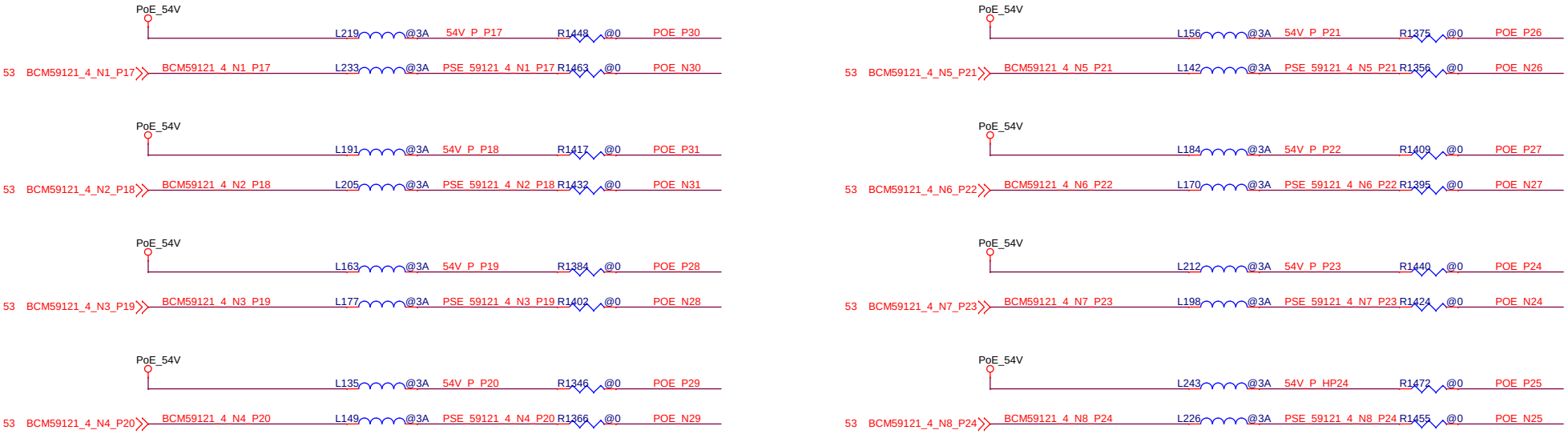
Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	BCM59121#4	Chaohua_Chung

Date: Tuesday, March 08, 2016 Sheet 53 of 66

30 POE_P[24:31]

30 POE_N[24:31]



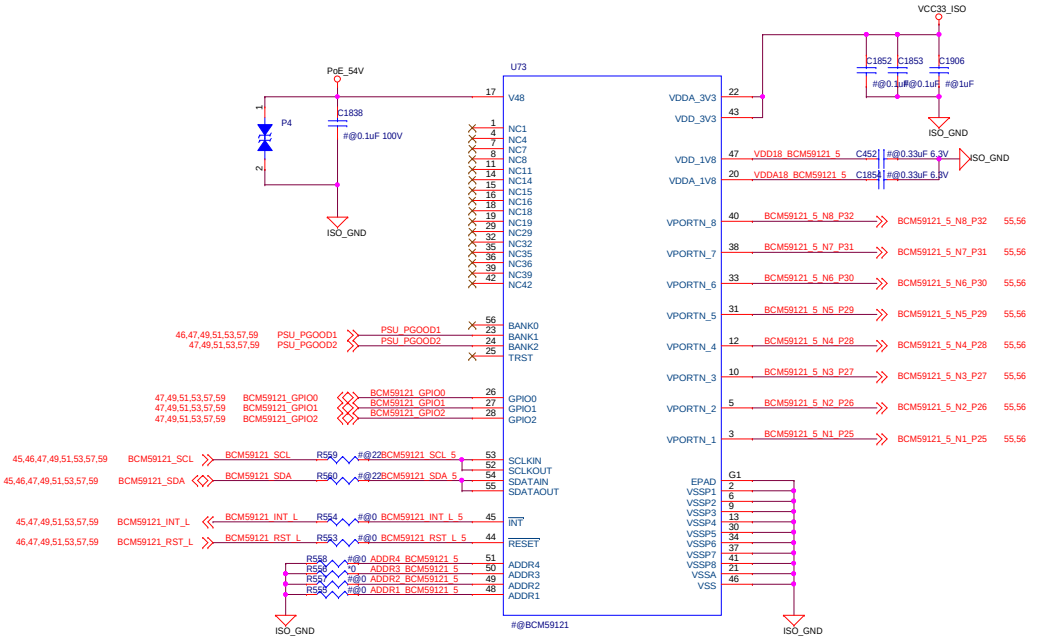
FMA-HW01008-01 R01

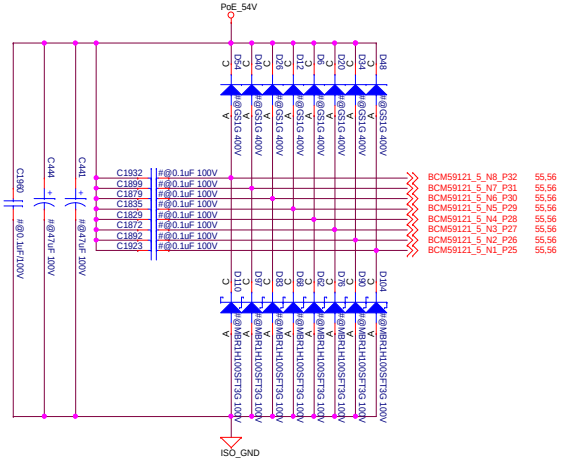
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Model Name: AS4610		Rev: R01
Size: B	Page Name: EMI_Filter #4	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 54 of 66	





Device Address 0b0100

Internal Pull-Up or Pull-Down Resistor of Pins						
SCLKIN, SCLKOUT	–	R_{UP}	90	140	–	kΩ
SDATAIN, SDATAOUT	–	R_{UP}	90	140	–	kΩ
nINT	–	R_{UP}	90	140	–	kΩ
ADDR1, ADDR0, ADDR2, ADDR3, nRESET	–	R_{UP}	30	50	–	kΩ
Bank 0, Bank 1, Bank 2	–	R_{DOWN}	30	50	–	kΩ

FMA-HW01008-01 R01

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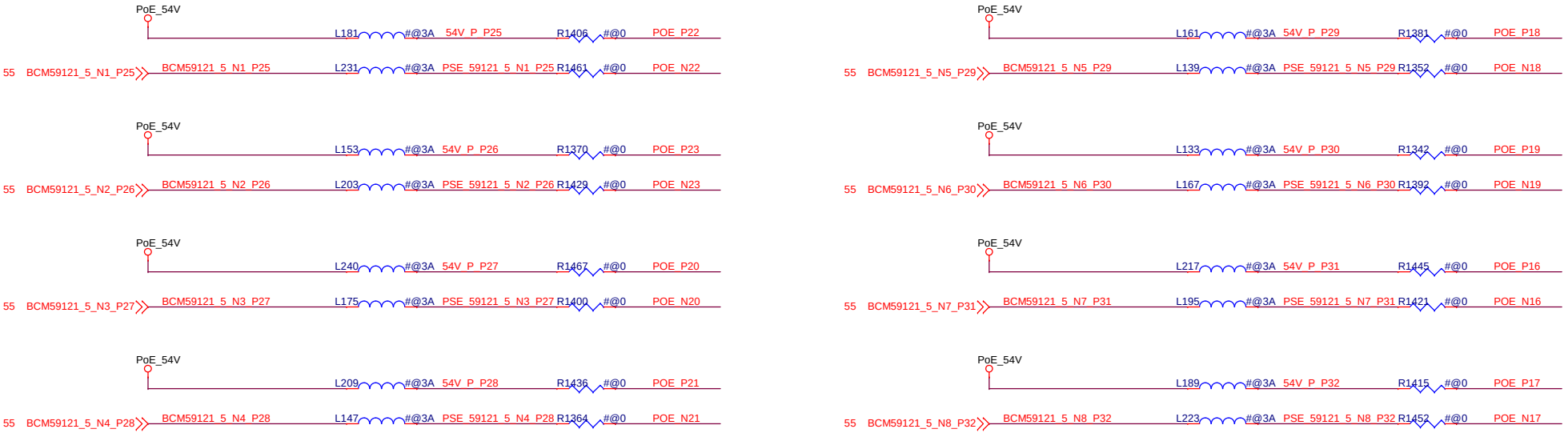
Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	BCM59121#5	Chaohua_Chung

Date: Tuesday, March 08, 2016 Sheet 55 of 66

29 POE_P[16:23]

29 POE_N[16:23]



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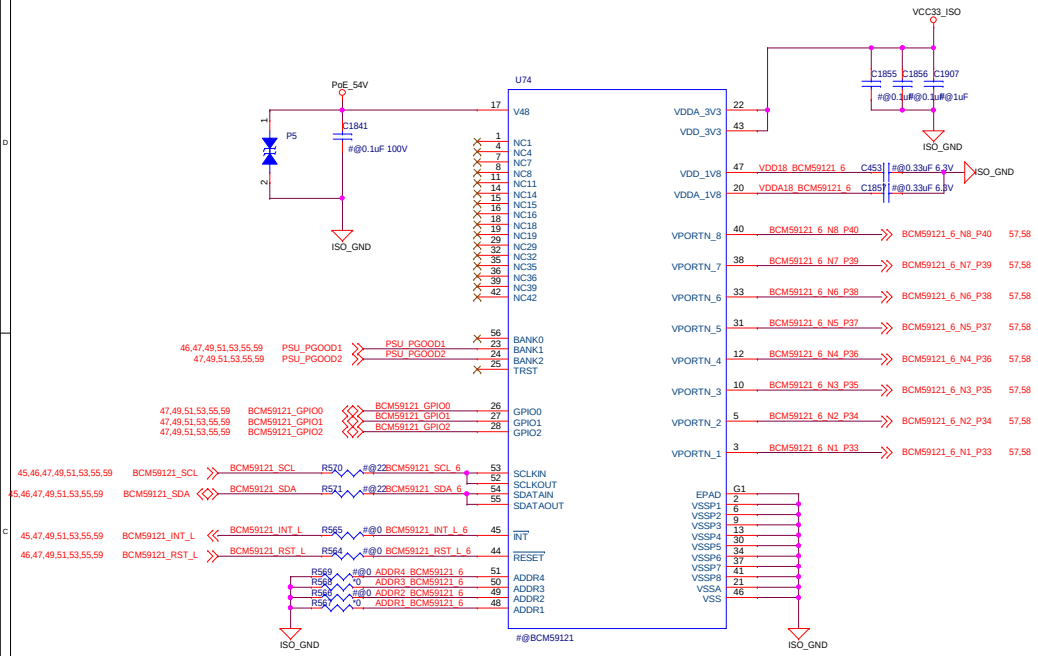
Accton

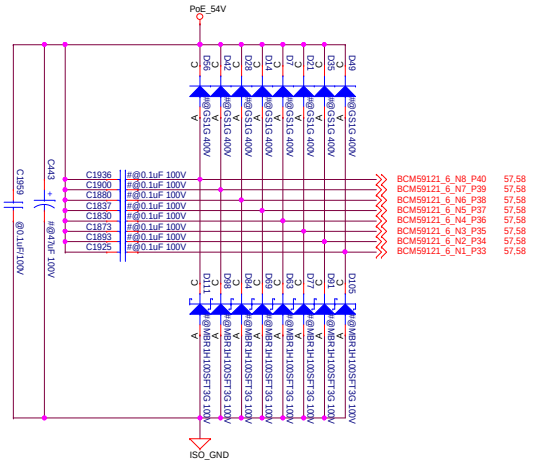
Making Partnership Work

Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
B	EMI_Filter #5	Chaohua_Chung

Date: Tuesday, March 08, 2016 Sheet 56 of 66





Device Address 0b0101

Internal Pull-Up or Pull-Down Resistor of Pins						
SCLKIN, SCLKOUT	–	R_{UP}	90	140	–	kΩ
SDATAIN, SDATAOUT	–	R_{UP}	90	140	–	kΩ
nINT	–	R_{UP}	90	140	–	kΩ
ADDR1, ADDR0, ADDR2, ADDR3, nRESET	–	R_{UP}	30	50	–	kΩ
Bank 0, Bank 1, Bank 2	–	R_{DOWN}	30	50	–	kΩ

PRELIMINARY

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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	BCM59121#6	Chaohua_Chung

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28 POE_P[8:15]

28 POE_N[8:15]





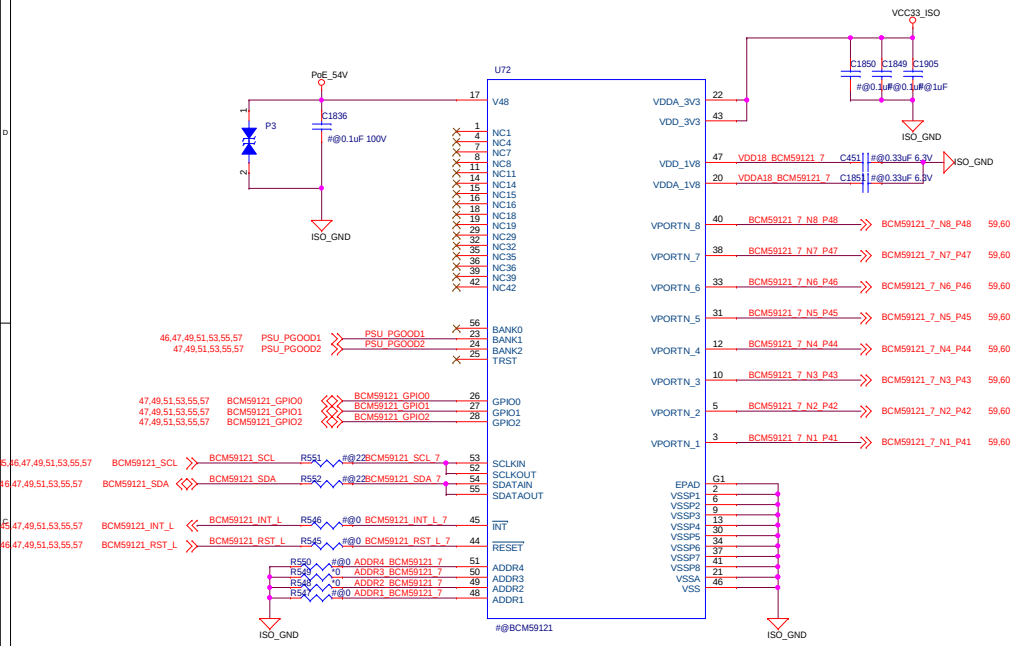
FMA-HW01008-01 R01

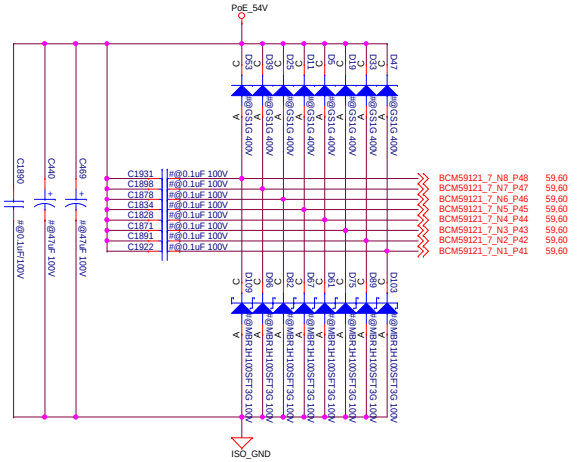
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Model Name: AS4610		Rev: R01
Size: B	Page Name: EMI_Filter #6	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 58 of 66	





Device Address 0b0110

Internal Pull-Up or Pull-Down Resistor of Pins						
SCLKIN, SCLKOUT	–	R_{UP}	90	140	–	kΩ
SDATAIN, SDATAOUT	–	R_{UP}	90	140	–	kΩ
nINT	–	R_{UP}	90	140	–	kΩ
ADDR1, ADDR0, ADDR2, ADDR3, nRESET	–	R_{UP}	30	50	–	kΩ
Bank 0, Bank 1, Bank 2	–	R_{DOWN}	30	50	–	kΩ

PRELIMINARY

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Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	BCM59121#7	Chaohua_Chung

Date: Tuesday, March 08, 2016 Sheet 59 of 66

27 POE_P[0:7]

27 POE_N[0:7]





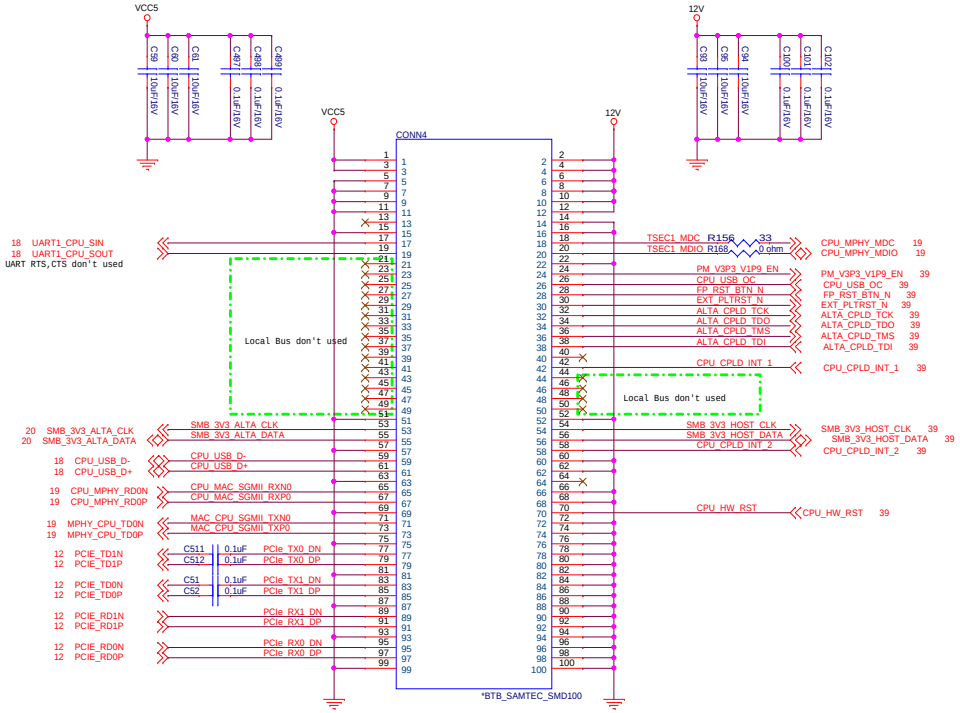
FMA-HW01008-01 R01

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Model Name: AS4610		Rev: R01
Size: B	Page Name: EMI_Filter #7	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 60 of 66	

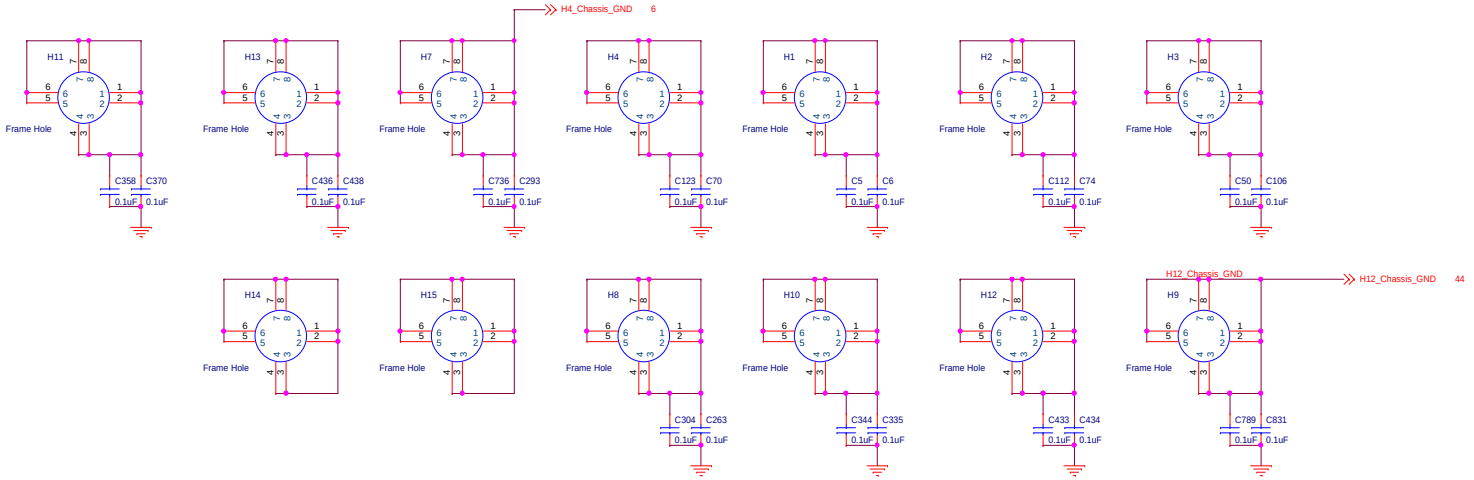


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Model Name: AS4610		Rev: R01
Size: C	Page Name: Ext_Board_Connecter	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 61 of 66	



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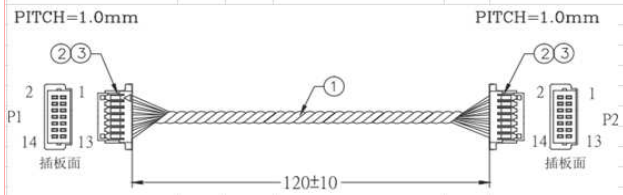
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Model Name: AS4610		Rev: R01
Size: C	Page Name: Frame Hole	Engineer: Chaohua_Chung
Date: Tuesday, March 08, 2016	Sheet 62 of 66	

Mainboard-P1			
CPLD_Reserved_1	1	2	CPLD_Reserved_3
CPLD_Reserved_2	3	4	CPLD_Reserved_4
CPLD_LED_RESET	5	6	CPLD_LED_RCLK
Push_bottom_Reset	7	8	CPLD_LED_CLK
Register_Enable	9	10	CPLD_LED_DATA
VCC33	11	12	GND
VCC33	13	14	GND

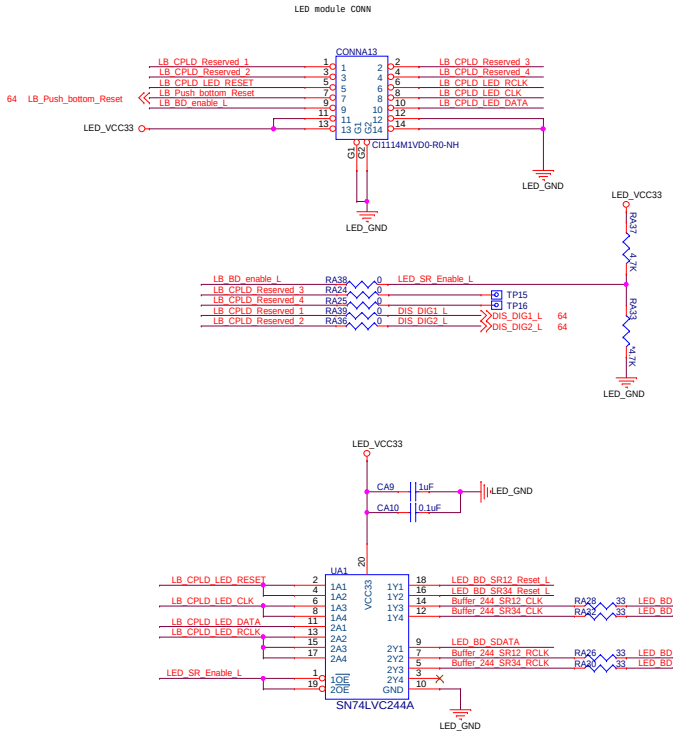
Module-P2			
CPLD_Reserved_1	1	2	CPLD_Reserved_3
CPLD_Reserved_2	3	4	CPLD_Reserved_4
CPLD_LED_RESET	5	6	CPLD_LED_RCLK
Push_bottom_Reset	7	8	CPLD_LED_CLK
Register_Enable	9	10	CPLD_LED_DATA
VCC33	11	12	GND
VCC33	13	14	GND



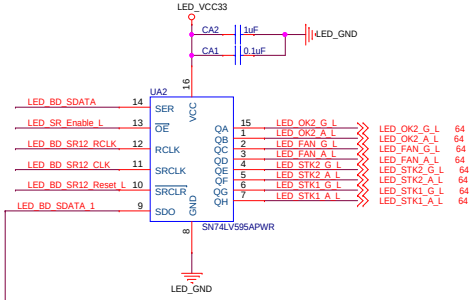
WIRE LIST

P1	P2	
1	1	RED
2	2	BLACK
3	3	BLACK
4	4	BLACK
5	5	BLACK
6	6	BLACK
7	7	BLACK
8	8	BLACK
9	9	BLACK
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13	13	BLACK
14	14	BLACK

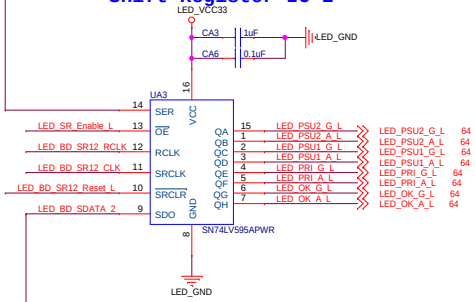
LED board CONN



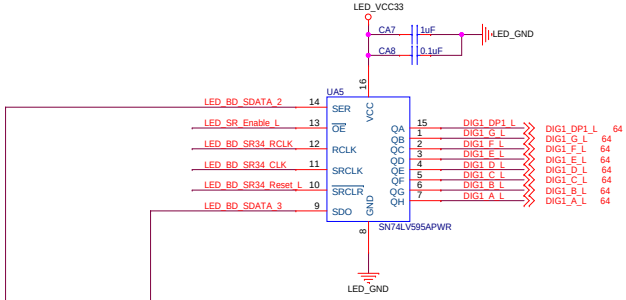
Shift Register IC-1



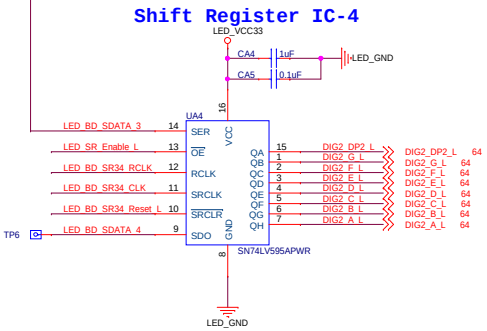
Shift Register IC-2



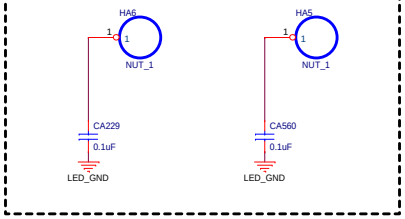
Shift Register IC-3



Shift Register IC-4



LED BOARD use



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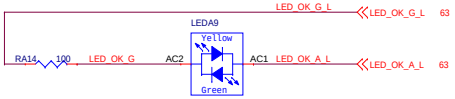
Size	Page Name	Engineer
C	CONN_PUSH BOTTOM	Chaohua_Chung

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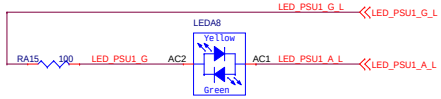
OK LED

Green: Systemp Diag & OS OK



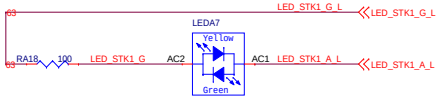
PSU1 LED

Green: PSU OK
Amber: PSU Fail



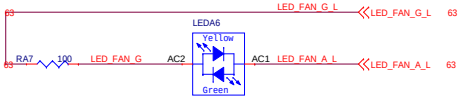
STK1 LED

Green: Stacking ports in stacking mode
Off: Uplink ports in standalone mode or No Link



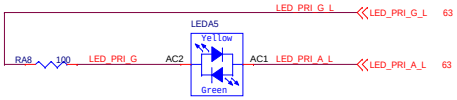
FAN LED

Green: FAN OK
Amber: FAN Fail



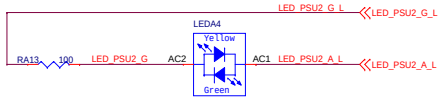
PRI LED

Green : Primary unit
Amber: Secondary unit



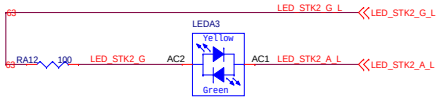
PSU2 LED

Green: PSU OK
Amber: PSU Fail



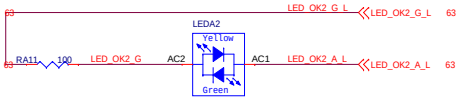
STK2 LED

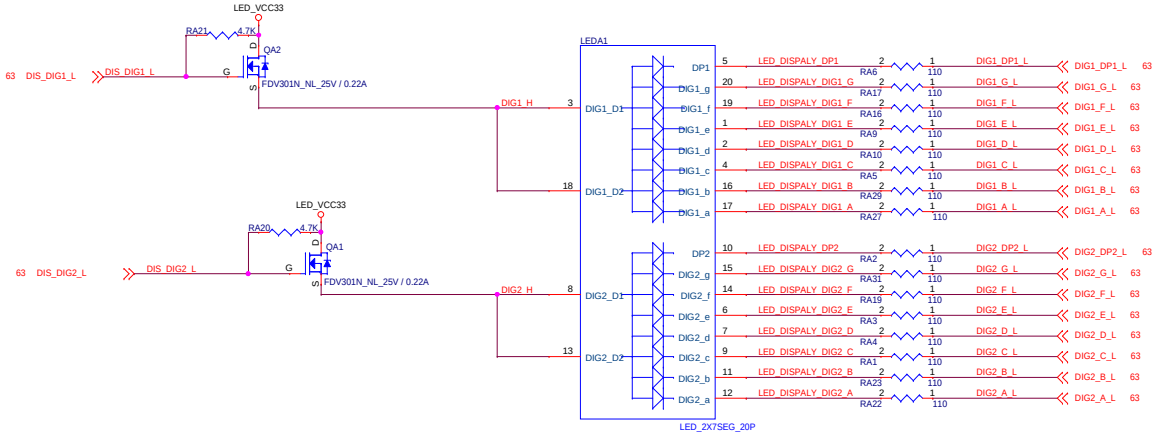
Green: Stacking ports in stacking mode
Off: Uplink ports in standalone mode or No Link

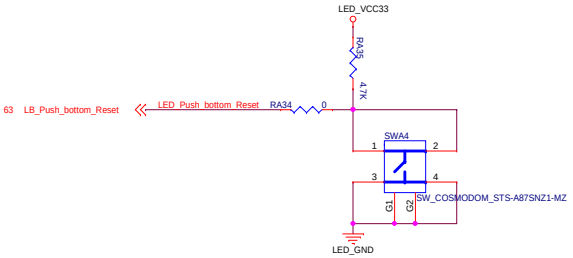


OK2 LED

Green: External CPU Diag & OS OK
Green blinking: External CPU Diag & OS in progress
Amber: External CPU Diag & OS Fail







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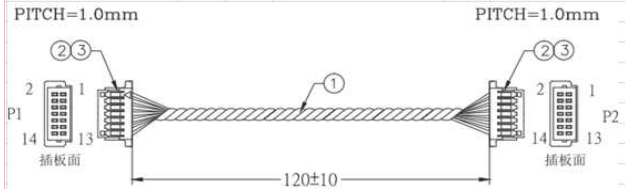
Model Name	Rev
AS4610	R01

Size	Page Name	Engineer
C	LED Dispaly & SYSTEM LED	Chaohua_Chung

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Mainboard-P1			
CPLD_Reserved_1	1	2	CPLD_Reserved_3
CPLD_Reserved_2	3	4	CPLD_Reserved_4
CPLD_LED_RESET	5	6	CPLD_LED_RCLK
Push_bottom_Reset	7	8	CPLD_LED_CLK
Register_Enable	9	10	CPLD_LED_DATA
VCC33	11	12	GND
VCC33	13	14	GND

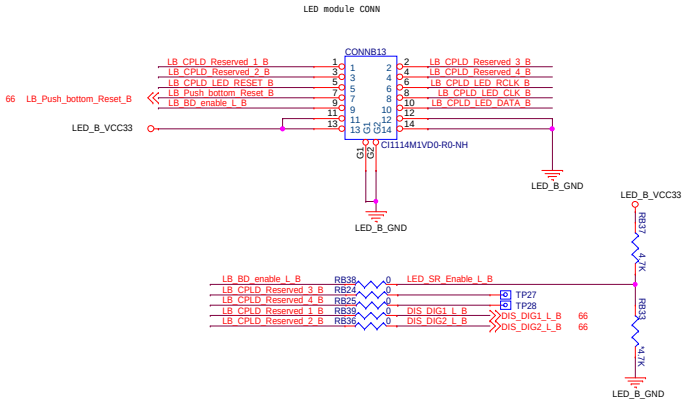
Module-P2			
CPLD_Reserved_1	1	2	CPLD_Reserved_3
CPLD_Reserved_2	3	4	CPLD_Reserved_4
CPLD_LED_RESET	5	6	CPLD_LED_RCLK
Push_bottom_Reset	7	8	CPLD_LED_CLK
Register_Enable	9	10	CPLD_LED_DATA
VCC33	11	12	GND
VCC33	13	14	GND



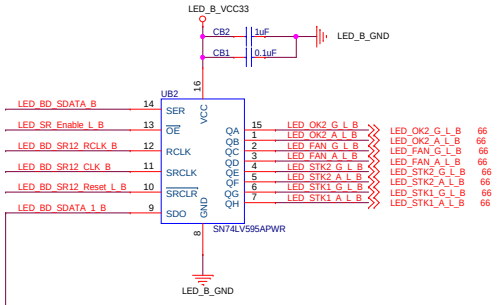
WIRE LIST

P1	P2	
1	1	RED
2	2	BLACK
3	3	BLACK
4	4	BLACK
5	5	BLACK
6	6	BLACK
7	7	BLACK
8	8	BLACK
9	9	BLACK
10	10	BLACK
11	11	BLACK
12	12	BLACK
13	13	BLACK
14	14	BLACK

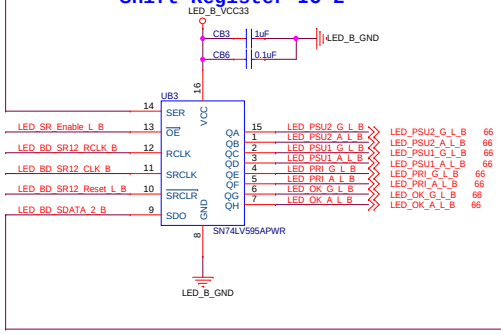
LED board CONN



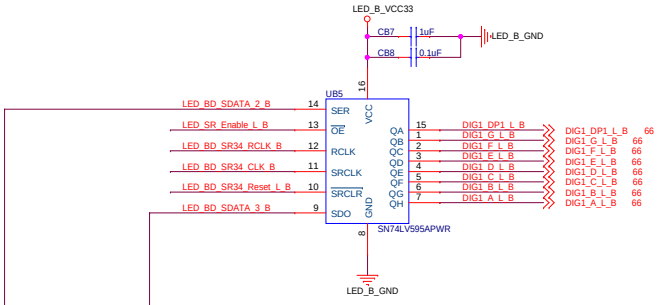
Shift Register IC-1



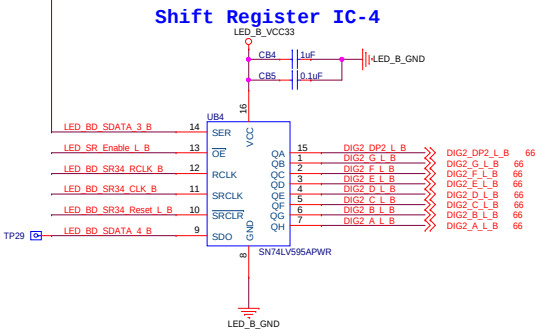
Shift Register IC-2

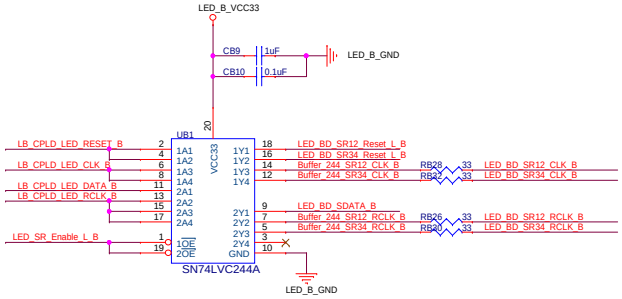


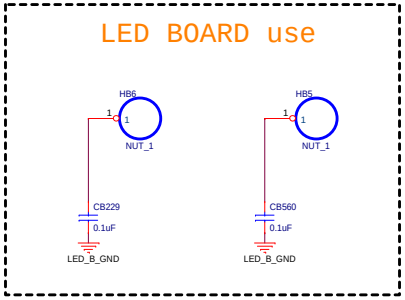
Shift Register IC-3



Shift Register IC-4







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Model Name	Rev
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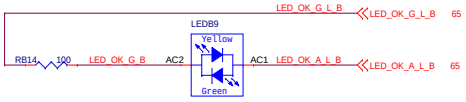
Size	Page Name	Engineer
C	CONN_PUSH BOTTOM	Chaohua_Chung

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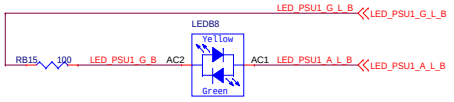
OK LED

Green: Systemp Diag & OS OK



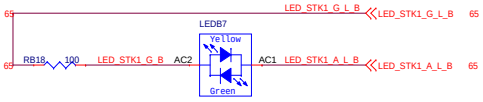
PSU1 LED

Green: PSU OK
Amber: PSU Fail



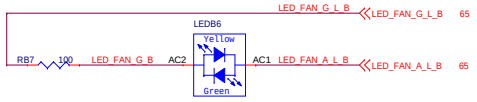
STK1 LED

Green: Stacking ports in stacking mode
Off: Uplink ports in standalone mode or No Link



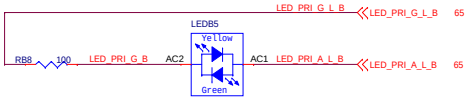
FAN LED

Green: FAN OK
Amber: FAN Fail



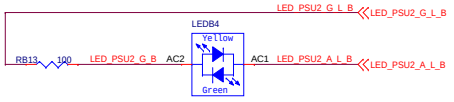
PRI LED

Green : Primary unit
Amber: Secondary unit



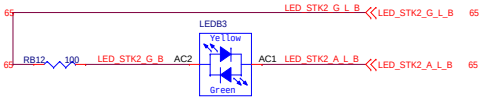
PSU2 LED

Green: PSU OK
Amber: PSU Fail



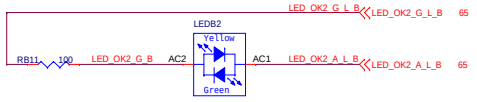
STK2 LED

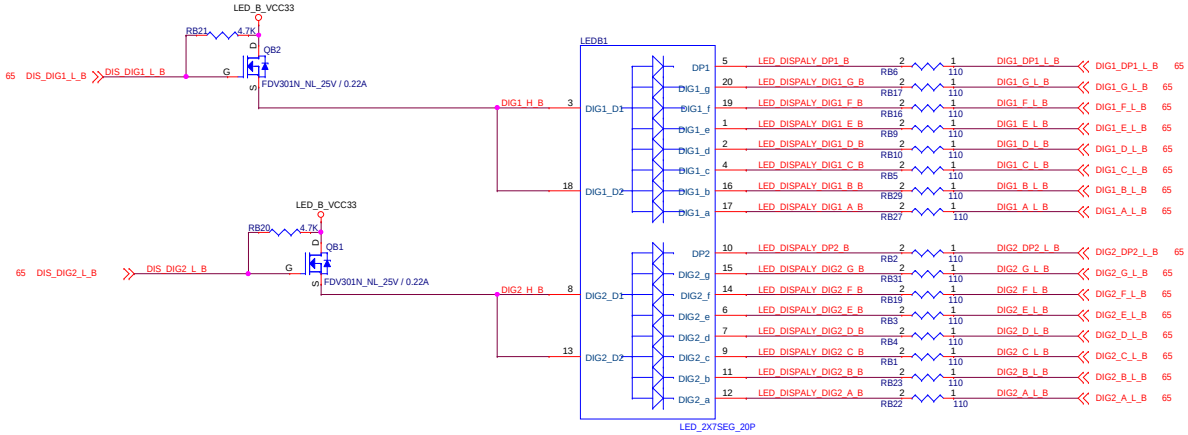
Green: Stacking ports in stacking mode
Off: Uplink ports in standalone mode or No Link

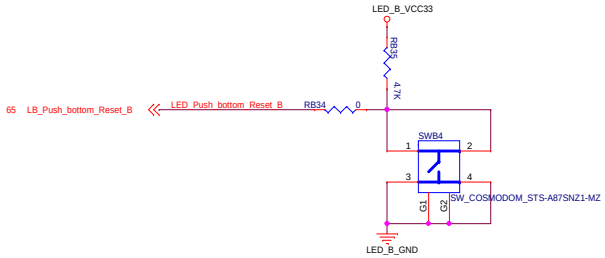


OK2 LED

Green: External CPU Diag & OS OK
Green blinking: External CPU Diag & OS in progress
Amber: External CPU Diag & OS Fail







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Size: C	Page Name: LED Dispaly & SYSTEM LED	Engineer: Chaohua_Chung
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