

Accton_4X4 Radio

01_Title_Page
02_System Block Diagram
03_5G Beeliner_Block Diagram
04_2G Beeliner_Block Diagram
05_System Power Tree
06_5G & 2G & Power Tree
07_IPQ_8068 DC to DC Power
08_IPQ8068 - Clocks, Test
09_IPQ8068 - DDR3, GPIOs
10_IPQ8068 - Power Gnd
11_IPQ8068-USB,PCIE,SGMII,RGMII
12_DDR3 MEMORY
13_GPIO muxing and Bootstrap
14_NAND FLASH & SPI Flash & TPM
15_Level Translators
16_LED&JTAG&URAT&TMP
17_PHY1_SGMII AR8033
18_PHY2_SGMII AR8033
19_Bridge rectifier
20_TI TPS23751_POE
21_CC2540_Bluetooth_RF
22_2G_BEELINER_GPIO,UART,EEPROM
23_2G_BEELINER_Clock&PCIE
24_2G_BEELINER_Power,Regulator
25_2G_BEELINER_TX&RX Control
26_2G_BEELINER_FEM_Chain_0
27_2G_BEELINER_FEM_Chain_1

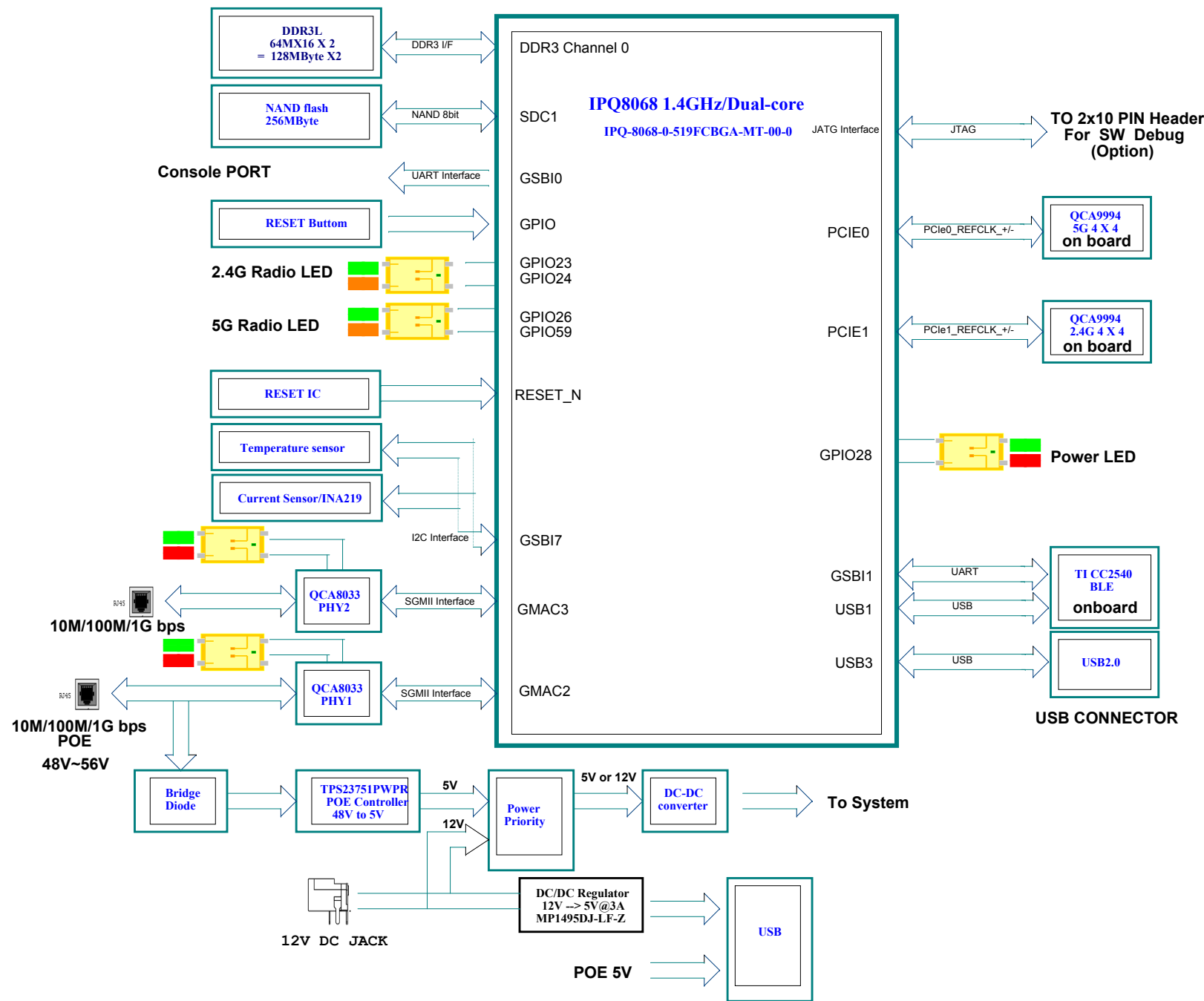
28_2G_BEELINER_FEM_Chain_2
29_2G_BEELINER_FEM_Chain_3
30_5G_BEELINER_GPIO_UART_EEPROM
31_5G_BEELINER_Clock & PCIE
32_5G_BEELINER_Power_Regulator
33_5G_BEELINER_TX&RX Control
34_5G_BEELINER_FEM_Chain_0
35_5G_BEELINER_FEM_Chain_1
36_5G_BEELINER_FEM_Chain_2
37_5G_BEELINER_FEM_Chain_3
38_Revision_History

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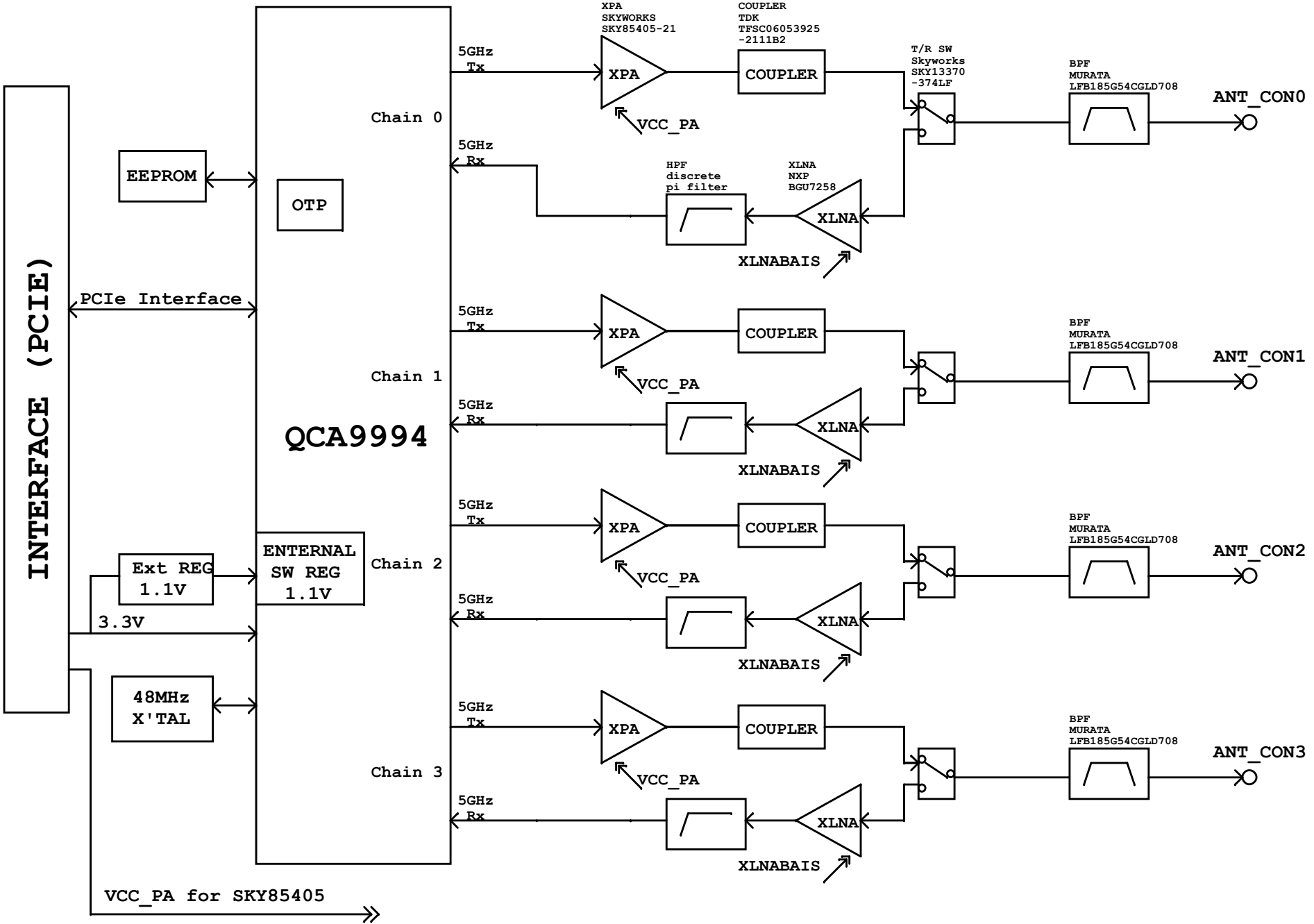


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Model Name		Rev
EAP1024A-FLF-ZZ		R01
Size	Page Name	Engineer
C	01_Title_Page	Yin_Lee
Date: Thursday, December 29, 2016 Sheet 1 of 42		



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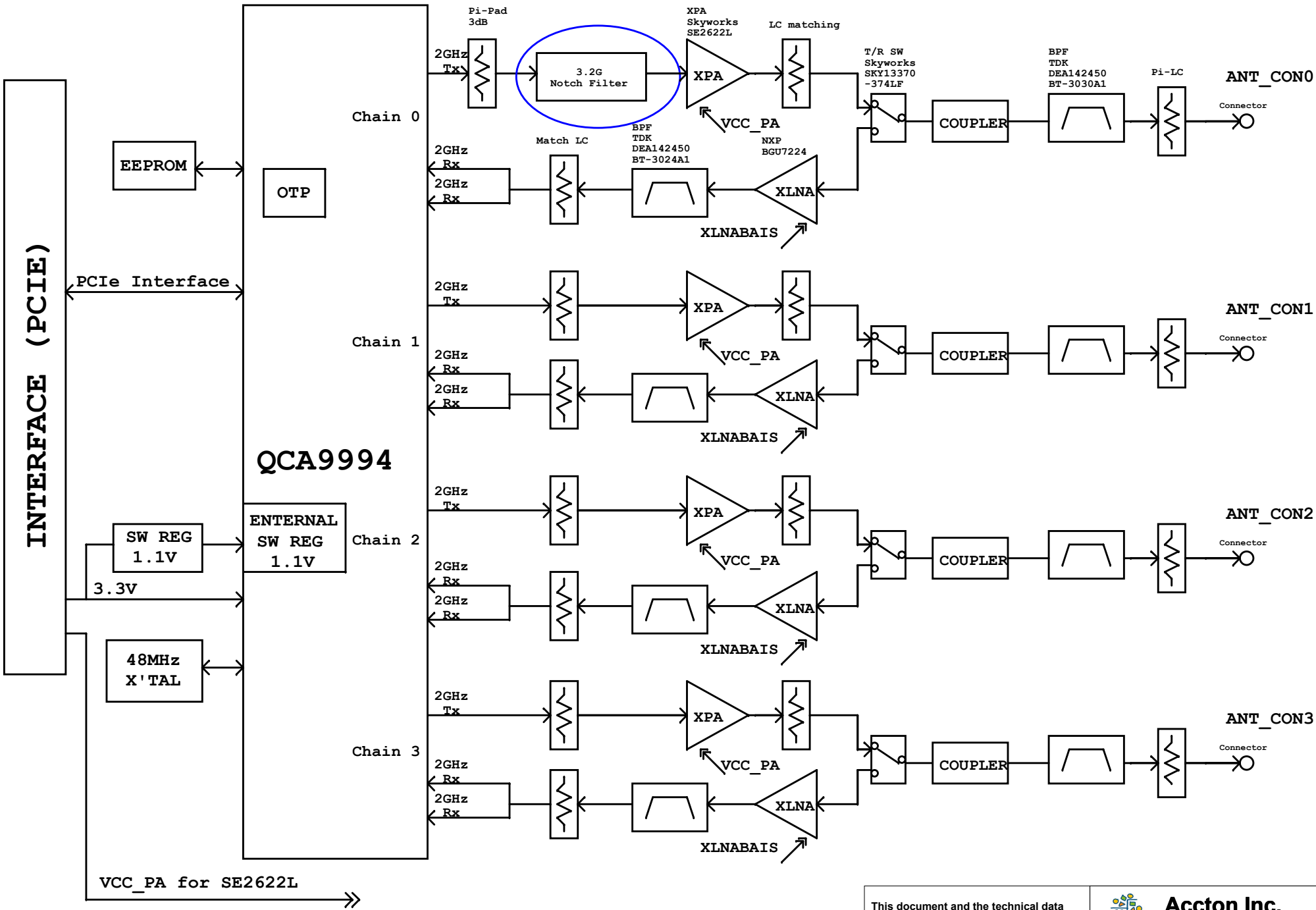
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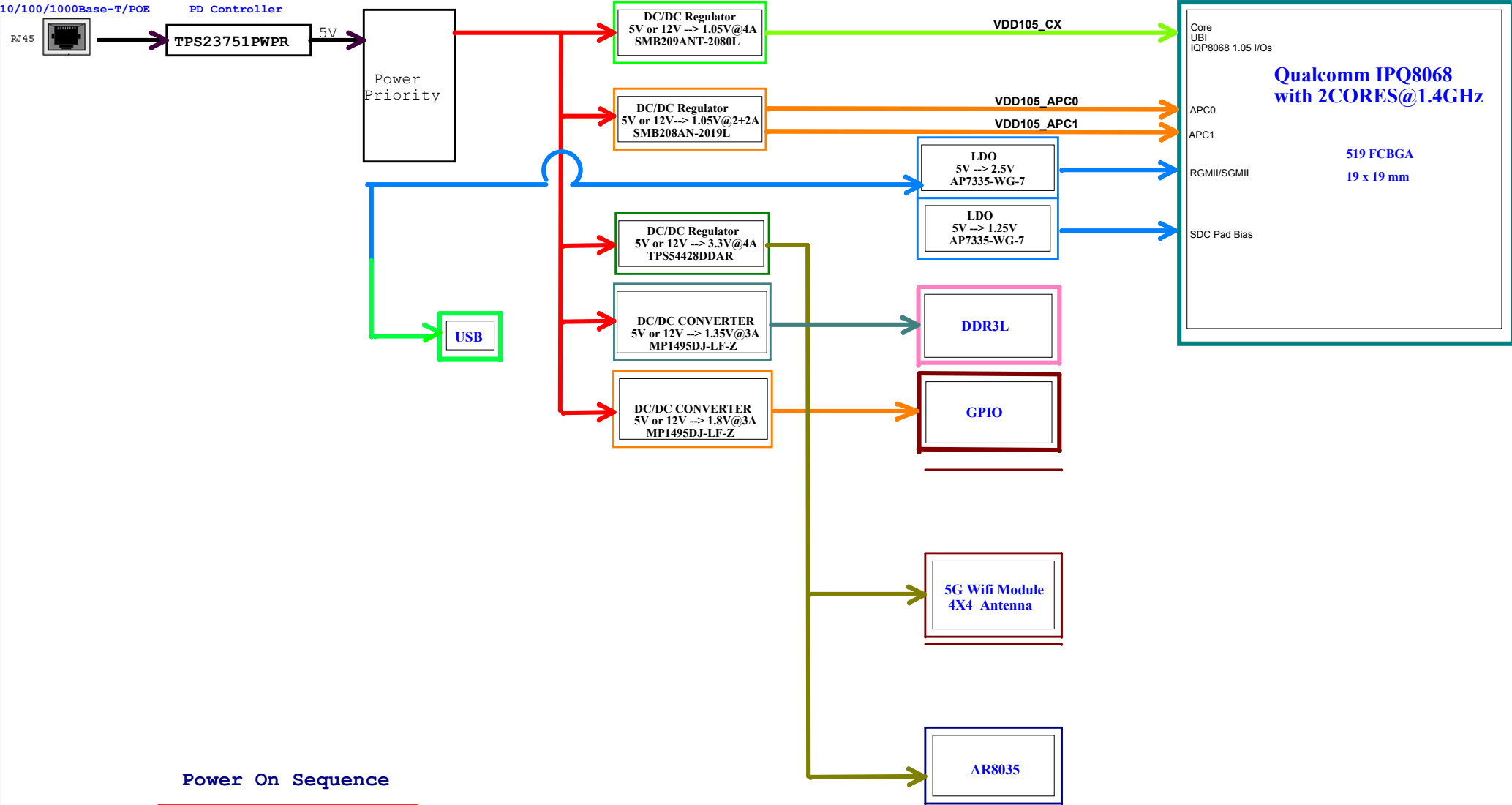
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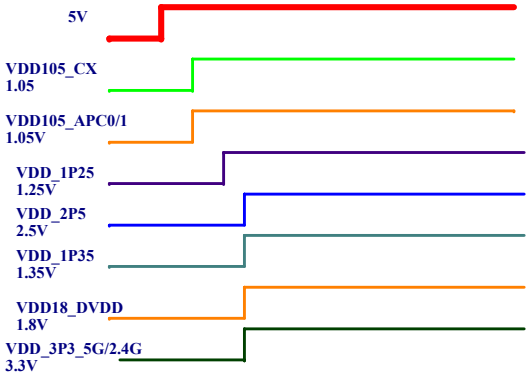
Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	03_5G Beeline Block Diagram	Yin_Lee
Date:	Thursday, December 29, 2016	Sheet 3 of 38



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Power On Sequence



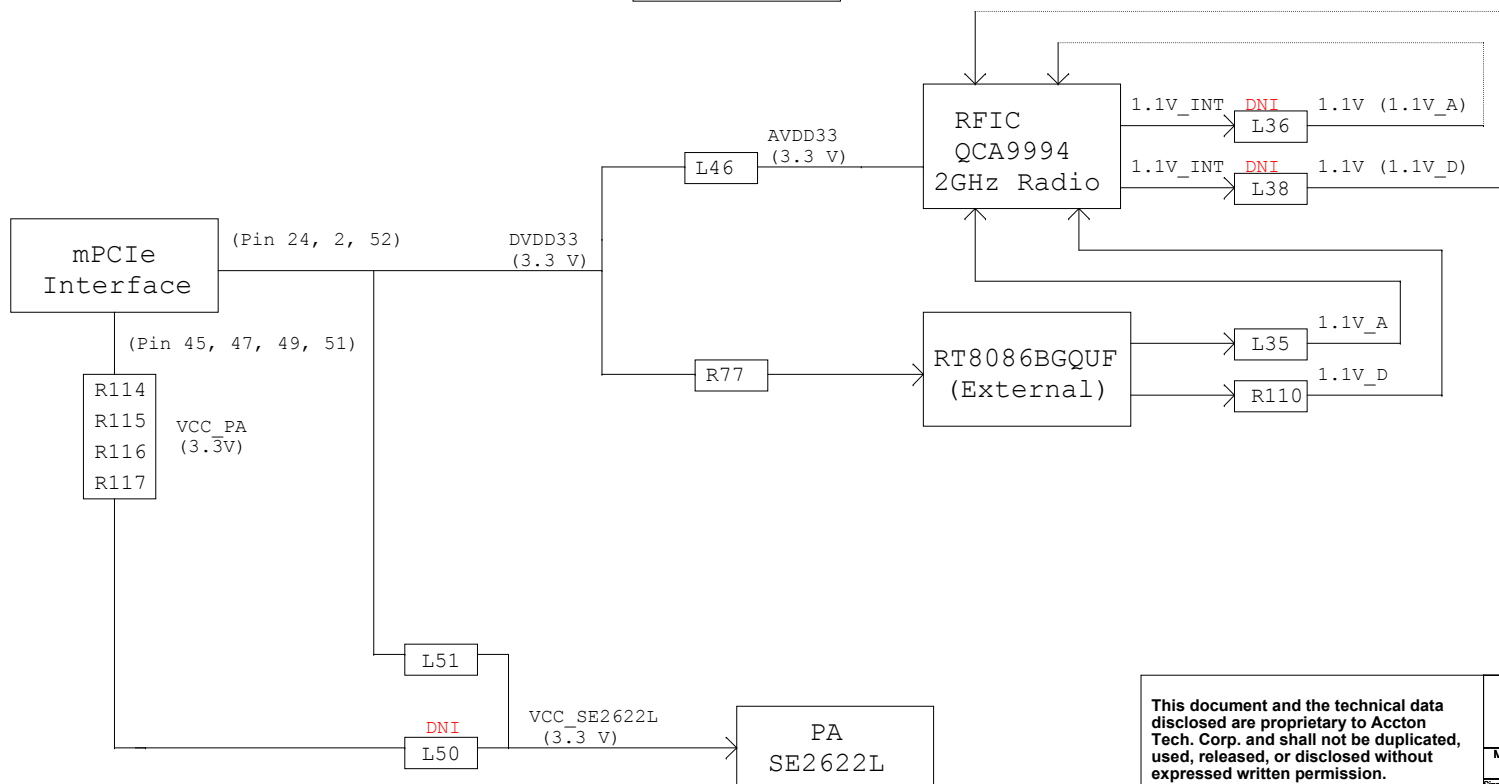
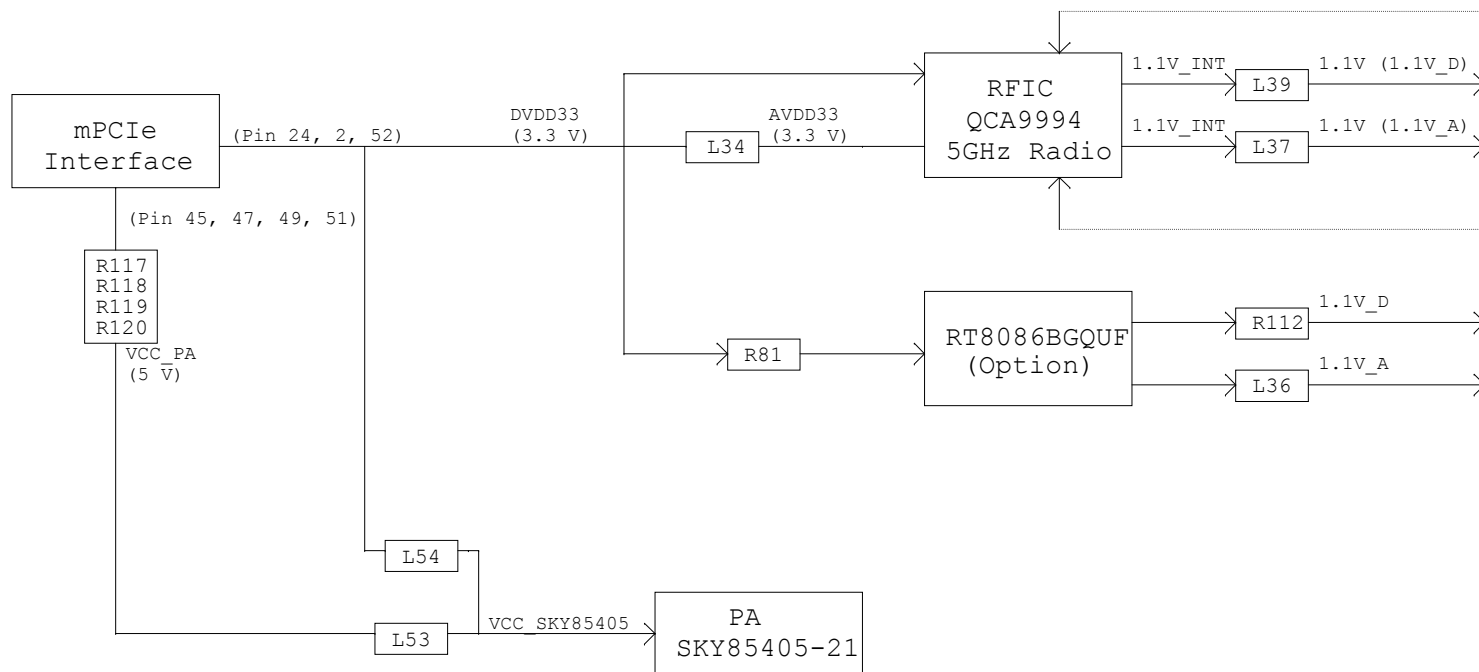
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Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	05_System Power_Tree	Yin_Lee
Date:	Thursday, December 29, 2016	Sheet 5 of 38



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Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	06_5G & 2G & . Power Tree	Yin_Lee
Date:	Thursday, December 20, 2016	Sheet 6 of 38

[illegible]

[illegible]

12V : 0.029A

POE 5V : 0.0536A

Vo = Vref * (1+RA/RB)
= 0.807 * [1+(40.2/32.4)] = 1.8082V

Voltage Range:		
Vin	Vout	Max
1.7V	1.8V	1.802V

[illegible]

The top diagram shows a USB-to-TTL converter circuit. It includes a 3.3V regulator (PMBT3304) connected to a 10K pull-up resistor (R242) and a 30K resistor (R243). The output of the regulator is connected to the TX pin of the USB-to-TTL converter. The TX pin is also connected to a 10K pull-up resistor (R242) and a 30K resistor (R243). The TX pin is also connected to a 10K pull-up resistor (R242) and a 30K resistor (R243).

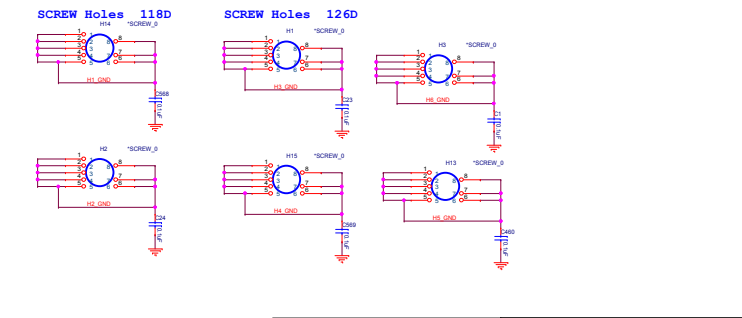
The bottom diagram shows a USB-to-TTL converter circuit. It includes a 5V regulator (PMBT3304) connected to a 10K pull-up resistor (R242) and a 30K resistor (R243). The output of the regulator is connected to the TX pin of the USB-to-TTL converter. The TX pin is also connected to a 10K pull-up resistor (R242) and a 30K resistor (R243). The TX pin is also connected to a 10K pull-up resistor (R242) and a 30K resistor (R243).

[illegible]

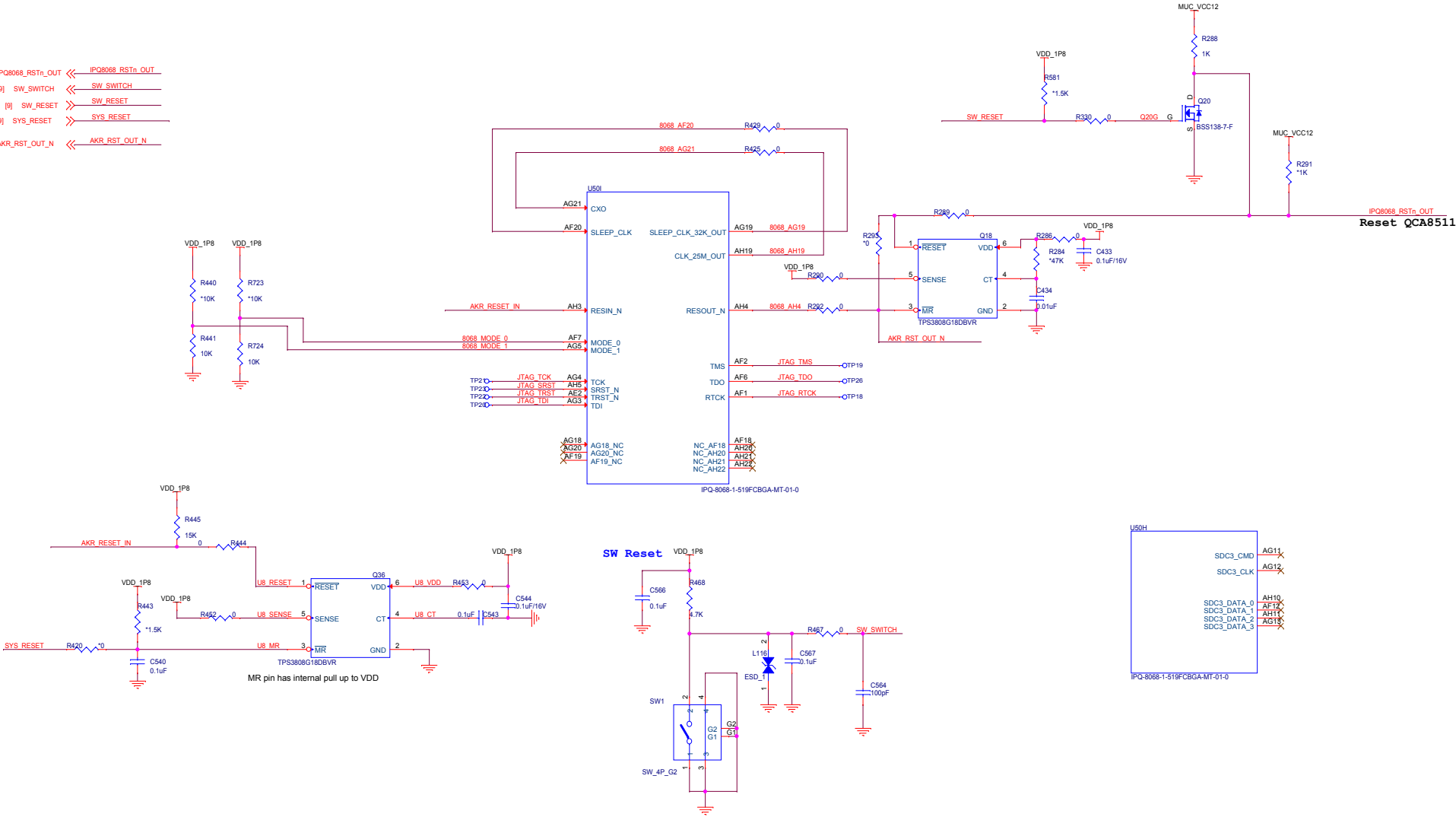
[illegible]

$V_o = V_{ref} * (1 + R_A/R_B)$
 $= 0.8 * [1 + (147K/68K)] = 2.529V$

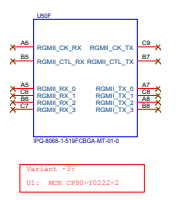
Voltage Range:		
Min	Type	Max
2.3V	2.5V	2.7V



- [16] IPQ8068_RSTn_OUT << IPQ8068_RSTn_OUT
- [9] SW_SWITCH << SW_SWITCH
- [9] SW_RESET << SW_RESET
- [9] SYS_RESET << SYS_RESET
- [14] AKR_RST_OUT_N << AKR_RST_OUT_N



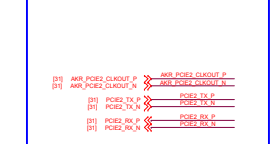
RGMI Interface



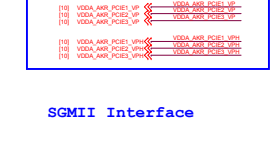
USB POWER



PCIE Interface



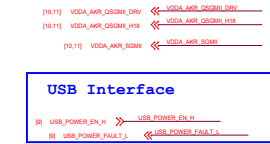
PCIE POWER



SGMII Interface



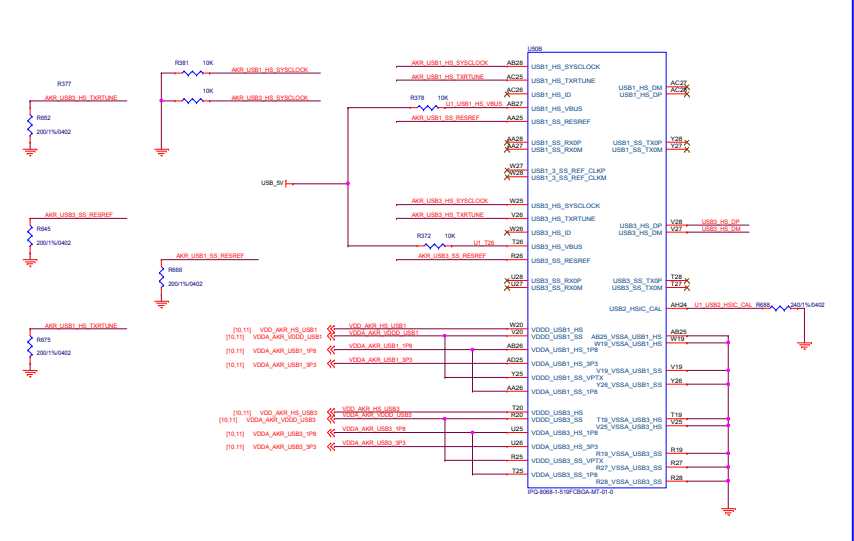
GMAC POWER



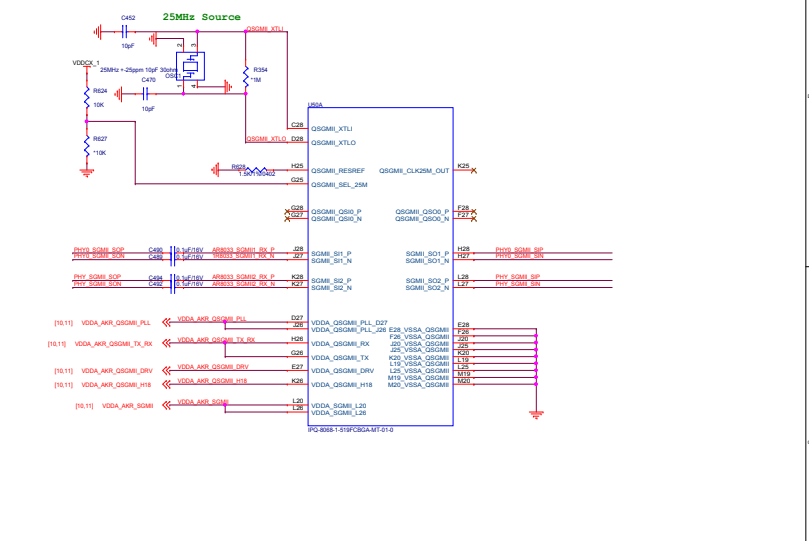
USB Interface



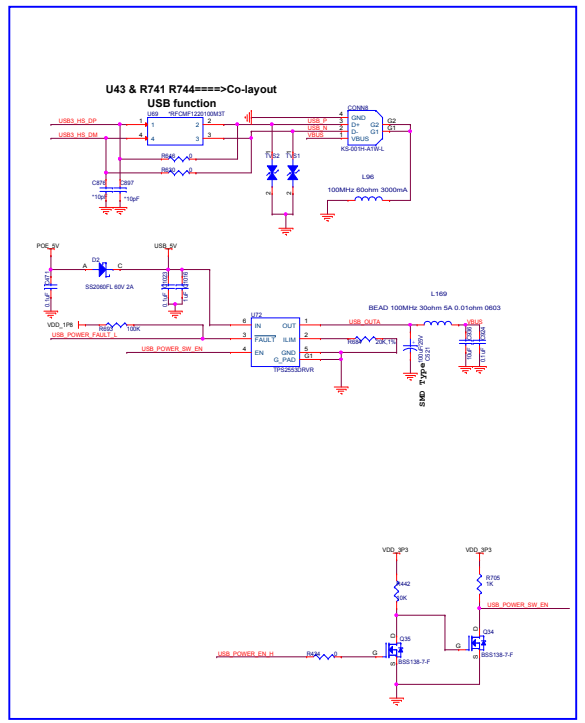
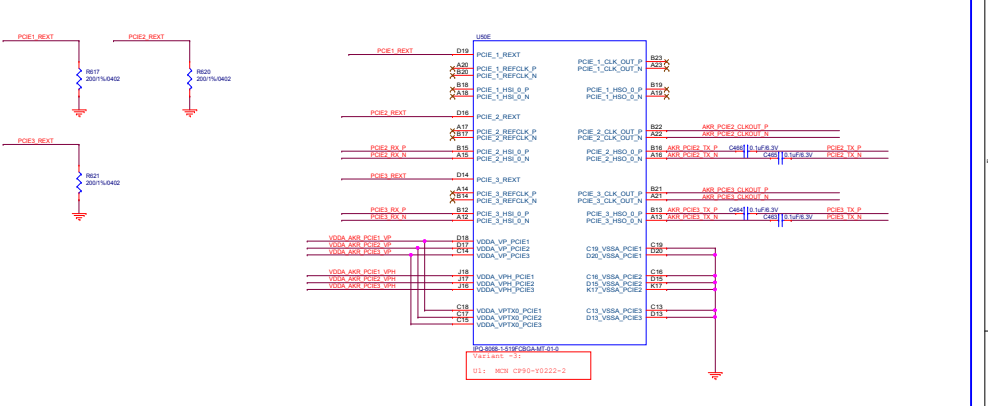
USB Interface



SGMII & QSGMII Interface



PCIE Interface



- [9] AKR_GPIO_3 << AKR_GPIO_3

[9] AKR_GPIO_10 << AKR_GPIO_10

[9] AKR_GPIO_11 << AKR_GPIO_11

[9] AKR_GPIO_51 << AKR_GPIO_51

[9] AKR_GPIO_52 << AKR_GPIO_52

[9] AKR_GPIO_12 << AKR_GPIO_12

[9] AKR_GPIO_13 << AKR_GPIO_13

[9] AKR_GPIO_14 << AKR_GPIO_14

[9] AKR_GPIO_14 << AKR_GPIO_14
- [9] AKR_GPIO_33 << AKR_GPIO_33

[9] AKR_GPIO_63 << AKR_GPIO_63

[9] AKR_GPIO_64 << AKR_GPIO_64

[9] AKR_GPIO_65 << AKR_GPIO_65

[9] AKR_GPIO_32 << AKR_GPIO_32

[9] AKR_GPIO_8 << AKR_GPIO_8

[9] AKR_GPIO_9 << AKR_GPIO_9

[9] AKR_GPIO_63 << AKR_GPIO_63

[9] AKR_GPIO_54 << AKR_GPIO_54

[9] AKR_GPIO_48 << AKR_GPIO_48

[9] AKR_GPIO_49 << AKR_GPIO_49

[9] AKR_GPIO_50 << AKR_GPIO_50
- [18] PHY2_INTn_OUT >> PHY2_INTn_OUT

[17] PHY1_INTn_OUT >> PHY1_INTn_OUT
- [31] PCIE2_WAKE_L >> PCIE2_WAKE_L

[31] PCIE3_CLKREQ_L >> PCIE3_CLKREQ_L

[31] PCIE2_PERST_L >> PCIE2_PERST_L

[23] PCIE3_PERST_L >> PCIE3_PERST_L

[23] PCIE3_WAKE_L >> PCIE3_WAKE_L

[23] PCIE3_CLKREQ_L >> PCIE3_CLKREQ_L
- [15] 1P8_UART_2_TX >> 1P8_UART_2_TX

[15] 1P8_UART_2_RX >> 1P8_UART_2_RX

[15] 1P8_UART_1_TX >> 1P8_UART_1_TX

[15] 1P8_UART_1_RX >> 1P8_UART_1_RX

[15] 1P8_UART_1_CTS >> 1P8_UART_1_CTS

[15] 1P8_UART_1_RTS >> 1P8_UART_1_RTS

[15] 1P8_I2C_1_SDA >> 1P8_I2C_1_SDA

[15] 1P8_I2C_1_SCL >> 1P8_I2C_1_SCL

[15] 1P8_I2C_2_SDA >> 1P8_I2C_2_SDA

[15] 1P8_I2C_2_SCL >> 1P8_I2C_2_SCL

[9] AKR_GPIO_29 >> AKR_GPIO_29

[9] AKR_GPIO_30 >> AKR_GPIO_30

[7] QFPROM_EN >> QFPROM_EN
- [14] BOOT_CONFIG1 >> BOOT_CONFIG1

[14] BOOT_CONFIG2 >> BOOT_CONFIG2

[14] BOOT_CONFIG3 >> BOOT_CONFIG3

[14] BOOT_CONFIG5 >> BOOT_CONFIG5

[14] BOOT_CONFIG6 >> BOOT_CONFIG6
- [14] BOOT_SPL_MOSI << BOOT_SPL_MOSI

[14] BOOT_SPL_MISO << BOOT_SPL_MISO

[14] BOOT_SPL_CS << BOOT_SPL_CS

[14] BOOT_SPL_CLK << BOOT_SPL_CLK

[9] AKR_GPIO_18 >> AKR_GPIO_18

[9] AKR_GPIO_19 >> AKR_GPIO_19

[9] AKR_GPIO_20 >> AKR_GPIO_20

[9] AKR_GPIO_21 >> AKR_GPIO_21

[21] CPU_BLUE_DEBUG_DATA >> CPU_BLUE_DEBUG_DATA

[21] CPU_BLUE_DEBUG_CLK >> CPU_BLUE_DEBUG_CLK

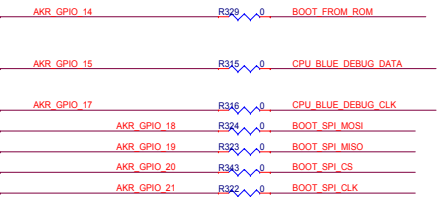
[9] AKR_GPIO_15 >> AKR_GPIO_15

[9] AKR_GPIO_17 >> AKR_GPIO_17

Boot configuration	
BOOT_CONFIG[0]	Setting
BOOT_CONFIG[1]	Low
BOOT_CONFIG[2]	Low
BOOT_CONFIG[3]	High
BOOT_CONFIG[4]	High
BOOT_CONFIG[5]	Low
BOOT_CONFIG[6]	High
BOOT_FROM_ROM	High
WDOG_DISABLE	Low

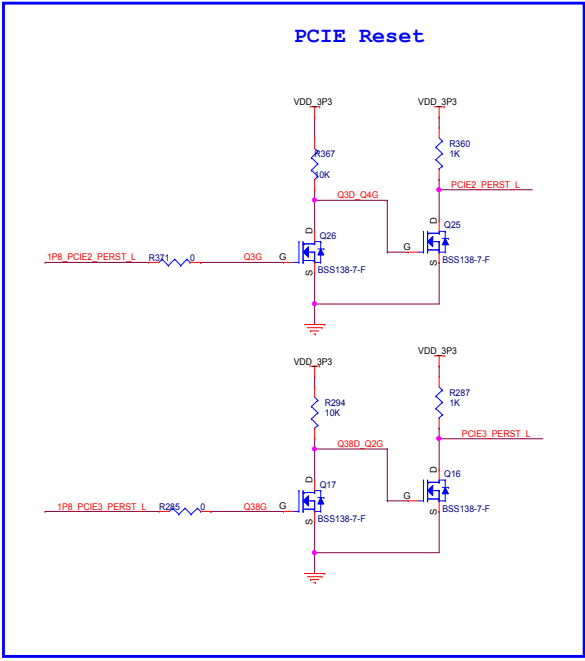
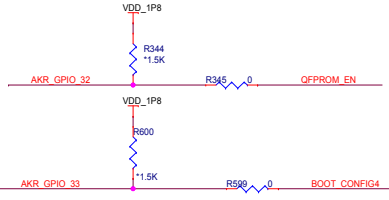
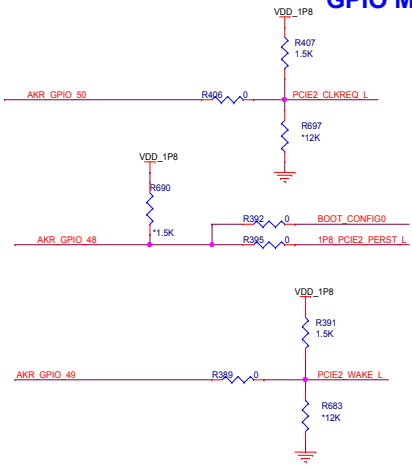
Boot Form NAND

NSS debug interface



SPI Interface

GPIO Muxing and Bootstrap

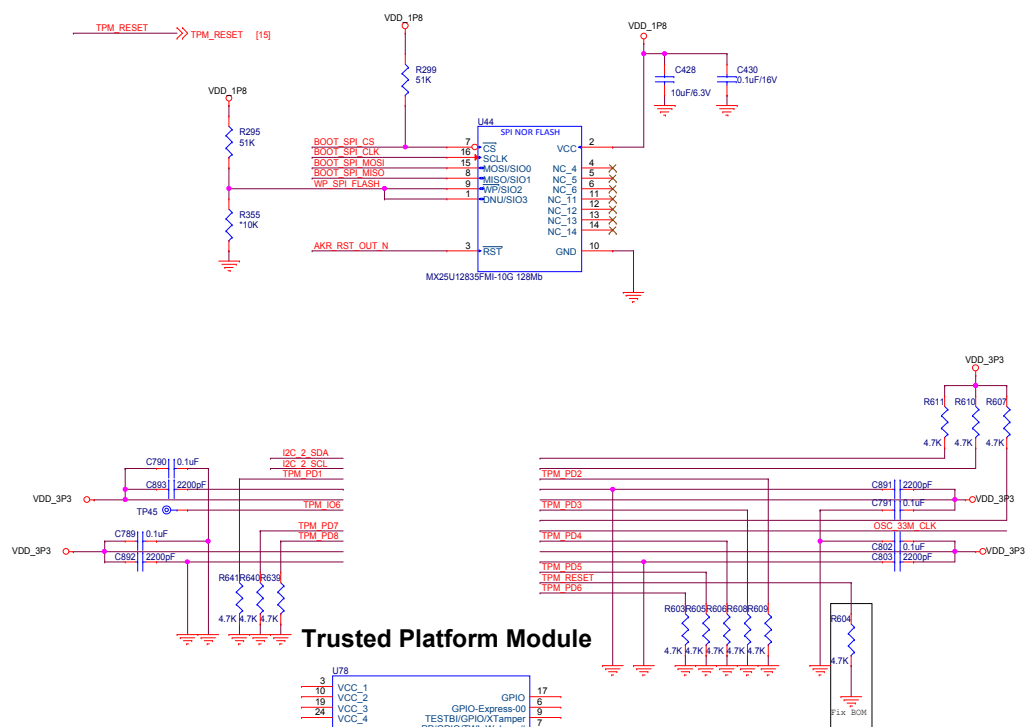
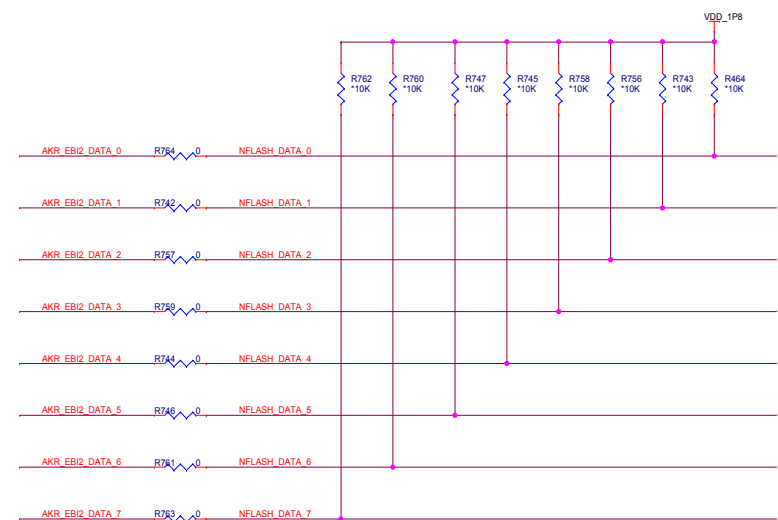
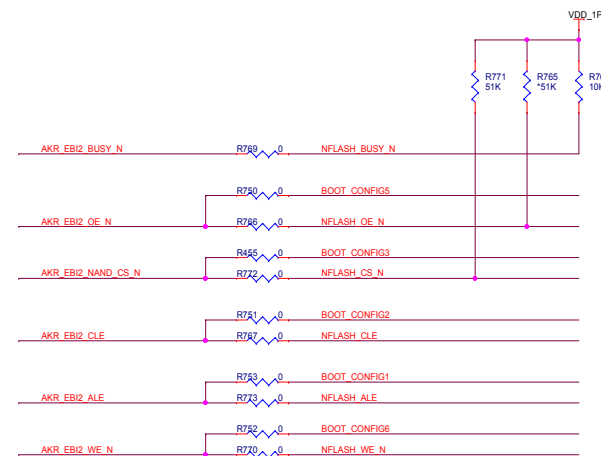
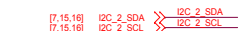


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Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	13_GPIO muxing and Bootstrap	Yin_Lee
Date:	Thursday, December 29, 2016	Sheet 13 of 38

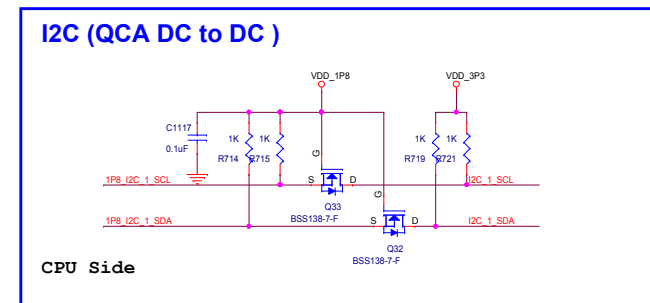
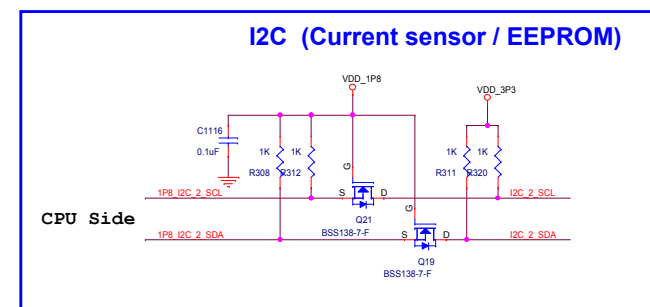
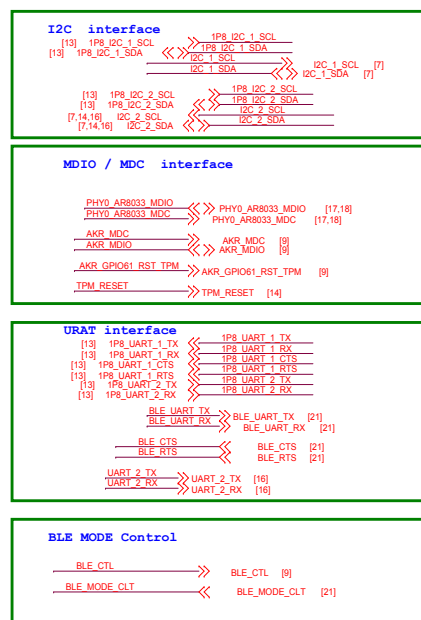
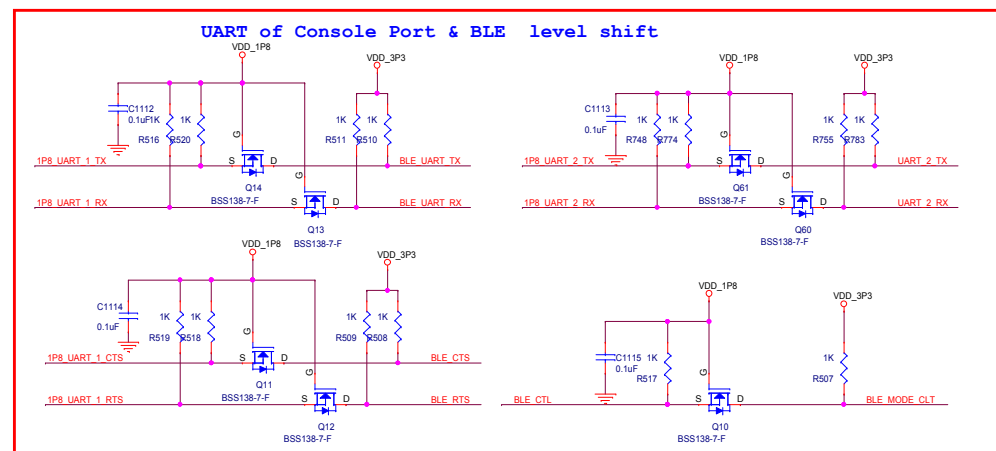
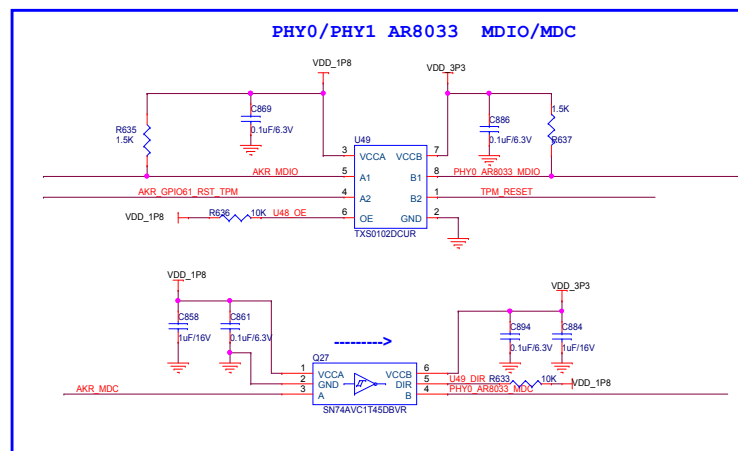


Pin Number	Pin Function	Pin Number	Pin Function
1	SM_DAT	17	GPIO
2	SM_SCK	18	GPIO
3		19	GPIO
4		20	GPIO
5		21	GPIO
6		22	GPIO
7		23	GPIO
8	TEST1	24	GPIO
9		25	GPIO
10		26	GPIO
11		27	GPIO
12		28	GPIO
13			
14			
15			
16	LRESET#		
17			
18			
19			
20			
21			
22	PIRQ#		
23	TWI_Wakeup#		
24			
25			
26			
27			
28			

AT97SC3205T-VGA13-10



Model Name		Rev	
EAP1024A-V2-2015-ZZ		R01	
Size	Page Name	Engineer	
C	14_NAND MMC FLASH	Yin Lee	
Date:	Thursday, December 29, 2016	Sheet	14 of 38



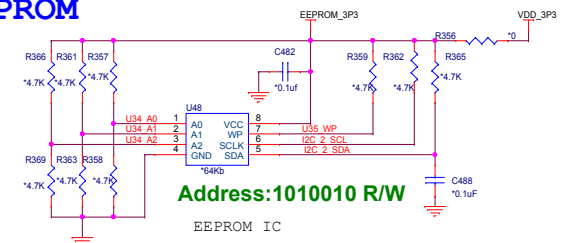
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Model Name	EAP1024A-V2-2015-ZZ	Rev	R01
Page Name	15_Level Translators	Engineer	Yin_Lee
Date:	Thursday, December 29, 2016	Sheet	15 of 38

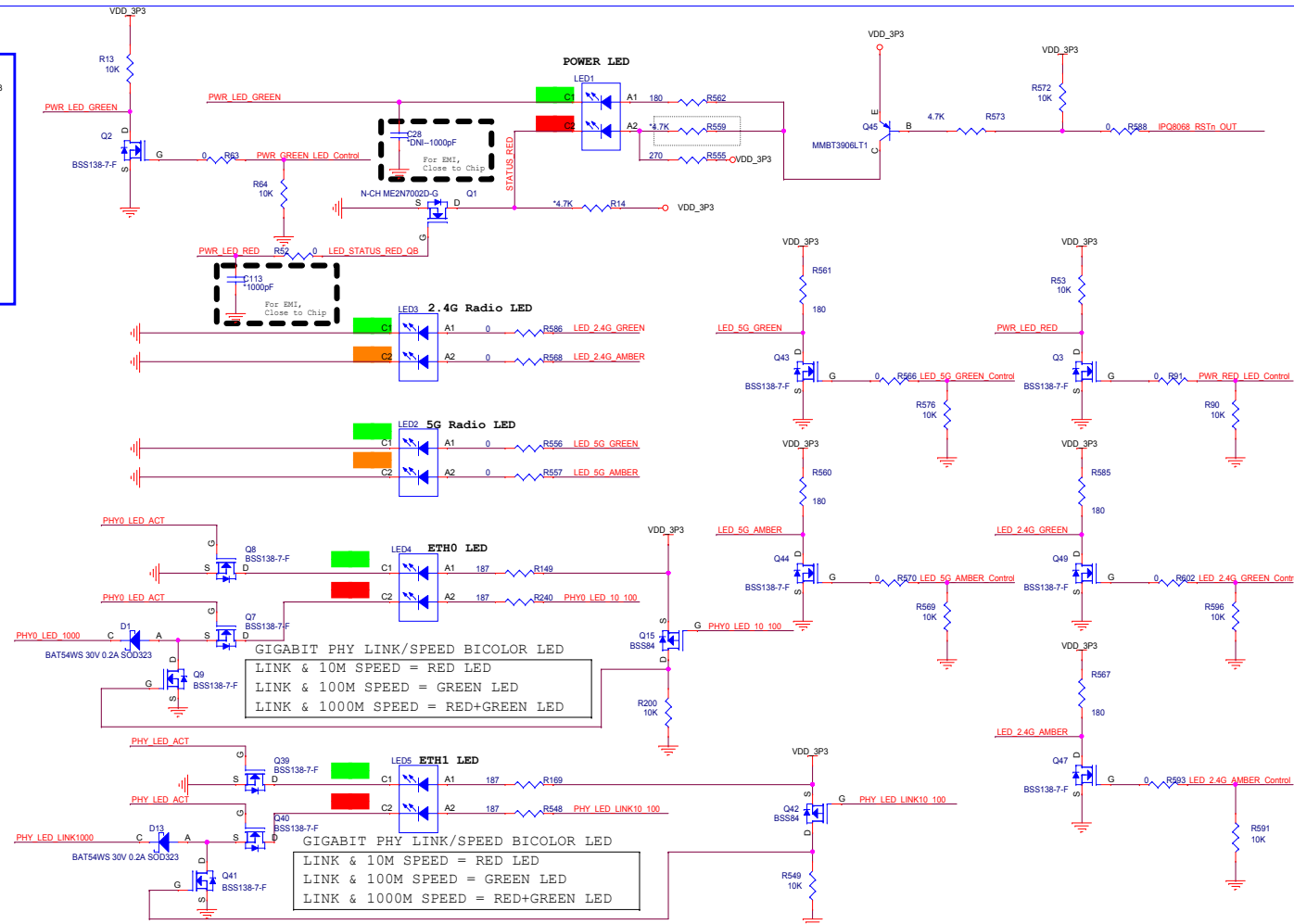
EEPROM



[7,14,15] I2C_2_SDA <<>> I2C_2_SDA
[7,14,15] I2C_2_SCL <<>> I2C_2_SCL

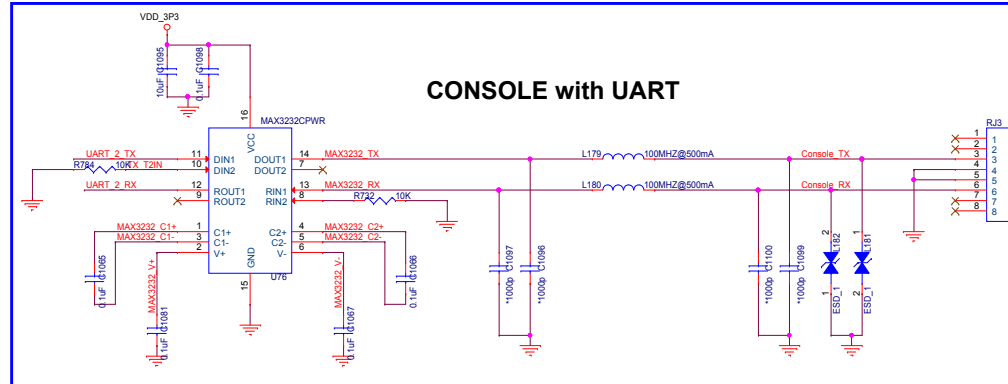
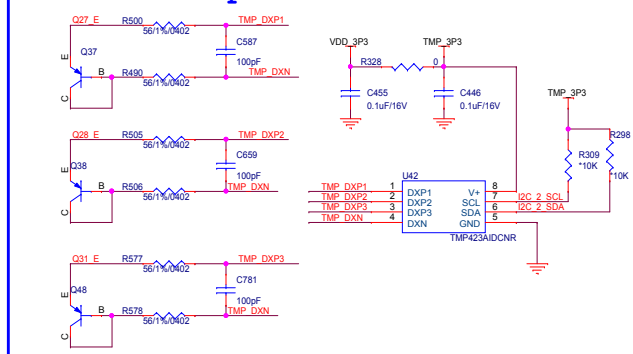
[15]	UART_2_TX	UART 2 TX
[15]	UART_2_RX	UART 2 RX

```
[17] PHY0_LED_10_100  >>> PHY0_LED_10_100
[17] PHY0_LED_1000    >>> PHY0_LED_1000
[18] PHY_LED_LINK10_100 >>> PHY_LED_LINK10_100
[18] PHY_LED_LINK1000   >>> PHY_LED_LINK1000
```



Temperature sensor

[17]	PHY0_LED_ACT	<<	PHY0_LED_ACT
[18]	PHY_LED_ACTn	<<	PHY_LED_ACT
[8]	IP08068_RSTn_OUT	>>	IP08068_RSTn_OUT
[9]	PWR_RED_LED_Control	>>	PWR_RED_LED_Control
[9]	LED_24G_GREEN_Control	>>	LED_24G_GREEN_Control
[9]	LED_24G_AMBER_Control	>>	LED_24G_AMBER_Control
[9]	LED_5G_GREEN_Control	>>	LED_5G_GREEN_Control
[9]	LED_5G_AMBER_Control	>>	LED_5G_AMBER_Control
[9]	PWR_GREEN_LED_Control	>>	PWR_GREEN_LED_Control



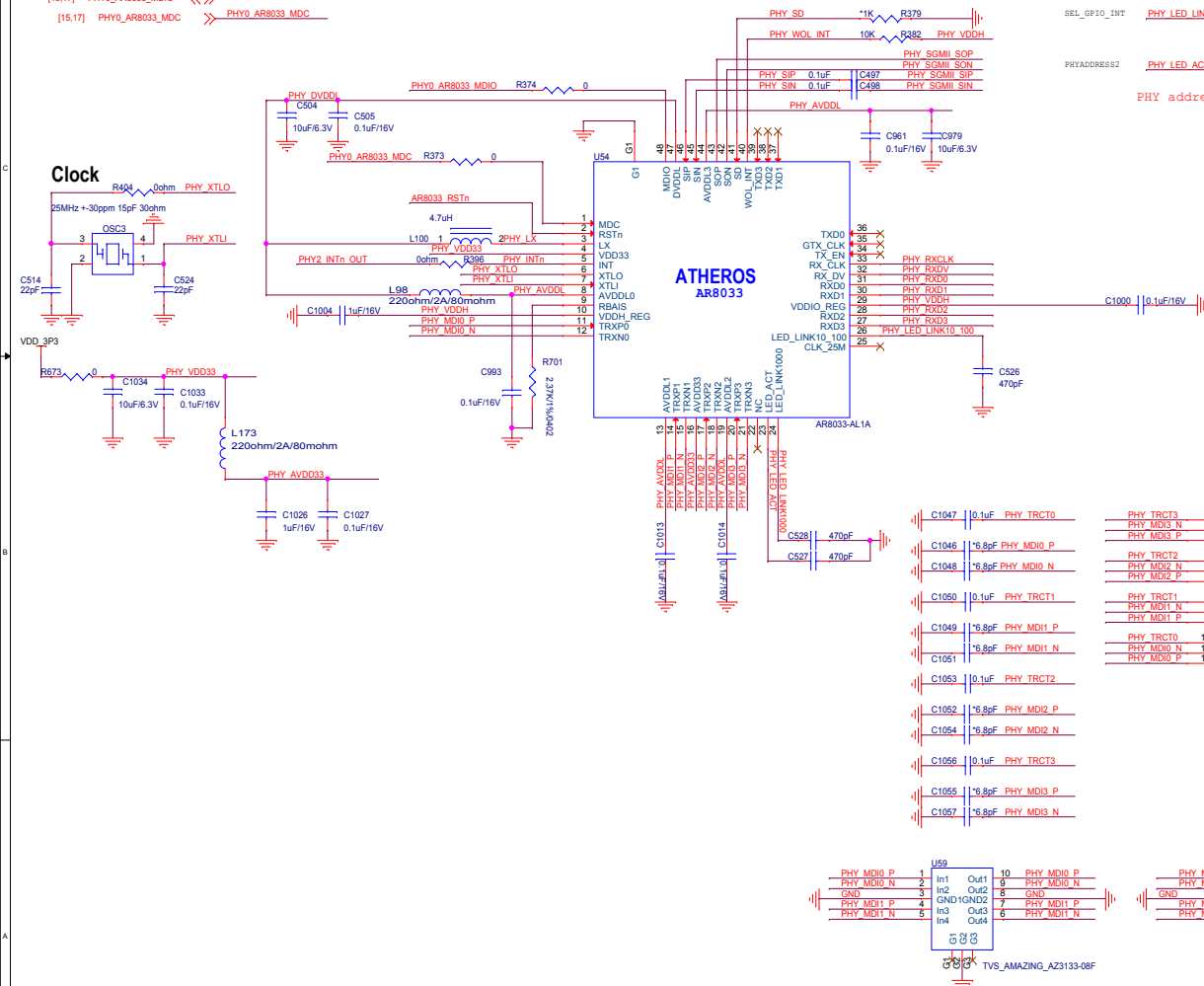
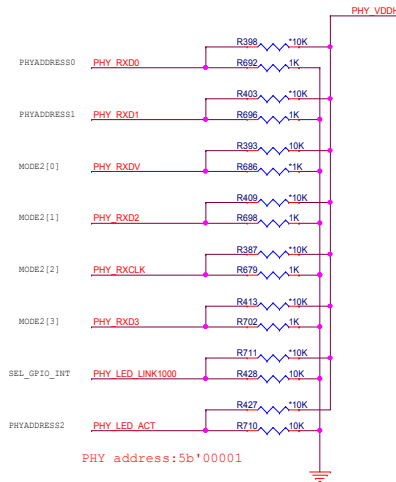
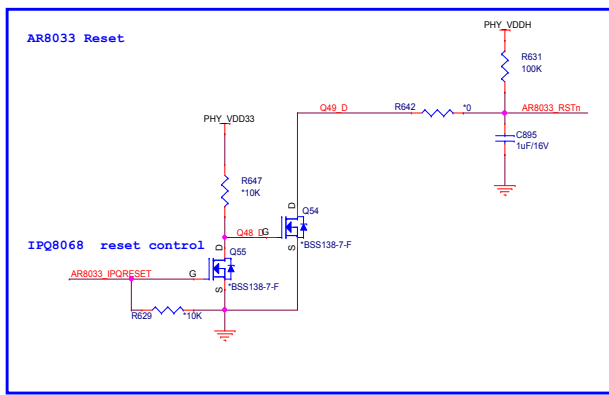
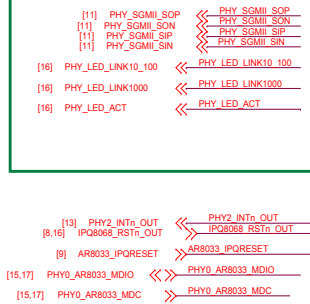
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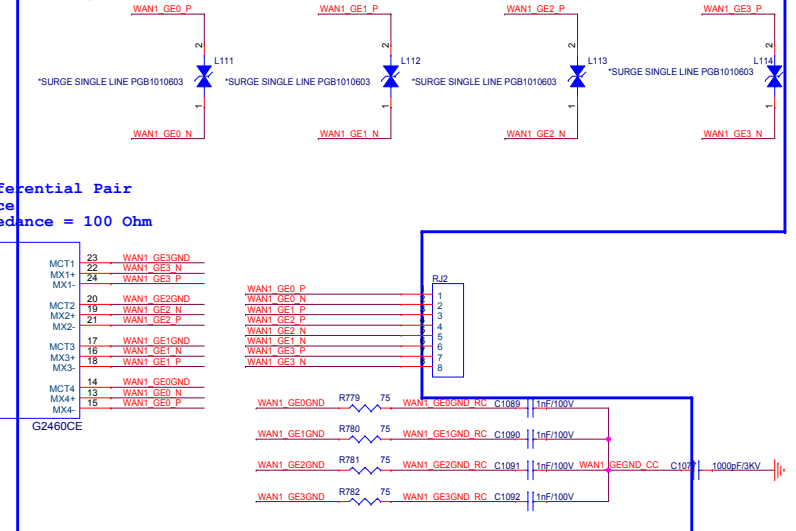
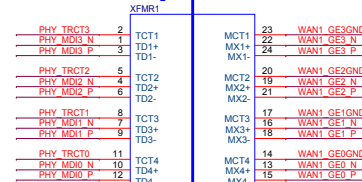


Model Name		EAP1024A-V2-2015-ZZ		Rev	R01
Size	Page Name	Engineer			
C	17_PHY1_SGMII_AR8033	Yin_Lee			
Date:	Thursday, December 29, 2016	Sheet	17	of	38

SGMII Interface



Primary side

Differential Pair
Trace
Impedance = 100 Ohm

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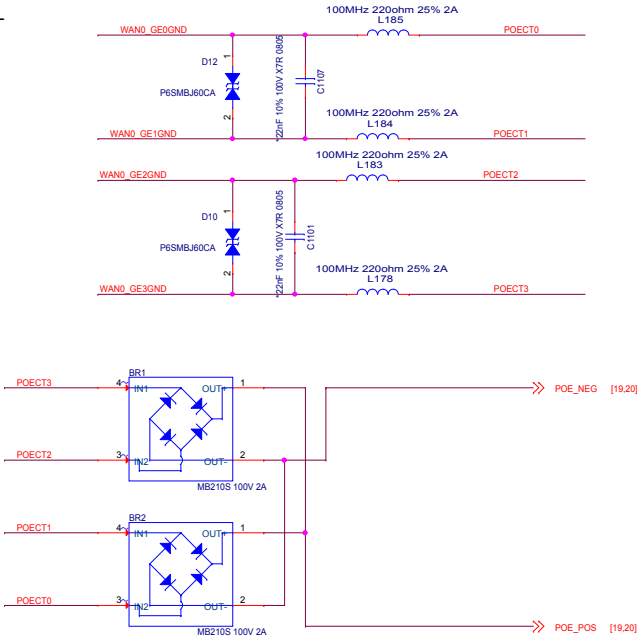


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Model Name		EAP1024A-V2-2015-ZZ	Rev	R01
Size	Page Name	18_PHY2_SGMII AR8033	Engineer	Yin_Lee
C				
Date:	Thursday, December 29, 2016	Sheet	18	of 38

[17] WAN0_GE0GND >> WAN0_GE0GND
[17] WAN0_GE1GND >> WAN0_GE1GND
[17] WAN0_GE2GND >> WAN0_GE2GND
[17] WAN0_GE3GND >> WAN0_GE3GND

[19,20] POE_POS << POE_POS
[19,20] POE_NEG << POE_NEG

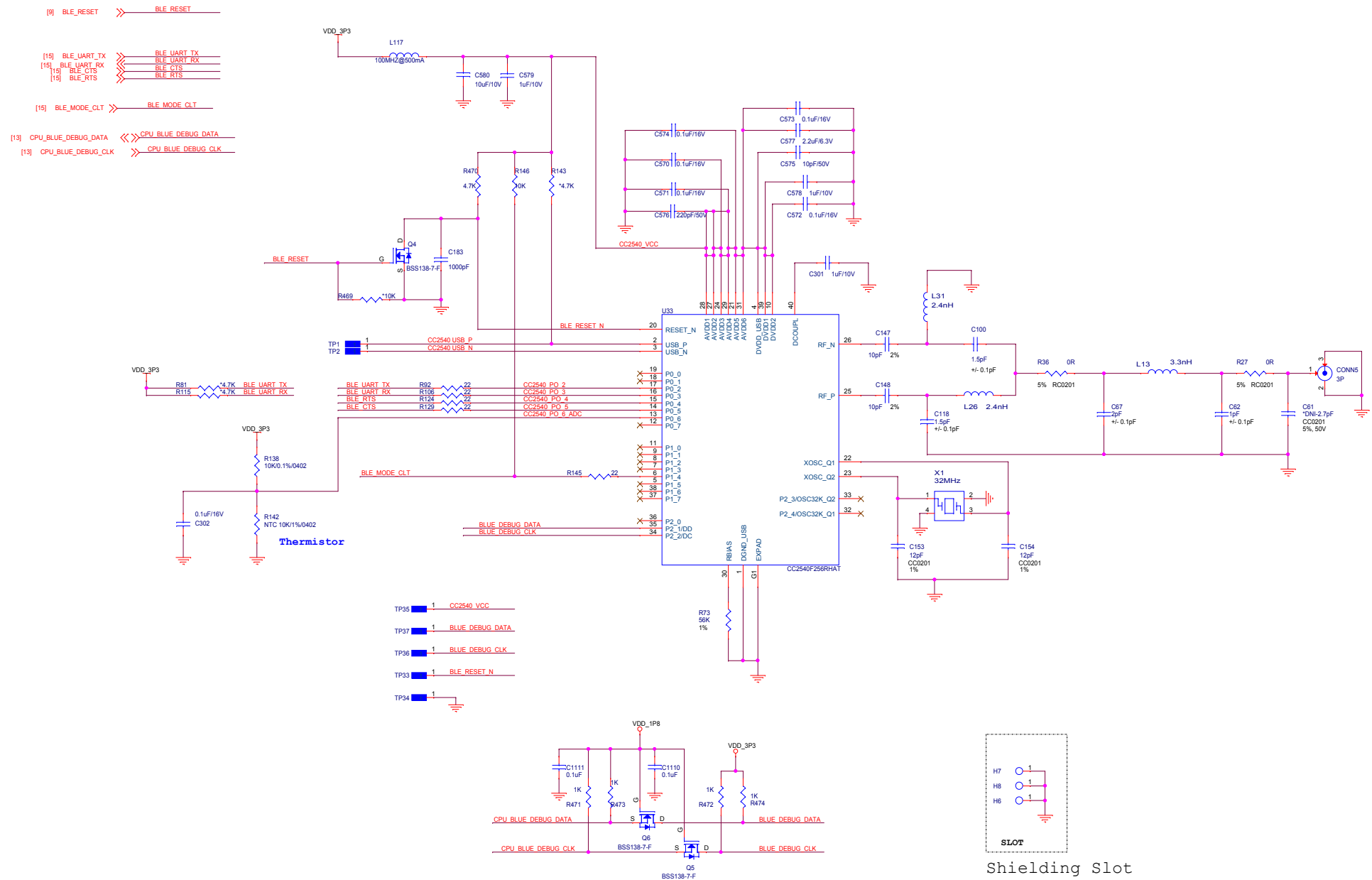


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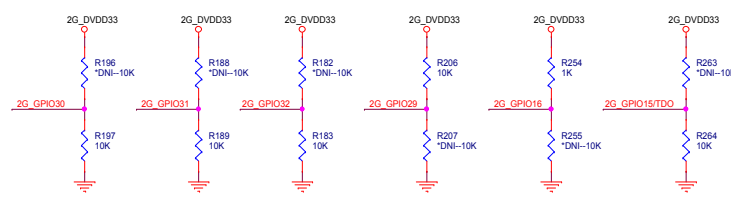
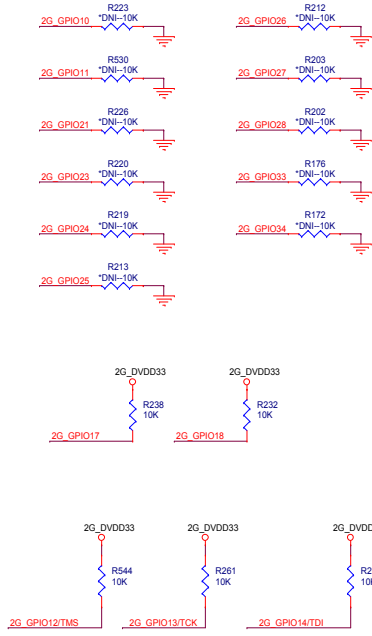
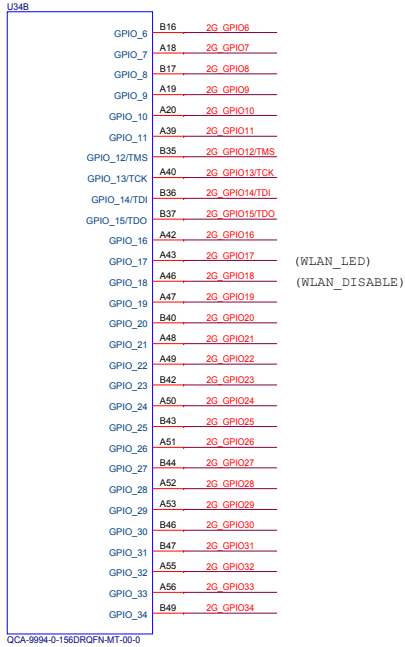


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Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	19 Bridge Diode	Yin_Lee
Date:	Thursday, December 29, 2016	Sheet 19 of 38

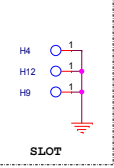
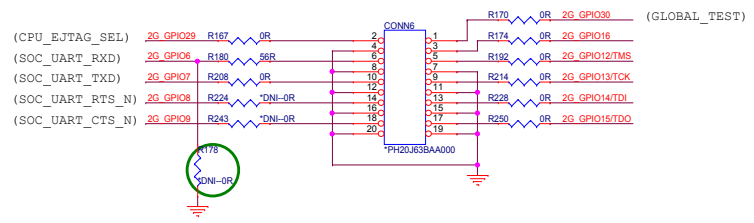


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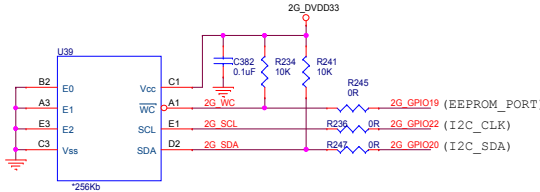


BOOTSTRAP

GPIO30 --> GLOBAL_TEST (LOW)
GPIO31 --> CHIP_TEST_MODE (LOW)
GPIO32 --> DIG_TEST_EN (LOW)
GPIO29 --> CPU_EJTAG_SEL (HIGH)
GPIO16 --> CPU_INIT_RST_N (HIGH)
GPIO15 --> REF_CLK_SEL (LOW)



Shielding Slot

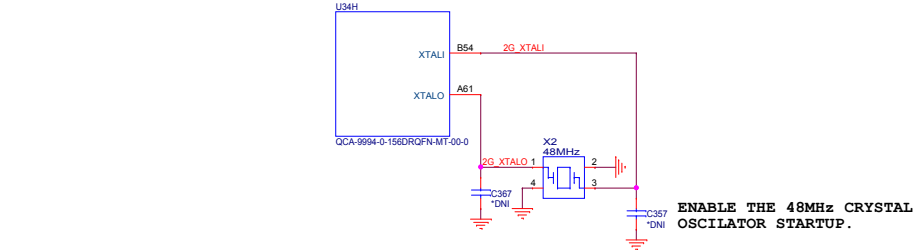
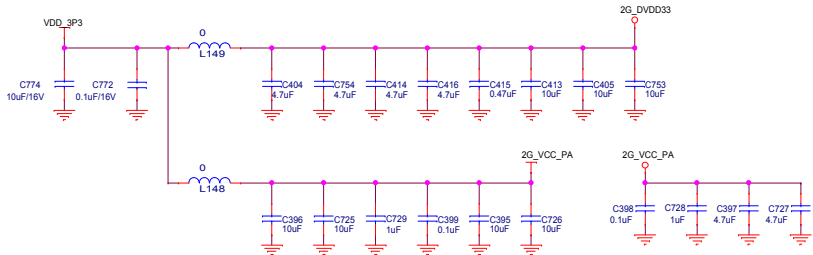
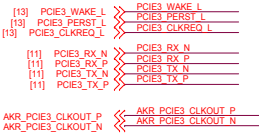


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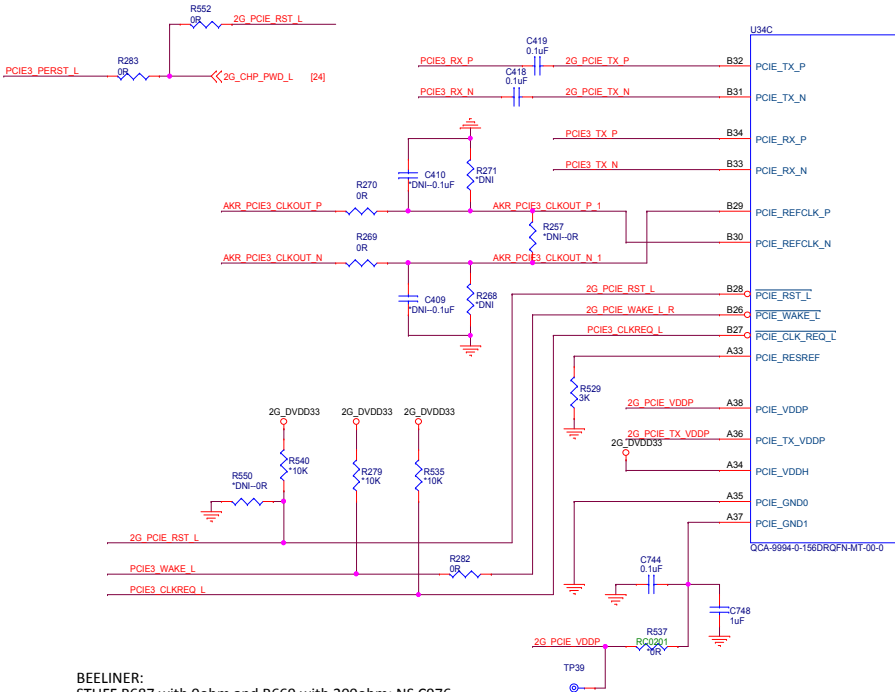


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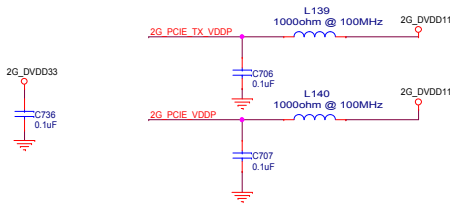
Model Name		EAP1024A-V2-2015-ZZ	Rev	R01
Size	Page Name	Engineer	Date	
C	22 2G_CASECADE_GPIO,UART,EEPROM	Hand	Thursday, December 29, 2016	
Sheet		22	of 38	



ENABLE THE 48MHz CRYSTAL OSCILATOR STARTUP.



BEEELINER:
STUFF R687 with 0ohm and R669 with 200ohm; NS C976
CASCADE:
STUFF C976, R687 with 0.1uF and R669 with 3kohm ; NS R678



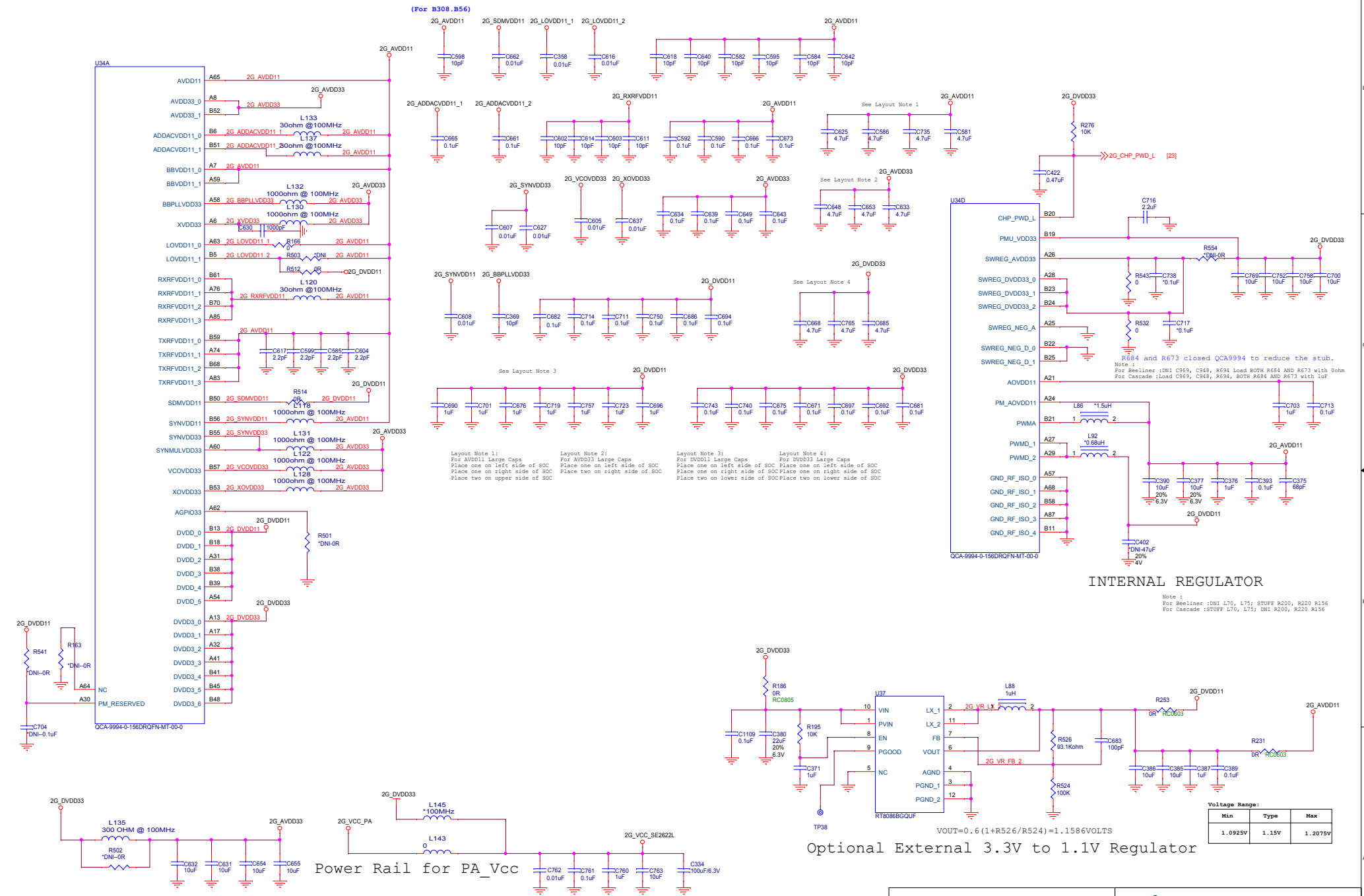
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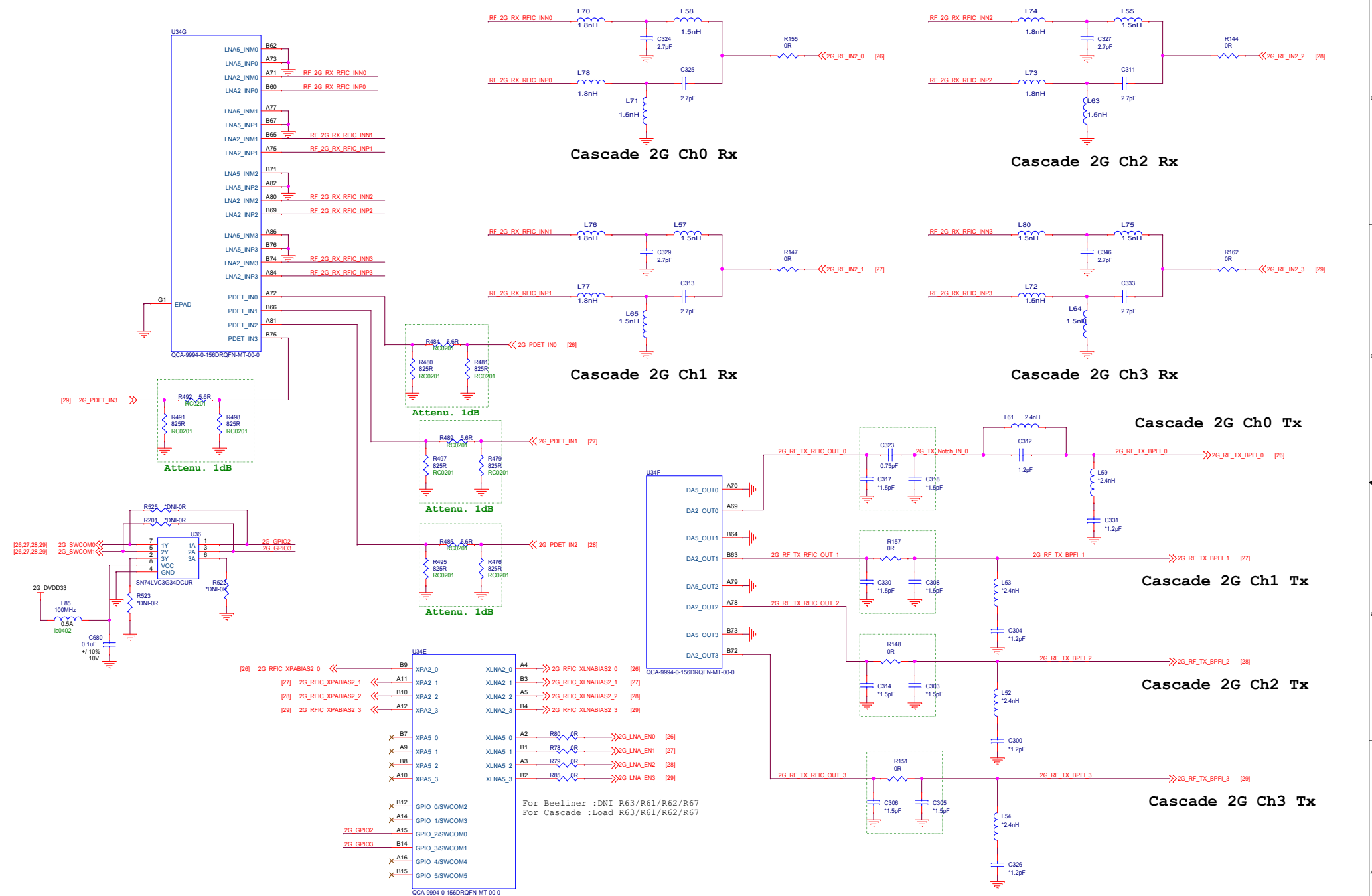


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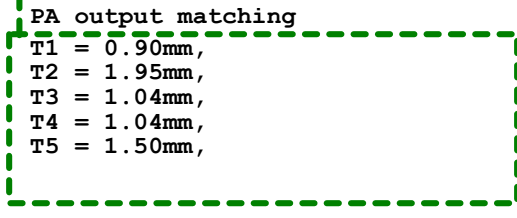
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Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	23 2G CASCADE Clock&PCIE	Fland
Date:	Thursday, December 29, 2016	Sheet 23 of 38





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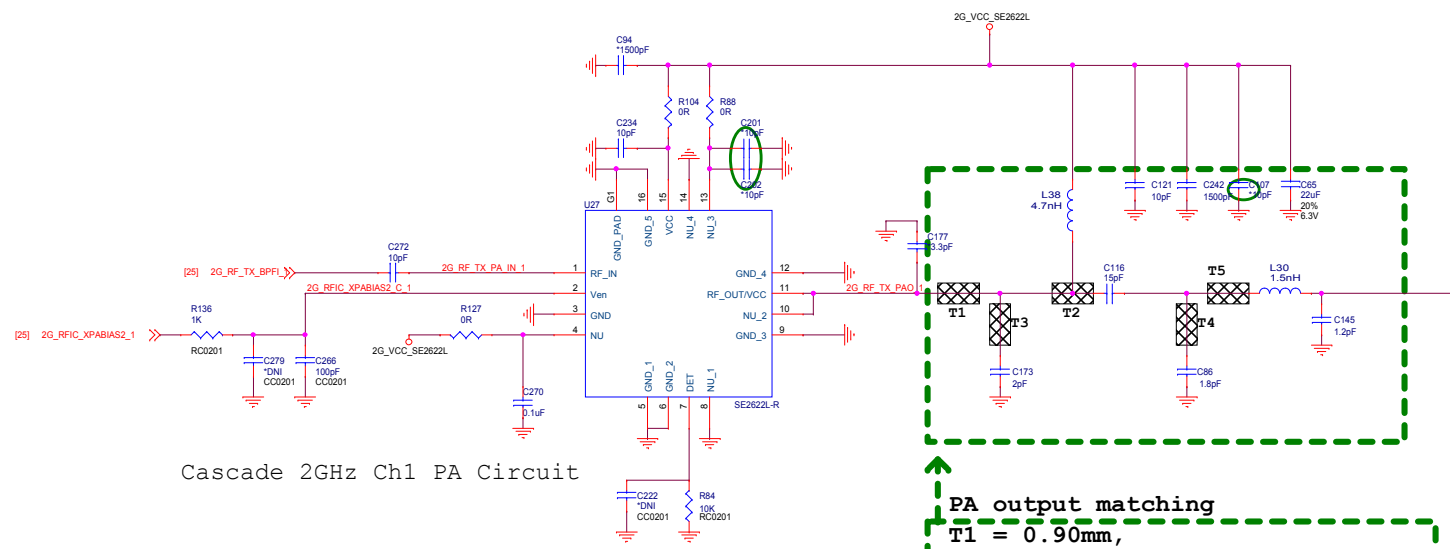
For Beeline :DNI L36/C221/C190/C189 and Load R75
For Cascade :Load L36/C221/C190/C189 and DNI R75



SKY13370-374LF truth table

MODE	Vcont1	Vcont2	OUTPUT1	OUTPUT2
TX	1	0	1	0
RX	0	1	0	1

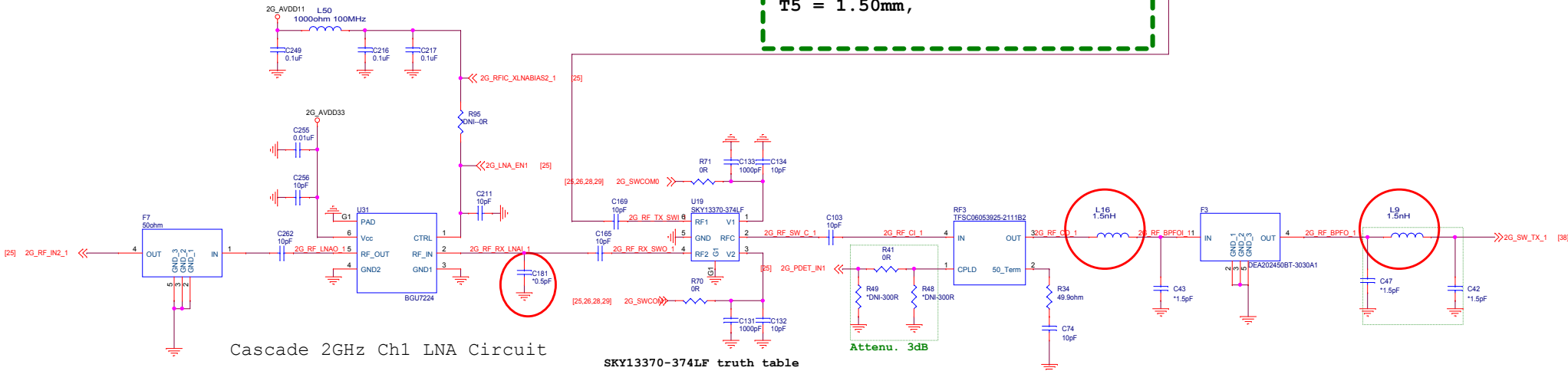
Model Name		Rev	
EAP1024A-V2-2015-ZZ		R01	
Size	Page Name	Engineer	
C	26_2G_CASECADE_FEM_Chain_0	Fland	
Date:	Thursday, December 29, 2016	Sheet	26 of 38



Cascade 2GHz Ch1 PA Circuit

PA output matching
T1 = 0.90mm,
T2 = 1.95mm,
T3 = 1.04mm,
T4 = 1.04mm,
T5 = 1.50mm,

For Beeline :DNI L35/C220/C187/C188 and Load R74
For Cascade :Load L35/C220/C187/C188 and DNI R74



Cascade 2GHz Ch1 LNA Circuit

SKY13370-374LF truth table

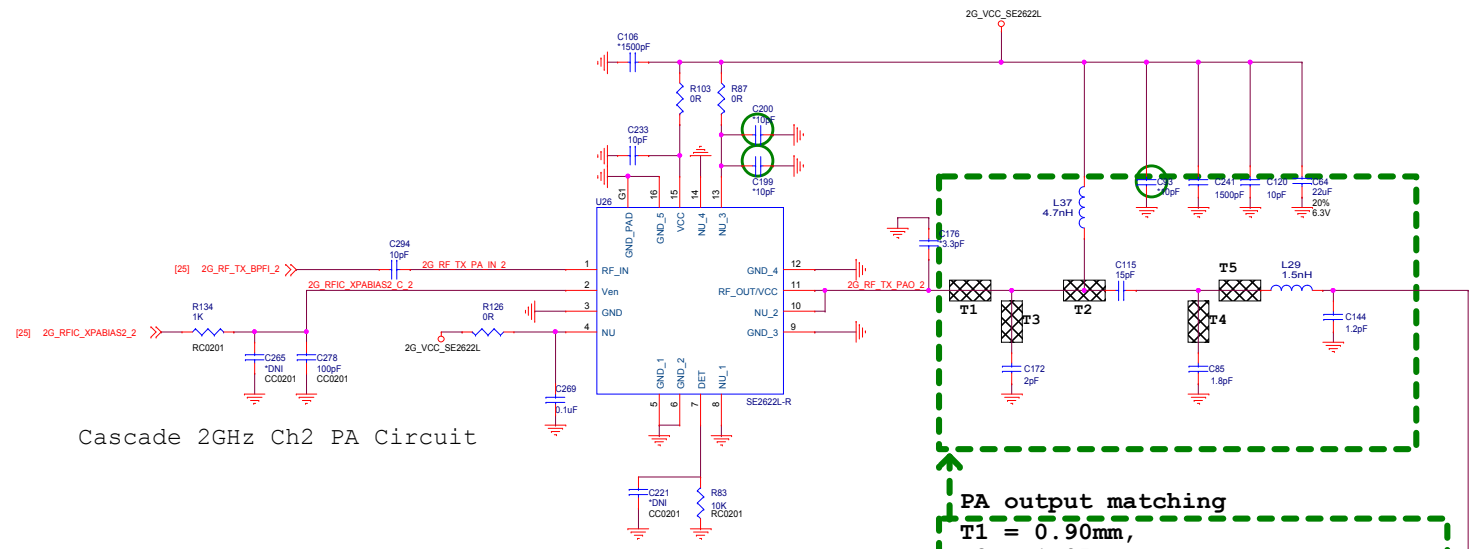
MODE	Vcont1	Vcont2	OUTPUT1	OUTPUT2
TX	1	0	1	0
RX	0	1	0	1

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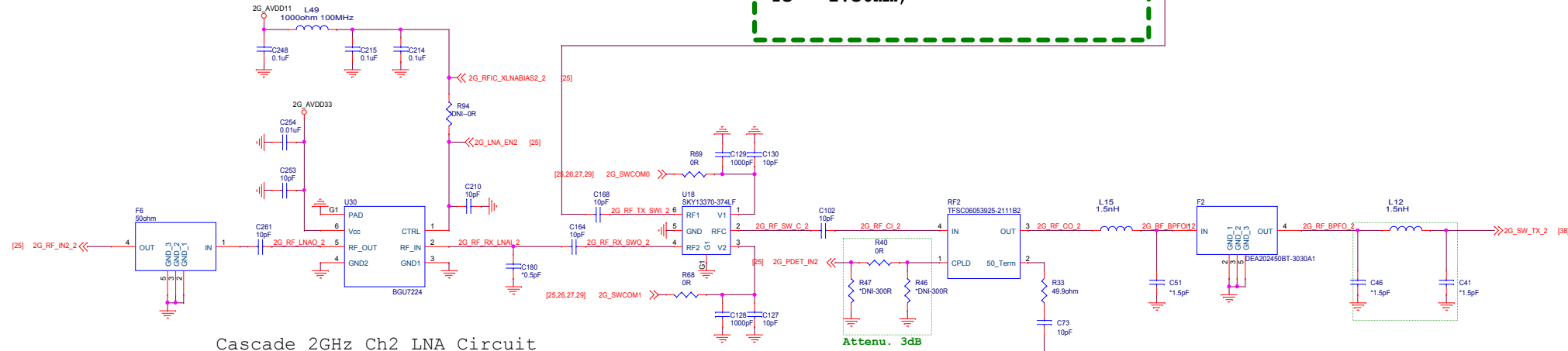
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Model Name		EAP1024A-V2-2015-ZZ	Rev	R01
Size	Page Name	Engineer		
C	27 2G CASECADE_FEM_Chain	Fland		
Date:	Thursday, December 29, 2016	Sheet	27	of 38



Cascade 2GHz Ch2 PA Circuit

For Beeliner :DNI L34/C219/C186/C185 and Load R73
For Cascade :Load L34/C219/C186/C185 and DNI R73



Cascade 2GHz Ch2 LNA Circuit

SKY13370-374LF truth table

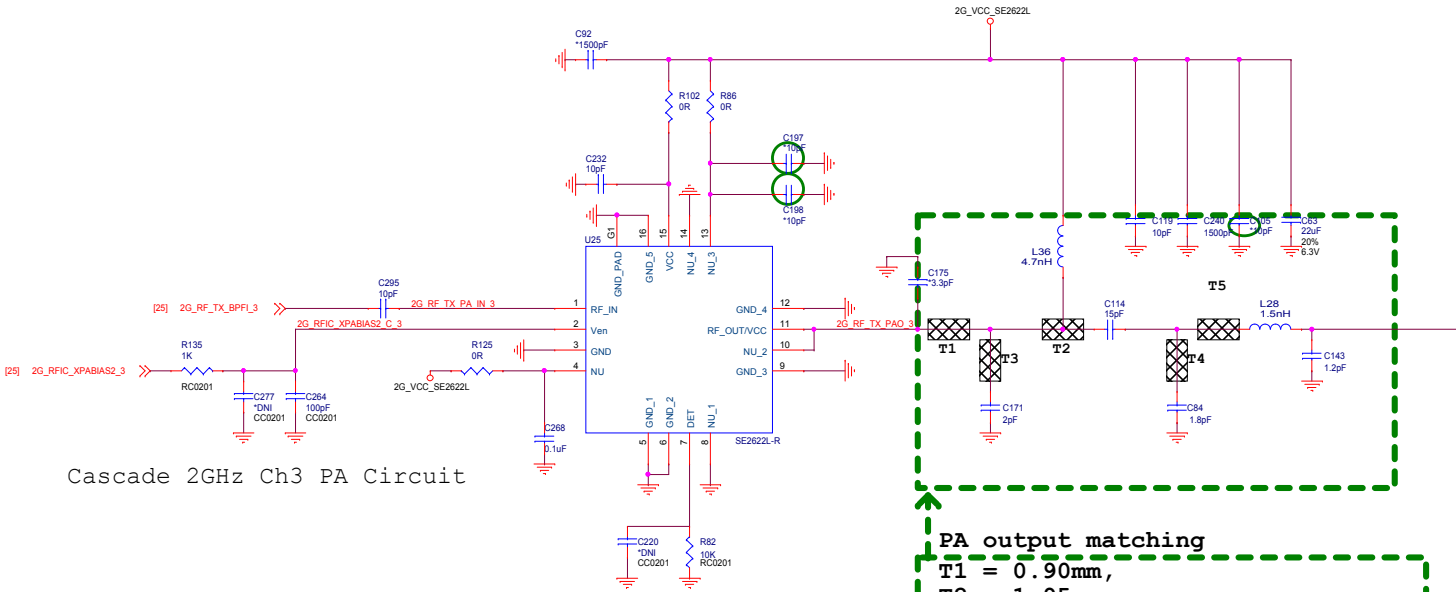
MODE	Vcont1	Vcont2	OUTPUT1	OUTPUT2
TX	1	0	1	0
RX	0	1	0	1

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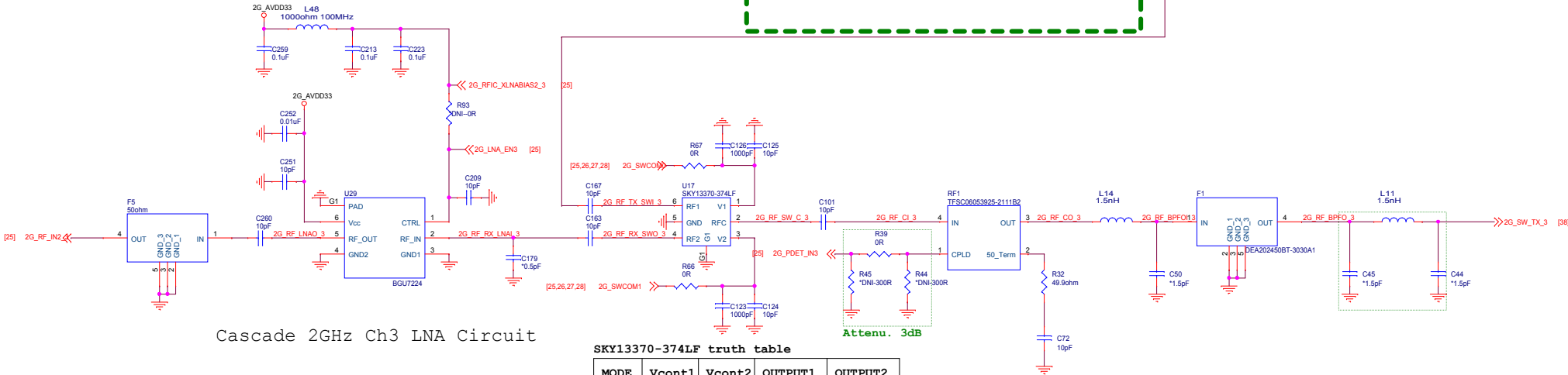
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Model Name		EAP1024A-V2-2015-ZZ	Rev	R01
Size	Page Name	28 2G CASECADE_FEM_Chain_2	Engineer	
C			Fland	
Date:	Thursday, December 29, 2016	Sheet	28	of 38



Cascade 2GHz Ch3 PA Circuit

For Beeliner :DNI L33/C230/C184/C194 and Load R72
For Cascade :Load L33/C230/C184/C194 and DNI R72

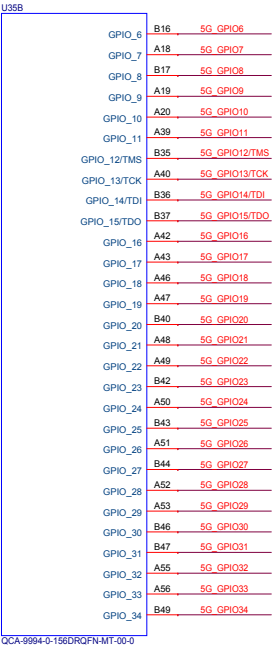


Cascade 2GHz Ch3 LNA Circuit

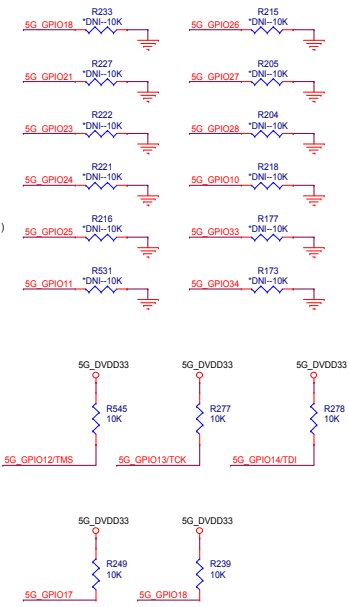
SKY13370-374LF truth table

MODE	Vcont1	Vcont2	OUTPUT1	OUTPUT2
TX	1	0	1	0
RX	0	1	0	1

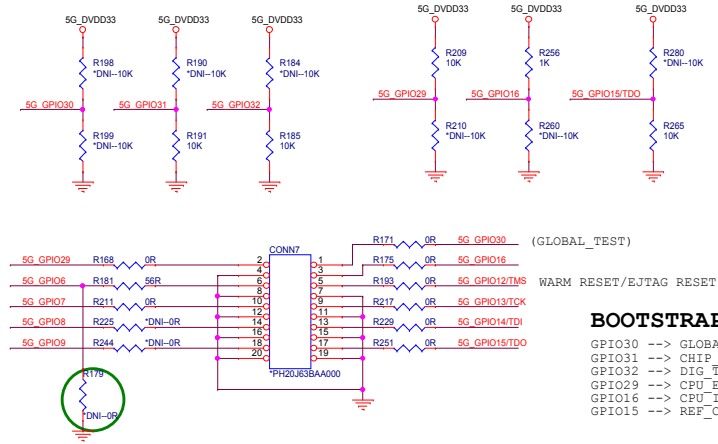
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(WLAN_LED)
(WLAN_DISABLE)



(CPU_EJTAG_SEL)
(SOC_UART_RXD)
(SOC_UART_TXD)
(SOC_UART_RTS_N)
(SOC_UART_CTS_N)

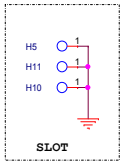


(GLOBAL_TEST)

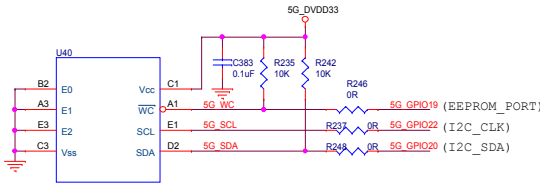
WARM RESET/EJTAG RESET

BOOTSTRAP

GPIO30 --> GLOBAL_TEST
GPIO31 --> CHIP_TEST_MODE
GPIO32 --> DIG_TEST_EN
GPIO29 --> CPU_EJTAG_SEL
GPIO16 --> CPU_INIT_RST_N
GPIO15 --> REF_CLK_SEL



Shielding Slot



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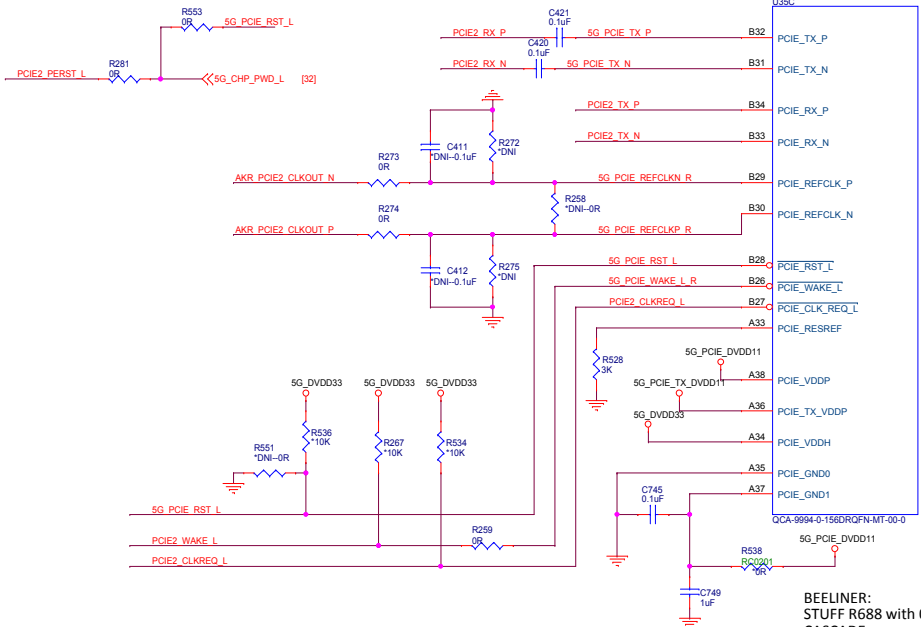
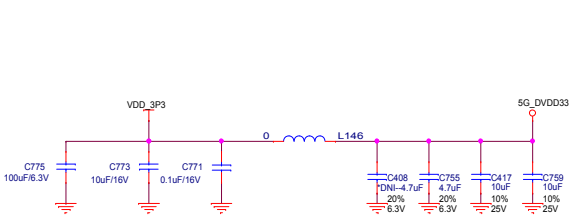
Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	30 5G CASECADE_GPIO_UART	EEPROM
Date:	Thursday, December 29, 2016	Sheet 30 of 38

[11] AKR_PCIE2_CLKOUT_P << AKR_PCIE2_CLKOUT_P

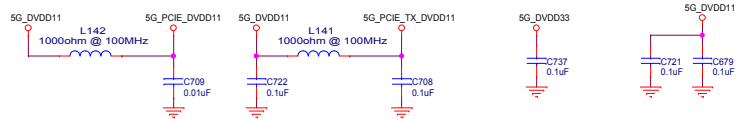
[11] AKR_PCIE2_CLKOUT_N << AKR_PCIE2_CLKOUT_N

PCIE2_WAKE_L << PCIE2_WAKE_L [13]
PCIE2_PERS_T_L << PCIE2_PERS_T_L [13]
PCIE2_CLKREQ_L << PCIE2_CLKREQ_L [13]

PCIE2_RX_N << PCIE2_RX_N [11]
PCIE2_TX_N << PCIE2_TX_N [11]
PCIE2_TX_P << PCIE2_TX_P [11]



BEELINER:
STUFF R688 with 0ohm, R670 with 200ohm; NS C977
CASCADE:
STUFF C977, R688 with 0.1uF and R670 with 3kohm ; NS R679

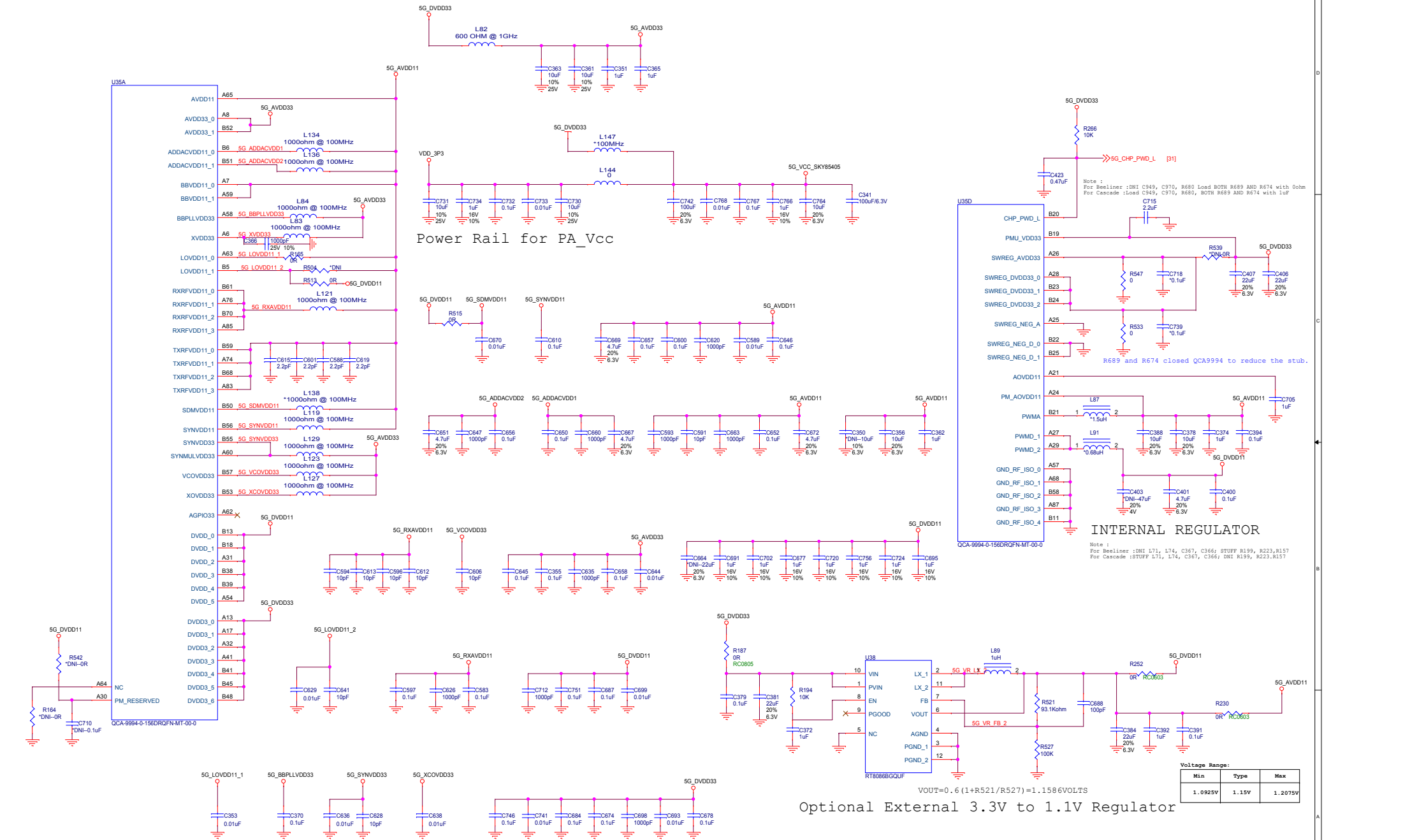


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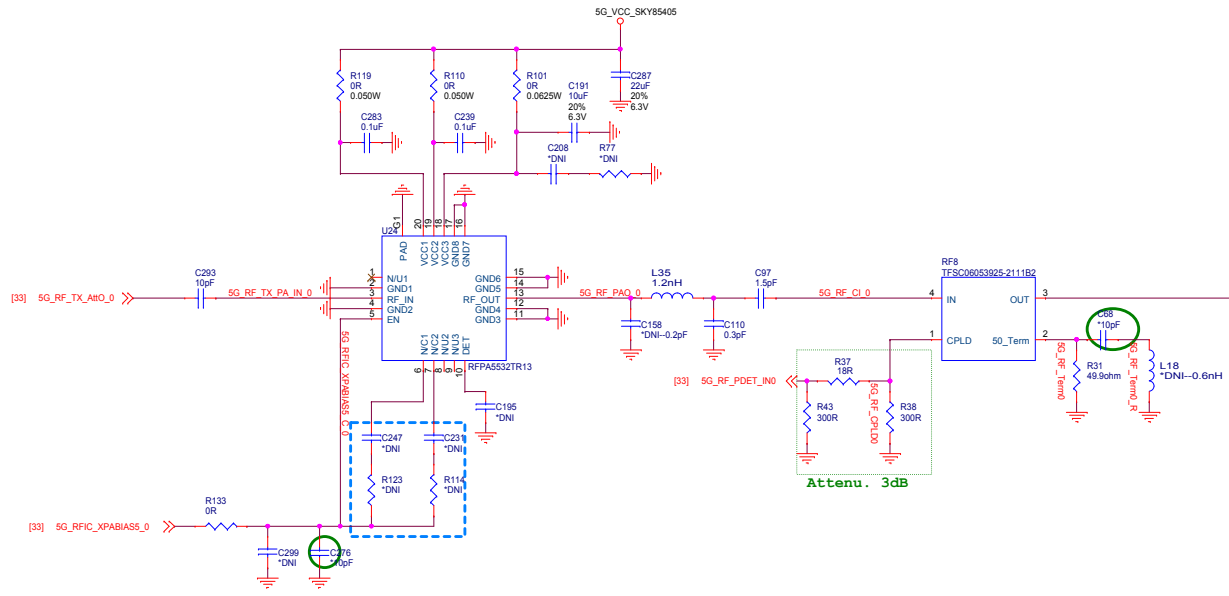


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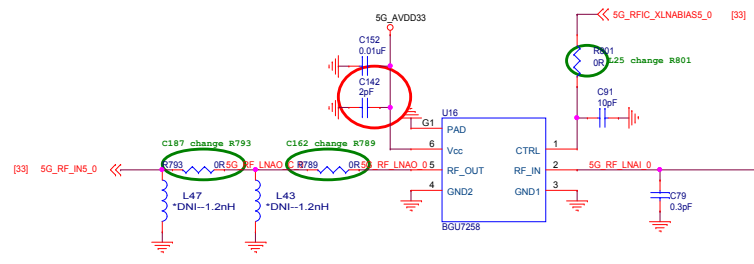
Model Name		EAP1024A-V2-2015-ZZ	Rev	R01
Size	Page Name	Engineer		
C	31 5G_CASECADE_Clock & PCIE	Fland		
Date:	Thursday, December 29, 2016	Sheet	31	of 38



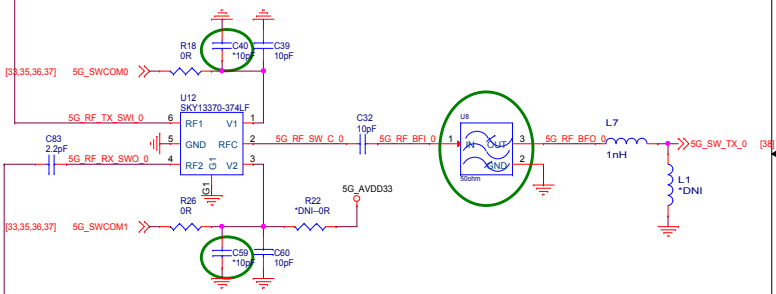
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Cascade 5GHz Ch0 PA Circuit



Cascade 5GHz Ch0 LNA Circuit



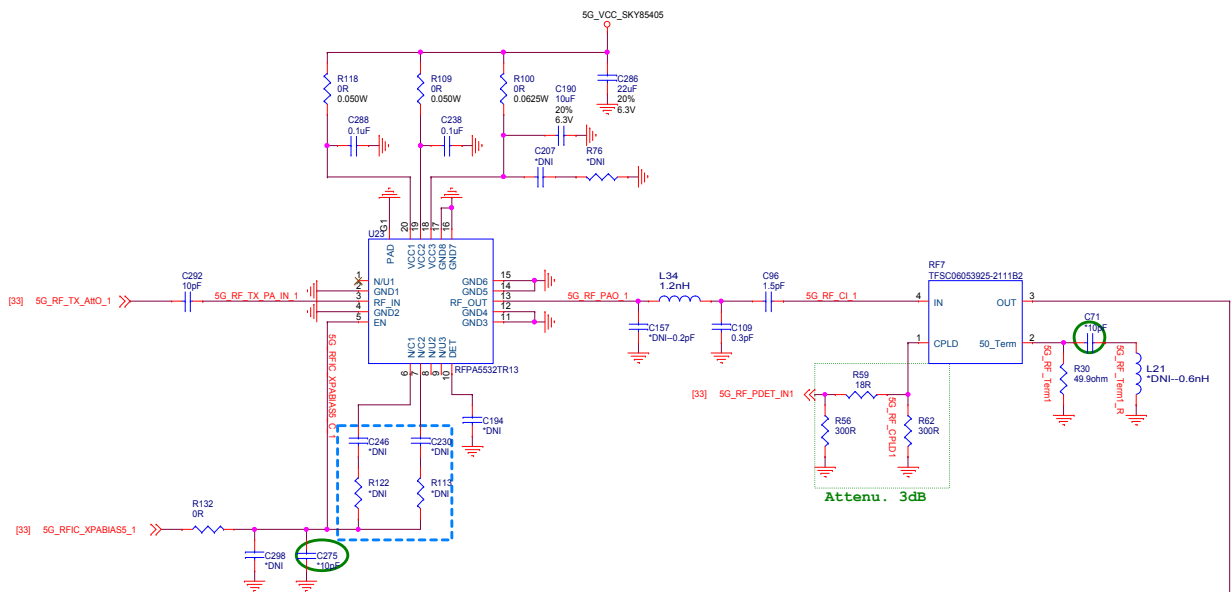
SKY13370-374LF truth table

MODE	V1	V2	RF1	RF2
TX	1	0	1	0
RX	0	1	0	1

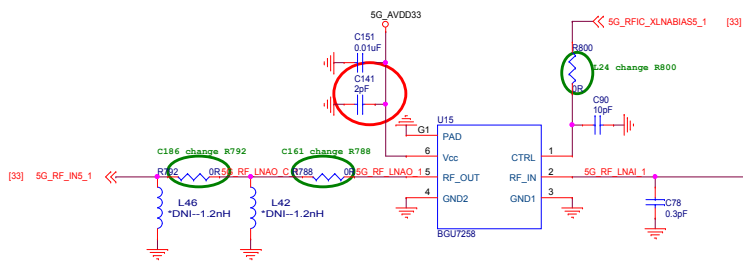
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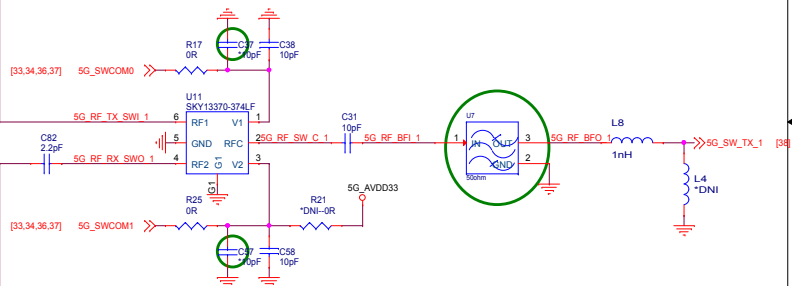
Model Name		EAP1024A-V2-2015-ZZ		Rev	R01
Size	C	Page Name	34 5G CASECADE_FEM_Chain	Engineer	Fland
Date:	Thursday, December 29, 2016	Sheet	34	of	38



Cascade 5GHz Ch1 PA Circuit



Cascade 5GHz Ch1 LNA Circuit



SKY13370-374LF truth table

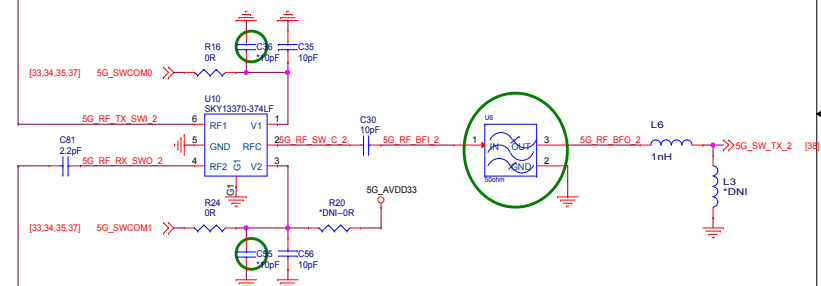
MODE	V1	V2	RF1	RF2
TX	1	0	1	0
RX	0	1	0	1

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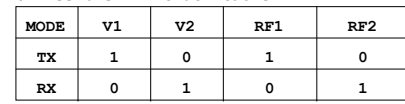


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Model Name		Rev
EAP1024A-V2-2015-ZZ		R01
Size	Page Name	Engineer
C	35_5G_CASECADE_FEM_Chain	1
Date:	Thursday, December 29, 2016	Sheet 35 of 38

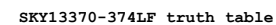
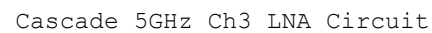
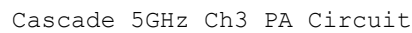


MODE	V1	V2	RF1	RF2
TX	1	0	1	0
RX	0	1	0	1



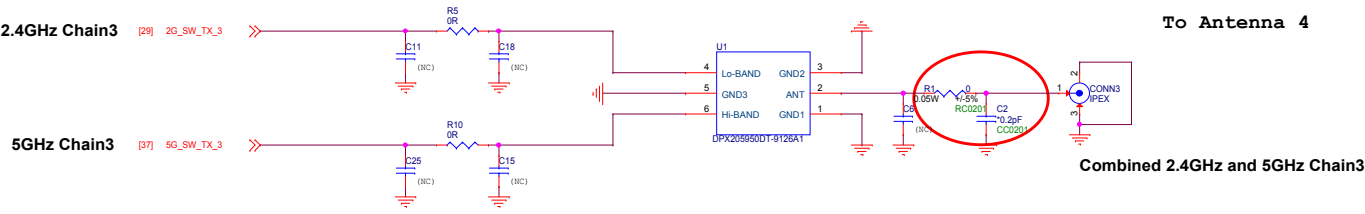
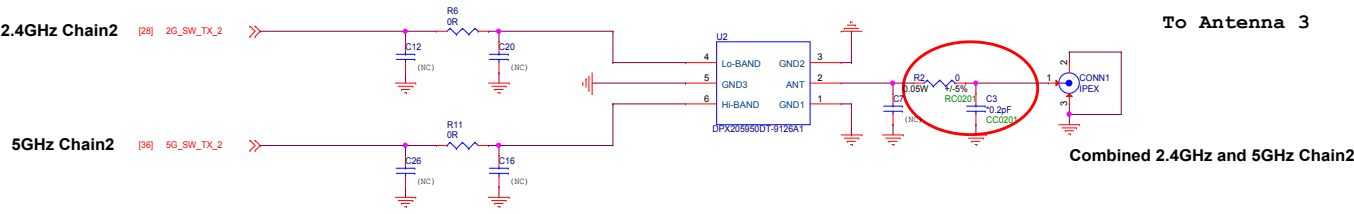
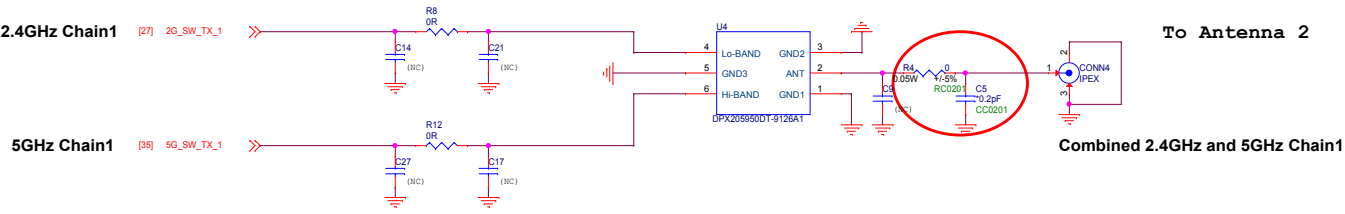
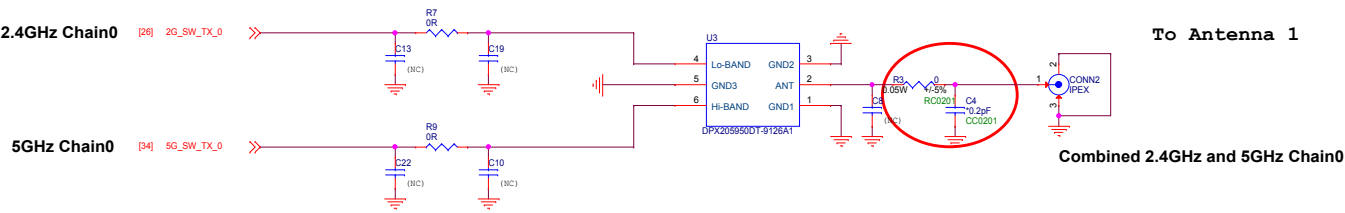
MODE	V1	V2	RF1	RF2
TX	1	0	1	0
RX	0	1	0	1

 Accton Inc. Making Partnership Work		Rev R01
Model Name EAP1024A-V2-2015-ZZ		
Page Name 36_5G_CASECADE_FEM_Chain	Engineer 2 Flad	
Date Thursday, December 29, 2016	Sheet 36 of 38	



MODE	V1	V2	RF1	RF2
TX	1	0	1	0
RX	0	1	0	1

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Model Name		EAP1024A-V2-2015-ZZ		Rev	
Size		Page Name		Engineer	
C		38 Diplexer circuits		Fland	
Date:		Thursday, December 29, 2016		Sheet 38 of 38	