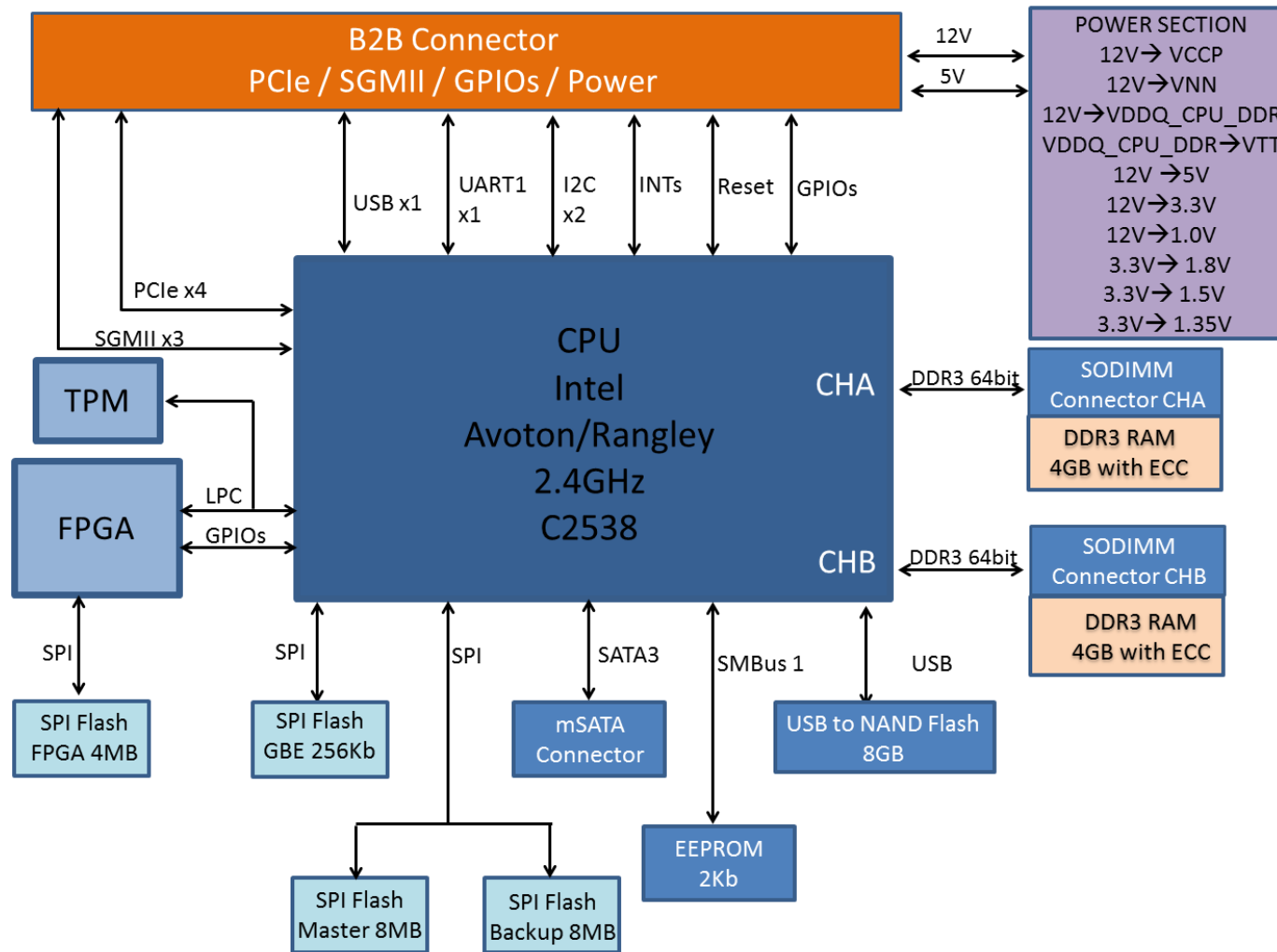


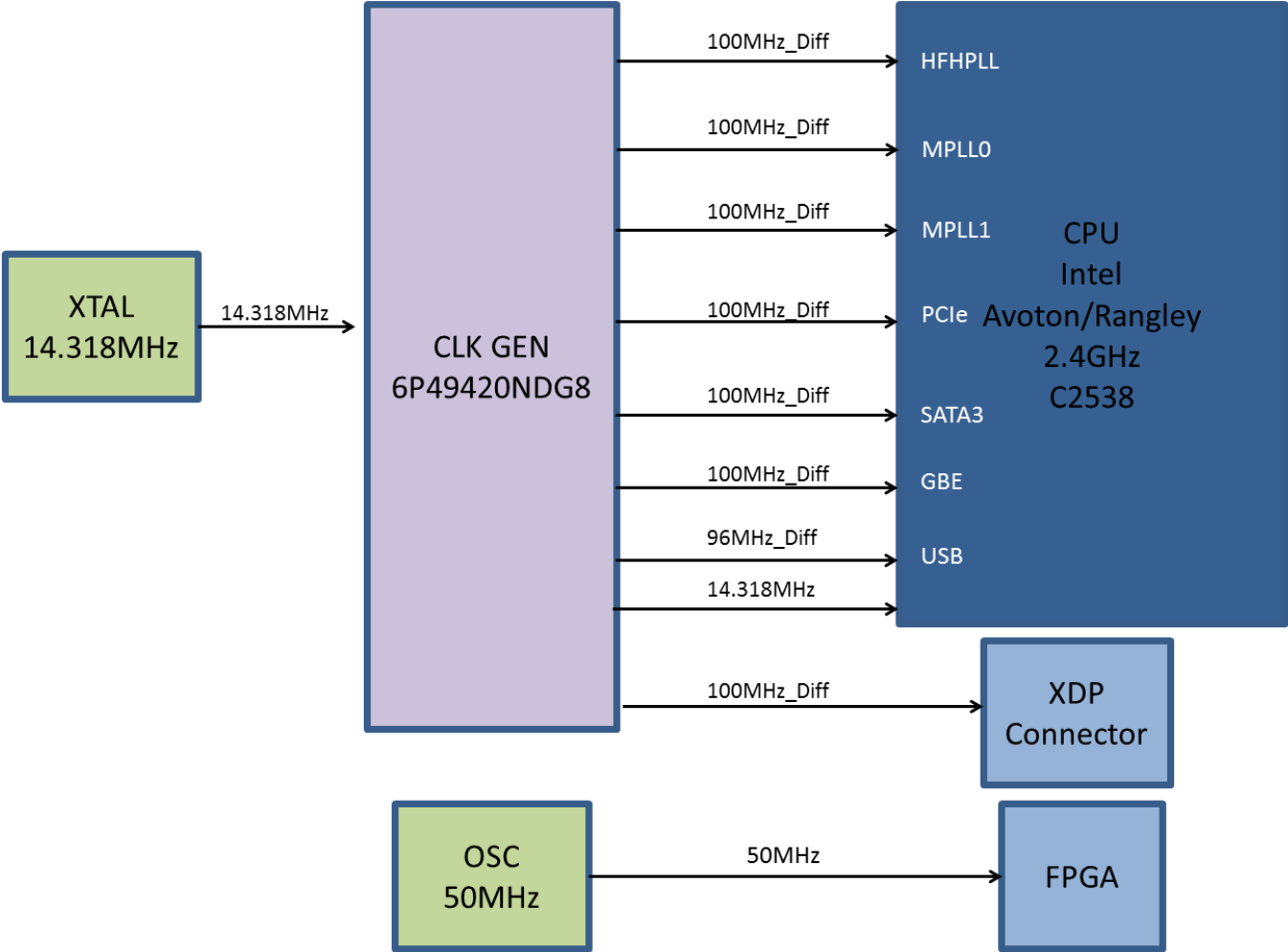
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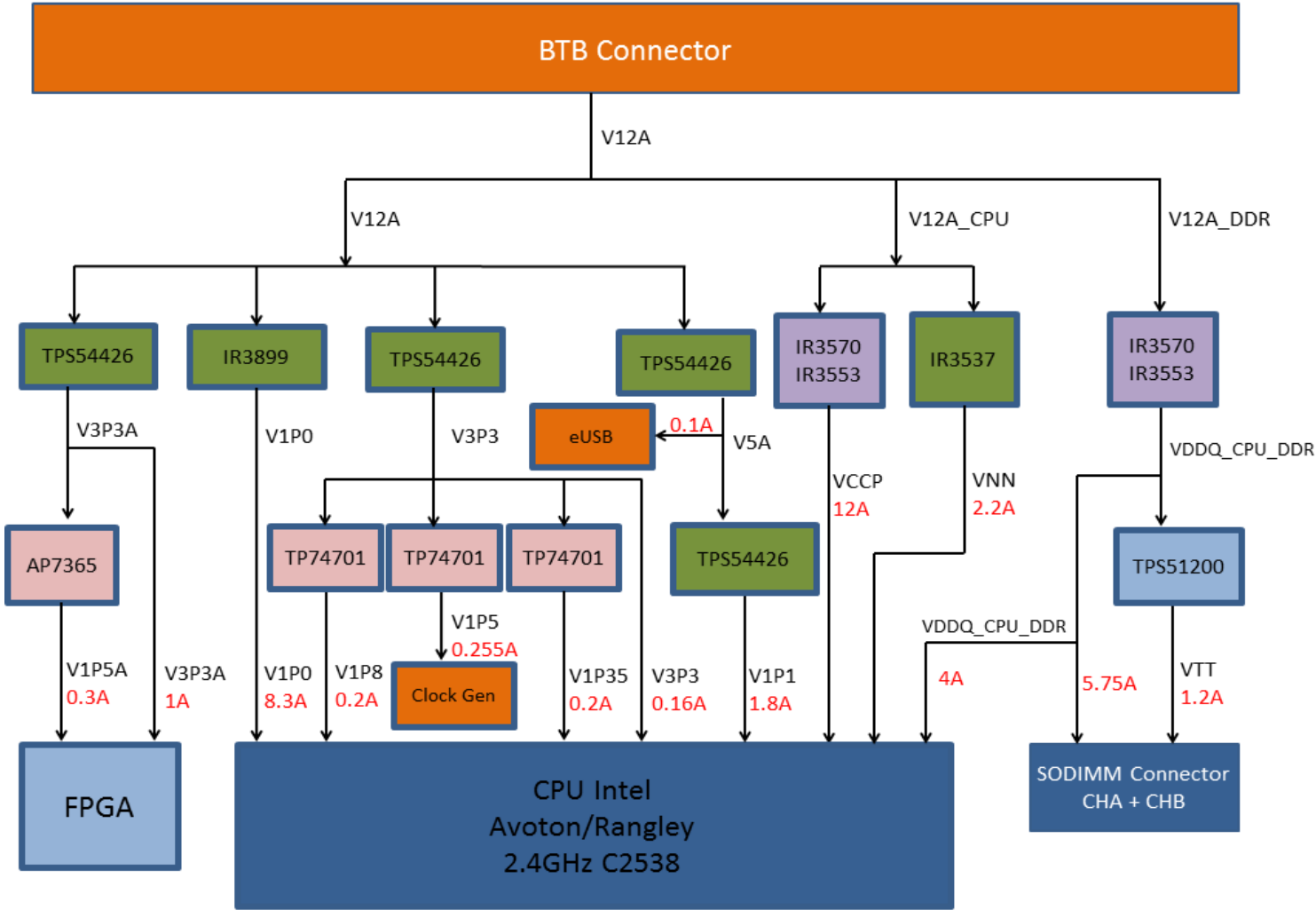
1	Cover Page	18	Clocks
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15	Rangeley Power	32	LDO_V1P8_V1P5_V1P35_V1P5A
16	Rangeley Power	33	Debug LED
17	Rangeley Power_GND		

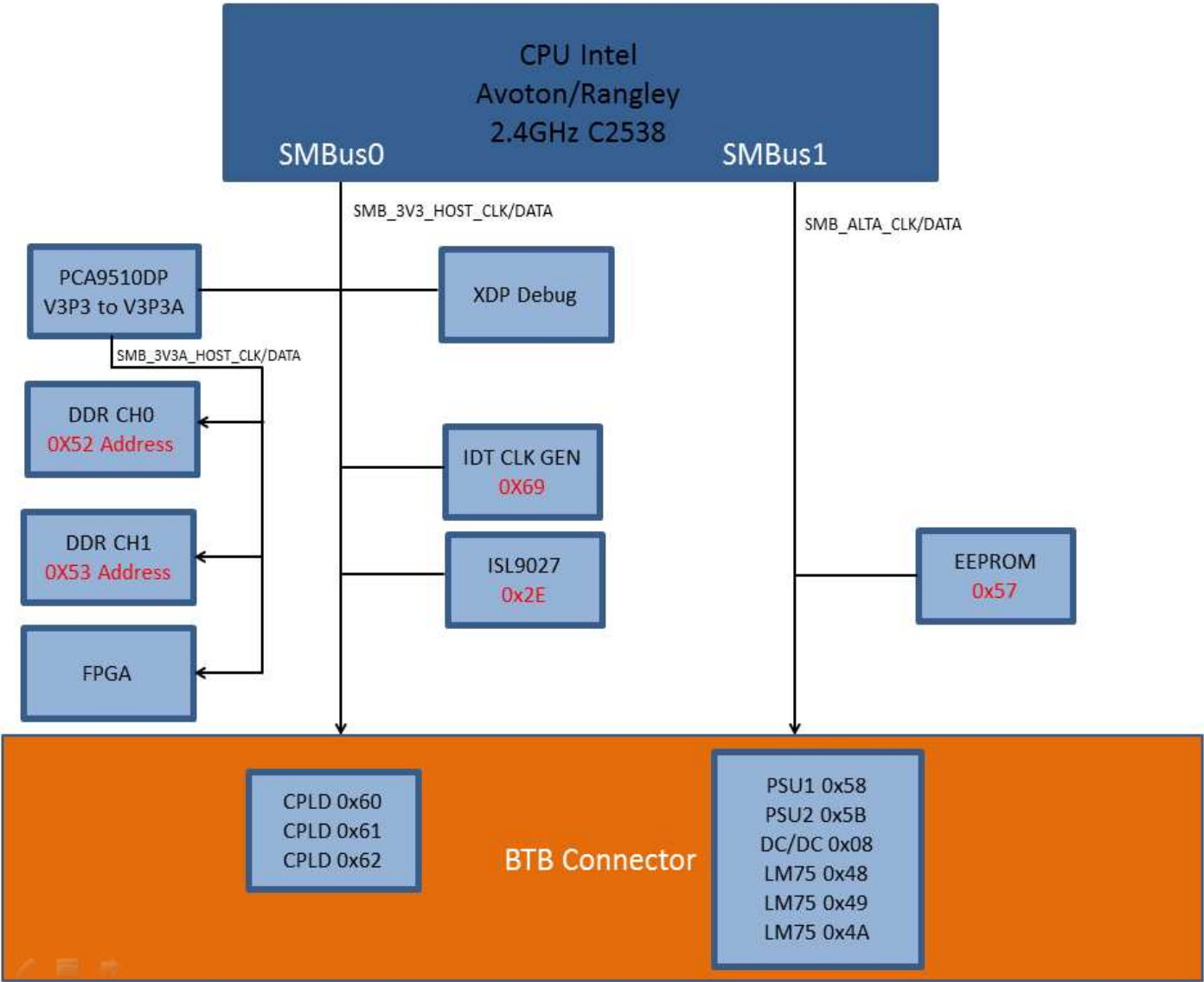
History

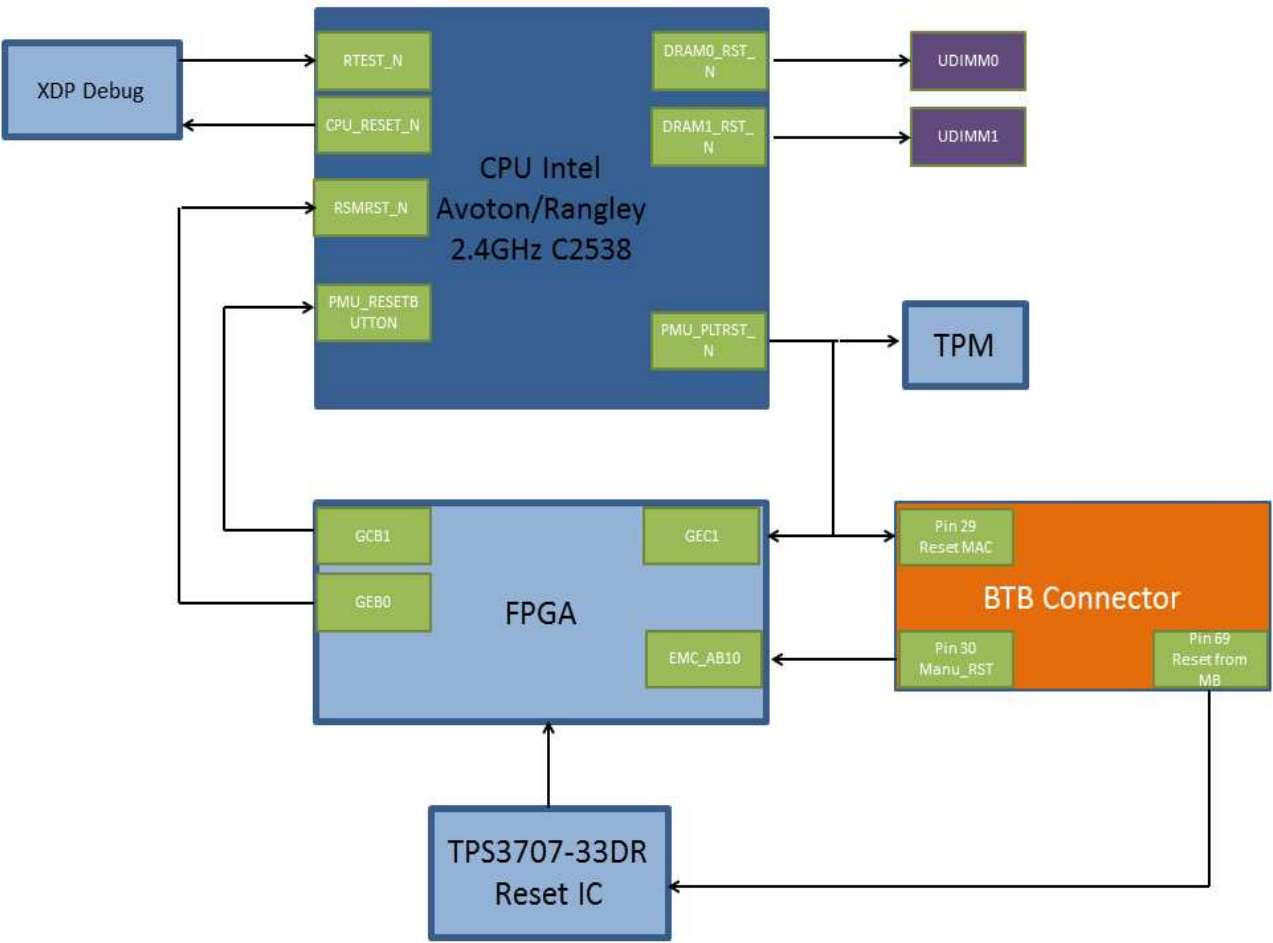
SCH Version	Date	Description
R0A	2015/08/26	Initial Version

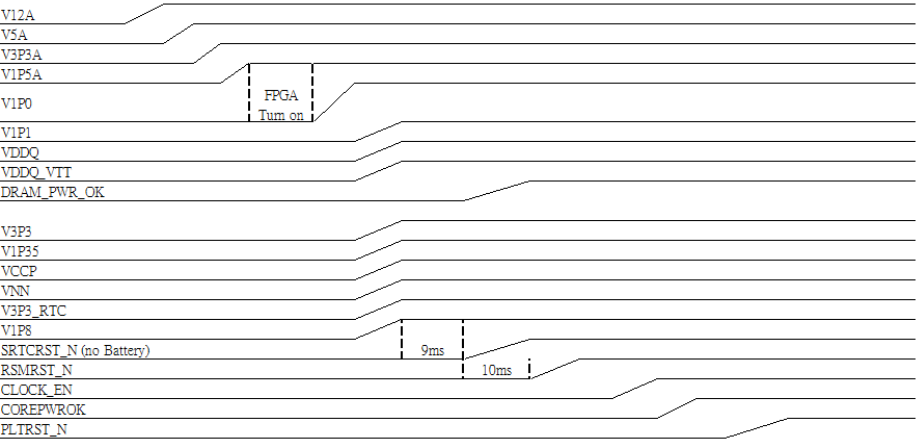




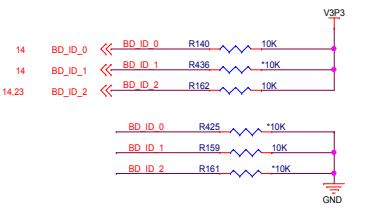






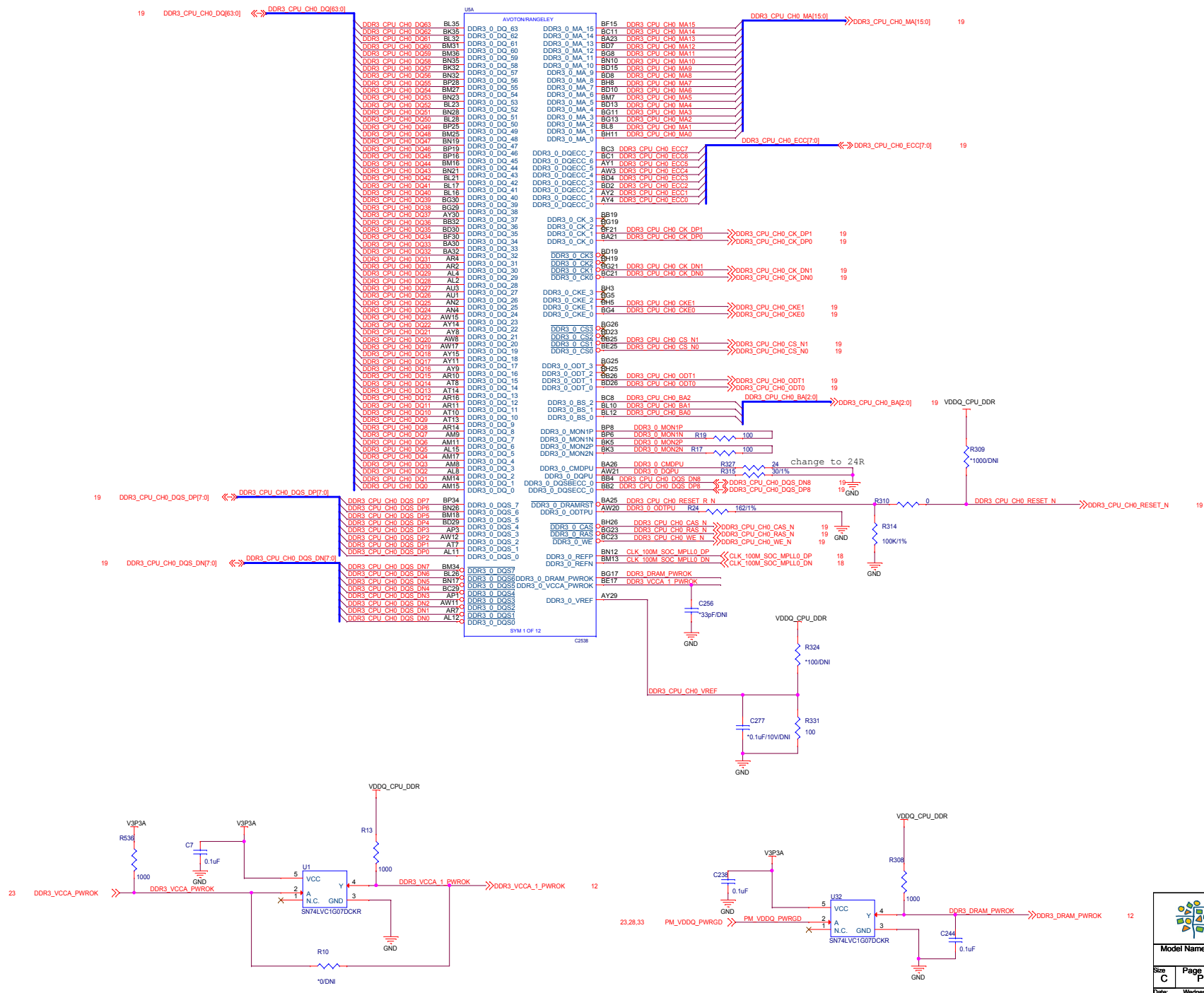


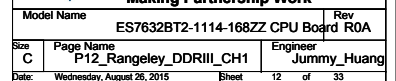
GPIOs	Pin#	Alternate Function	Rangeley Configuration	GPIOs	Pin#	Alternate Function	Rangeley Configuration
GPIO_0	AL56	NMI	Alternate Function	GPIO_SUS0	V66	N/A	ALTA_CFLD_TCK
GPIO_1	AL63	ERROR2_B	Alternate Function	GPIO_SUS1	W54	N/A	ALTA_CFLD_TDI
GPIO_2	AL62	ERROR1_B	Alternate Function	GPIO_SUS2	T53	N/A	BD_ID_2
GPIO_3	AL65	ERROR0_B	Alternate Function	GPIO_SUS3	Y63	CPU_RESET_B	Alternate Function
GPIO_4	AM52	IRERR_B	Alternate Function	GPIO_SUS4	Y57	SUSPWRDNACK	N/A ; pull up
GPIO_5	AL52	MCERR_B	Alternate Function	GPIO_SUS5	AD58	PMU_SUSCLK	N/A
GPIO_6	AG50	UART1_RXD	Alternate Function	GPIO_SUS6	AC52	PMU_SLP_DDRVTI_B	Goes to FPGA, Output
GPIO_7	AH50	UART1_TXD	Alternate Function	GPIO_SUS7	Y50	PMU_SLP_LAN_B	Goes to FPGA, Output
GPIO_8	AN62	SMB_CLK0	Alternate Function	GPIO_SUS8	AD66	PMU_WAKE_B	Alternate Function
GPIO_9	AP62	SMB_DATA0	Alternate Function	GPIO_SUS9	AC49	PMU_PWRBTN_B	Alternate Function
GPIO_10	AL58	SMB_ALRT_N0	Alternate Function	GPIO_SUS10	AB65	SUS_STAT_B	N/A, pull down
GPIO_11	AN63	SMB_DATA1	Goes to Mainboard	GPIO_SUS11	AD63	USB_OC0_B	Alternate Function
GPIO_12	AR63	SMB_CLK1	Goes to Mainboard	GPIO_SUS12	AC58	SPL_CS1_B	Alternate Function
GPIO_13	AN65	SMB_DATA2	UART0_TXD	GPIO_SUS13	W51	GBE_EE_DI	Alternate Function
GPIO_14	AR65	SMB_CLK2	UART0_RXD	GPIO_SUS14	W60	GBE_EE_DO	Alternate Function
GPIO_15	AT63	SATA_GPO	BD_ID_0	GPIO_SUS15	T50	GBE_EE_SK	Alternate Function
GPIO_16	AL49	SATA_LEDN	N/A	GPIO_SUS16	R59	GBE_EE_CS	Alternate Function
GPIO_17	AH51	SATA3_GPO	BD_ID_1	GPIO_SUS17	T58	GBE_SDP0_0	CPLD_INT_L
GPIO_18	AH54	SATA3_LEDN	Alternate Function	GPIO_SUS18	T48	GBE_SDP0_1	CPLD2_INT_L
GPIO_19	AH59	FLEX_CLK_SB0	Alternate Function	GPIO_SUS19	P46	GBE_LED0	N/A, pull down
GPIO_20	AG56	FLEX_CLK_SE1	Alternate Function	GPIO_SUS20	W50	GBE_LED1	N/A, pull down
GPIO_21	AG54	LPC_LAD0	Alternate Function	GPIO_SUS21	P48	GBE_LED2	N/A, pull down
GPIO_22	AM53	LPC_LAD1	Alternate Function	GPIO_SUS22	R58	GBE_LED3	N/A, pull down
GPIO_23	AL53	LPC_LAD2	Alternate Function	GPIO_SUS23	V63	GBE_WOL	N/A, pull down
GPIO_24	AG59	LPC_LAD3	Alternate Function	GPIO_SUS24	W56	GBE_MDIO0_L2C_CLK	MDIO0_CLK
GPIO_25	AH56	LPC_FRAMEB	Alternate Function	GPIO_SUS25	W59	GBE_MDIO0_L2C_DATA	MDIO0_DATA
GPIO_26	AG51	LPC_CLKOUT0	Alternate Function	GPIO_SUS26	Y54	GBE_MDIO1_L2C_CLK	ALTA_CFLD_TDO
GPIO_27	AM49	LPC_CLKOUT1	Alternate Function	GPIO_SUS27	Y53	GBE_MDIO1_L2C_DATA	ALTA_CFLD_TMS
GPIO_28	AH48	LPC_CLKRUNB	Alternate Function				
GPIO_29	AT50	ILE_SERIRQ	Alternate Function				
GPIO_30	AM58	PMU_RESETBUTTON_B	Alternate Function				

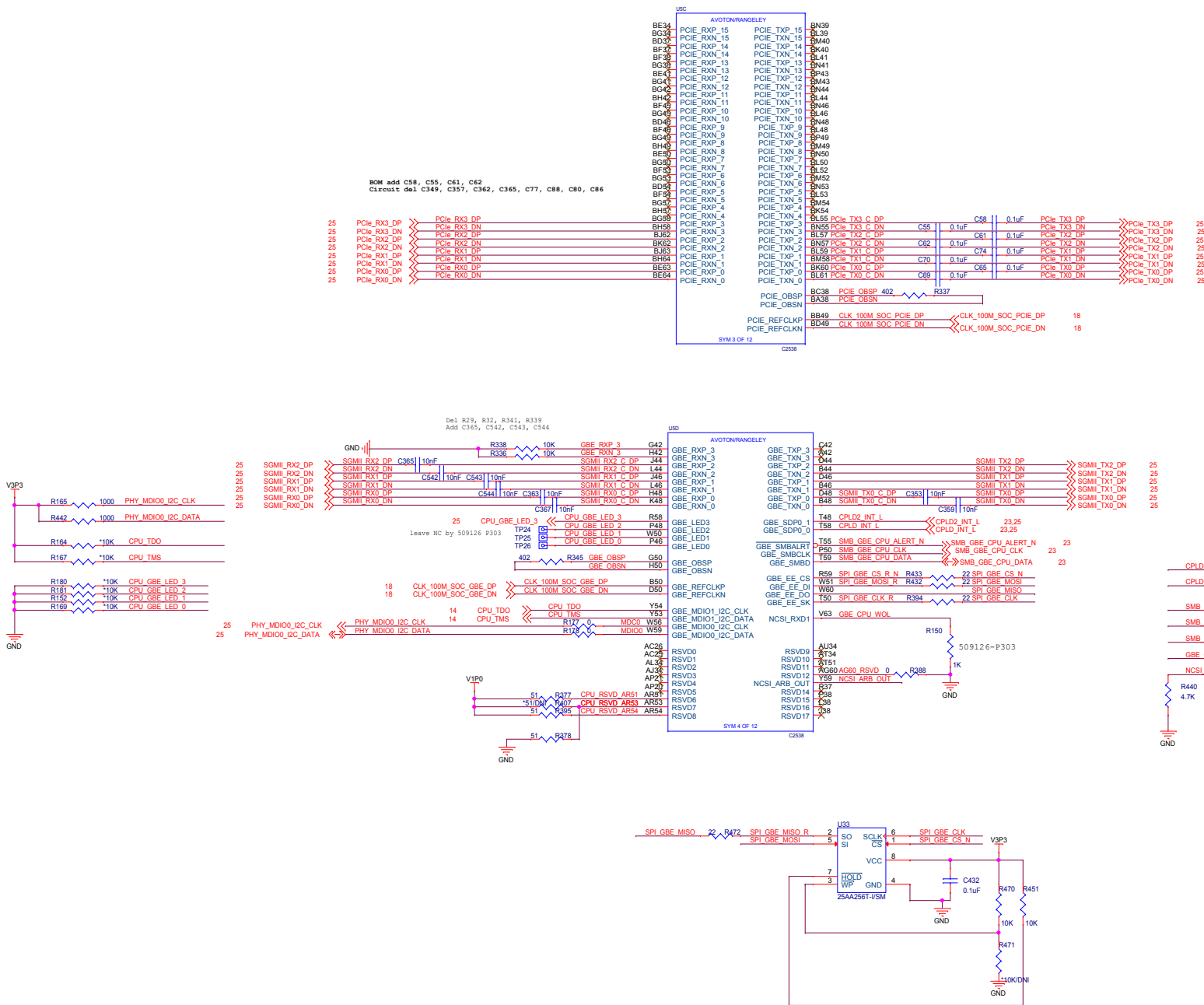


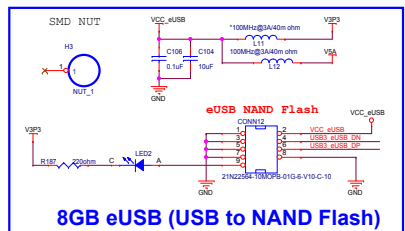
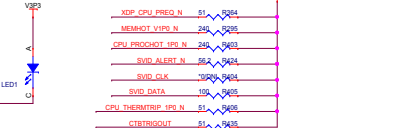
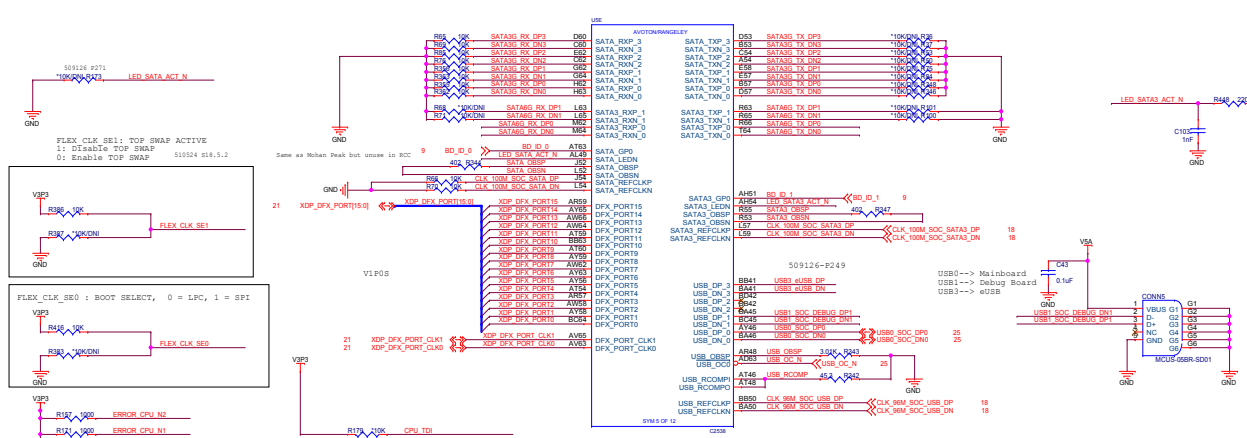
Board assignments			
BD_ID_2	BD_ID_1	BD_ID_0	Board Type
0	0	0	Lyon Peak SV
0	0	1	Lyon Peak BDV
0	1	0	Lyon Peak PPV
1	0	0	Mohon Peak
1	0	1	Intel Project 2
1	1	0	Tiger Cove

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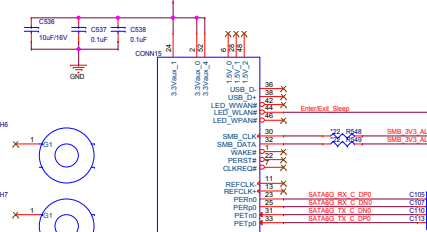
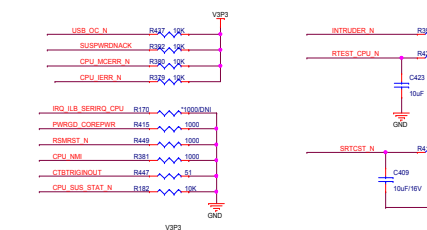
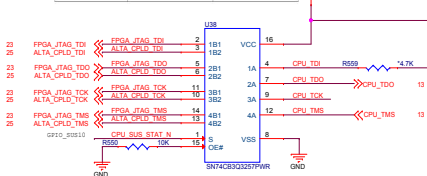
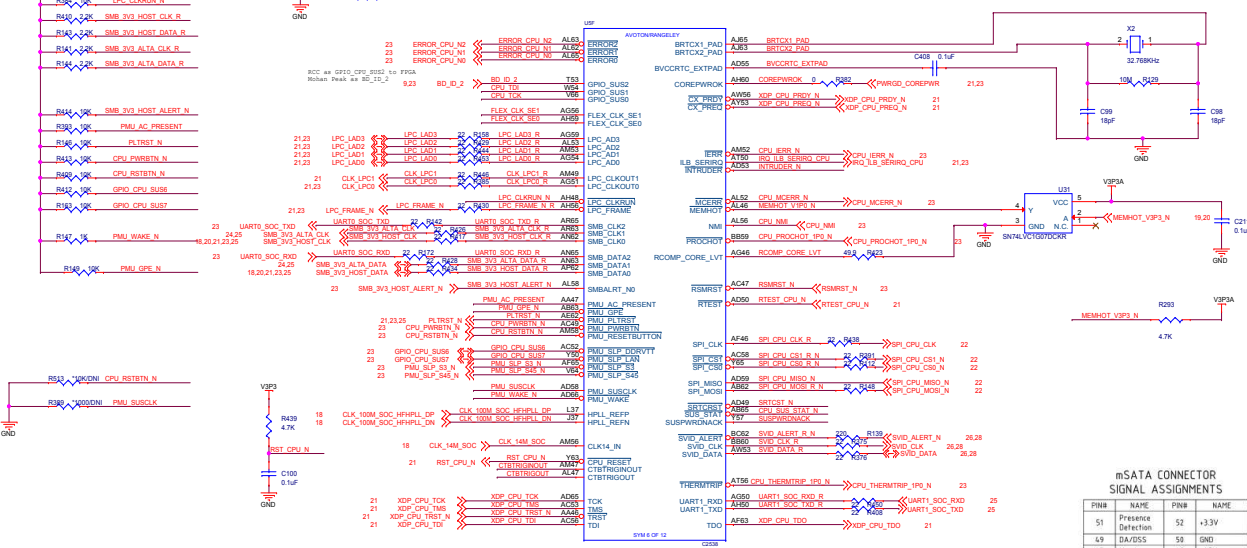




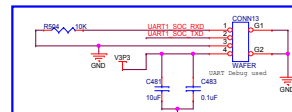
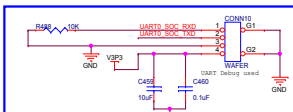




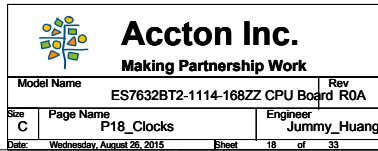
INPUTS		INPUT/OUTPUT	FUNCTION
OE	S	A	
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

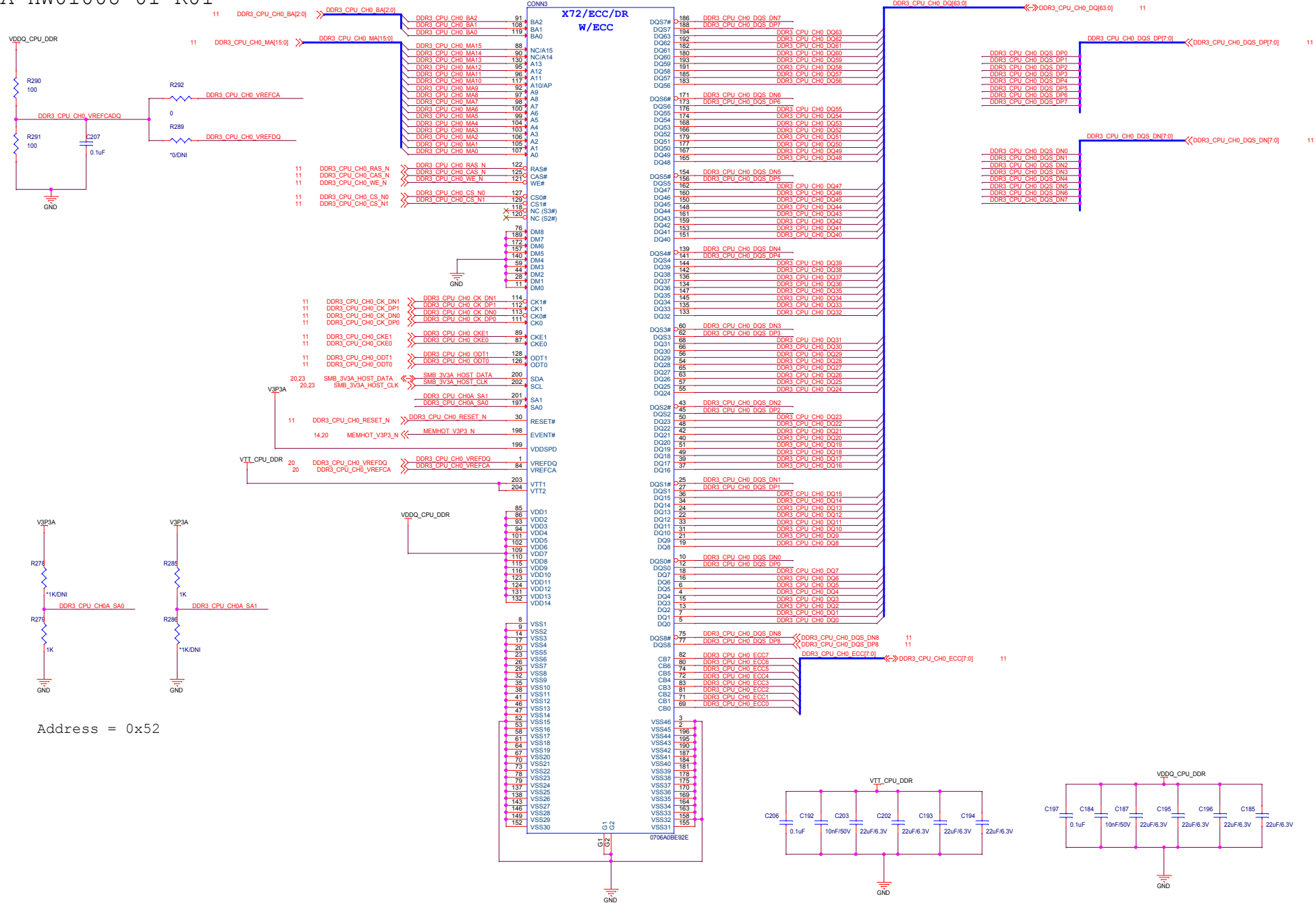


mSATA CONNECTOR SIGNAL ASSIGNMENTS			
Pin#	NAME	Pin#	NAME
51	Presence Detection	52	+3.3V
49	DA/PESS	50	GND
47	Vendor	48	+1.5V
45	Vendor	46	Reserved
43	No Connect	44	Reserved
41	+3.3V	42	Reserved
39	+3.3V	38	Reserved
35	GND	36	GND
33	+A	34	GND
31	-A	32	Two Wire Interface
29	GND	30	Two Wire Interface
27	GND	28	+1.5V
25	-B	26	GND
23	+B	24	+3.3V
21	GND	22	Reserved
19	Reserved	20	Reserved
17	Reserved	18	GND
MECHANICAL KEY			
15	GND	16	Reserved
13	Reserved	12	Reserved
11	Reserved	10	Reserved
9	GND	10	Reserved
7	Reserved	8	Reserved
5	Reserved	6	+1.5V
3	Reserved	4	Reserved
1	Reserved	2	+3.3V







$$H=9.2\text{mm}$$


Address = 0x52



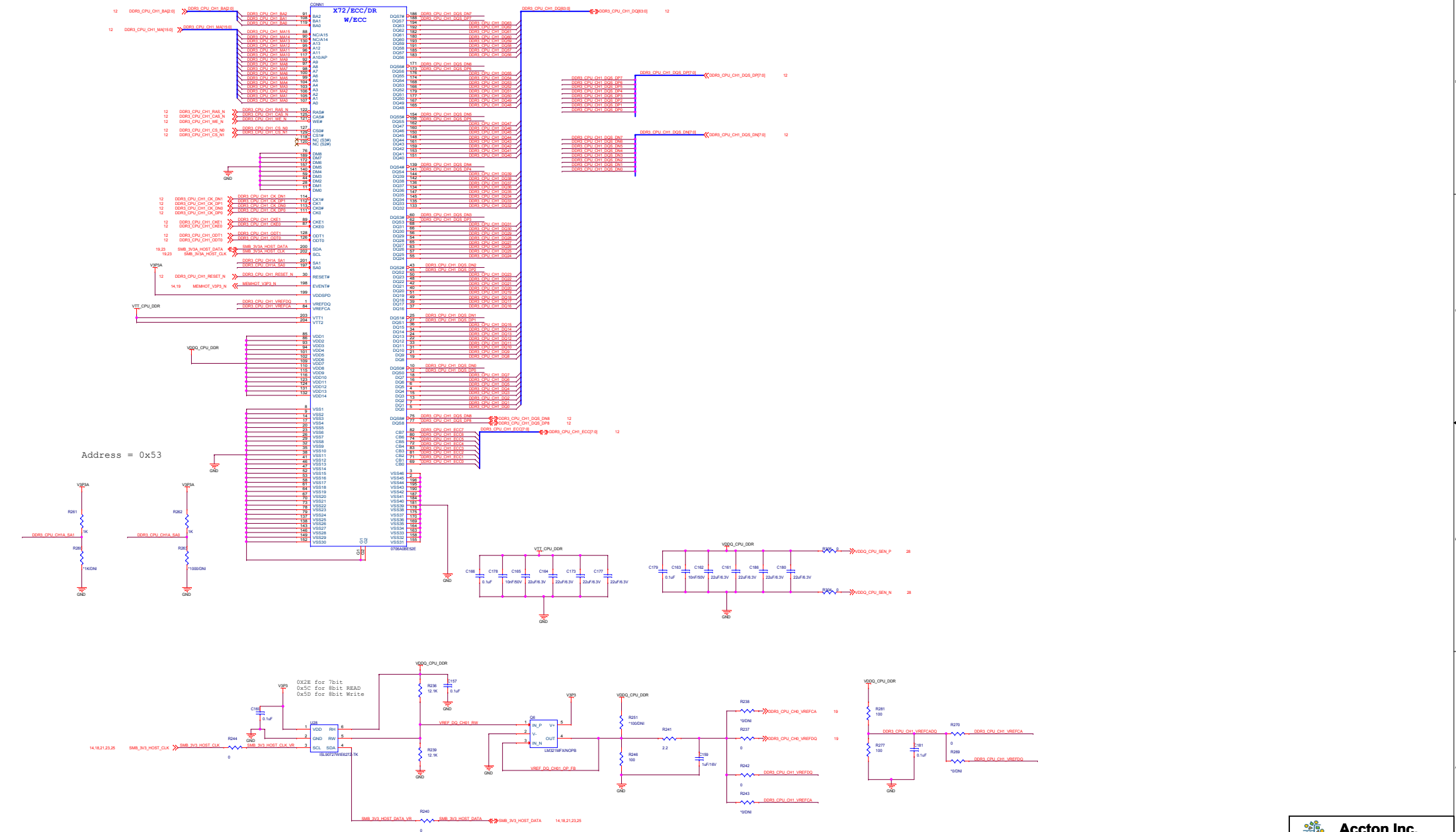
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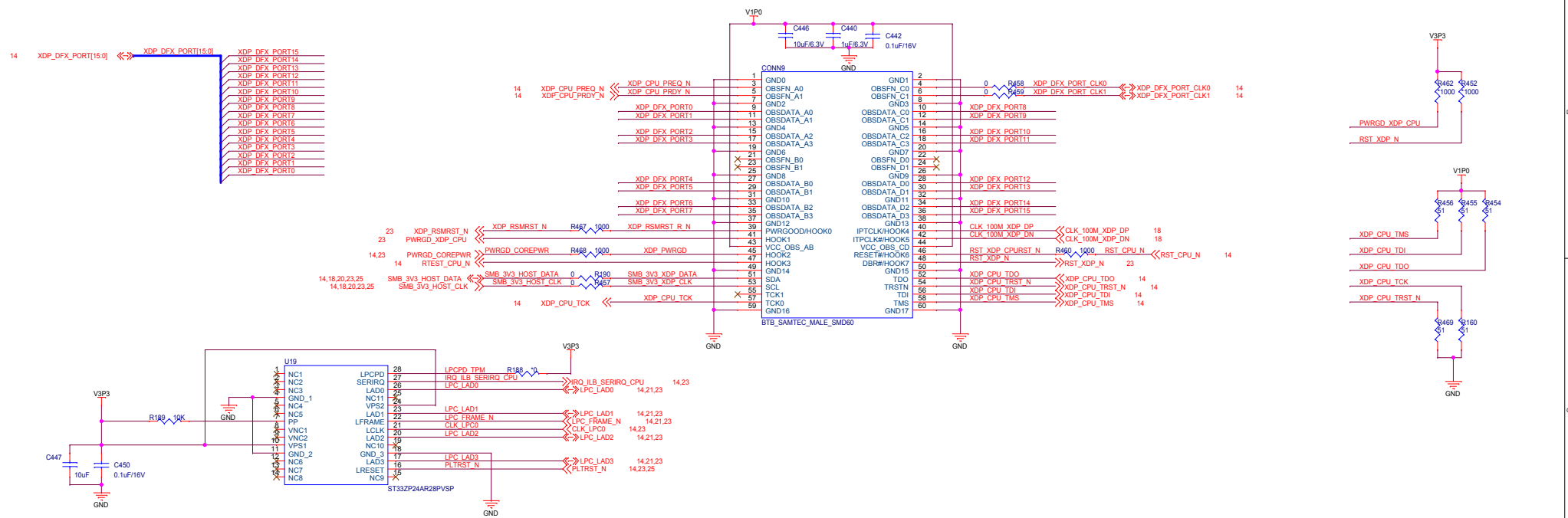
Model Name	ES7632BT2-1114-168ZZ CPU Board R0A	Rev	
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Size C	Page Name P19_DDR3 SODIMM_CH0	Engineer Jummy_Huang
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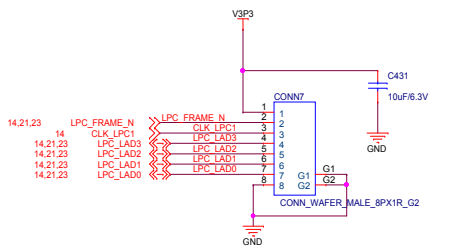
Date: Wednesday, August 26, 2015 Sheet 19 of 33

H = 5.2mm

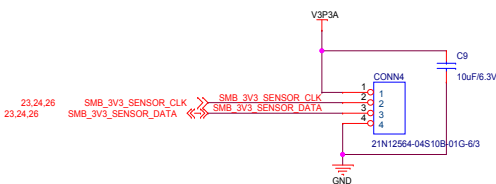


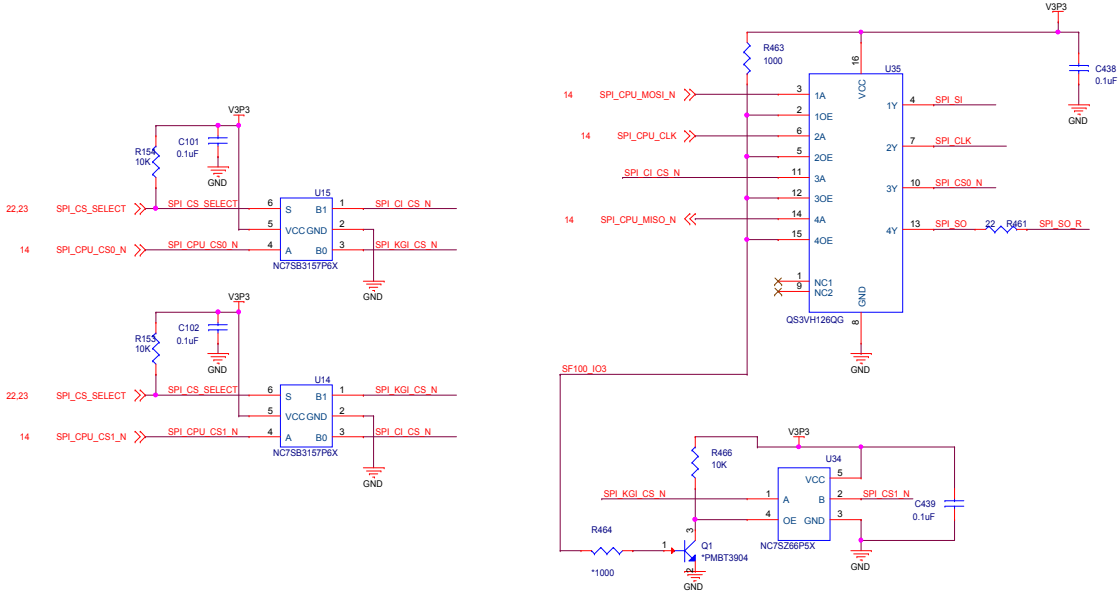
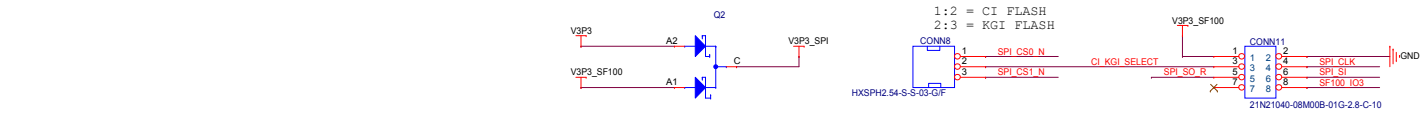


Port 80 Debug Header
Use LPC decoder board

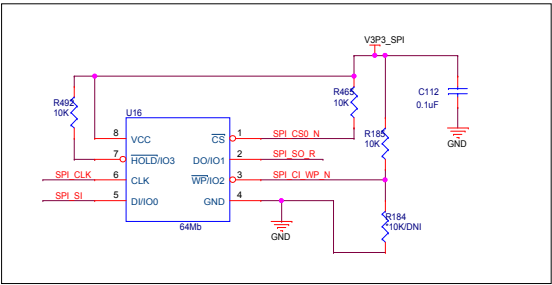


Port 80 Debug Header
Use I2C bus to connector HW debug board

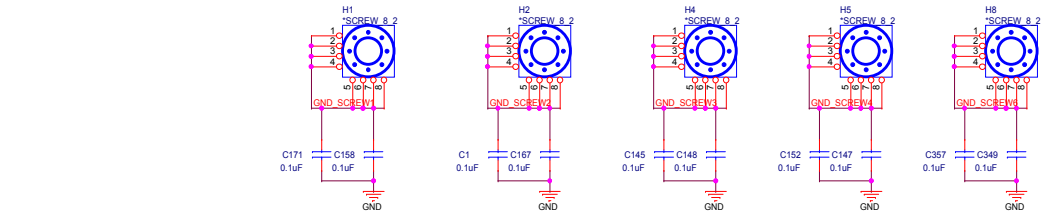
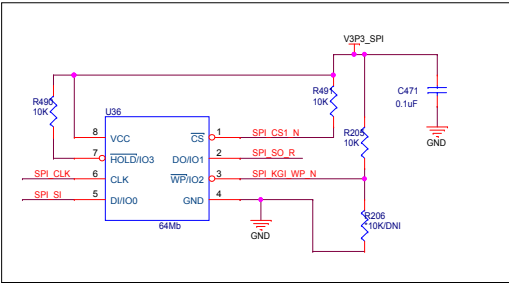




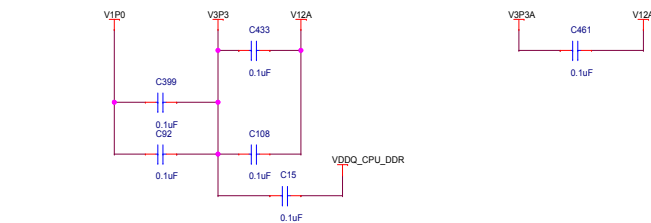
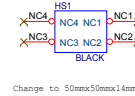
SPI CI Flash

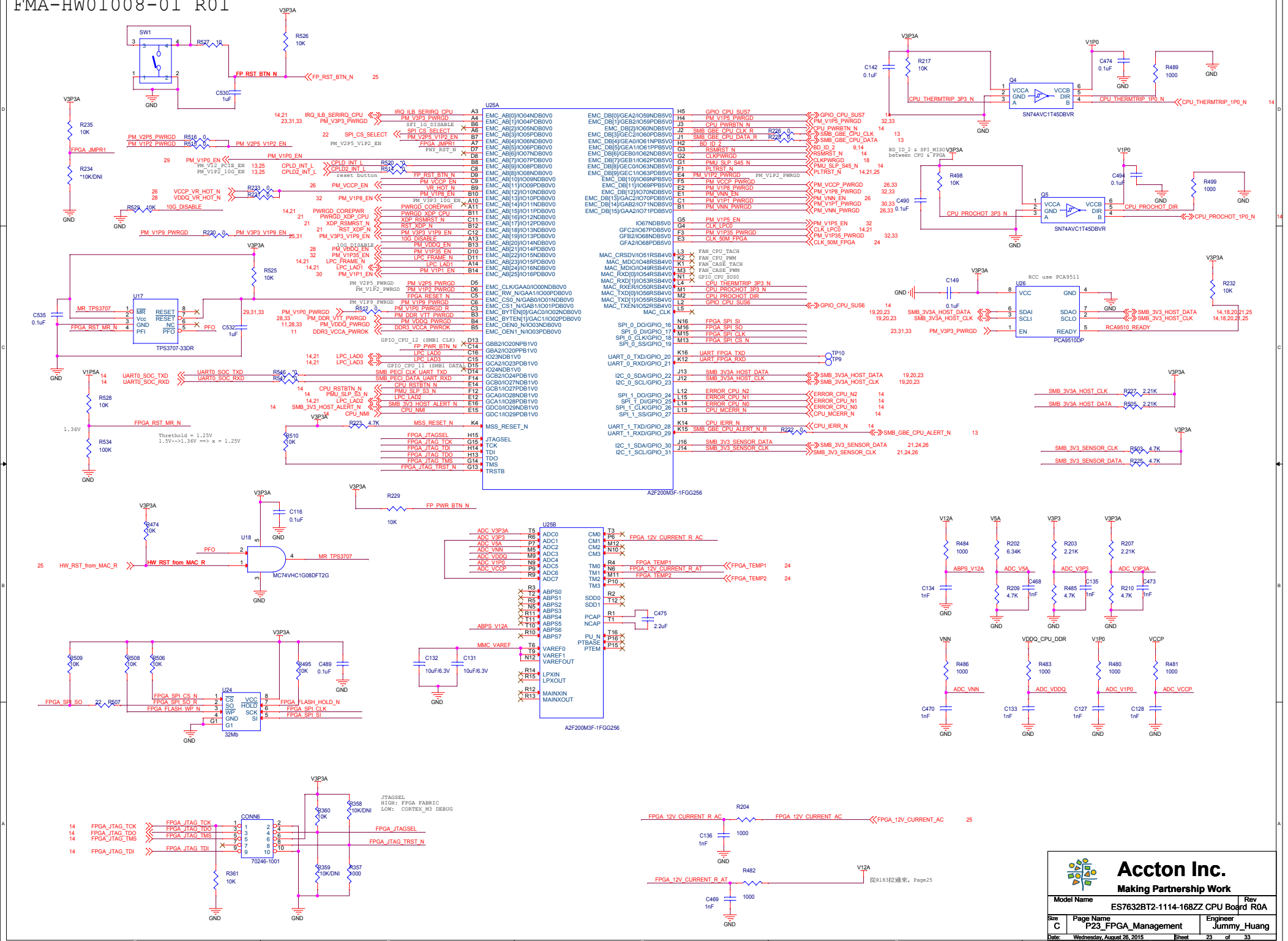


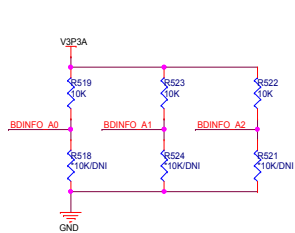
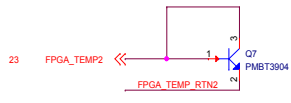
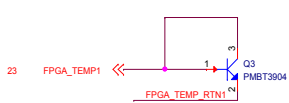
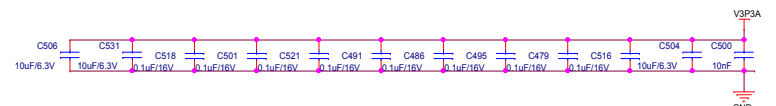
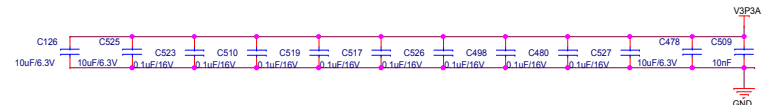
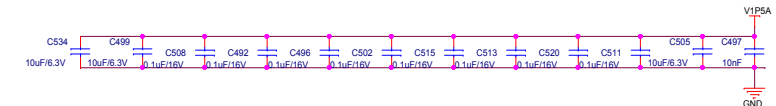
SPI KGI Flash



CPU Heatsink





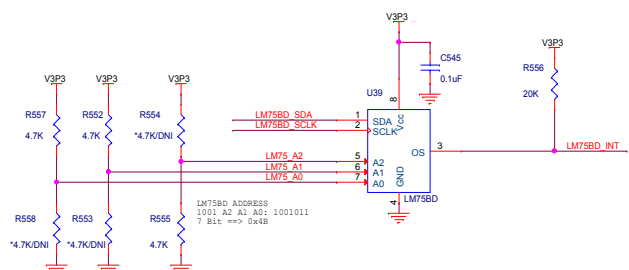
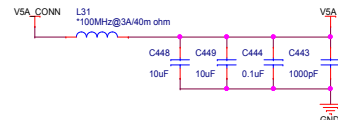
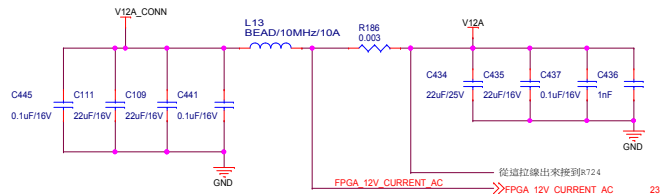
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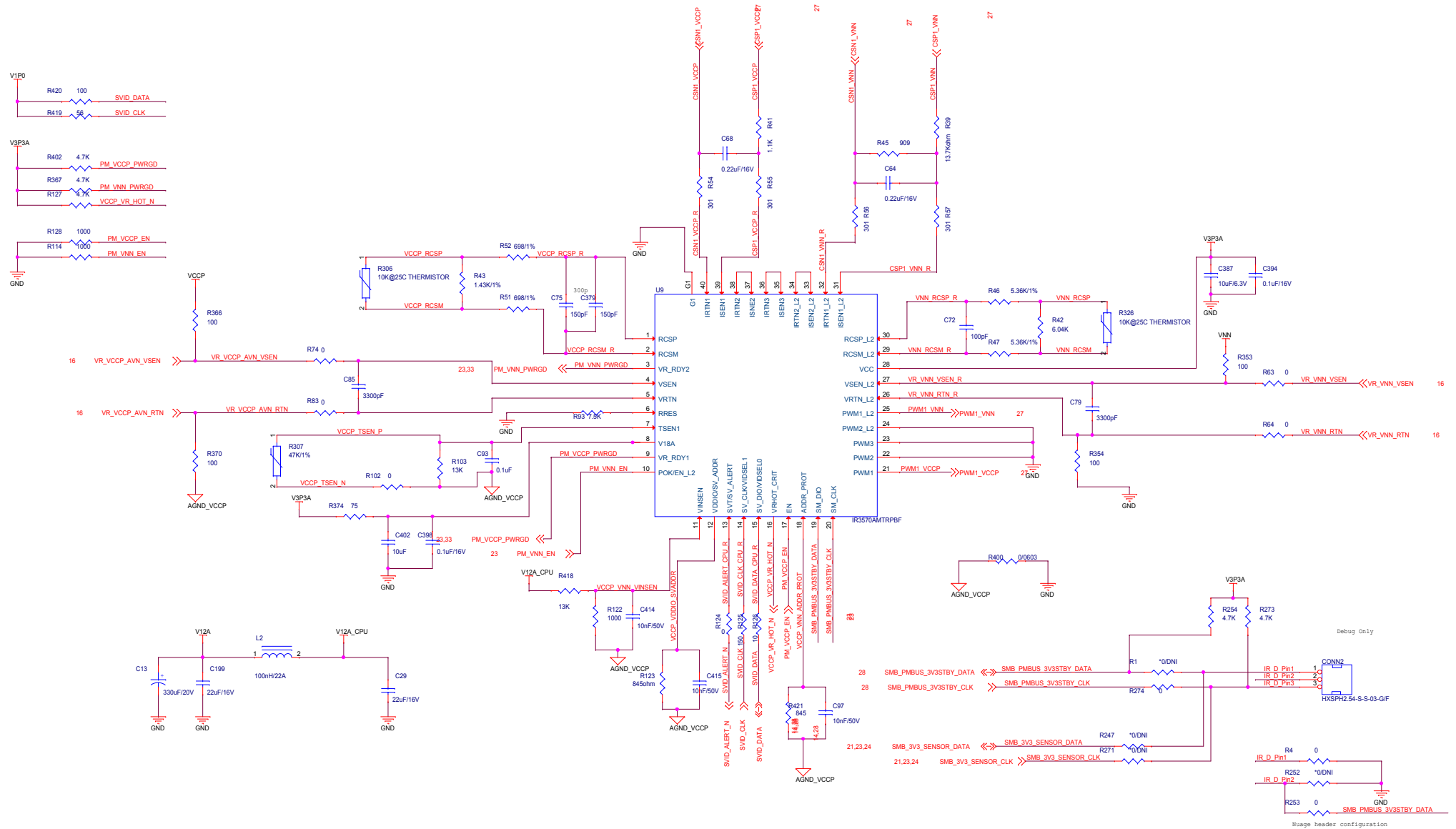
		P13_Rangeley_PCIe, GBE	
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13	SGMII_TX0_DN	>>	SGMII_TX0_DN
13	SGMII_TX1_DP	>>	SGMII_TX1_DP
13	SGMII_TX1_DN	>>	SGMII_TX1_DN
13	SGMII_TX2_DP	>>	SGMII_TX2_DP
13	SGMII_TX2_DN	>>	SGMII_TX2_DN
13	SGMII_RX0_DP	>>	SGMII_RX0_DP
13	SGMII_RX0_DN	>>	SGMII_RX0_DN
13	SGMII_RX1_DP	>>	SGMII_RX1_DP
13	SGMII_RX1_DN	>>	SGMII_RX1_DN
13	SGMII_RX2_DP	>>	SGMII_RX2_DP
13	SGMII_RX2_DN	>>	SGMII_RX2_DN
13	PCIe_TX0_DP	>>	PCIe_TX0_DP
13	PCIe_TX0_DN	>>	PCIe_TX0_DN
13	PCIe_TX1_DP	>>	PCIe_TX1_DP
13	PCIe_TX1_DN	>>	PCIe_TX1_DN
13	PCIe_TX2_DP	>>	PCIe_TX2_DP
13	PCIe_TX2_DN	>>	PCIe_TX2_DN
13	PCIe_TX3_DP	>>	PCIe_TX3_DP
13	PCIe_TX3_DN	>>	PCIe_TX3_DN
13	PCIe_RX0_DP	>>	PCIe_RX0_DP
13	PCIe_RX0_DN	>>	PCIe_RX0_DN
13	PCIe_RX1_DP	>>	PCIe_RX1_DP
13	PCIe_RX1_DN	>>	PCIe_RX1_DN
13	PCIe_RX2_DP	>>	PCIe_RX2_DP
13	PCIe_RX2_DN	>>	PCIe_RX2_DP
13	PCIe_RX3_DP	>>	PCIe_RX3_DP
13	PCIe_RX3_DN	>>	PCIe_RX3_DP
13	PHY_MDIO0_02C_CLK	>>	PHY_MDIO0_02C_CLK
13	PHY_MDIO0_02C_DATA	>>	PHY_MDIO0_02C_DATA
13	CPD0_INT_L	>>	CPD0_INT_L
13	CPD0_INT_U	>>	CPD0_INT_U
13	CPD0_GBE_LED_3	>>	CPD0_GBE_LED_3

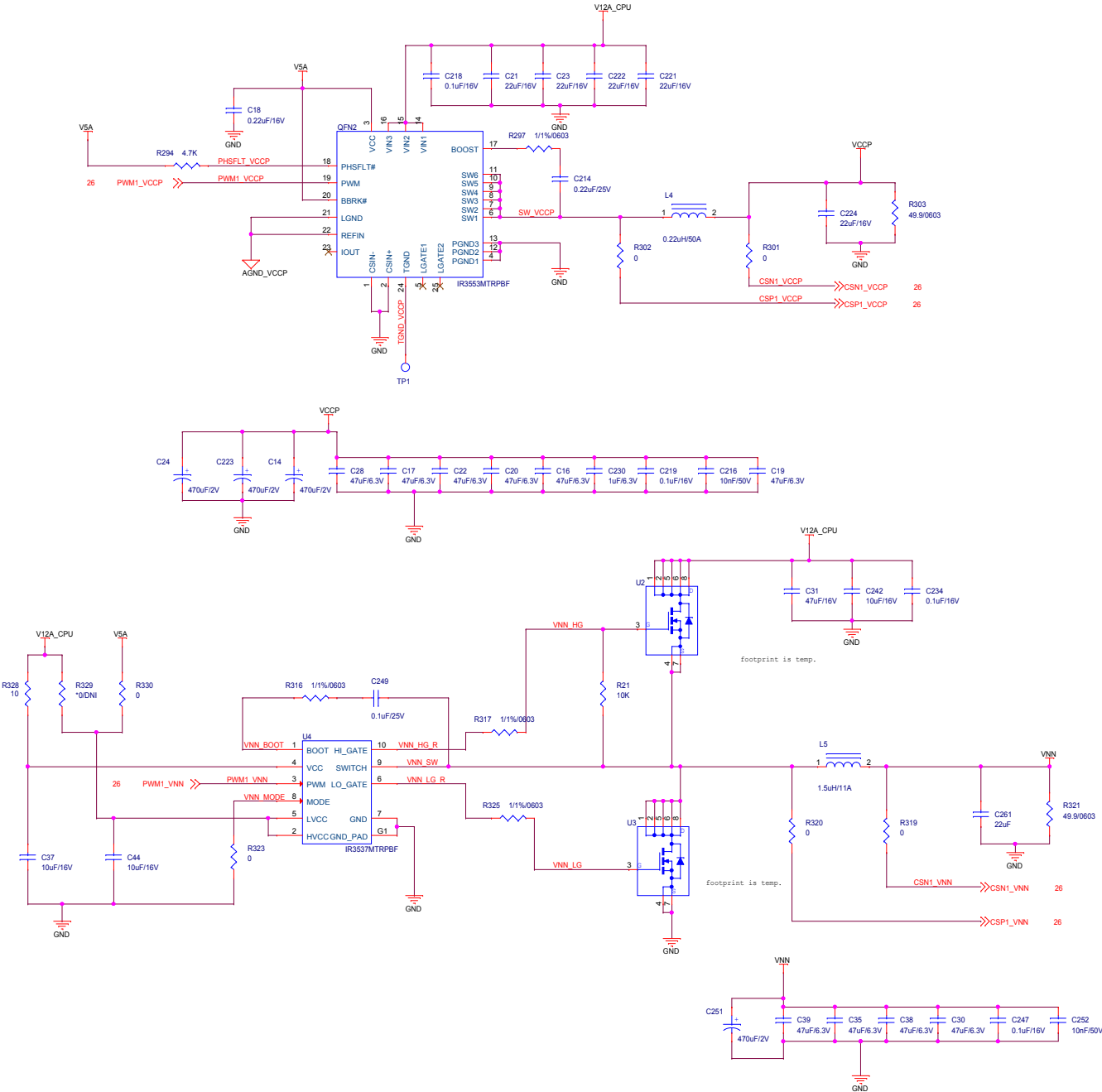
P14_RangeIO SATA,USB,MISC			
14,18,20,21,23	SMB_3V3_HOST_CLK	↔	SMB_3V3_HOST_CLK
18,20,21,23	SMB_3V3_HOST_DATA	↔	SMB_3V3_HOST_DATA
14,24	SMB_3V3_ALTA_CLK	↔	SMB_3V3_ALTA_CLK
14,24	SMB_3V3_ALTA_DATA	↔	SMB_3V3_ALTA_DATA
14	USBD_S0C_DPO	↔	USBD_S0C_DPO
14	USBD_S0C_DWI	↔	USBD_S0C_DWI
14	UART1_S0C_TXD	↔	UART1_S0C_TXD
14	UART1_S0C_RXD	↔	UART1_S0C_RXD
14	ALTA_CPLD_T0I	↔	ALTA_CPLD_T0I
14	ALTA_CPLD_T0K	↔	ALTA_CPLD_T0K
14	ALTA_CPLD_T0L	↔	ALTA_CPLD_T0L
14	ALTA_CPLD_T0M	↔	ALTA_CPLD_T0M
14,21,23	PLTRST_N	↔	PLTRST_N
14	USB_OC_N	↔	USB_OC_N

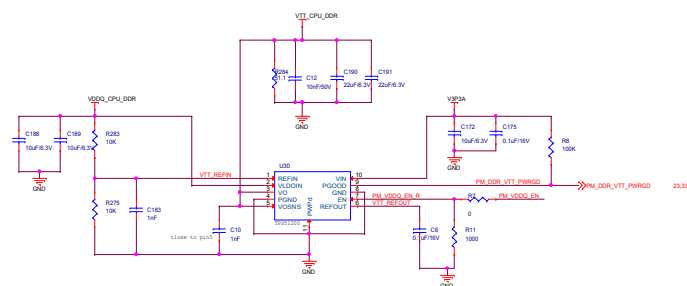
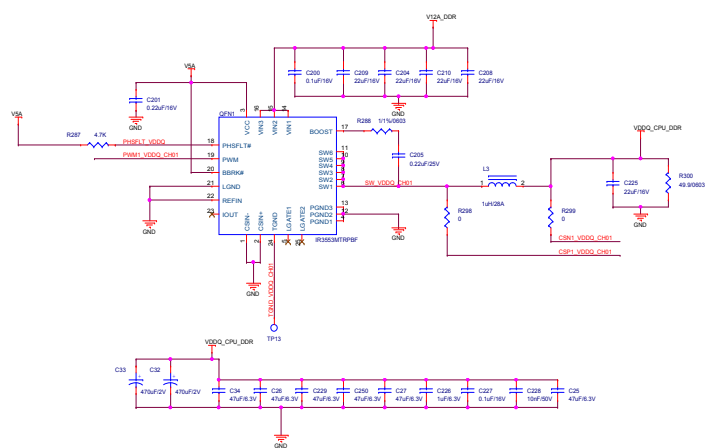
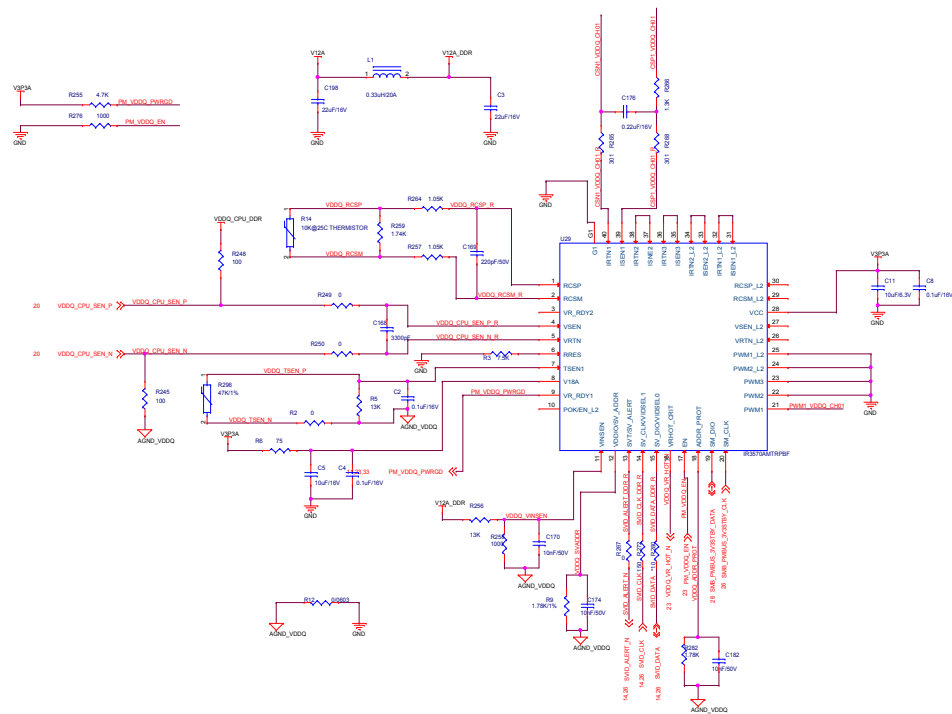
P24_FPGA_Management

23,31	PM_V3P3_V1P9_EN	>>	PM_V3P3_V1P9_EN
23	HW_RST_from_MAC_R	<<	HW_RST_from_MAC_R
23	FP_RST_BTN_N	<<	FP_RST_BTN_N

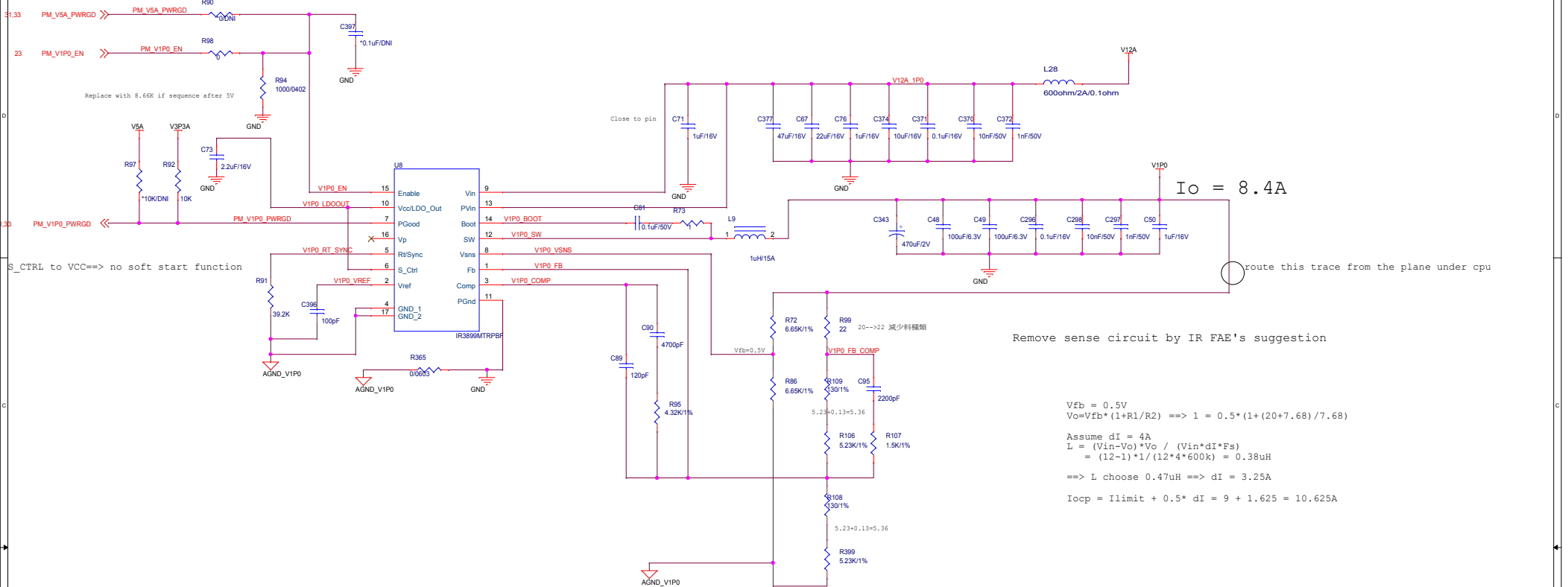


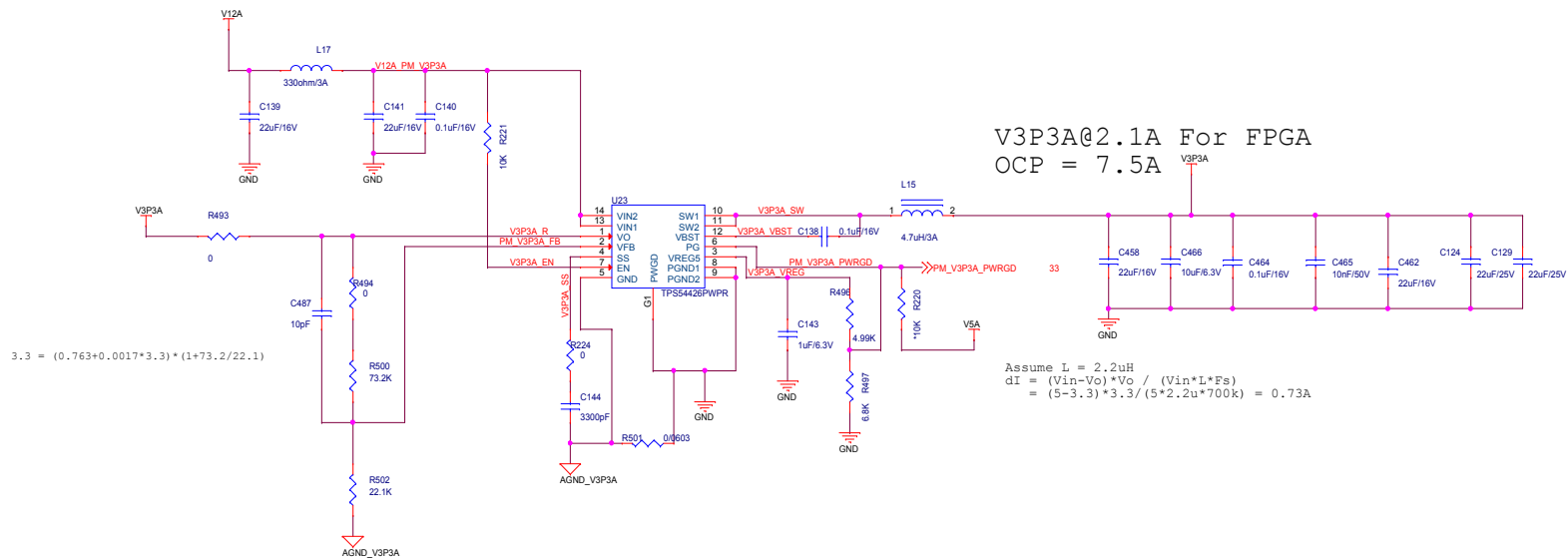
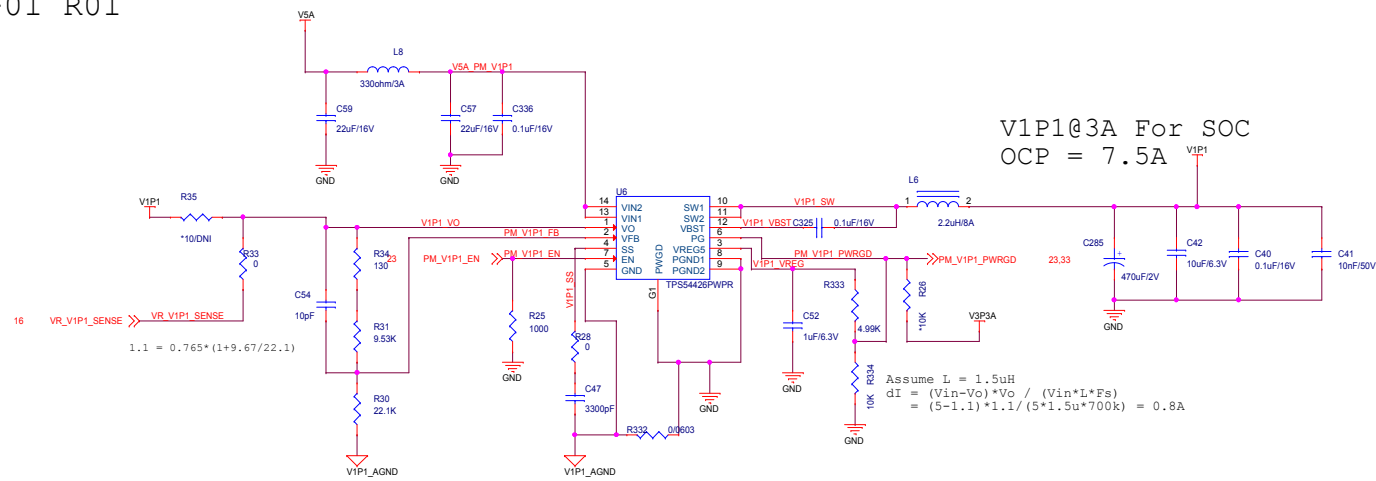






FMA-HW01008-01 R01

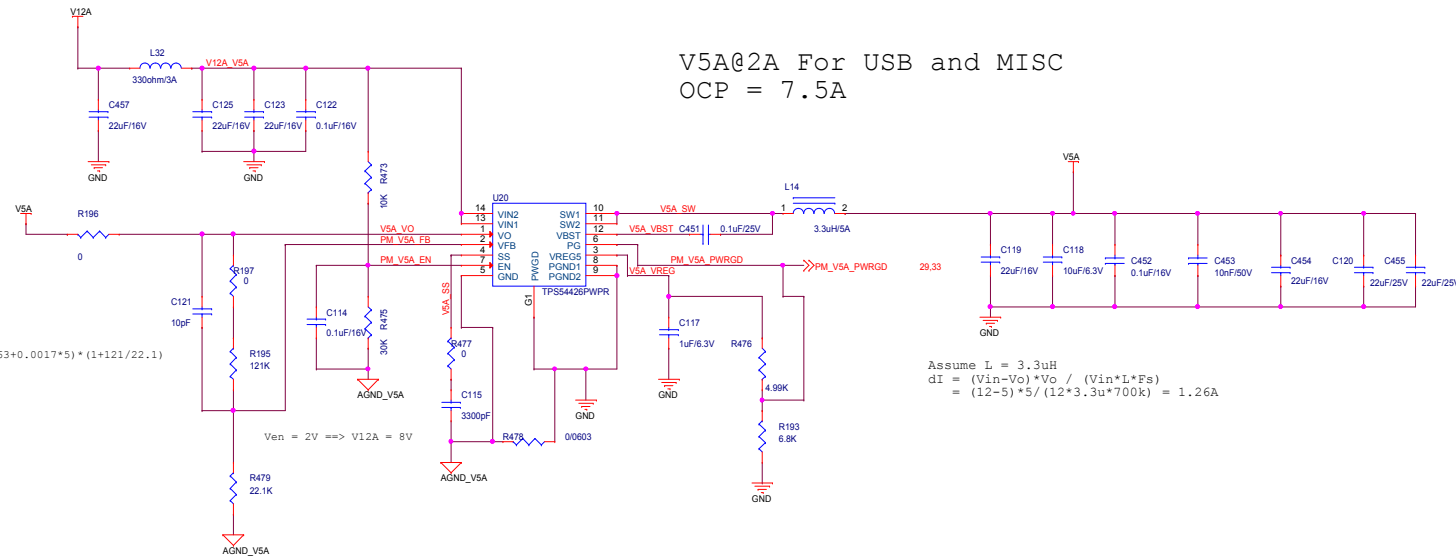




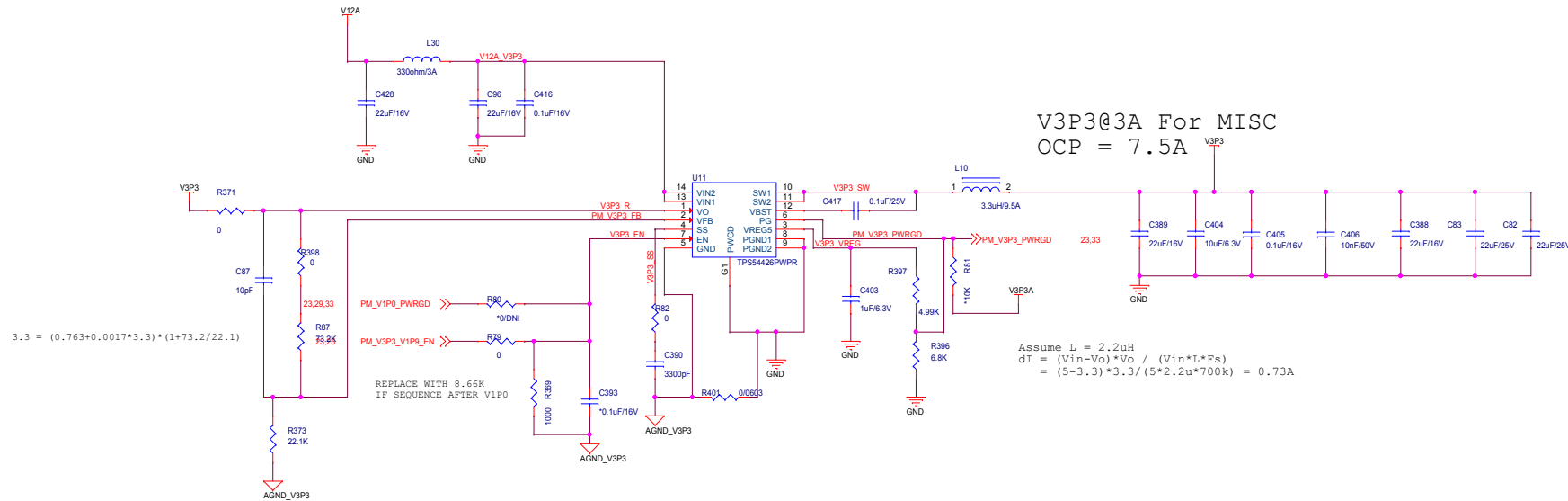
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Size	Page Name	P30_V3P3A_V1P1	Engineer
C			Jummy_Huang
Date: Wednesday, August 26, 2015		Sheet	30 of 33

V5A@2A For USB and MISC OCP = 7.5A

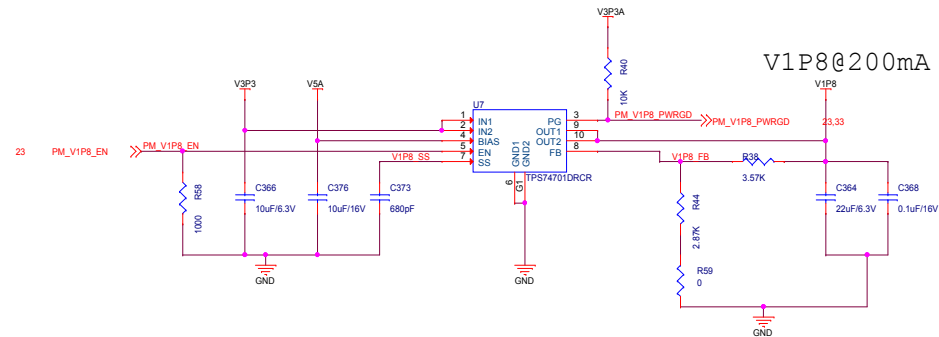


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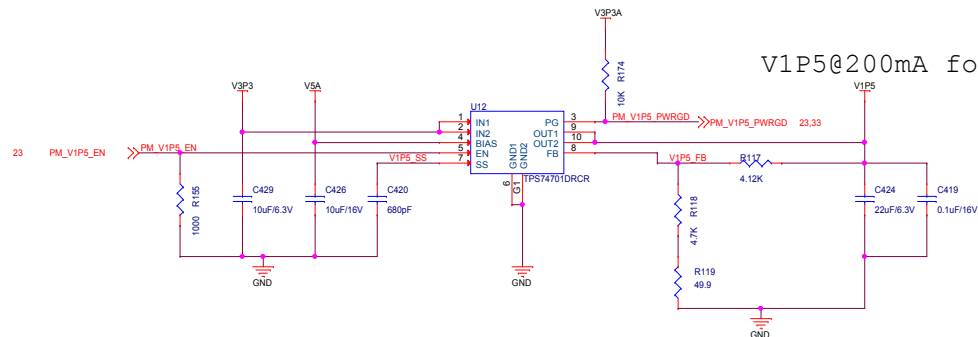


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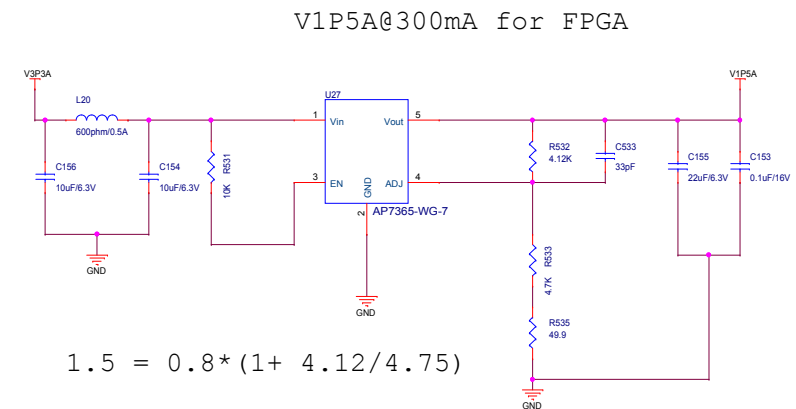
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ES7632BT2-1114-168ZZ CPU Board R0A		
Size	Page Name	Engineer
C	P31_V5A_V3P3	Jummy_Huang
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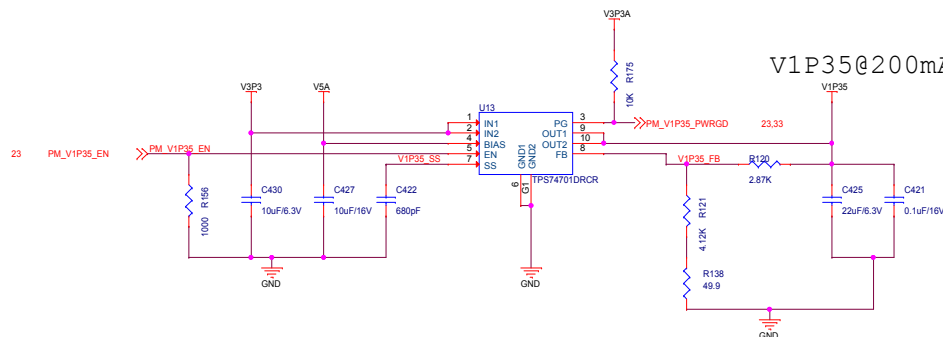
$$1.8 = 0.8 * (1 + 3.57/2.87)$$



$$1.5 = 0.8 * (1 + 4.12/4.75)$$



$$1.5 = 0.8 * (1 + 4.12/4.75)$$



$$1.35 = 0.8 * (1 + 2.87/4.12)$$

- Sequence
- 1. V5A / V3P3A
 - 2. V1P5A
 - 3. V1P0
 - 4. V1P1 / VDDQ/VTT...else power

