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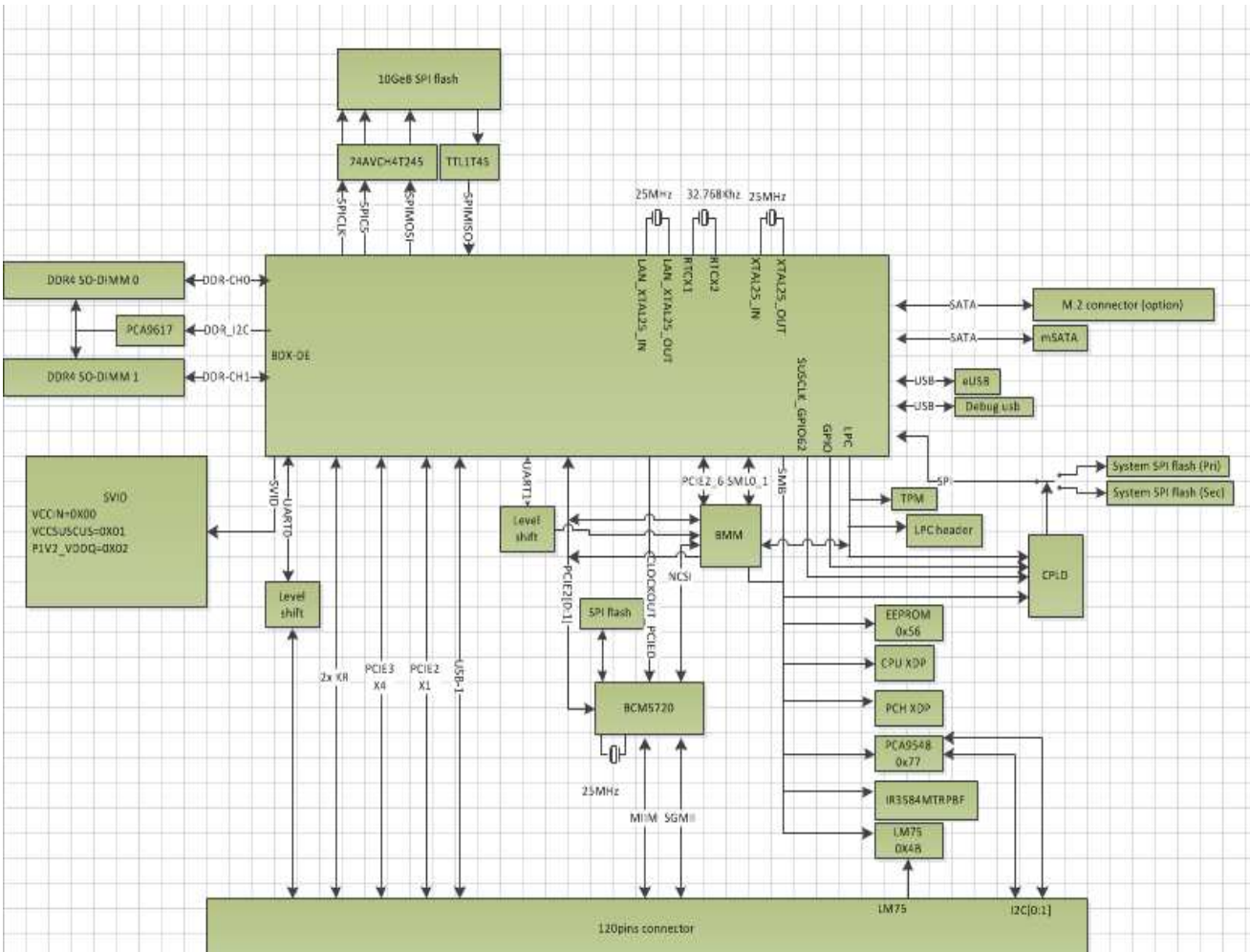
Model Name		Rev	
BDX-DE CPU Board		R0B	
Size	Page Name	Engineer	
C	01_History	Forbidian Kuo	
Date:	Wednesday, July 15, 2015	Sheet	1 of 39

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Model Name		Rev
BDX-DE CPU Board		R0B
Size	Page Name	Engineer
C	02_Index	Forbidian Kuo
Date: Wednesday, July 15, 2015		Sheet 2 of 39



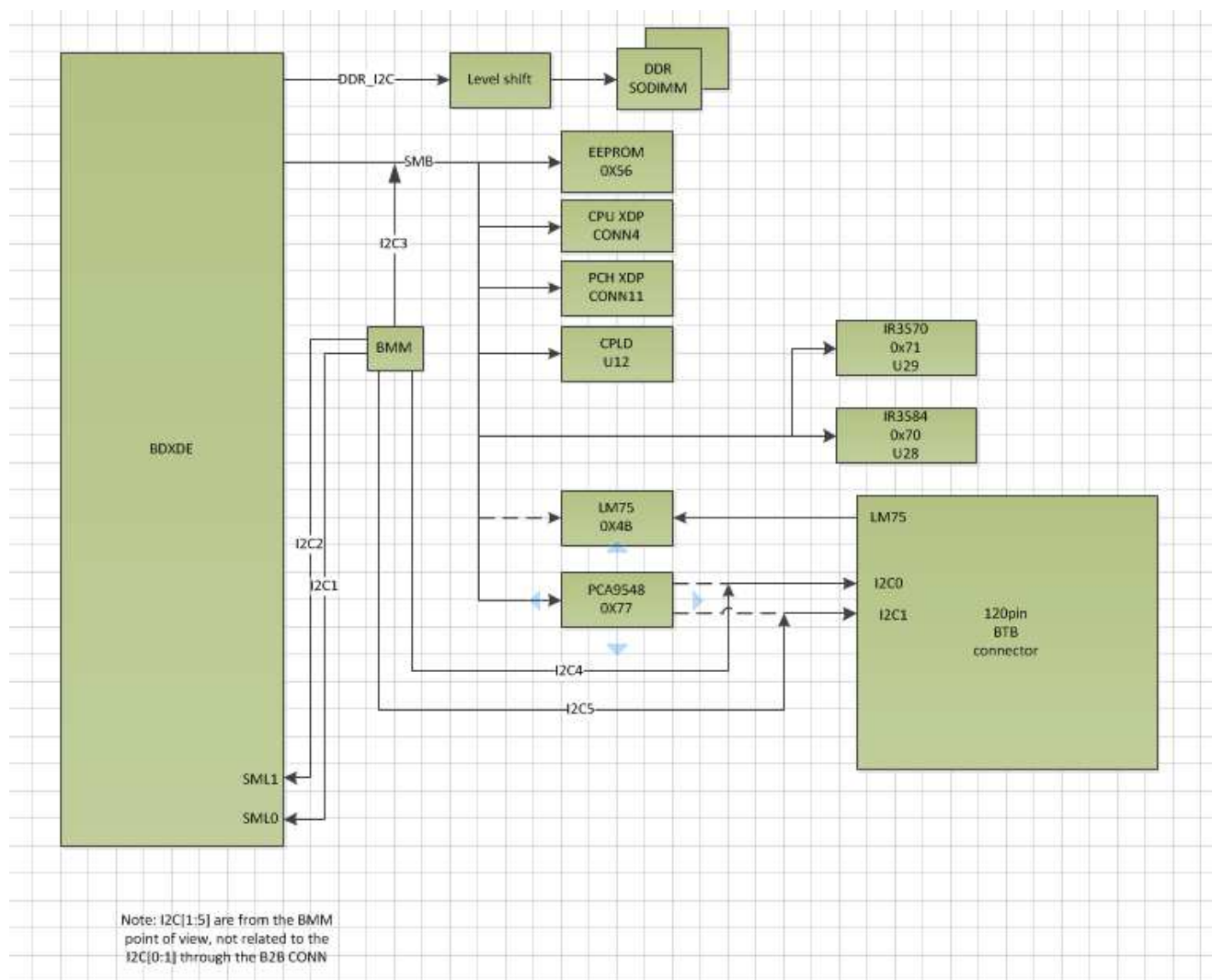
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Model Name		BDX-DE CPU Board	Rev	R0B
Size	Page Name	03_Block Diagram		
C		Engineer		
		Forbidian Kuo		
Date		Wednesday, July 15, 2015	Sheet	3 of 39



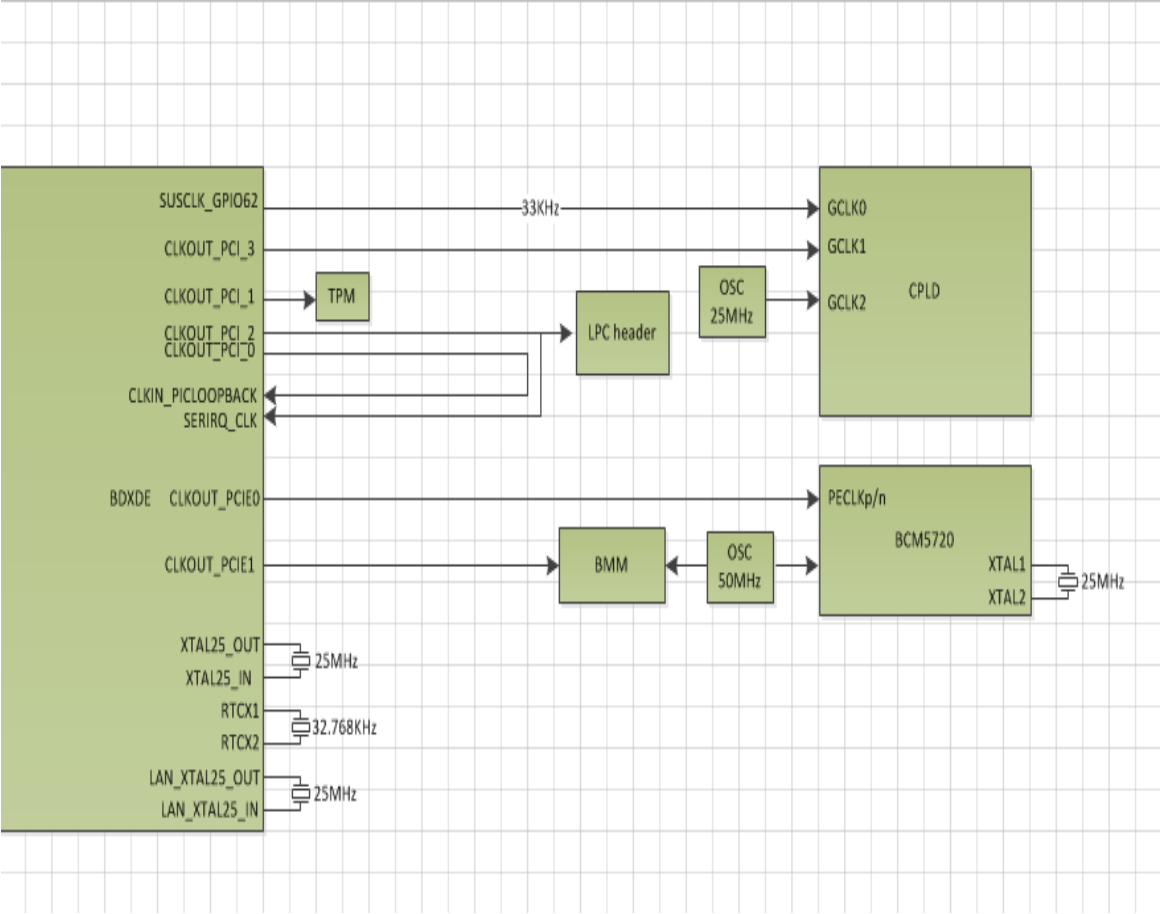
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Model Name		BDX-DE CPU Board	Rev	R0B
Size	Page Name	Engineer		
C	04_SMBUS	Forbidian Kuo		
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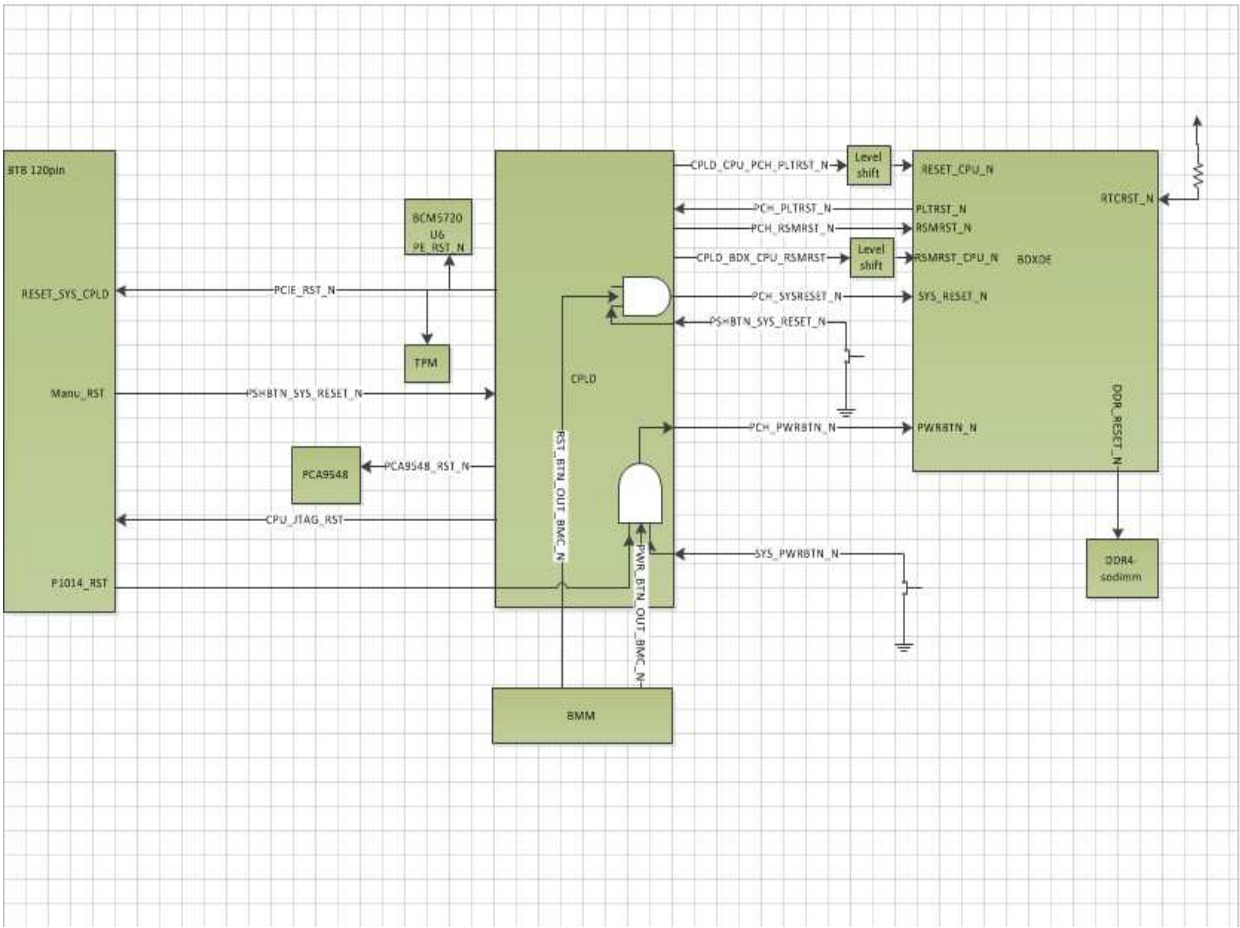
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Model Name		Rev
BDX-DE CPU Board		R0B
Size	Page Name	Engineer
C	05_Clock	Forbidian Kuo
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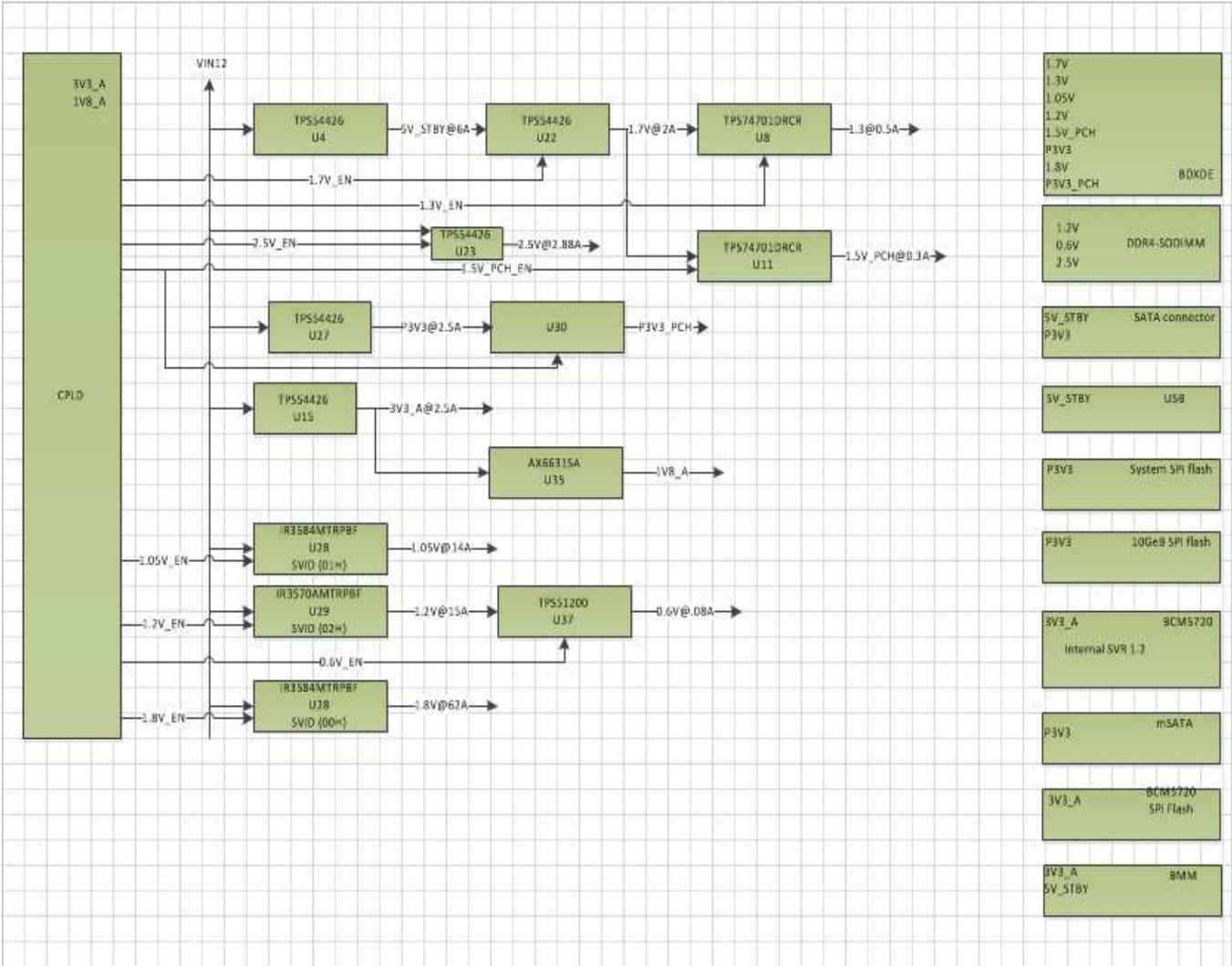
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Model Name				Rev	
BDX-DE CPU Board				R0B	
Size	Page Name			Engineer	
C	06_RESET			Forbidian Kuo	
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Model Name		BDX-DE CPU Board	Rev	R0B
Size	C	Page Name	07_Power	Engineer
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Grangeville / TBC

CPLD

P3V3_A

CPLD checks 12V good

Standby rails

PSV_STBY

P3V3_STBY

10mS

Assert DPWROK

1mS

Assert APWROK

South Complex

VCCSCFUSESUS

VCCIOIN

VCCKRHV

VCCG8E

VCCSCSUS

10mS

Assert SC_PWRGD

10uS

Assert CPU_RSMRST

SLP_54 transitions high

Memory

DDR4_VPP

P1V2_VDDQ

Camelback Mountain

CPLD

P3V3_A

CPLD Checks 12V good

Standby rails

PSV_STBY

P3V3 (only standby rails come up)

10mS

Assert DPWROK

1mS

Assert APWROK

South Complex

VCCSCFUSESUS

P1V05

VCCKRHV

—Connected to P1V05

—Connected to P1V05

10mS

Assert SC_PWRGD

10uS

Assert CPU_RSMRST

Camelback Mountain does not monitor SLP sig.

Memory

DDR4_VPP

P1V2_VDDQ

P0V6_VTT_DIMM

PCH Core

P1V05_PROC_IO

P1V5_PCH

P3V3

CPU Core

VCCIN

Assert PCH_PWROK

1mS

Assert DRAM_PWROK

Assert SYS_PWRGD to PCH

PCH drives CPU_PWRGD_PCH to CPU

P0V6_VTT_DIMM

PCH Core

P1V05 comes up (ABOVE)

P1V5_PCH

P3V3_PCH – switched version of P3V3

CPU Core

VCCIN

Assert PCH_PWROK

1mS

Assert DRAM_PWROK

Assert SYS_PWRGD to PCH

PCH Drives CPU_PWRGD_PCH

BroadWell_STRAP

SIGNAL	VALUE	Note
LGSPARE4_DDR_STRAP	0	DDR3
	1	DDR4 (Default) ,IPU
PU_TXT_PLTEN	0	The platform is Intel TXT (Default) ,IPU to 1.05
	1	The platform is not Intel TXT
PU_TXT_AGENT	0	The socket is the Intel TXT Agent (default) ,IPD
	1	The socket is not the Intel TXT Agent
ADR_STATUS_CLR	0	Disable Intel ME Crypto Transport Layer Security cipher suite (with confidentiality)
	1	Enable Intel ME Crypto Transport Layer Security cipher suite (with confidentiality)
MANF_MODE_STRAP	0	Enable security measures defined in the Flash Descriptor (Default, IPD)
	1	Disable Flash Descriptor Security
BDX_INTVRMEN	0	DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source
	1	Integrated VRMs enabled: DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect
CLK_M2_SUSCLK	0	Disable PLL On-Die voltage regulator
	1	Enable PLL On-Die voltage regulator (Default, IPU)
PU_DSWODVREN	0	Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments
	1	Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards. (Default)
BDX_SPKR	0	Disable No Reboot mode.
	1	Enable No Reboot mode (default , IPD)
PU_GPIOS1, XDP_NOA9_PCH	0 1	RESERVED
	1 0	RESERVED
	1 1	BOOT from SPI (default)
	0 0	BOOT from LPC
GPI033	0	SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS (default , IPD)
	1	SoC TX is terminated to VCC/2.
BIST_ENABLE	0	Build-in Self Test Disable (Default) ,IPU
	1	Build-in Self Test Enable
RP_UART1_TX	0	Disable NVM Security (Default)
	1	Security Enabled
ADR_STATUS_RD_R / GPI016	0	SoC RX is terminated to VSS (default , IPD)
	1	SoC RX is terminated to 1/2 VCC
PD_GPI053	0	SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. (Default) ,IPU
	1	SoC is in DC-coupling mode.
FM BIOS_RCRV_BOOT_N GPI055	0	E
	1	F
BDX_CPLD_JTAG_ENABLE_R GPI056		This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N.
MAC_INT_L_R / GPI044		This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N.
CPU_JTAG_RST_R / GPI046		This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N.
BMCINIT	0	Low
	1	High
S_A	0	High
	1	Low
F_P	0	High
	1	Low
C_B	0	High
	1	Low
L_X	0	High
	1	Low
E_P	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
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C_C	0	High
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I_D	0	High
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C_C	0	High
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C_C	0	High
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C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
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C_C	0	High
	1	Low
I_D	0	High
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C_C	0	High
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I_D	0	High
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I_D	0	High
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C_C	0	High
	1	Low
I_D	0	High
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I_D	0	High
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I_D	0	High
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C_C	0	High
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I_D	0	High
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I_D	0	High
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C_C	0	High
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I_D	0	High
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C_C	0	High
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I_D	0	High
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C_C	0	High
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I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
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I_D	0	High
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C_C	0	High
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I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	High
	1	Low
C_C	0	High
	1	Low
I_D	0	

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Model Name		Rev
BDX-DE CPU Board		R0B
Size	Page Name	Engineer
C	10_blank	Forbidian Kuo
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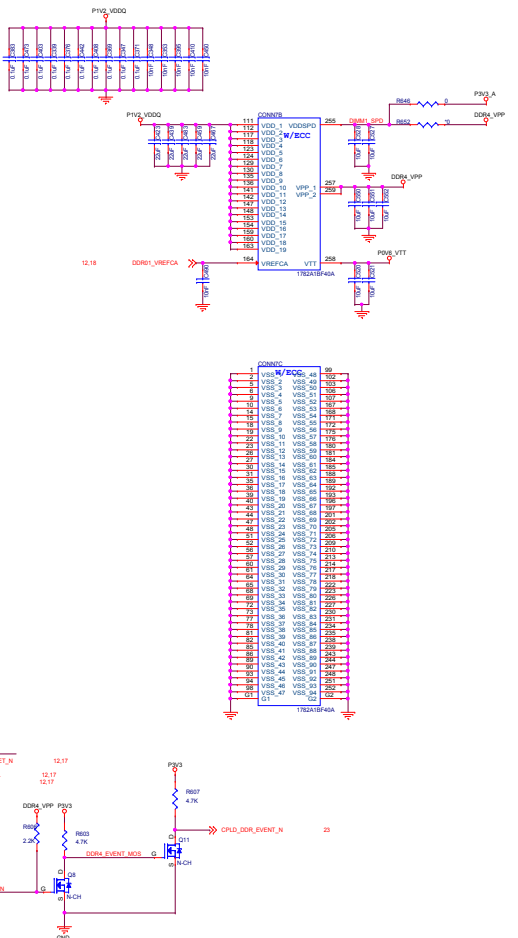
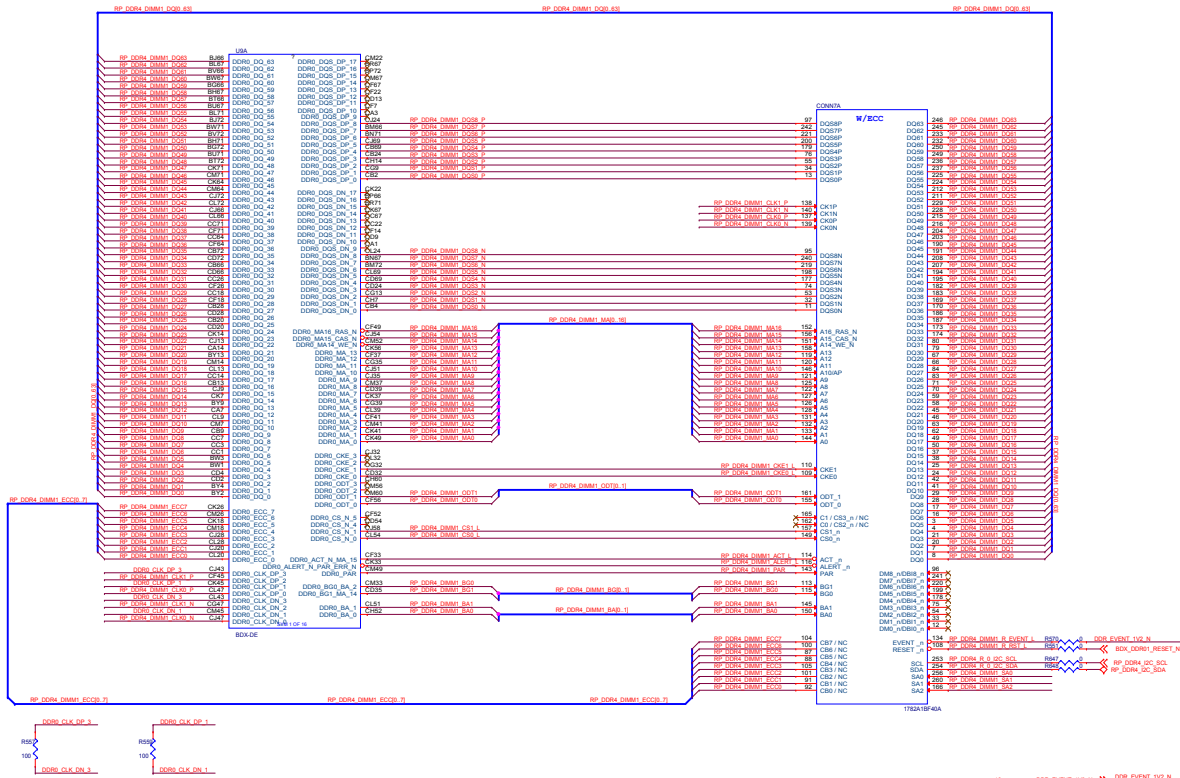
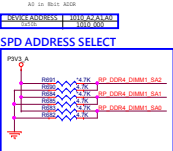


Table 4 - Function table

Input	Output
DR0	A
DR1	B
DR2	C
DR3	D

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Model Name: **BDX-DE CPU Board**

Rev: **R08**

Page Name: **RP_DDR4_SODIMM1**

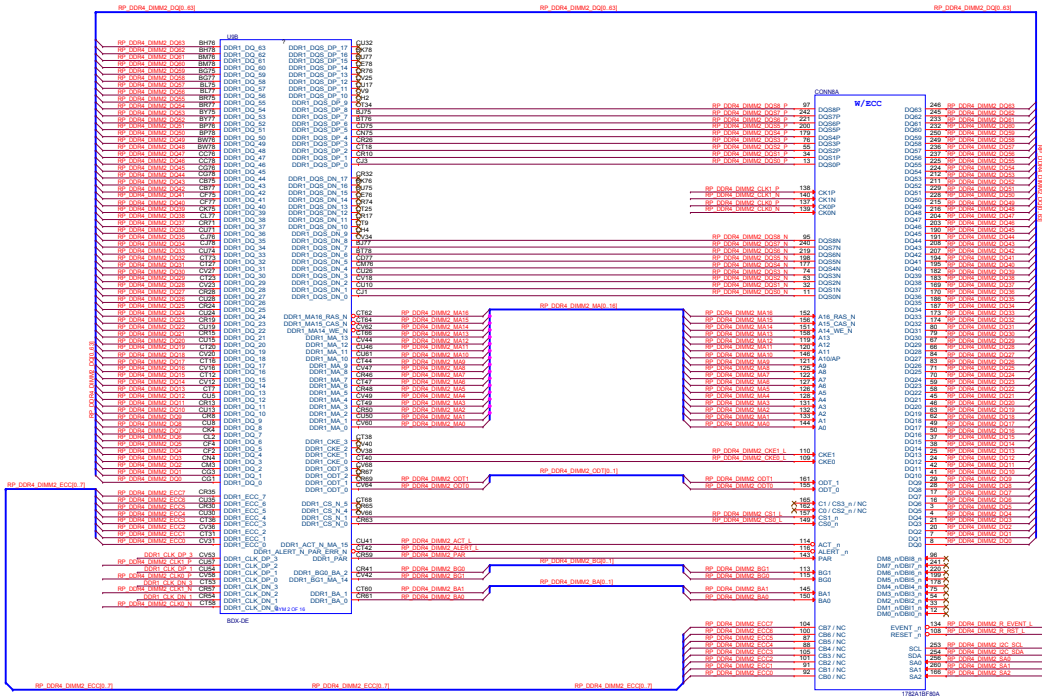
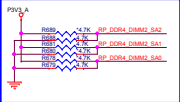
Location: **Forbidden Kuo**

Date: **Wednesday, Aug 15, 2018**

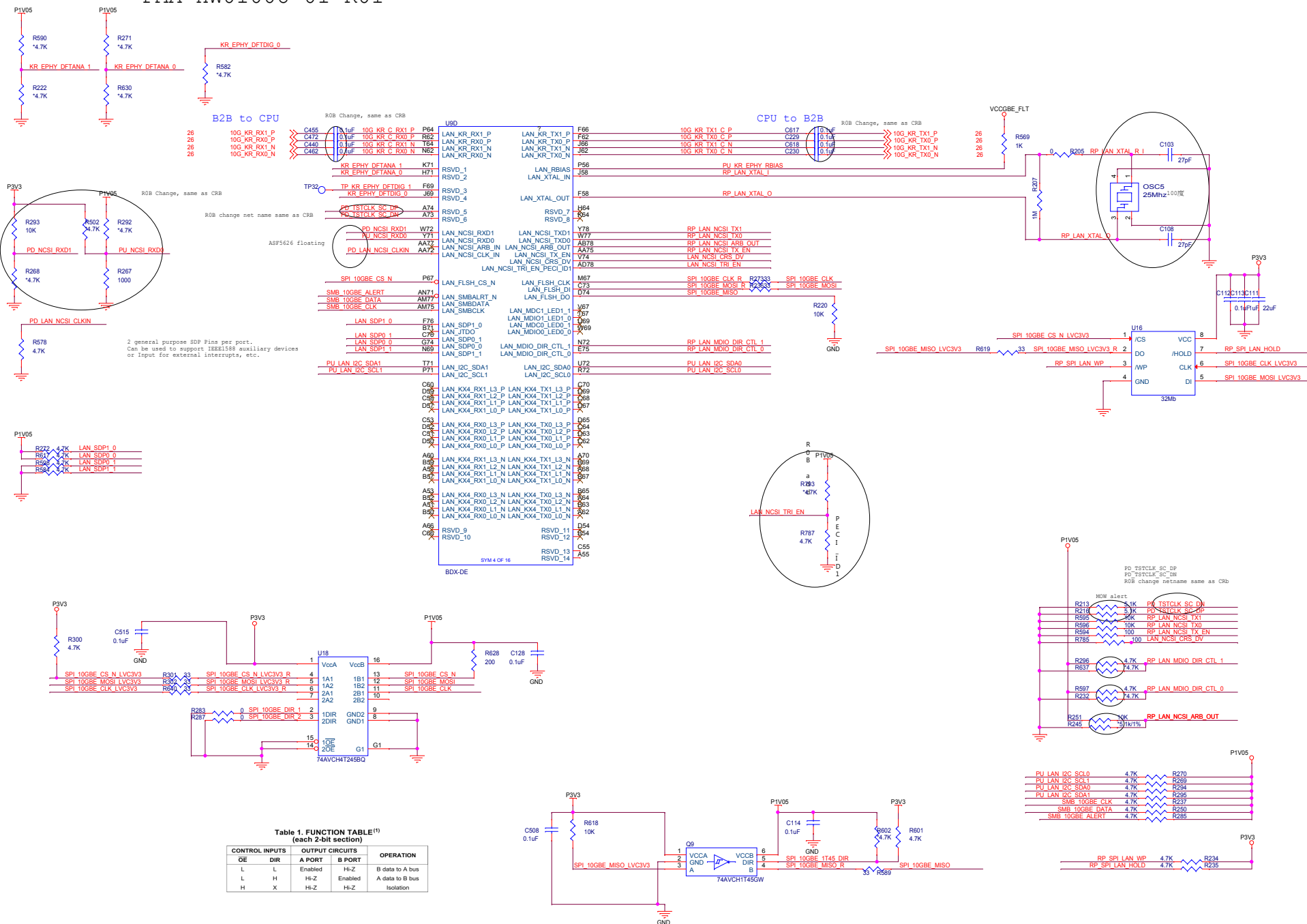
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SPD ADDRESS SELECT



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Model Name		R0B
BDX-DE CPU Board		
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RP_PCIE	Forbidian Kuo	
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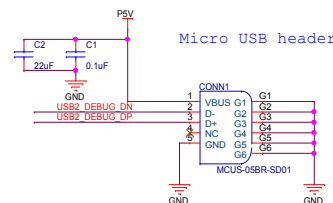
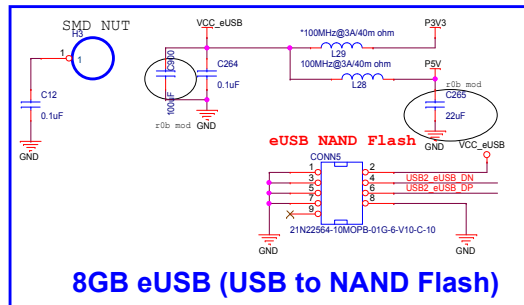
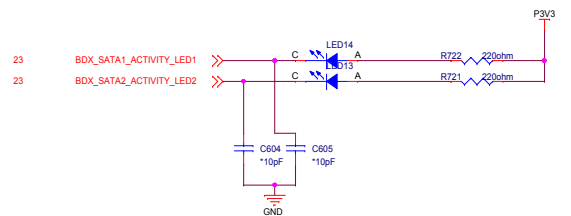
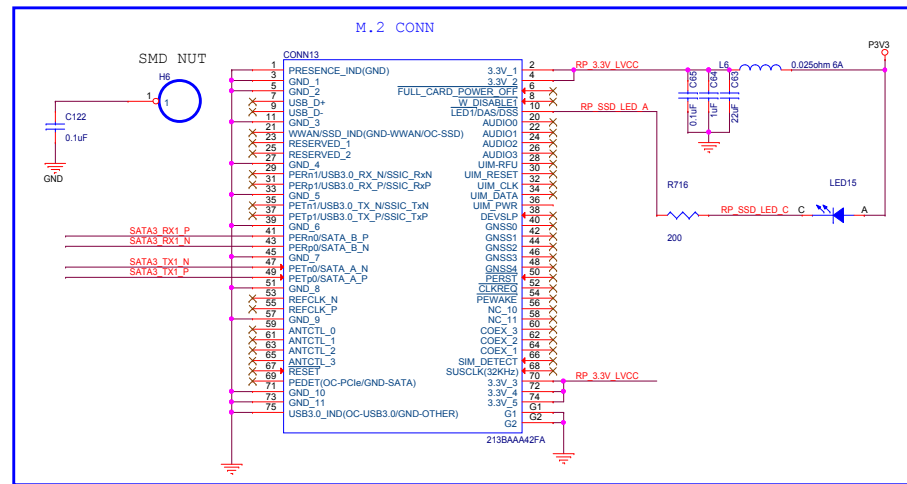
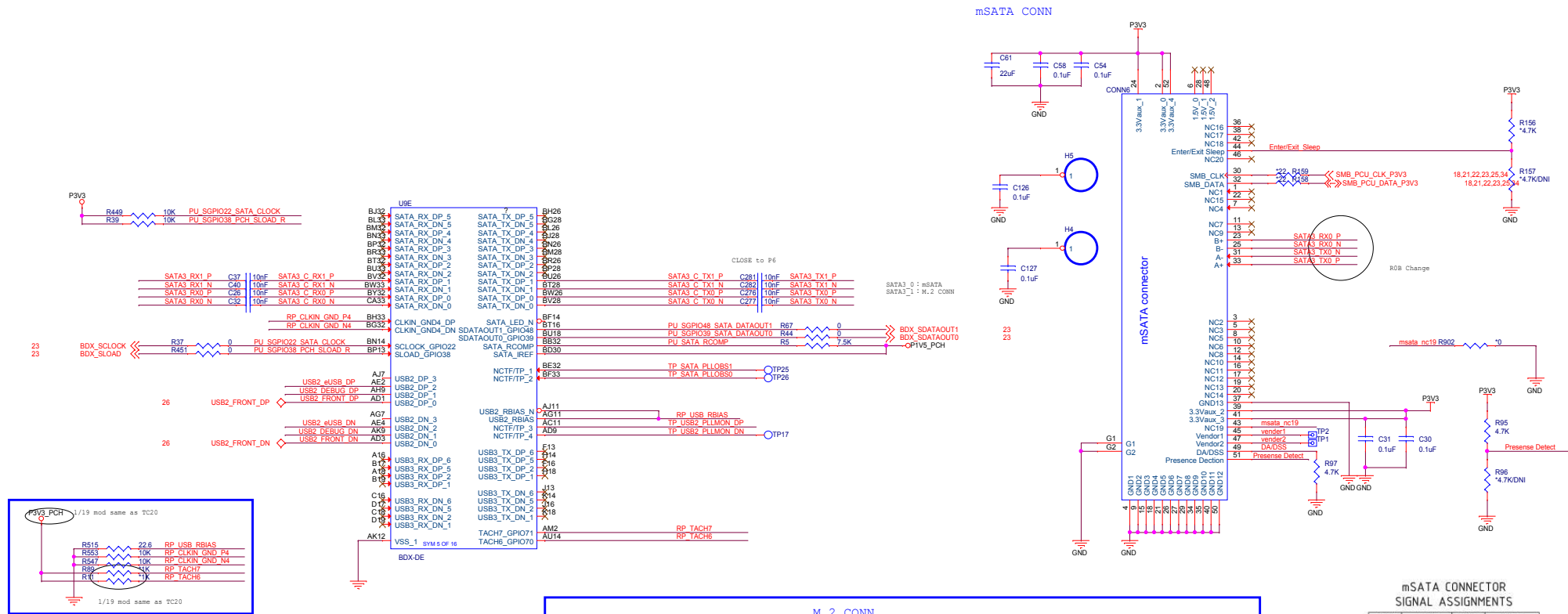
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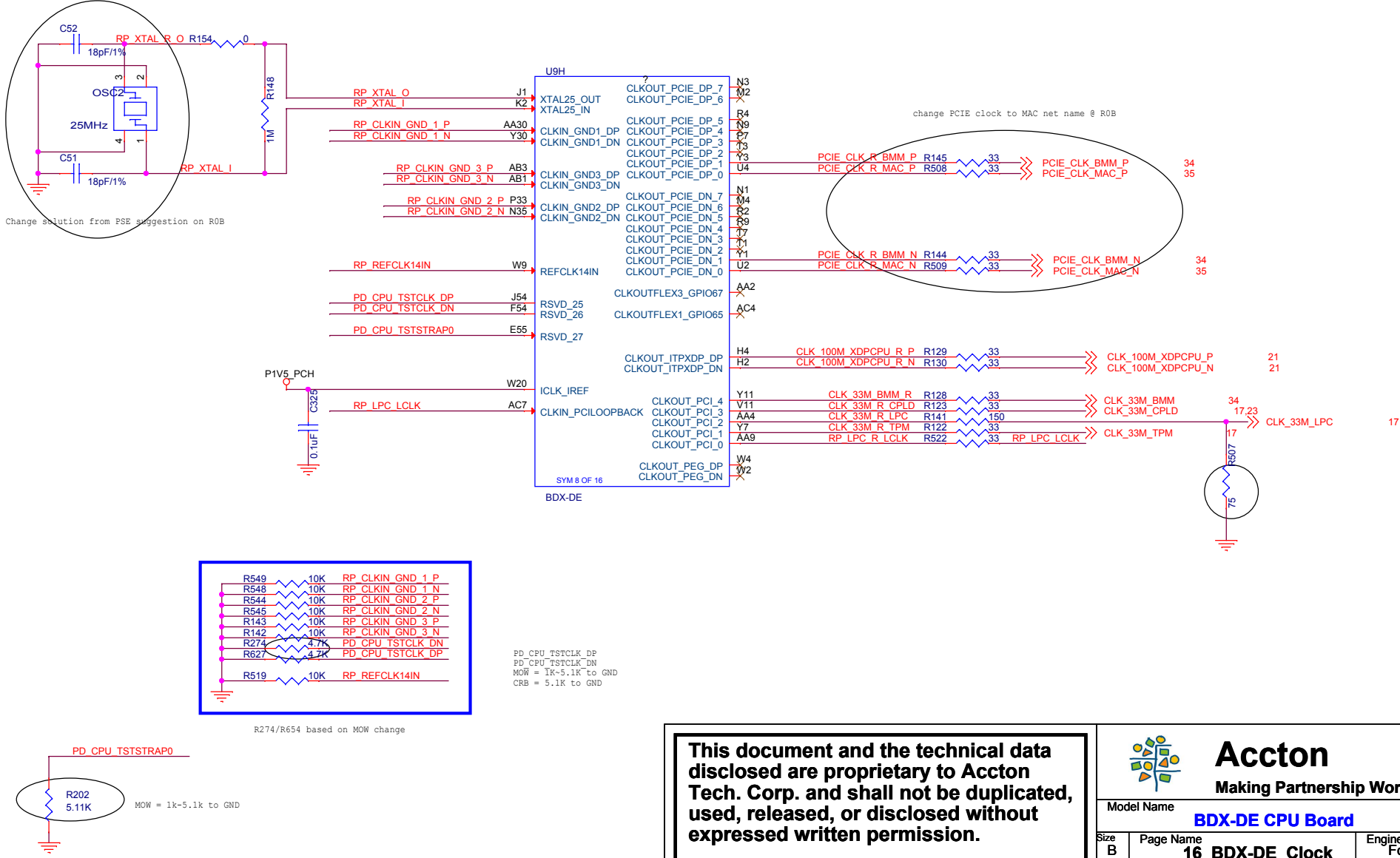
Model Name		BDX-DE CPU Board	Rev
Size		14_BDX-DE_10GB Ethernet	R0B
Page Name	Engineer	Forbidian Kuo	
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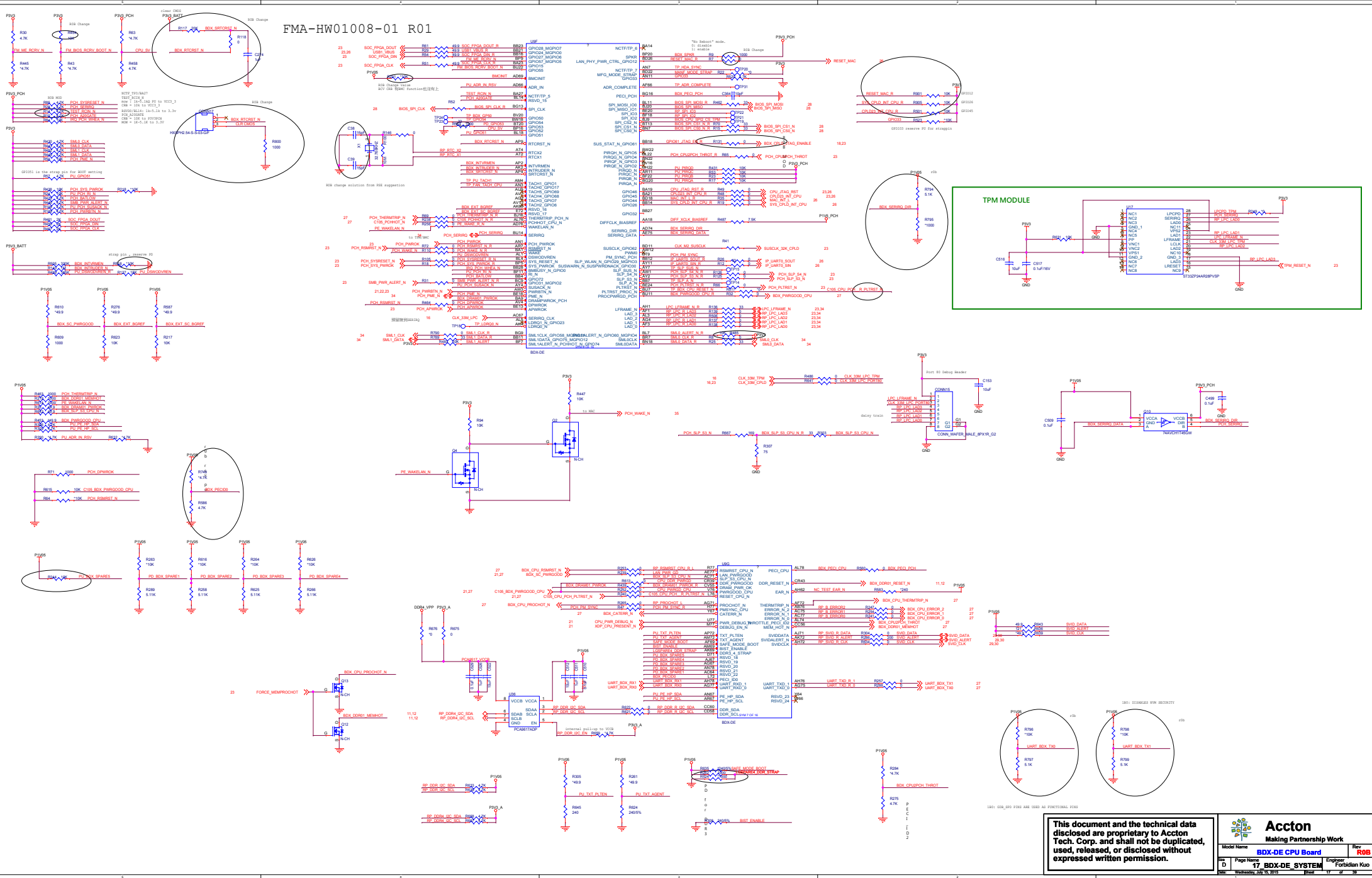


mSATA CONNECTOR SIGNAL ASSIGNMENTS

PIN#	NAME	PIN#	NAME
51	Presence Detection	52	+3.3V
49	DA/DSS	50	GND
47	Vendor	48	+15V
45	Vendor	46	Reserved
43	No Connect	44	Reserved
41	+3.3V	42	Reserved
39	+3.3V	40	GND
37	GND	38	Reserved
35	GND	36	Reserved
33	+A	34	GND
31	-A	32	Two Wire Interface
29	GND	30	Two Wire Interface
27	GND	28	+15V
25	-B	26	GND
23	+B	24	+3.3V
21	GND	22	Reserved
19	Reserved	20	Reserved
17	Reserved	18	GND
MECHANICAL KEY			
15	GND	16	Reserved
13	Reserved	14	Reserved
11	Reserved	12	Reserved
9	GND	10	Reserved
7	Reserved	8	Reserved
5	Reserved	6	+15V
3	Reserved	4	GND
1	Reserved	2	+3.3V

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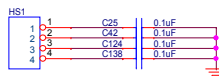




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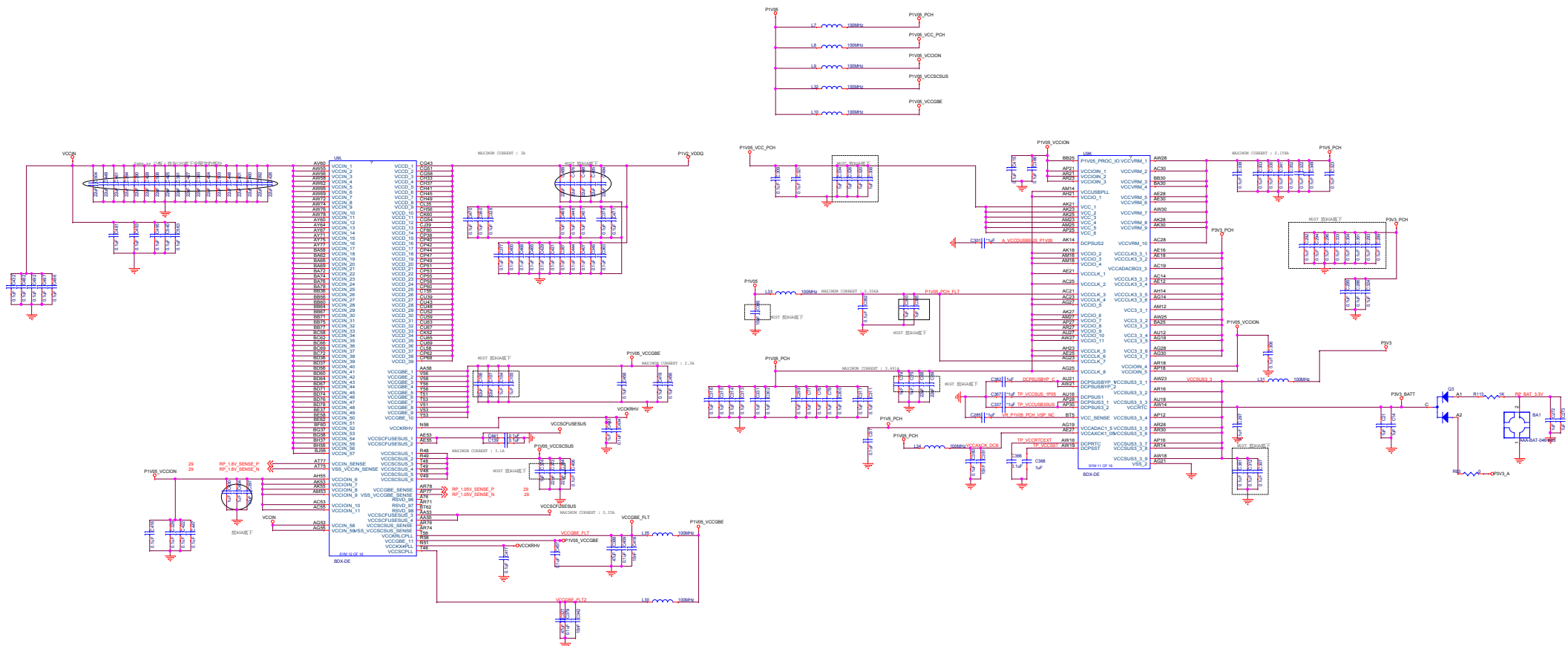


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Model Name		R0B
BDX-DE CPU Board		
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18_BDX-DE_STRIP	Forbidian Kuo	
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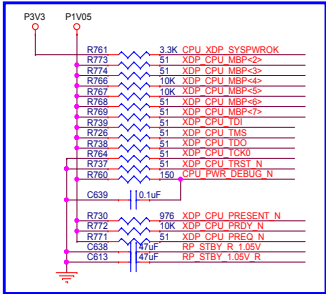
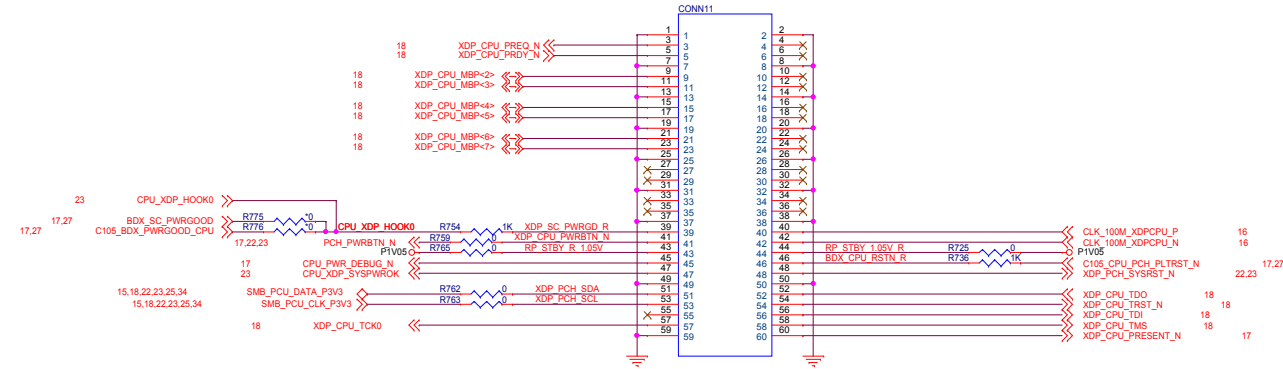


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Model Name		BDX-DE CPU Board		Rev	R0B
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GPI051 / XDP NOA9 PCH is the strap pin for BOOT setting



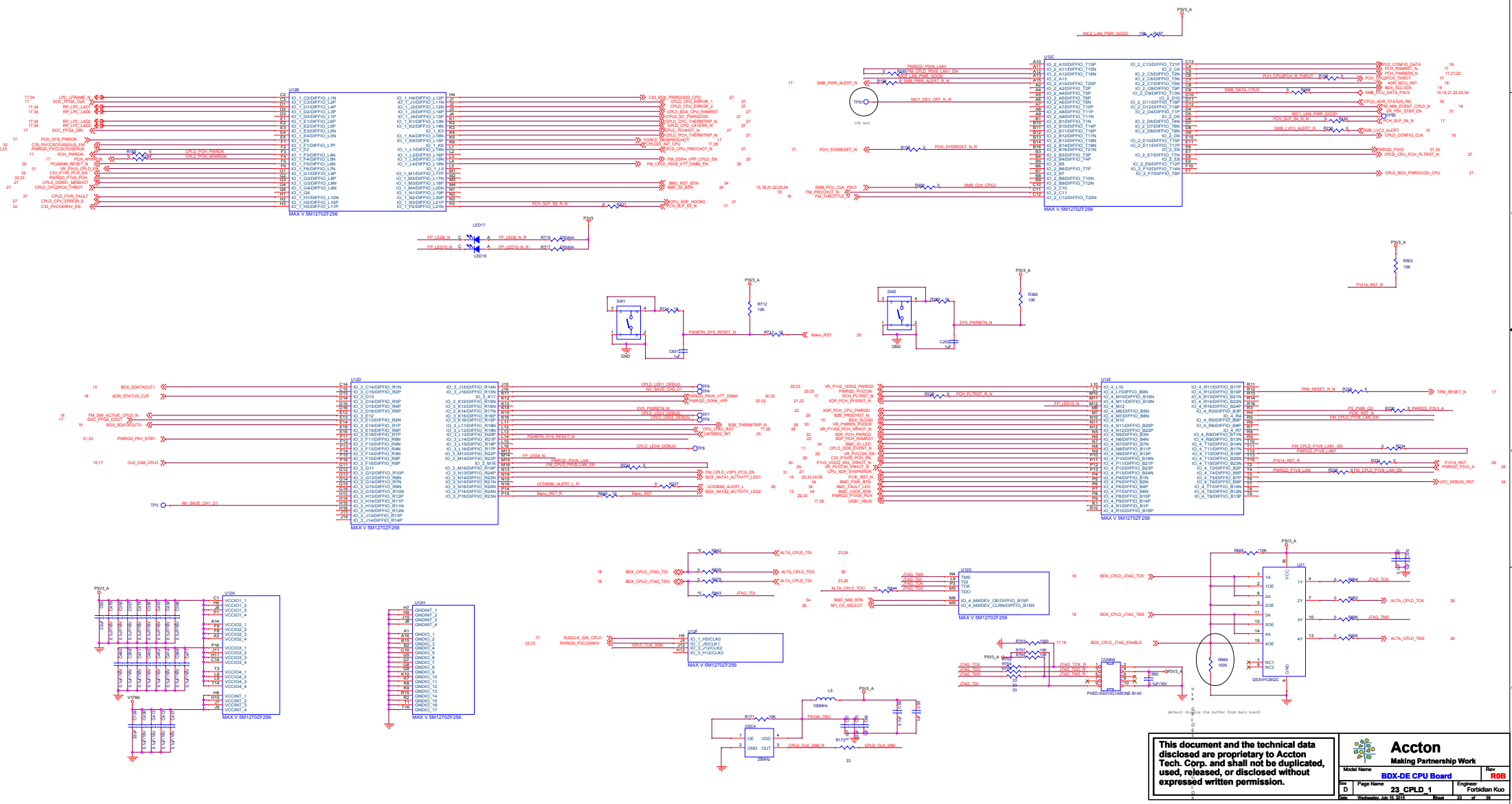
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Rev
ROB

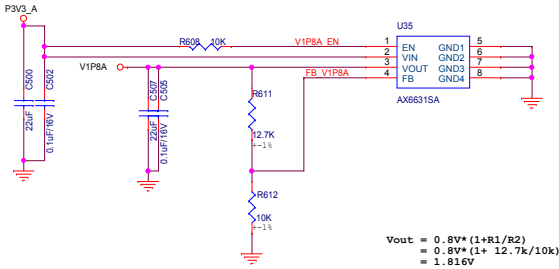
Size	Page Name	Engineer
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C	22	BDX-DE	PCH	XDP	CONN	Forbidian Kuo
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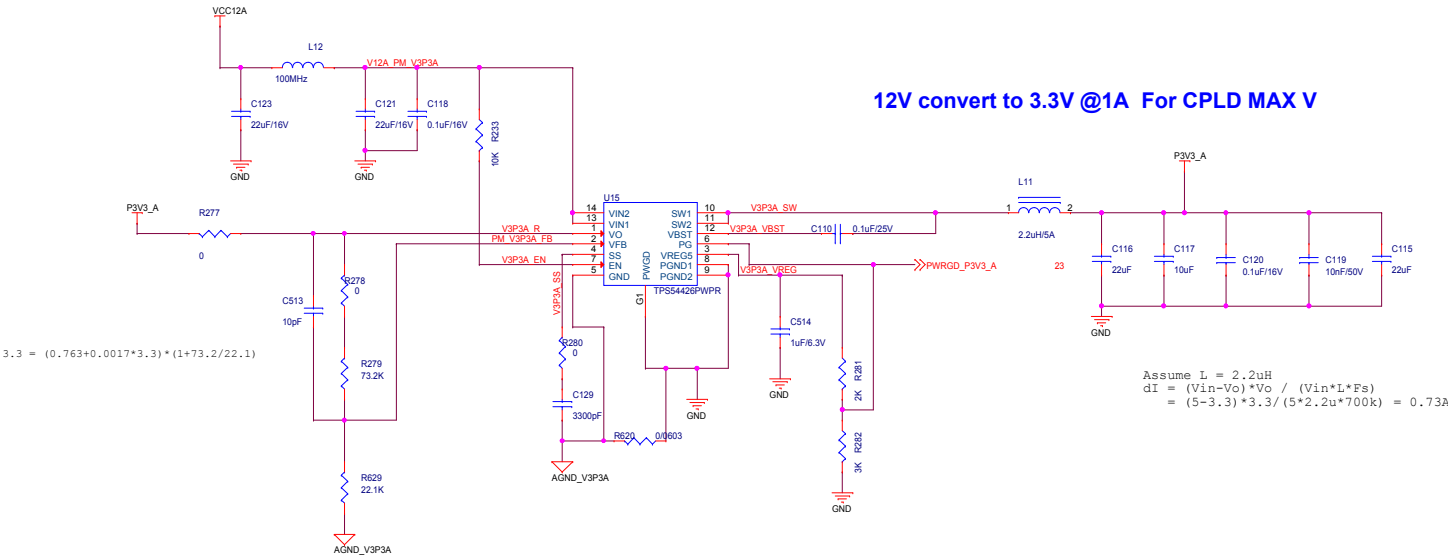


3.3V convert to 1.8V @0.8A For CPLD



Guaranteed 1.2A output current

12V convert to 3.3V @1A For CPLD MAX V



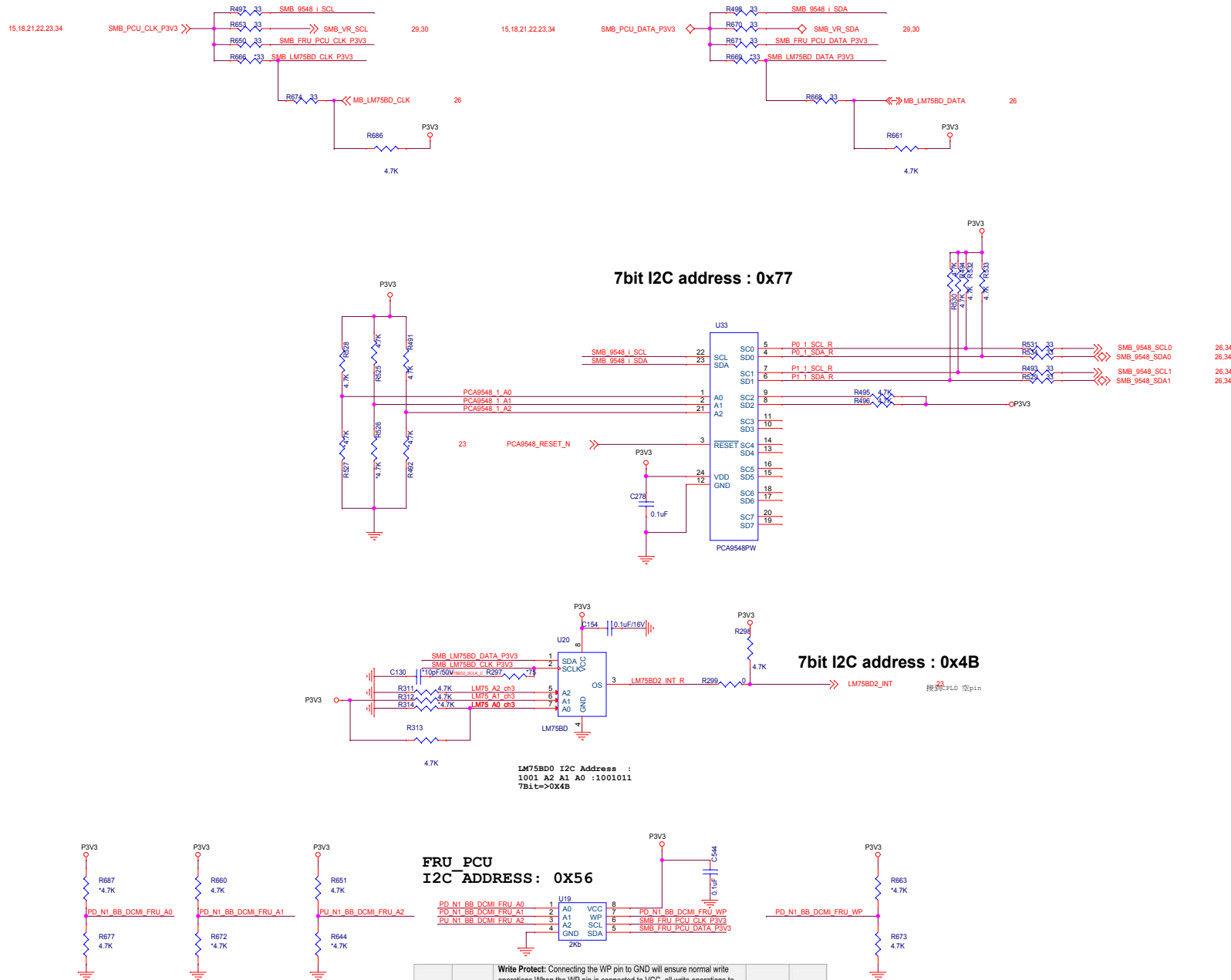
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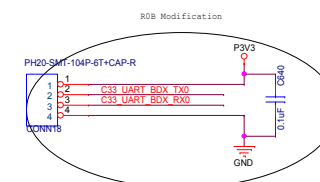
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Model Name		Rev	
BDX-DE CPU Board		R0B	
Size	Page Name	Engineer	
C24	CPLD PWR P3V3_A P1V8A	Forbidian Kuo	
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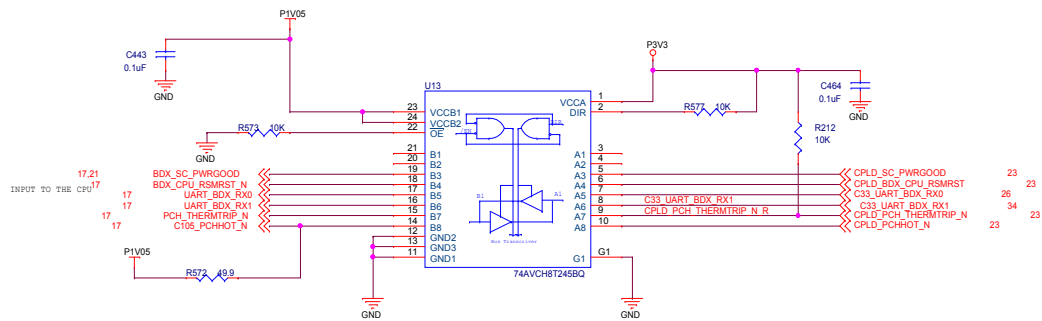


7	WP	Write Protect: Connecting the WP pin to GND will ensure normal write operations. When the WP pin is connected to VCC, all write operations to the memory are inhibited. Refer to Note 1 for behavior of the pin when not connected.	High	Input
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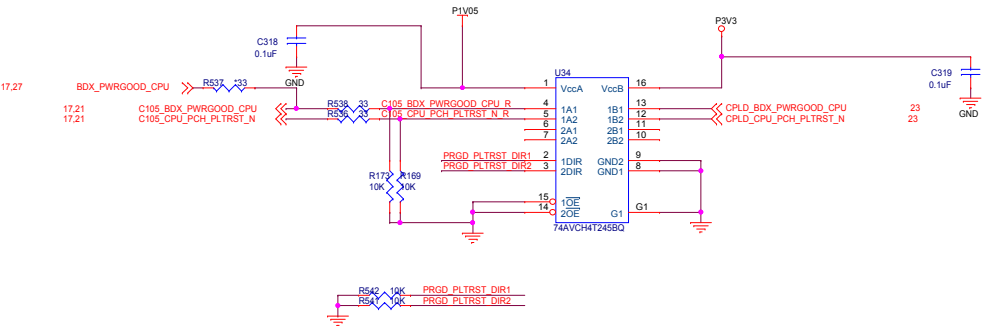
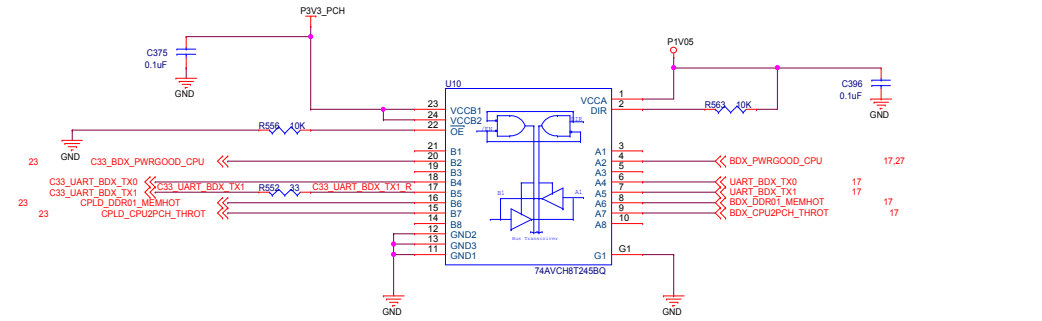
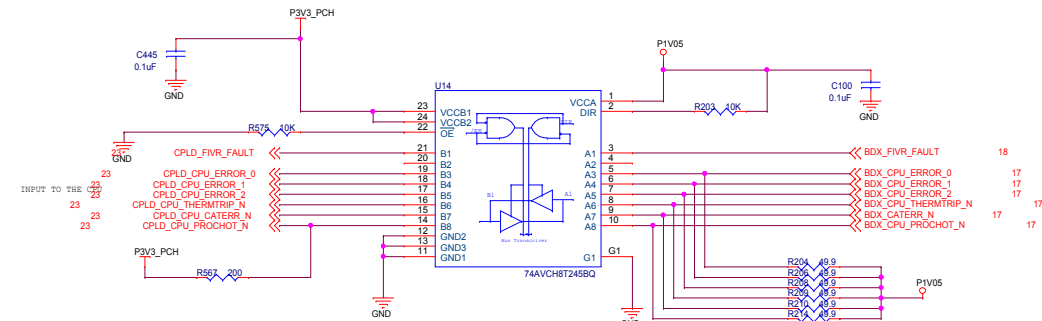


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BDX-DE CPU Board		R0B
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C	26 B2B Connector	Forbidian Kuo
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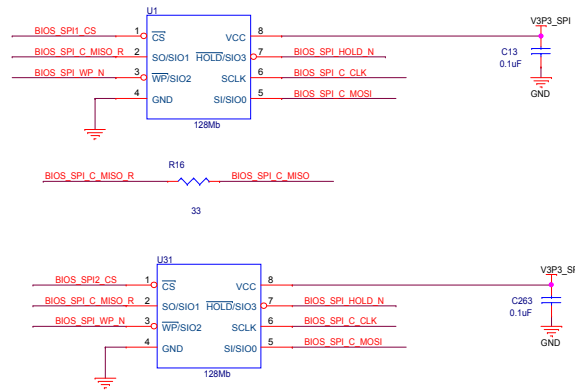
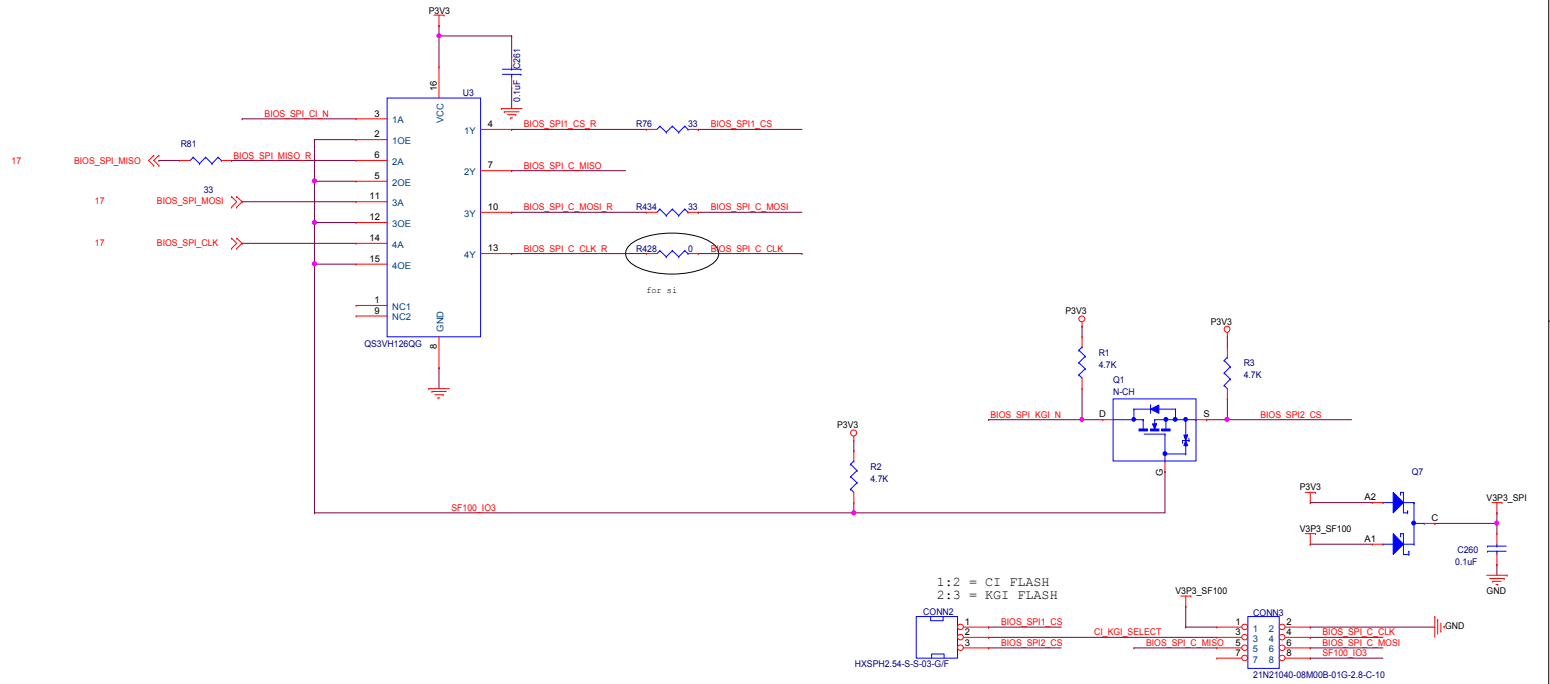
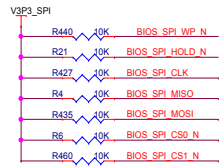
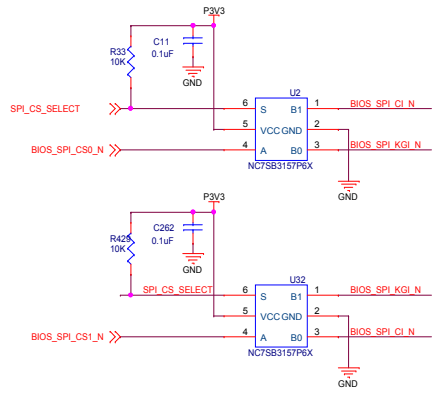


FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All outputs Hi-Z



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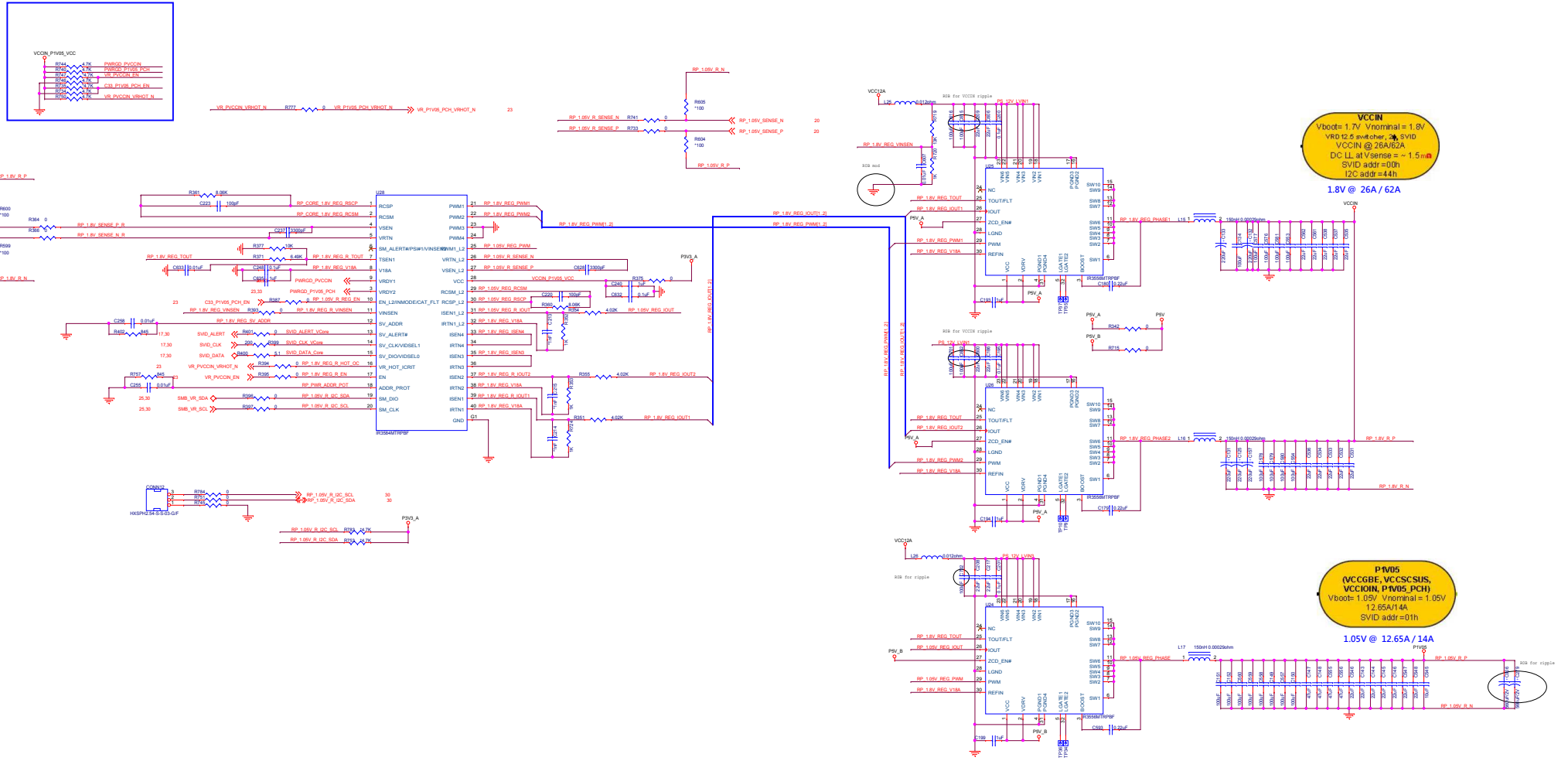
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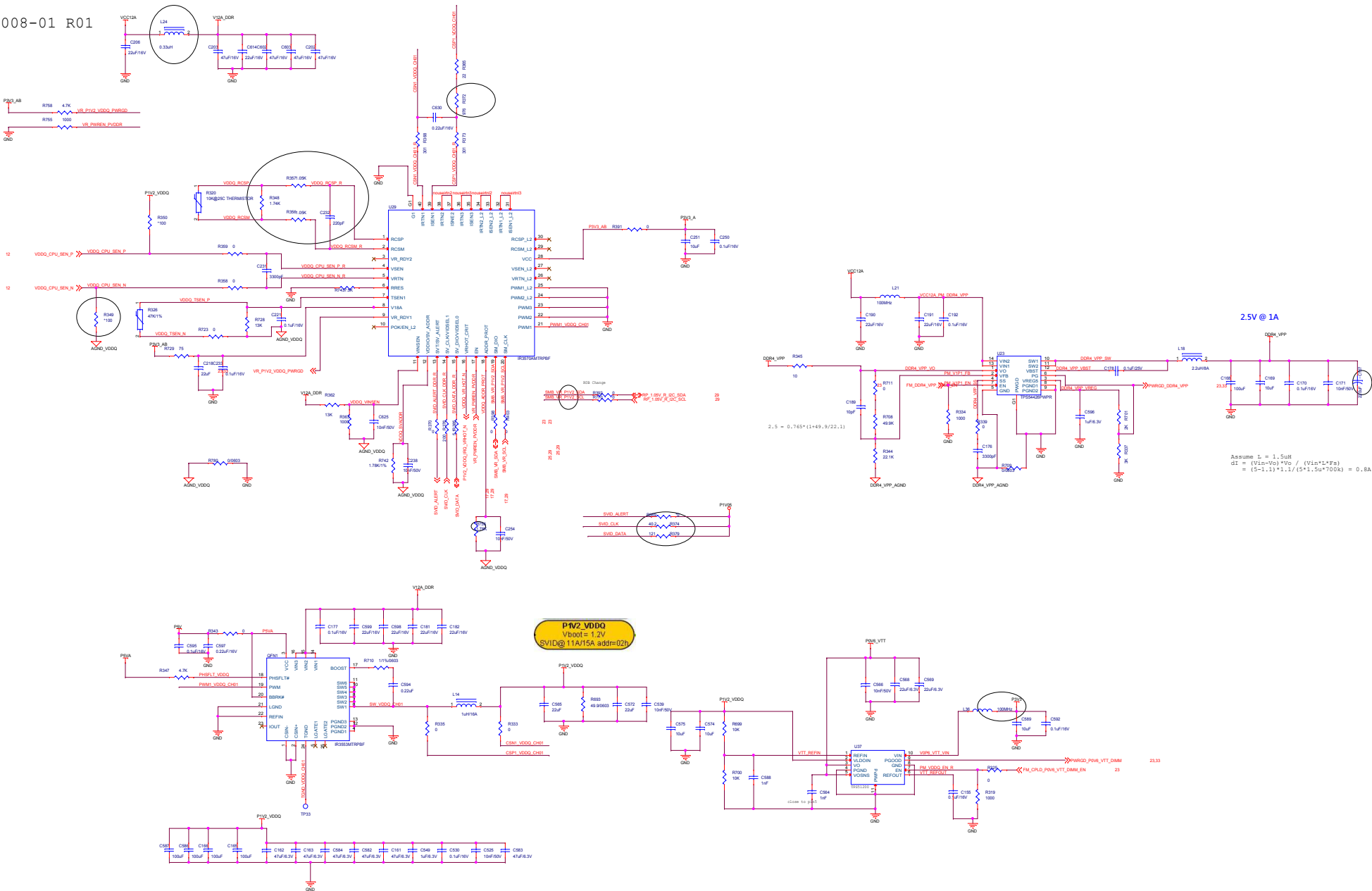
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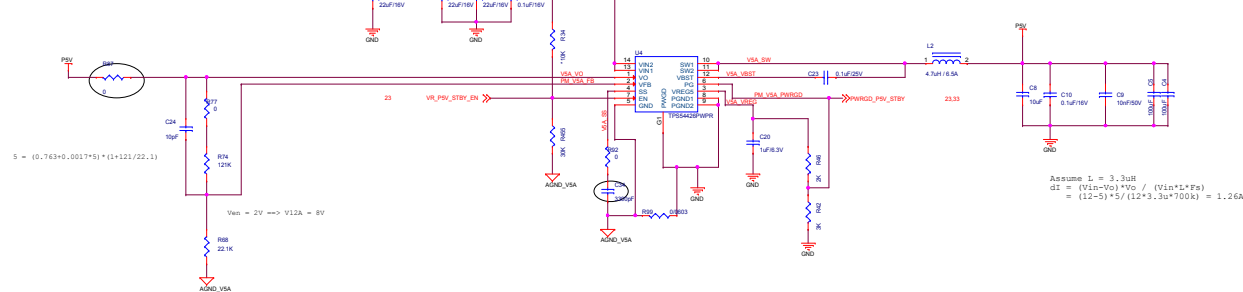


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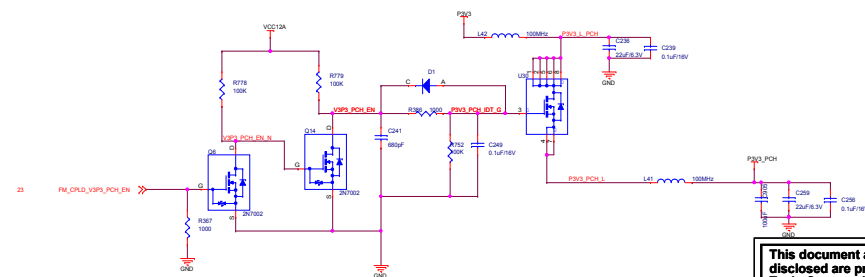
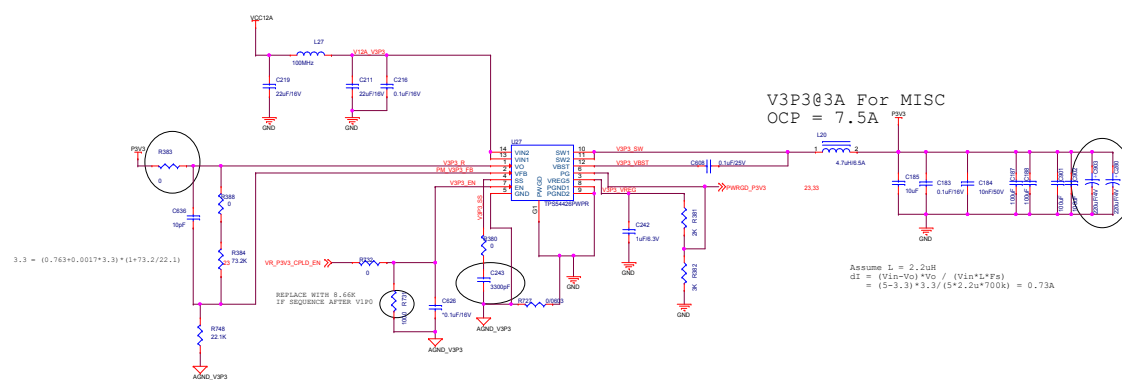


FMA-HW01008-01 001

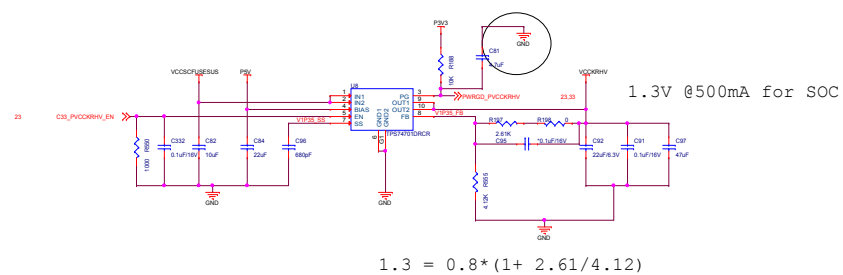
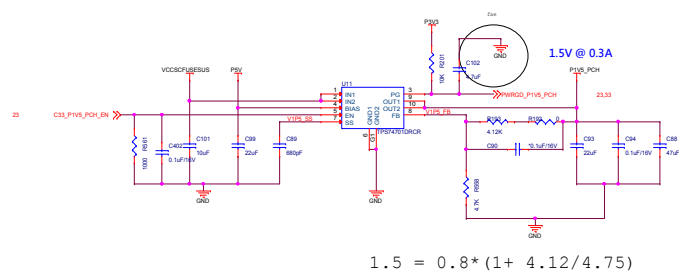
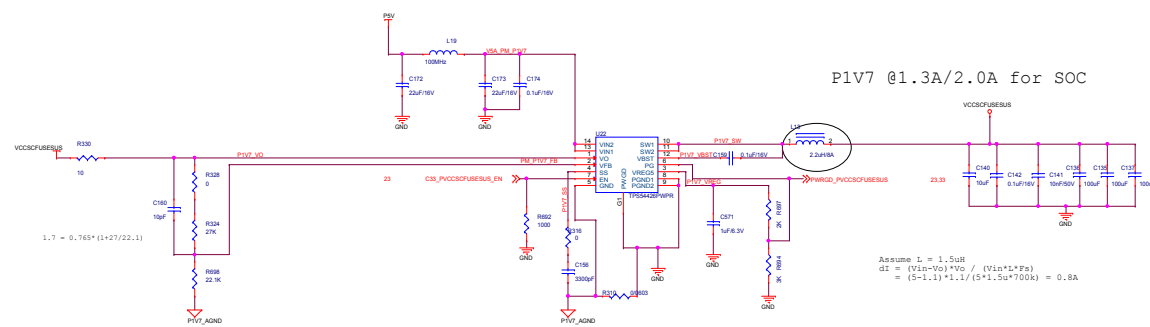
V5A@3A For USB and MISC
 OCP = 7.5A



V3P3@3A For MISC
 OCP = 7.5A

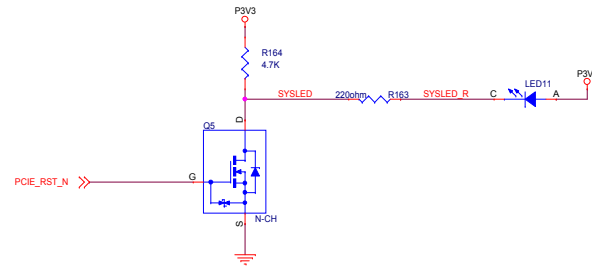
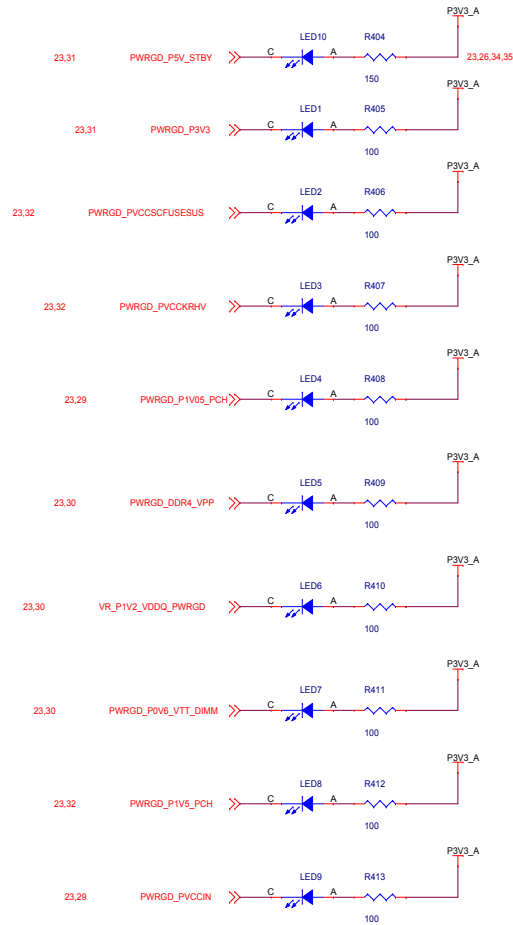
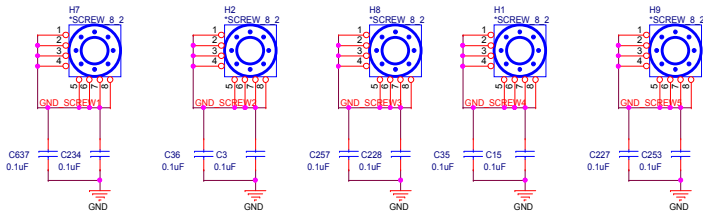


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Sequence

1. P3V3_A
2. P5V
3. P3V3
4. P1V7
5. P1V3
6. P1V05
7. VPP
8. VDDQ
9. VTT / VCCIN / P1V5 /

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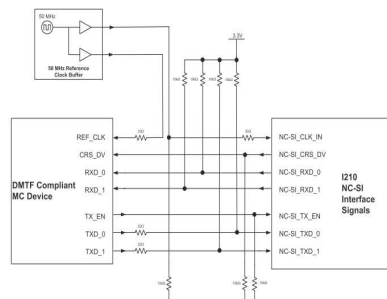
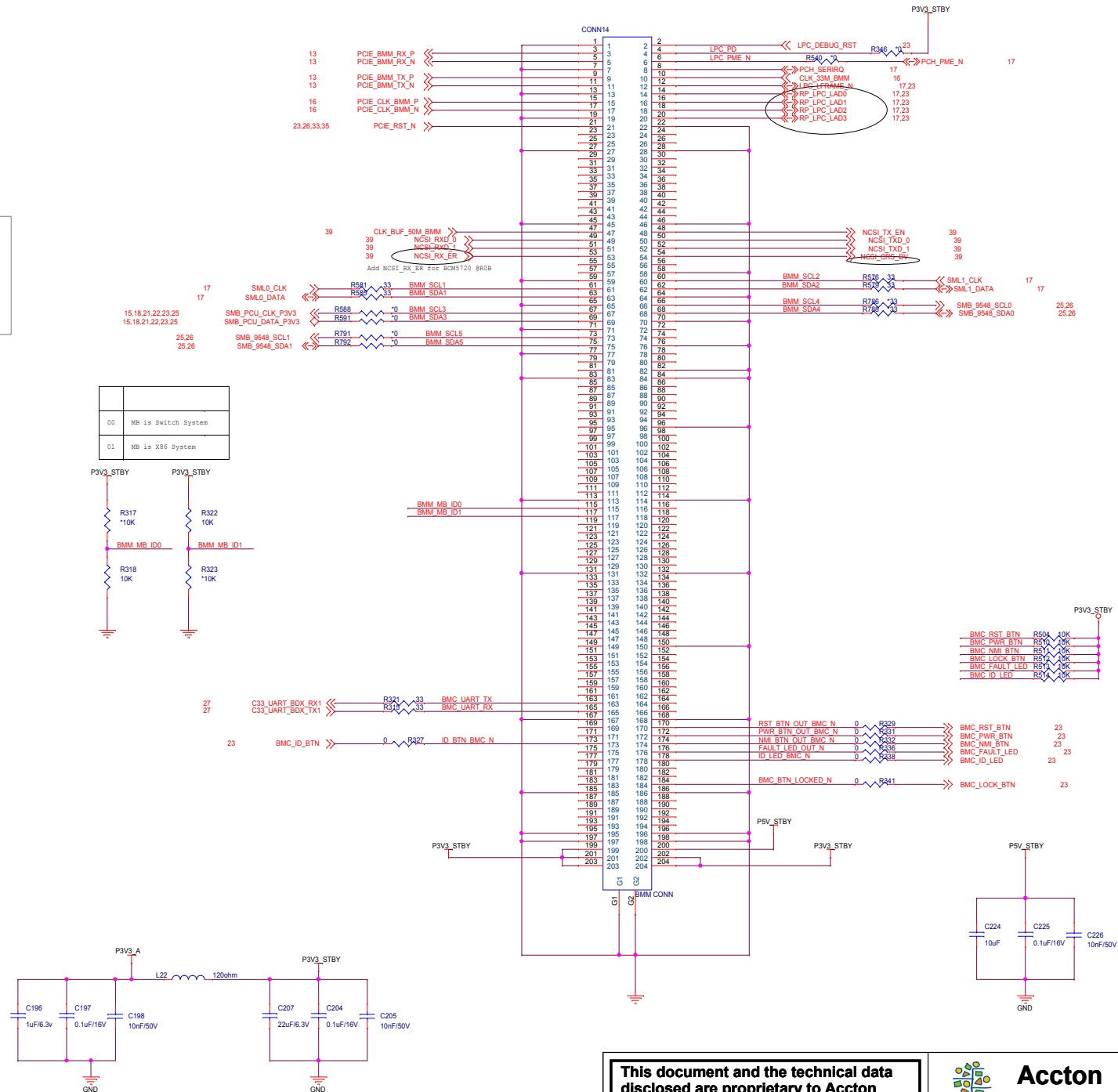


Figure 12-14.NC-SI Connection Requirements - Single-Drop Configuration

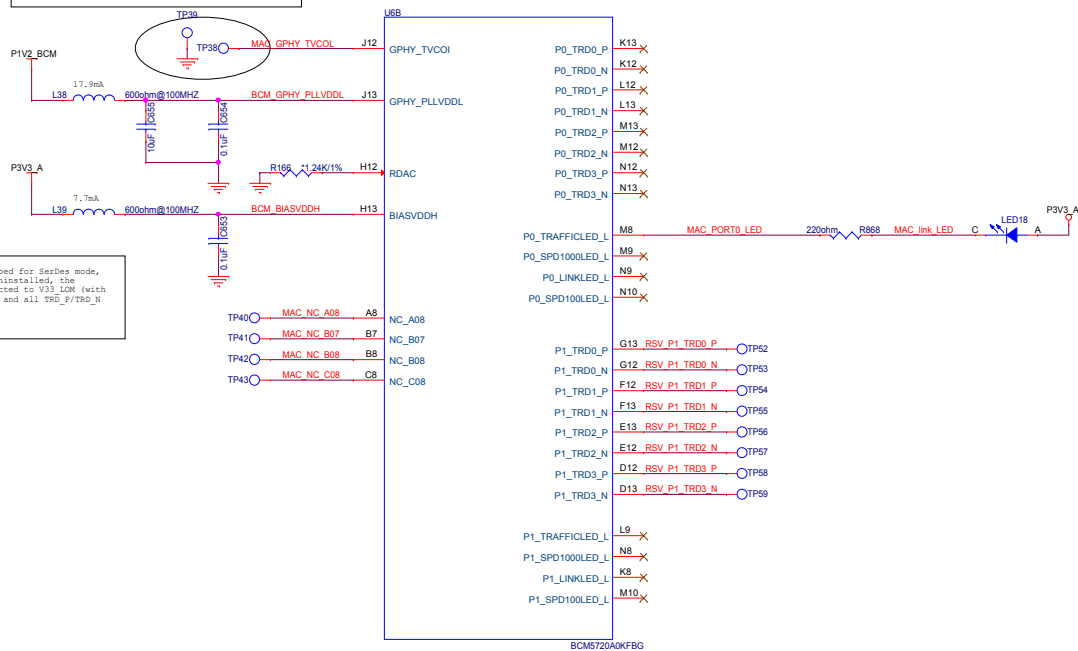


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Place the GND test point next to the GPHY_TVCOL test point to allow good signal integrity probing.

The MDI termination is integrated in the controller.

When both Ethernet ports are strapped for SerDes mode, the RDAC resistor to GND may be uninstalled, the BIASVDDH supply input may be connected to V33_L0W (with the filter) or optionally to GND, and all TRD_P/TRD_N pins may be left unconnected.

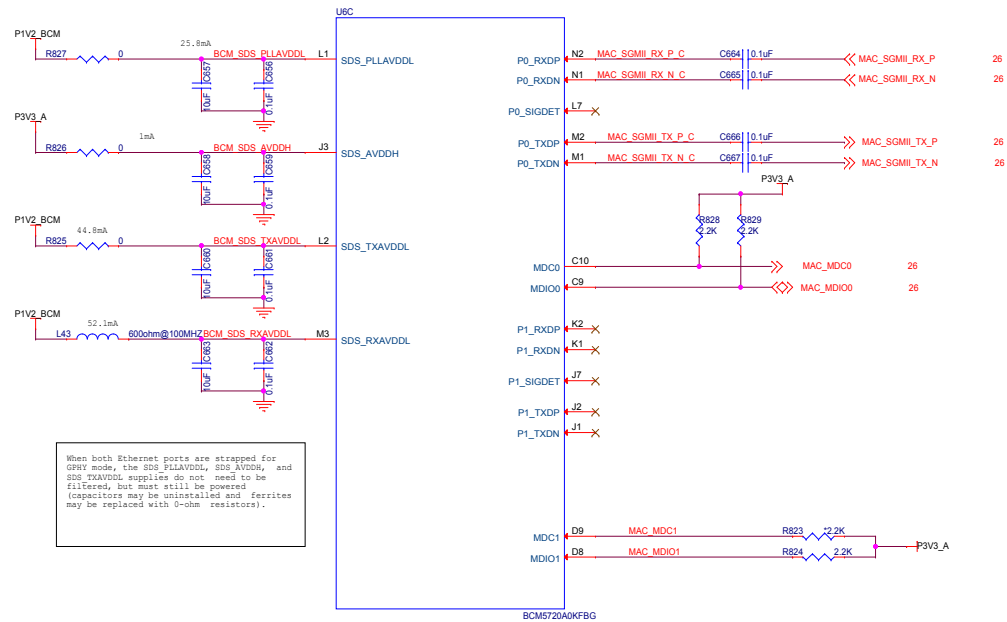


GPHY PORTS, LEDs

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MDC1	MDC0	Ethernet Port 1	Ethernet Port 0	
0	0	GPHY	GPHY	(By default)
0	1	GPHY	SerDes	
1	0	SerDes	GPHY	
1	1	SerDes	SerDes	

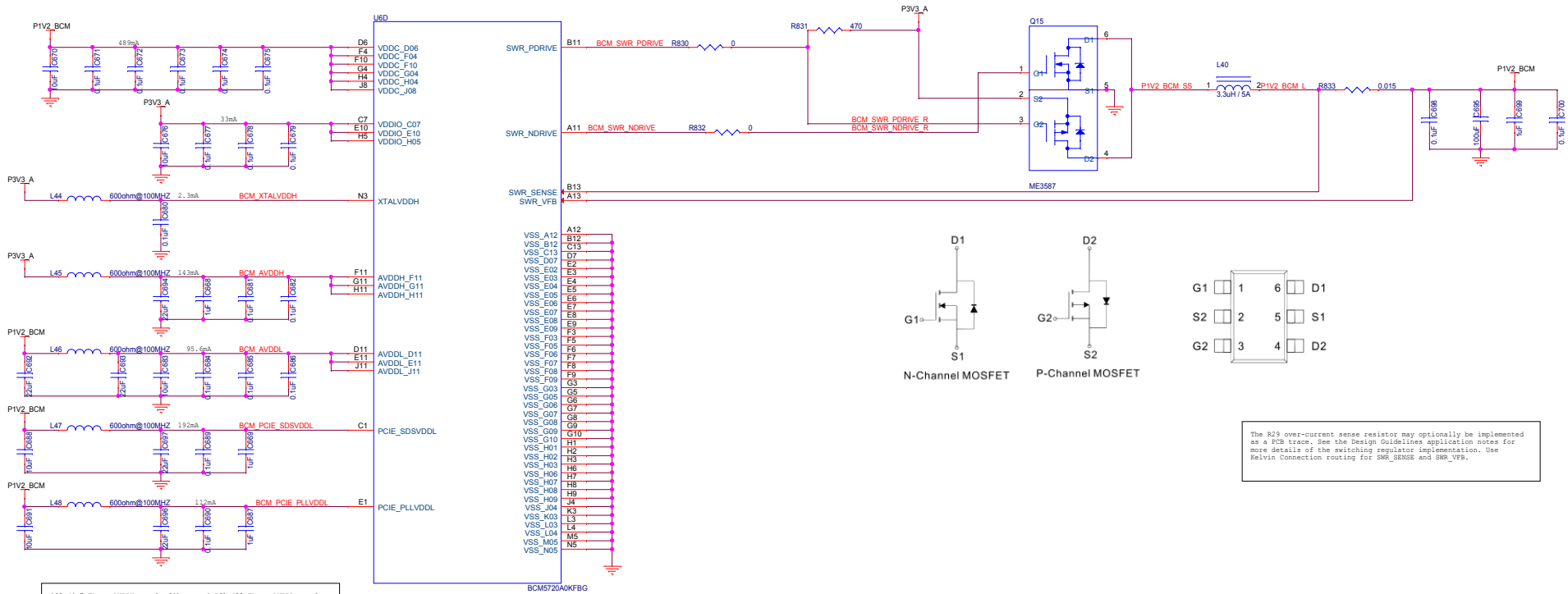
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C60 (4.7uF) on AVDDH supply filter and C61 (22uF) on AVDDL supply filter are the minimum requirement on the RSE-enabled platform. Higher built capacitance may be used for smaller voltage transients.

For AVDDL filter, C52 (4.7uF) and C61 (22uF) can be combined into a single 27uF or larger capacitor in designs where RSE will be used. A 4.7uF is the minimum requirement if RSE is not used.

The R29 over-current sense resistor may optionally be implemented as a PCB trace. See the Design Guidelines application notes for more details of the switching regulator implementation. Use Kelvin Connection routing for SWR_SENSE and SWR_VFB.

POWER

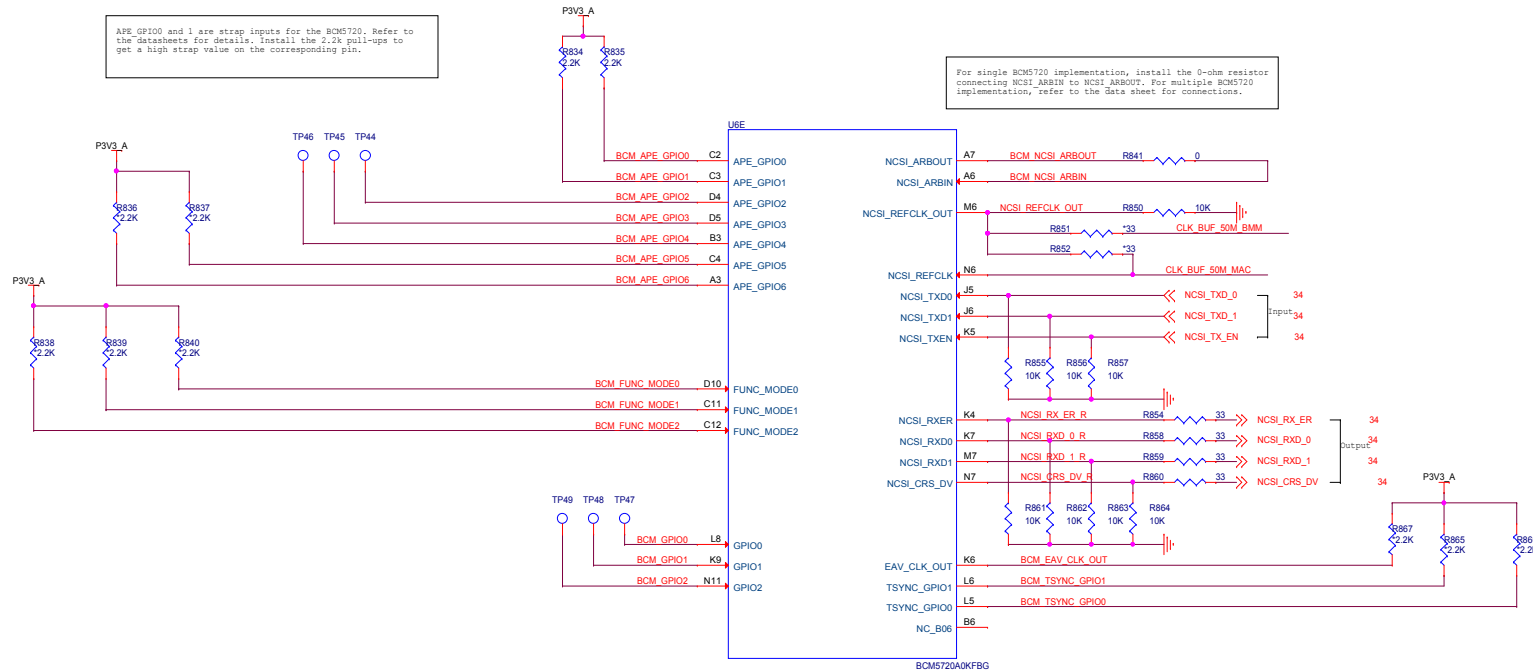
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APE_GPIO0 and 1 are strap inputs for the BCM5720. Refer to the datasheets for details. Install the 2.2K pull-ups to get a high strap value on the corresponding pin.



For single BCM5720 implementation, install the 0-ohm resistor connecting NCSI_ARBIN to NCSI_ARBOUT. For multiple BCM5720 implementation, refer to the Data sheet for connections.

Optional 50MHz NC-SI reference clock source. When used, the 22-ohm source termination may be required depending on clock distribution details. A weak (10K) pull-down resistor is needed if the NCSI_REFCLK_OUT is disabled. Note: fanout buffer clock distribution may be necessary with three or more NC-SI reference clock loads.

Refer to the data sheet for NC-SI signal connections when the NC-SI interface is not used.

The external 10-kohm pull-down resistors are recommended to prevent the NC-SI I/O pins from floating when not driven. If the Management Controller has the on-chip pull-downs, then the external pull-downs are not needed.

The 22-ohm resistor source termination on NC-SI outputs may not be the appropriate termination, depending on the NC-SI bus system design particulars. Any termination should be appropriate for the actual system implementation.

Optional time synchronization assist system connections.

NC-SI, GPIO, MODE STRAPPING, TIME SYNC

The management FW samples APE_GPIO[6:5] during initialization and may assign the sampled values to NC-SI Package ID [1:0]. APE_GPIO[6:5] are internally pulled down.

The FUNC_MODE[2:0] are strap inputs to control the PCIe function and Ethernet port disable configuration. The value is strapped at PERST_L deassertion. The system may control FUNC_MODE[2:0] pins, which are internally pulled down.

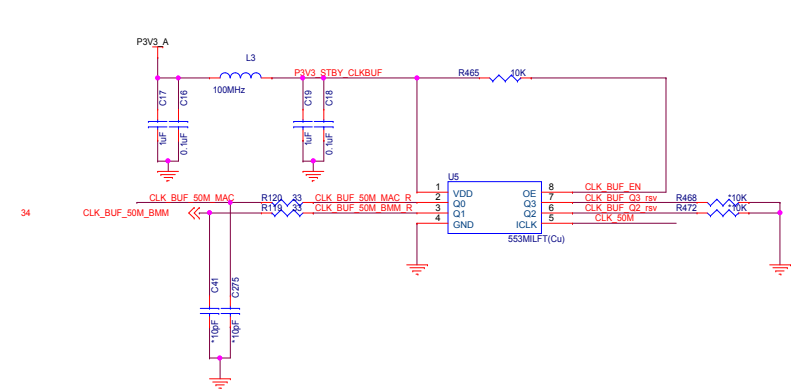
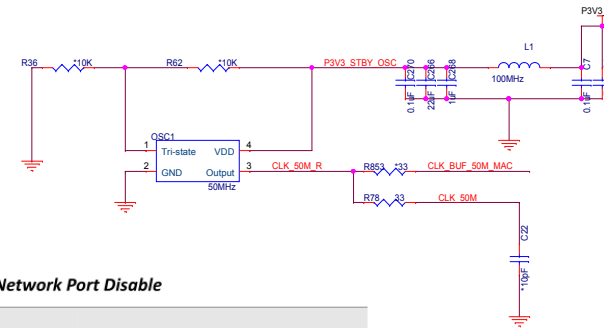


Table 6: PCI Express Function and Network Port Disable

FUNC_MODE [2:0]	Port 0	Port 1	Function 0	Function 1	Comments
000	Enabled	Enabled	Visible	Visible	Default configuration.
001	Enabled	Disabled	Visible	Invisible	No host traffic through Port 1.
010	Enabled	Disabled	Visible	Visible	No host traffic through Port 1, but PCIe Function 1 remains visible as a dummy function.
011	Disabled	Enabled	Visible	Visible	No host traffic through Port 0, but PCIe Function 0 remains visible as a dummy function.
1xx	Disabled	Disabled	Invisible	Invisible	No host traffic through either port.

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Model Name **BDX-DE CPU Board** Rev **R0B**

Size C Page Name **39_MAC_NCSI** Engineer **Forbidian Kuo**

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