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History

SCH Version	Date	Description
R0A	2014/12/29	Initial Version
R0A1	2015/02/12	For new PCB Part number used
R0B	2015/05/27	For R0B
R01	2015/09/01	R01 Released for MP

Change list between R0A1 and R0B

- 1. cpu_jtag_rst and UCD9090_ALERT_L should go thru level shift IC.
- 2. Change C41 from 3.3nF to 15nF.
- 3. Remove pull up resistor R131.
- 4. Change R228 from 1K ohm to 330 ohm for JTAG_TCK application.
- 5. Change R144, R145 from 1K ohm to 4.7K ohm.
- 6. Change R128 from 4.7K ohm to 1K ohm.
- 7. Reserve SDIO level shift IC.
- 8. Change BTB connector pin define

Change list between R0B and R01

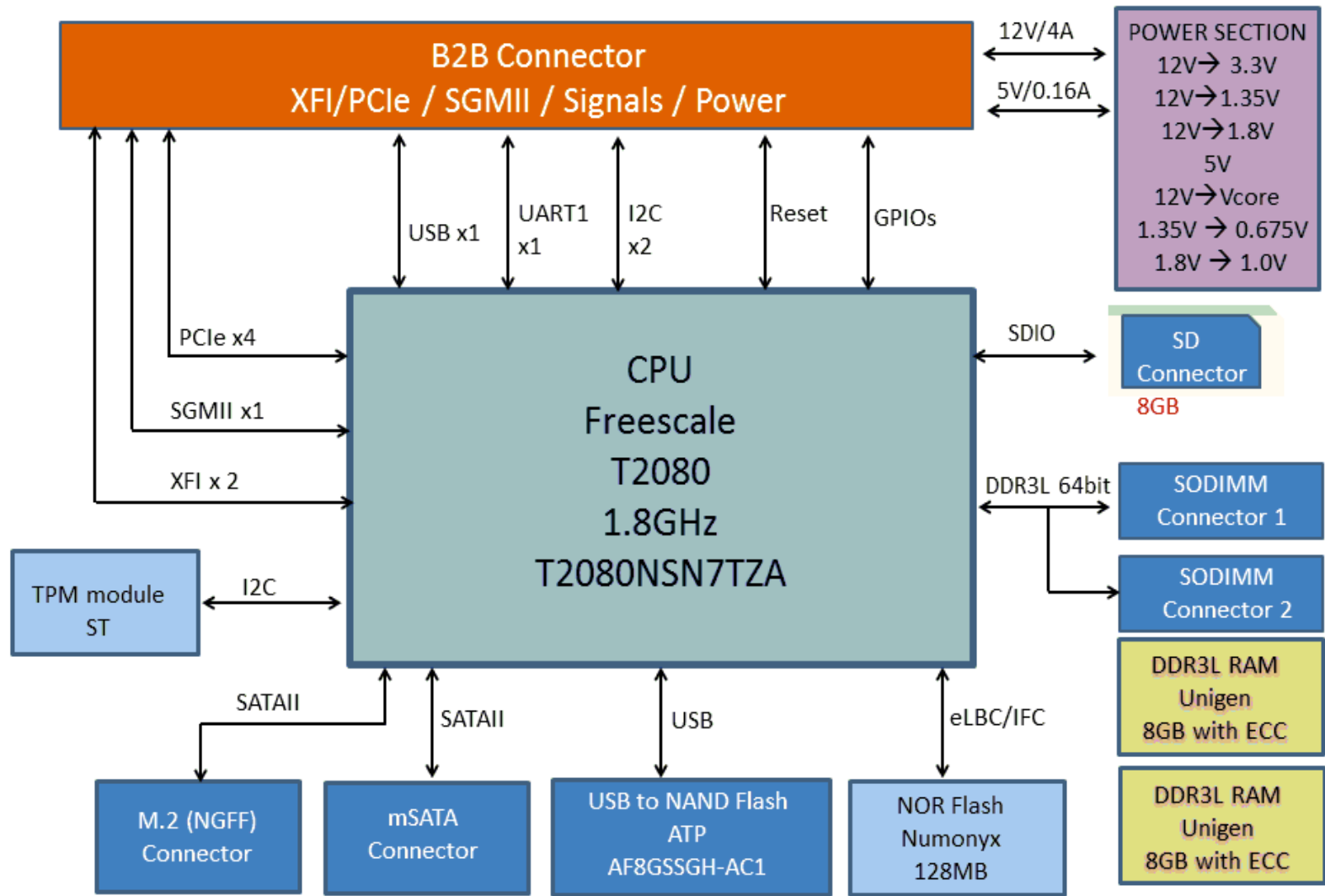
- 1. Change Version from R0B to R01

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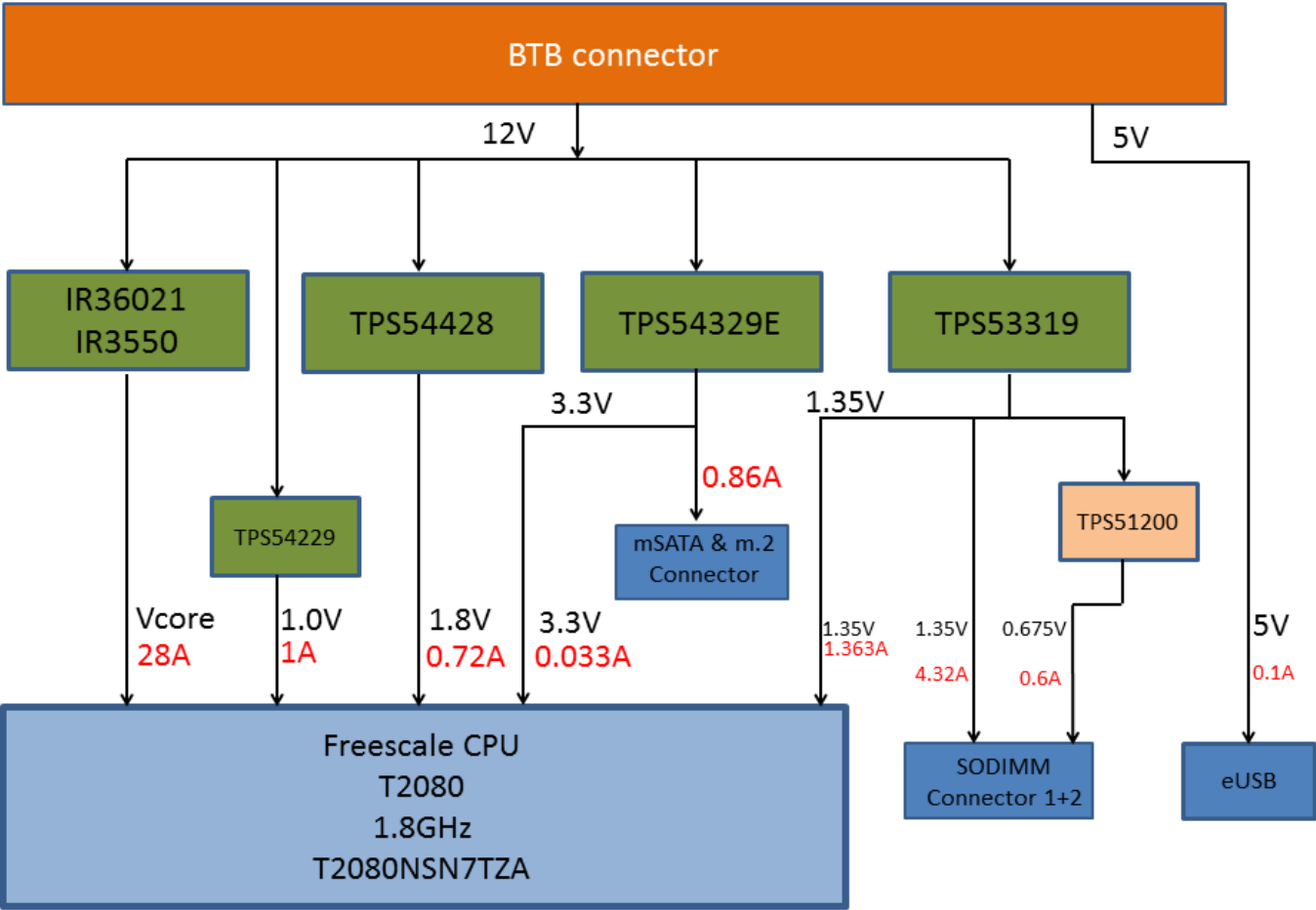


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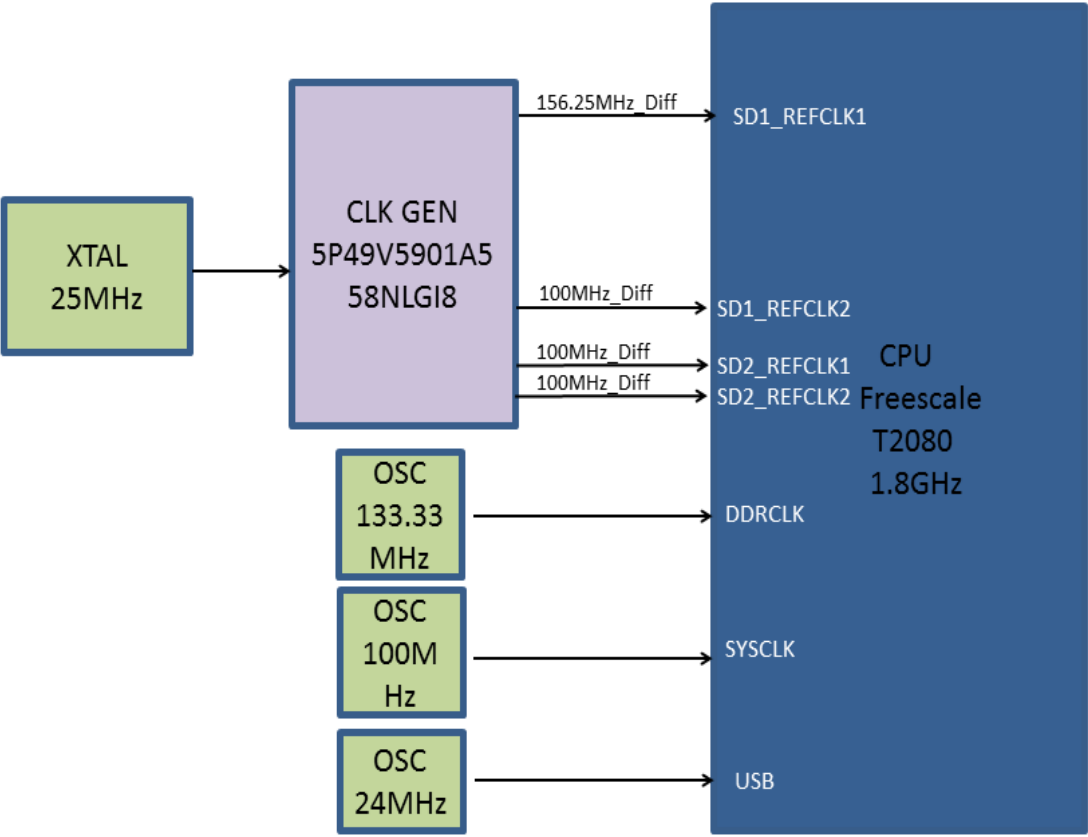


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C	Block Diagram	Jummy Huang
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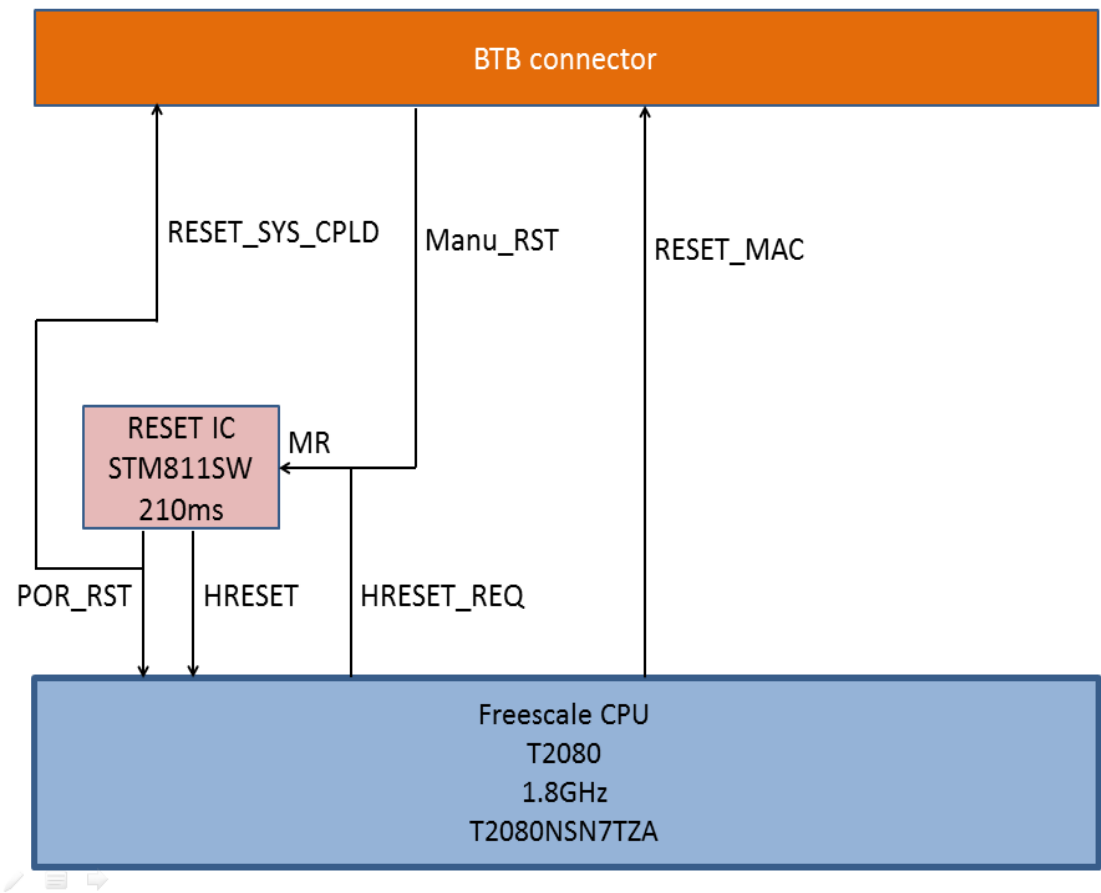


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Model Name ES7632BT-168AO		Rev R01
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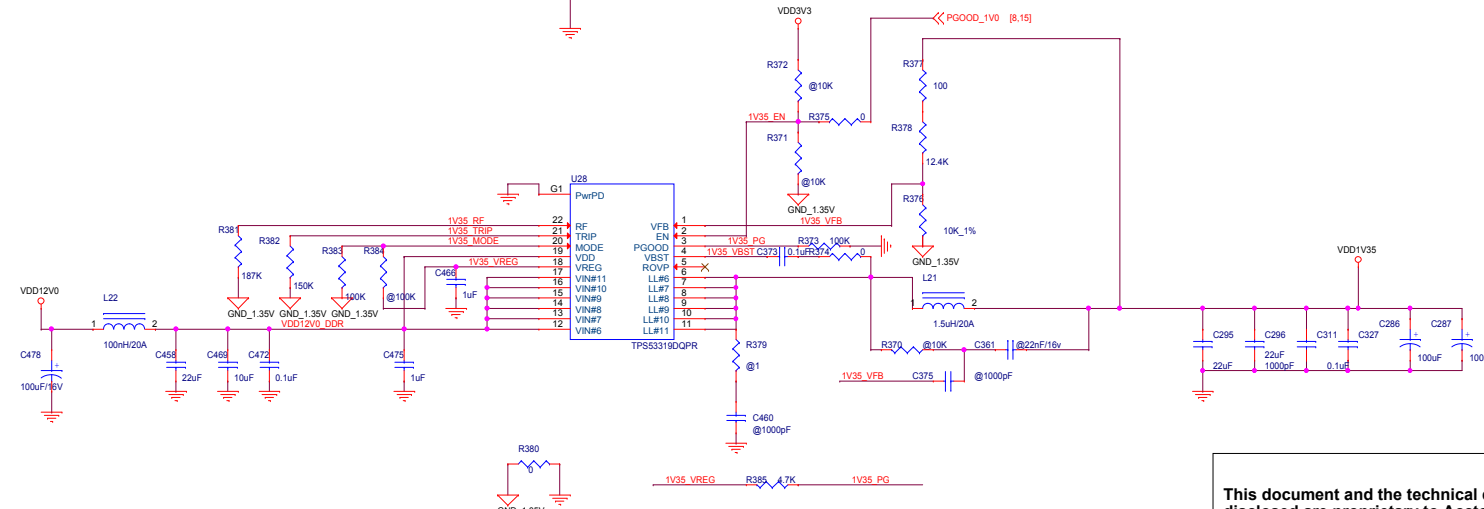
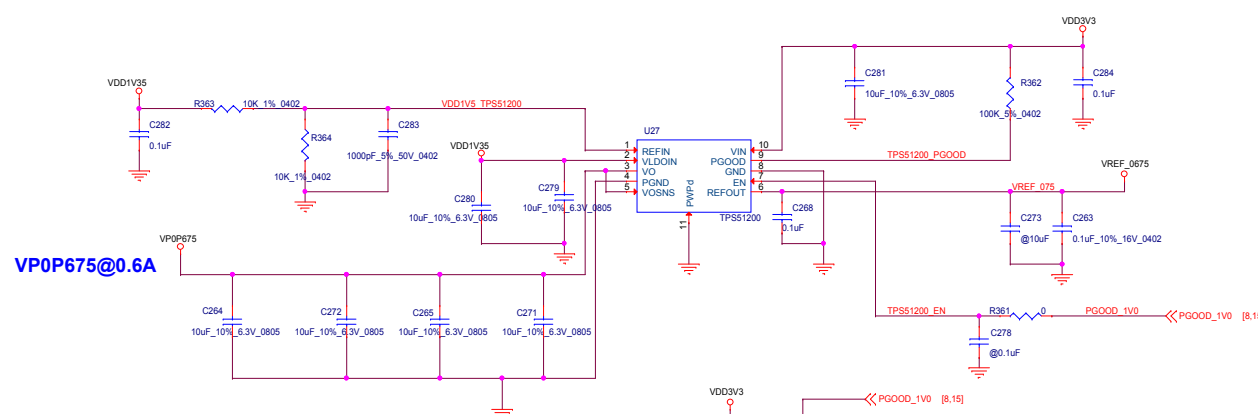
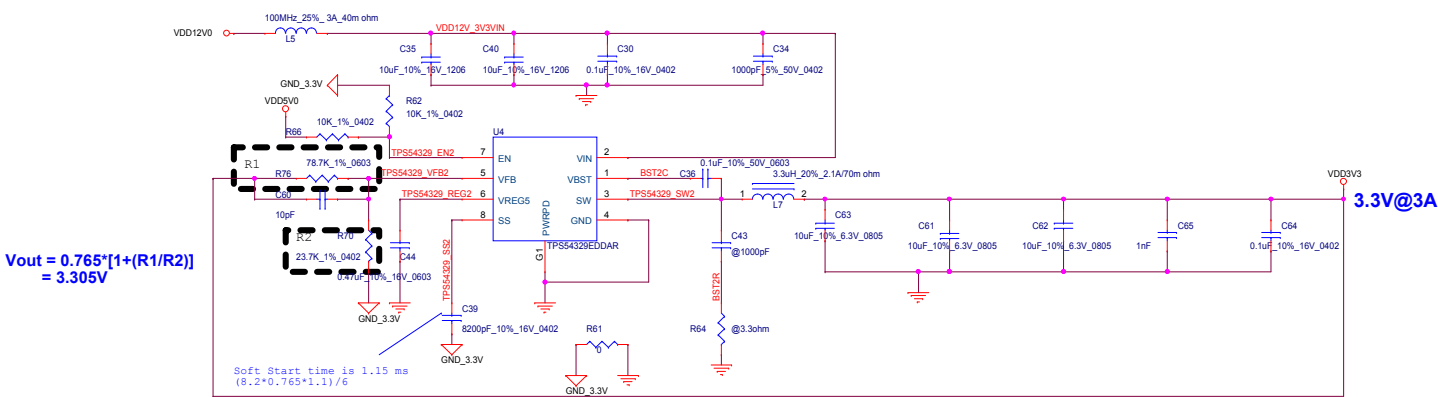
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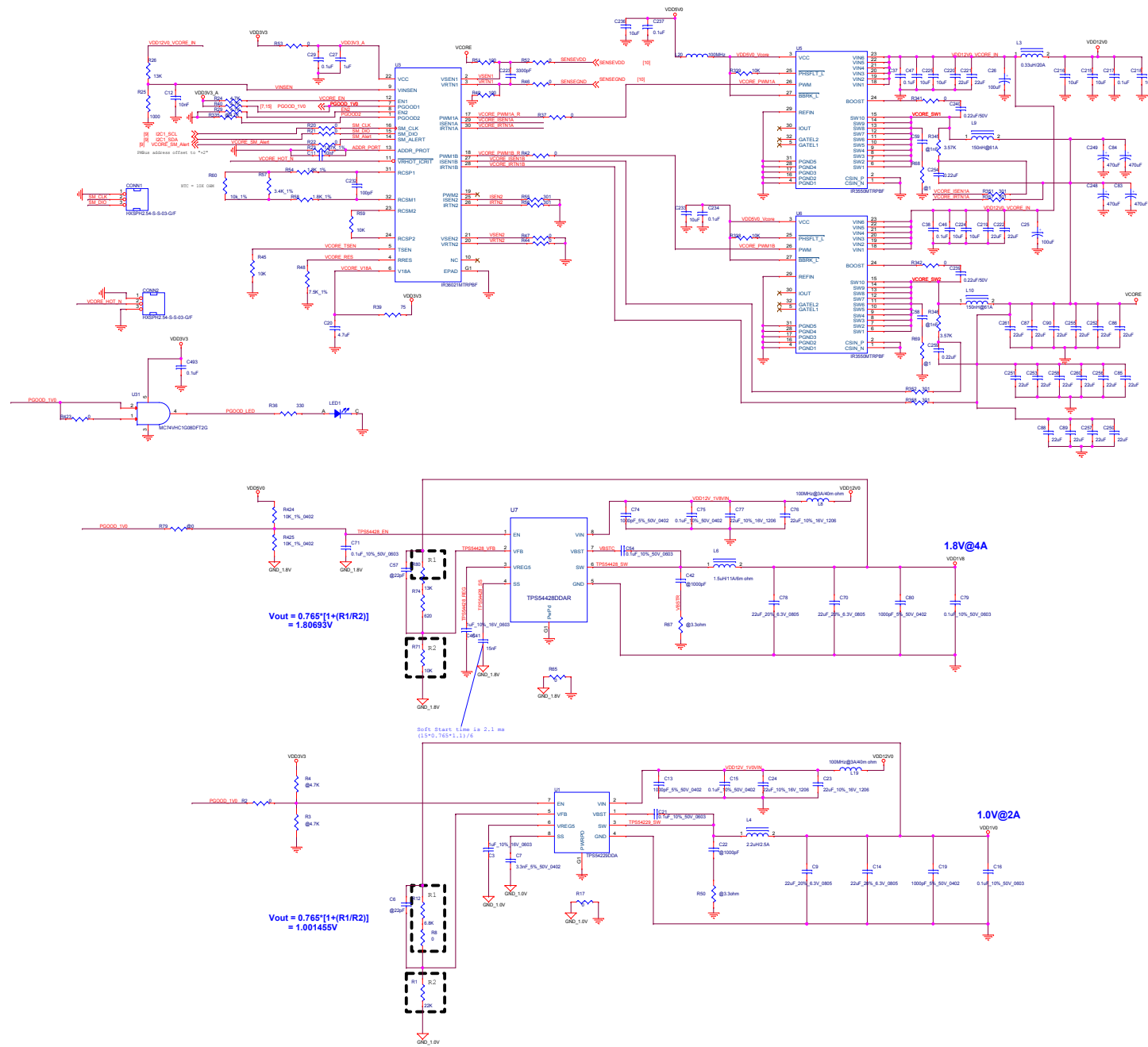
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Model Name ES7632BT-168AO		Rev R01
Size C	Page Name Reset Tree	Engineer Jummy Huang
Date:	Sheet	6 of 18

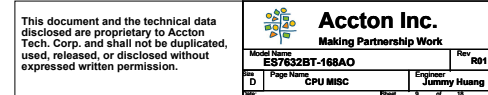
Power Up Sequence
Bring up VDD, SnVDD, USB_SVDD,VDD_LP,USB_HVDD,LVDD, DVDD, VCDD, USB_OVDD, OVDD, TH_VDD, AVDD, G1VDD, XnVDD and AVDD_SDn_PLLn



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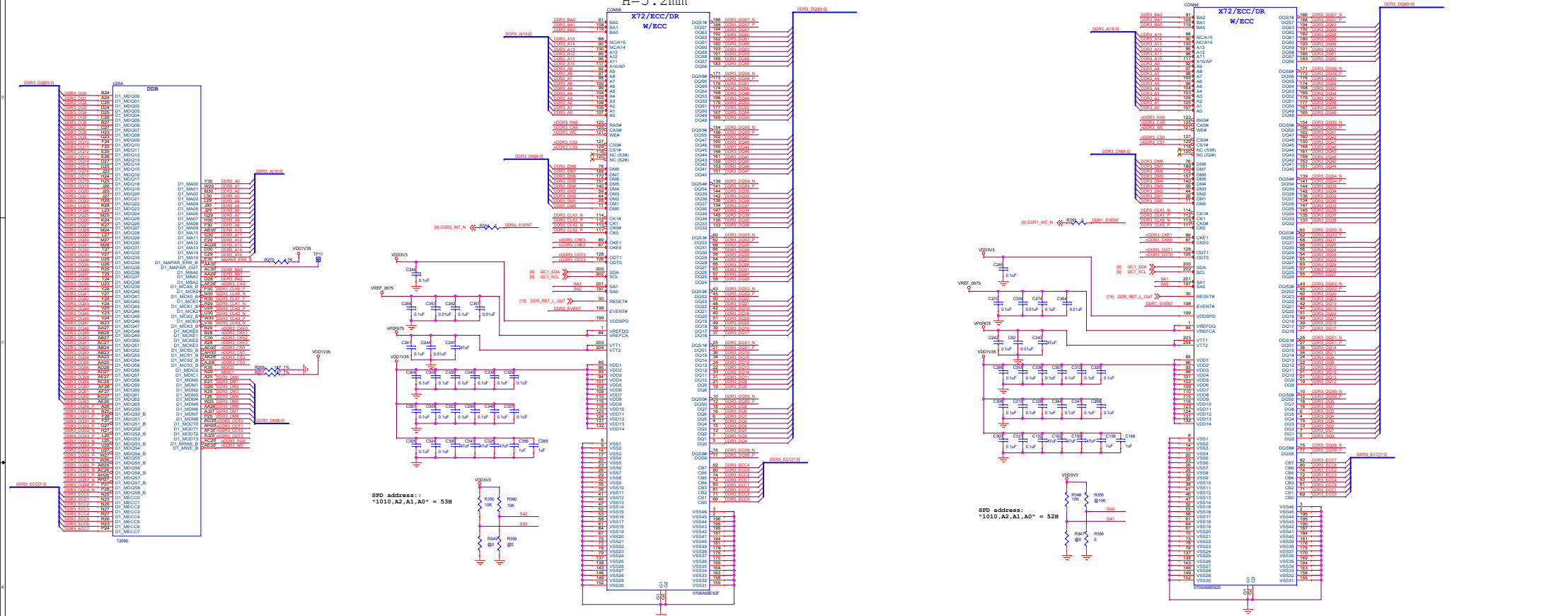
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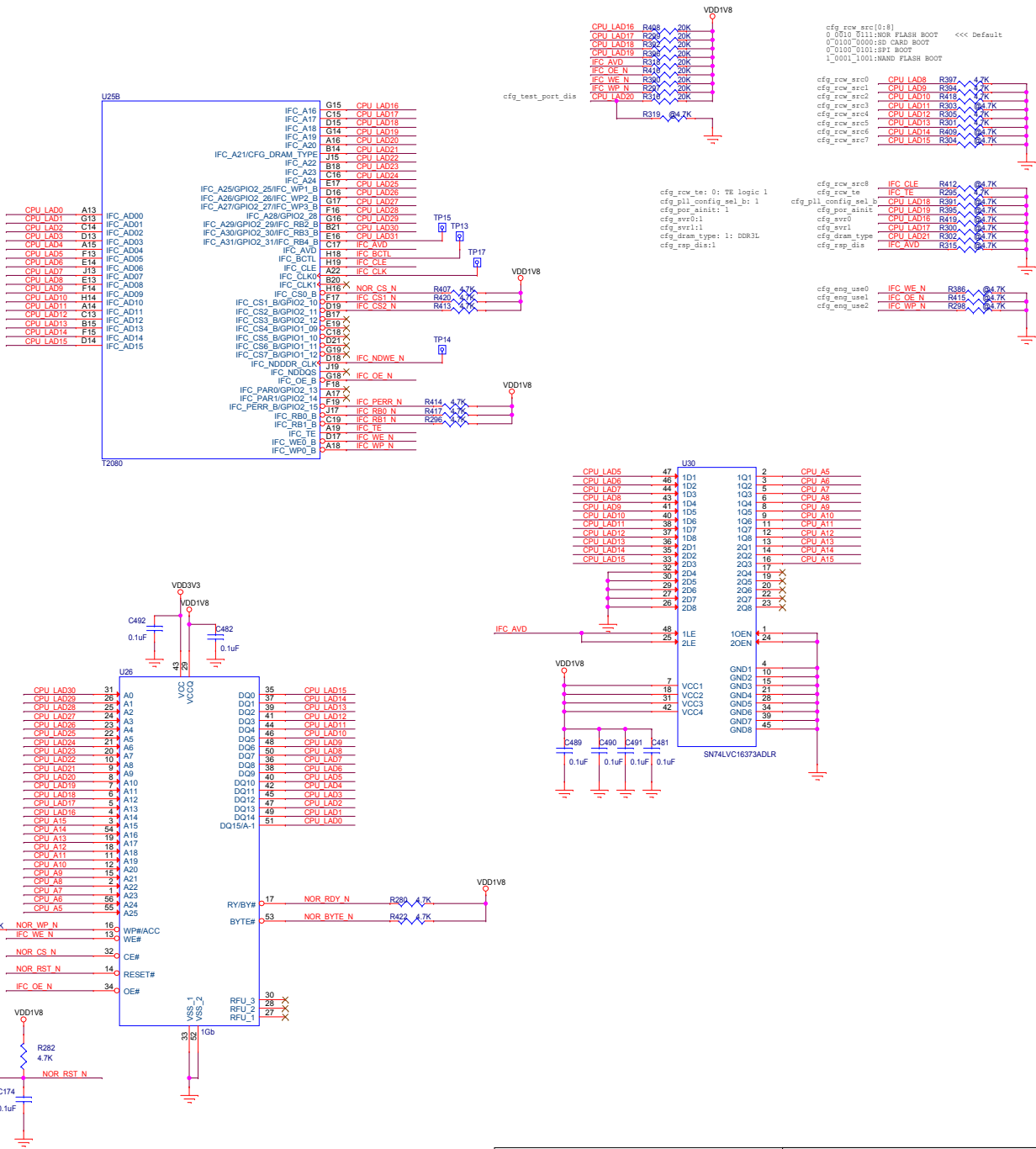




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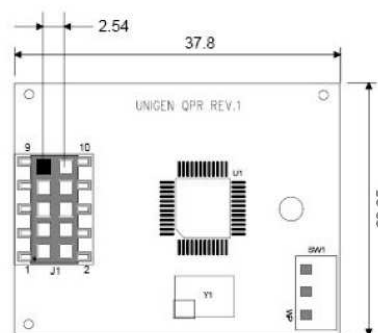
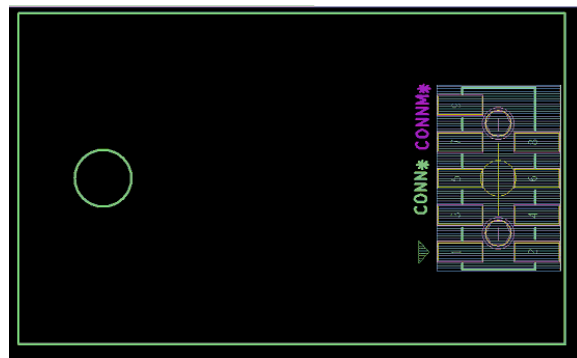
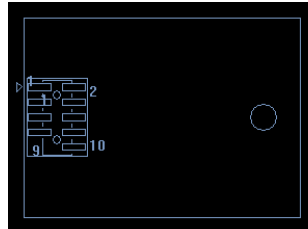
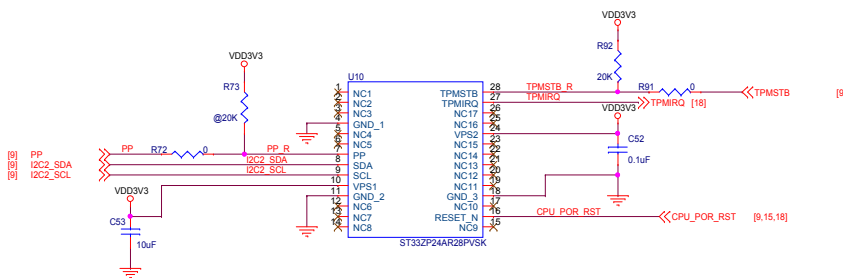


Table 2-2: 10 pin USB Connector Pin Assignments and Description

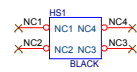
Pin No.	Signal	Signal Types	Function
1	VCC	PWR	Input Power
3	D-	I/O	Differential Signal
5	D+	I/O	Differential Signal
7	VSS	GND	Ground
9			Key
2,4,6,8		NC	No Connect
10	LED	I/O	Activity



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Heak Hink for T2080 (PUSH TYPE)
50mm x 50mm x 20mm

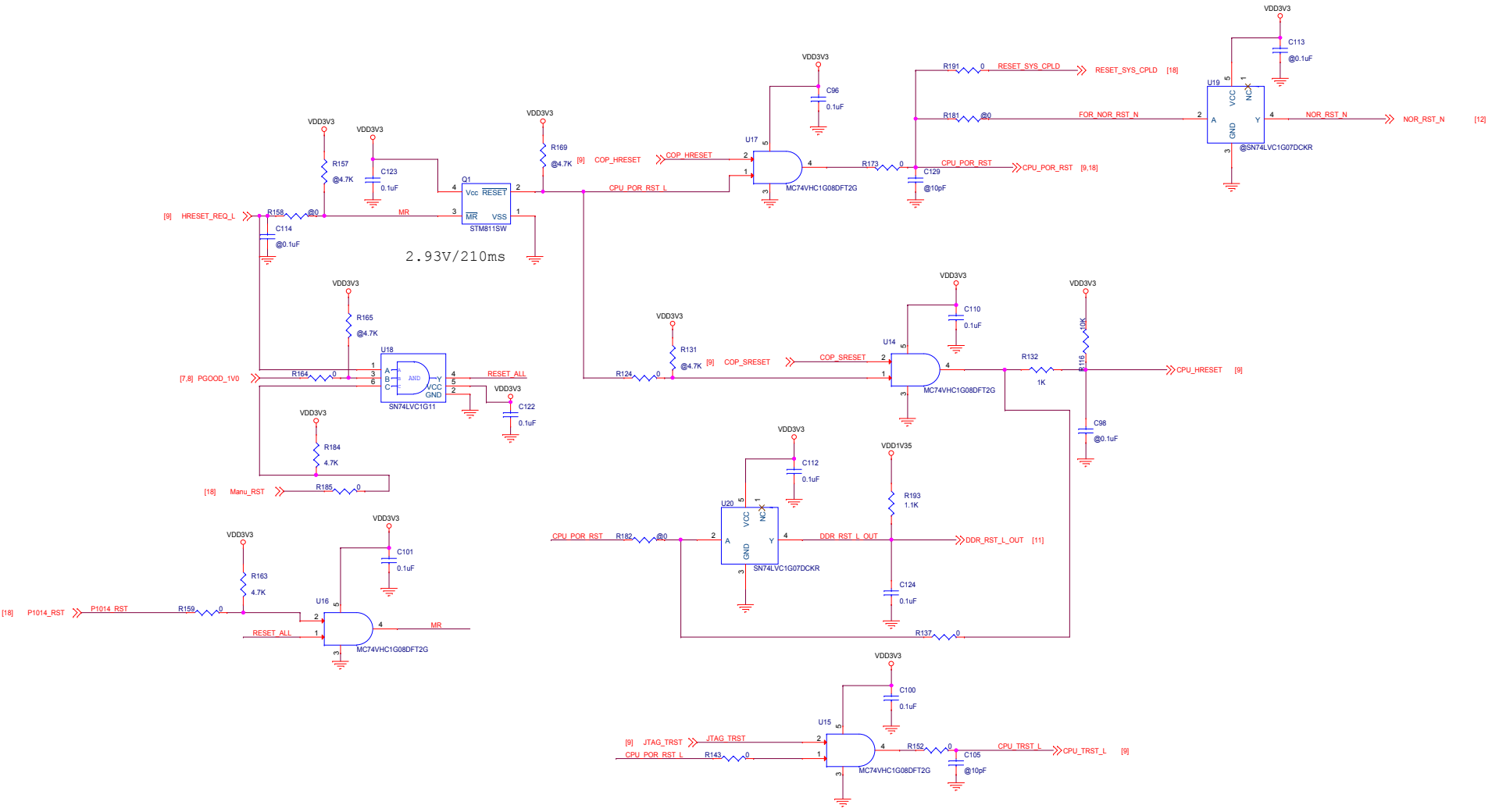


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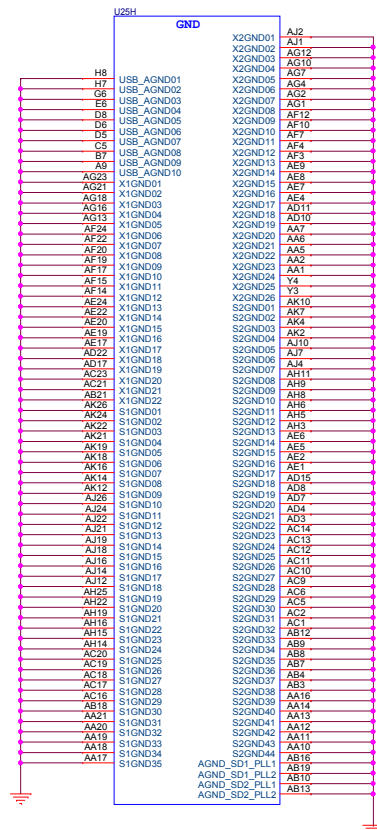
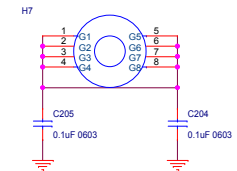


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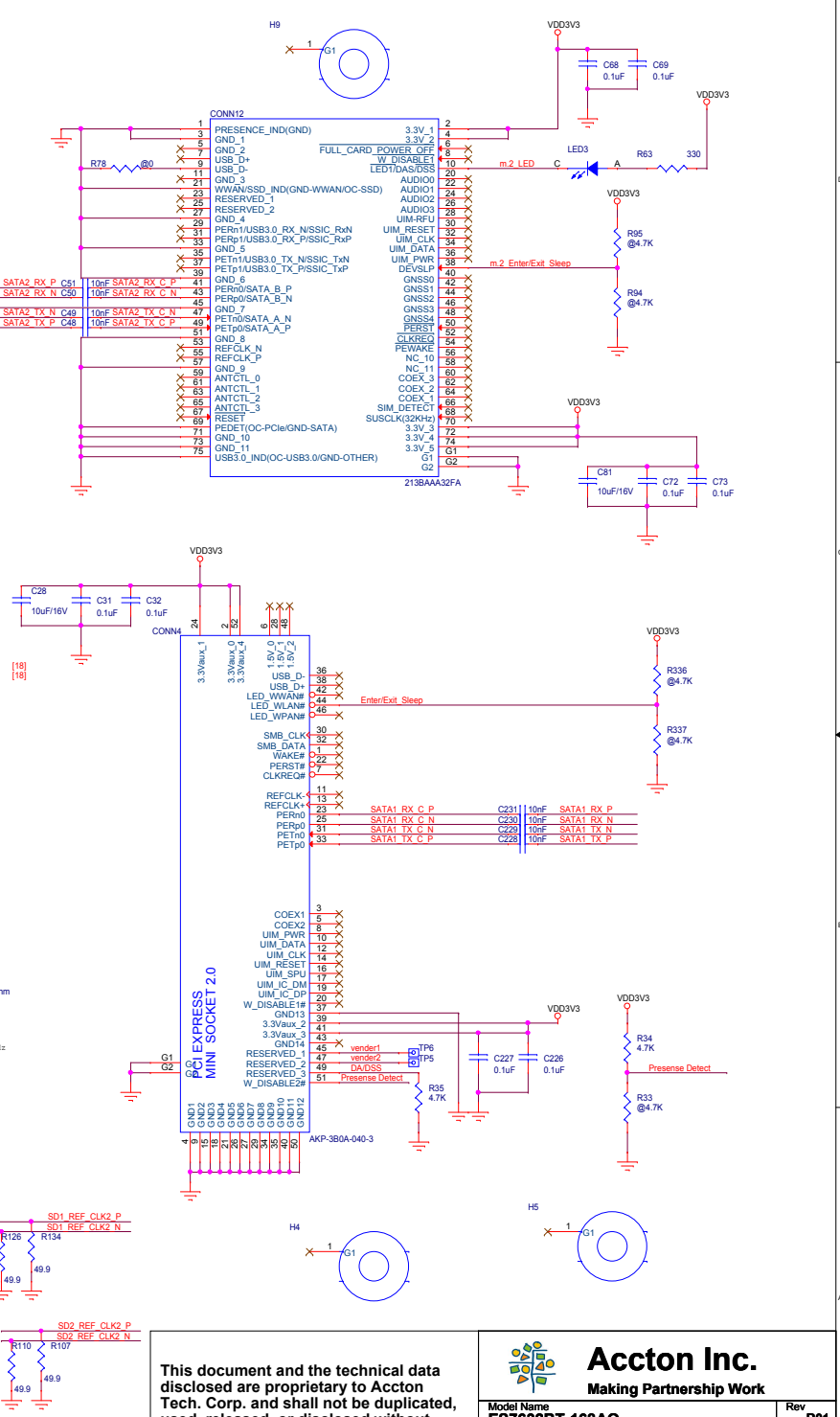
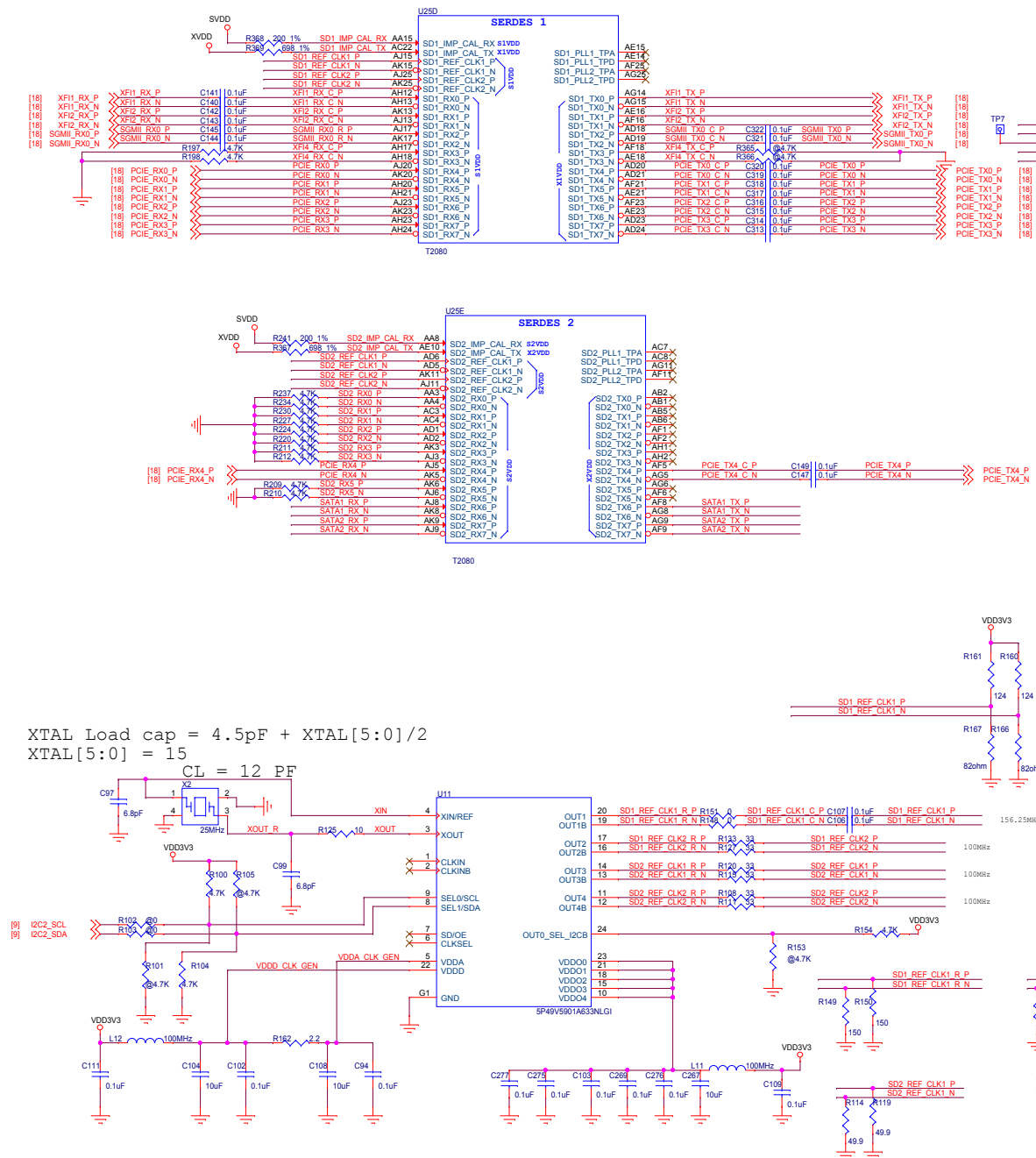


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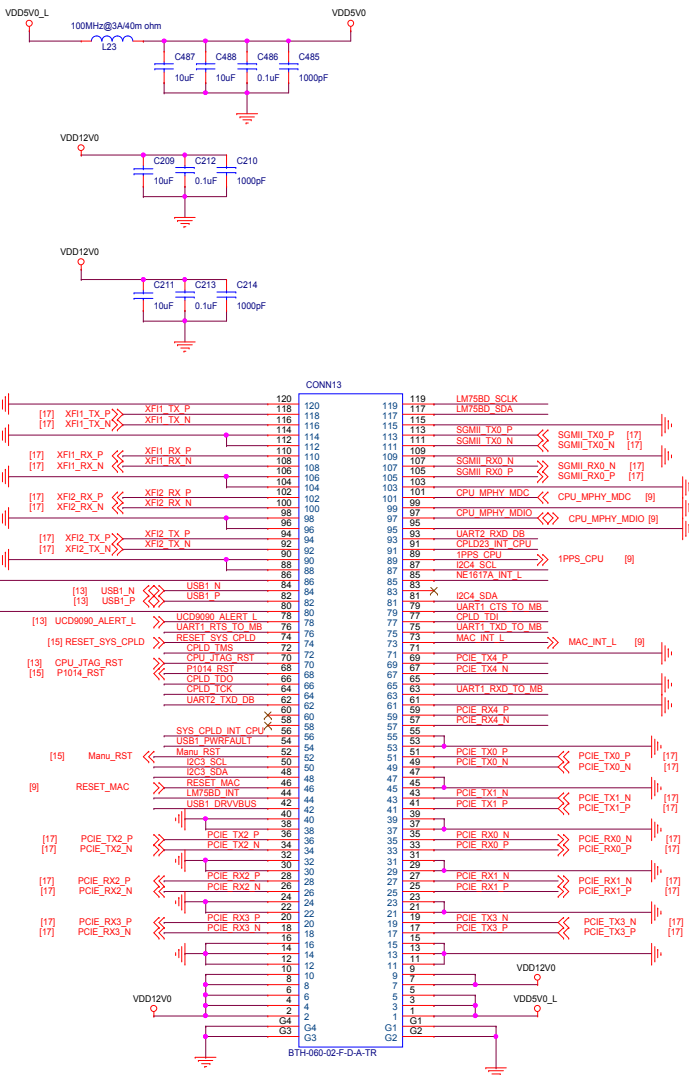
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Size	Page Name	Engineer
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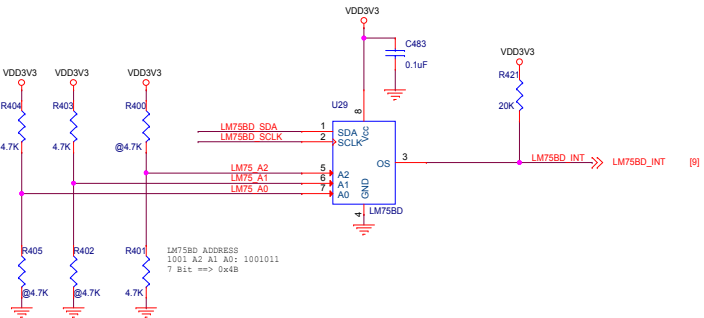


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USB1_DRVVBUS	USB1_DRVVBUS	[13]
USB1_PWRFAULT	USB1_PWRFAULT	[13]
UART1_CTS_TO_MB	UART1_CTS_TO_MB	[9]
UART1_RTS_TO_MB	UART1_RTS_TO_MB	[9]
UART1_RXD_TO_MB	UART1_RXD_TO_MB	[9]
UART1_TXD_TO_MB	UART1_TXD_TO_MB	[9]
CPD1_TDO	CPD1_TDO	[9]
CPD1_TMS	CPD1_TMS	[9]
CPD1_TCK	CPD1_TCK	[9]
CPD1_TDI	CPD1_TDI	[9]
UART2_RXD_DB	UART2_RXD_DB	[9]
UART2_TXD_DB	UART2_TXD_DB	[9]
NE1617A_INT_L	NE1617A_INT_L	[9]
IC23_SCL	IC23_SCL	[9]
IC23_SDA	IC23_SDA	[9]
IC24_SCL	IC24_SCL	[9]
IC24_SDA	IC24_SDA	[9]
XFH1_TX_P	XFH1_TX_P	[17]
XFH1_TX_N	XFH1_TX_N	[17]
XFH2_TX_P	XFH2_TX_P	[17]
XFH2_TX_N	XFH2_TX_N	[17]
XFH3_TX_P	XFH3_TX_P	[17]
XFH3_TX_N	XFH3_TX_N	[17]
SGMII_TX0_P	SGMII_TX0_P	[17]
SGMII_TX0_N	SGMII_TX0_N	[17]
SGMII_TX1_P	SGMII_TX1_P	[17]
SGMII_TX1_N	SGMII_TX1_N	[17]
SGMII_TX2_P	SGMII_TX2_P	[17]
SGMII_TX2_N	SGMII_TX2_N	[17]
SGMII_TX3_P	SGMII_TX3_P	[17]
SGMII_TX3_N	SGMII_TX3_N	[17]
SGMII_TX4_P	SGMII_TX4_P	[17]
SGMII_TX4_N	SGMII_TX4_N	[17]
CPU_MPHY_MDC	CPU_MPHY_MDC	[9]
CPU_MPHY_MDIO	CPU_MPHY_MDIO	[9]

CPD023_INT_CPU	CPD023_INT_CPU	[9]
SYS_CPLD_INT_CPU	SYS_CPLD_INT_CPU	[9]
PCIE_RX0_P	PCIE_RX0_P	[17]
PCIE_RX0_N	PCIE_RX0_N	[17]
PCIE_RX1_P	PCIE_RX1_P	[17]
PCIE_RX1_N	PCIE_RX1_N	[17]
PCIE_RX2_P	PCIE_RX2_P	[17]
PCIE_RX2_N	PCIE_RX2_N	[17]
PCIE_RX3_P	PCIE_RX3_P	[17]
PCIE_RX3_N	PCIE_RX3_N	[17]
PCIE_RX4_P	PCIE_RX4_P	[17]
PCIE_RX4_N	PCIE_RX4_N	[17]
XFH1_RX_P	XFH1_RX_P	[17]
XFH1_RX_N	XFH1_RX_N	[17]
XFH2_RX_P	XFH2_RX_P	[17]
XFH2_RX_N	XFH2_RX_N	[17]
SGMII_RX0_P	SGMII_RX0_P	[17]
SGMII_RX0_N	SGMII_RX0_N	[17]



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