



OPEN

Compute Project

DS1000 Ethernet Access Switch Hardware Specification

1.0

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2. OCP Tenets Compliance

2.1. Openness

The DS1000 is a totally open design with a detailed design specification and all design files needed to recreate the design contributed to Open Compute.

2.2. Efficiency

The DS1000 has been designed as a cost effective and energy efficient design consuming under 200W at peak consumption. The power supplies used with the DS1000 support the 80 PLUS platinum power efficiency rating (90+% efficiency)

2.3. Impact

The DS1000 will be the first OCP Accepted design contributed through the Enterprise Connectivity Solutions (ECS) group. This contribution is a useful Ethernet Access switch used in the Enterprise, can be used for follow on derivative works, as well as acting as a catalyst for other contributions to the ECS project.

2.4. Scale

The DS1000, although contributed through the ECS group as an Enterprise switch, may also be used as a rack management switch for the data center environment. This dual use case should lead to high volume deployments achieving significant scale in deployment.

3. Revision Table

Date	Revision #	Author	Description
October 17 2022	1.0	Jeff Catlin	Initial Release

4. Scope

This document defines technical specifications for the DS1000 Ethernet Access Switch platform used in Open Compute Project. This document, along with the product design package shall comprise product's technical specification.

5. Overview

DS1000 is an Ethernet Access switch providing connectivity and aggregation services for 1G/10G attached devices. DS1000 support 48x1Gb RJ45 Ethernet ports and 8XSFP 10Gb Ethernet ports. There are numerous use cases for DS1000 including use as a cost effective in-rack management switch for data center use or a cost effective Enterprise switch. The DS1000 supports an x86 CPU complex with sufficient resources to run add-on applications in addition to the standard NOS.



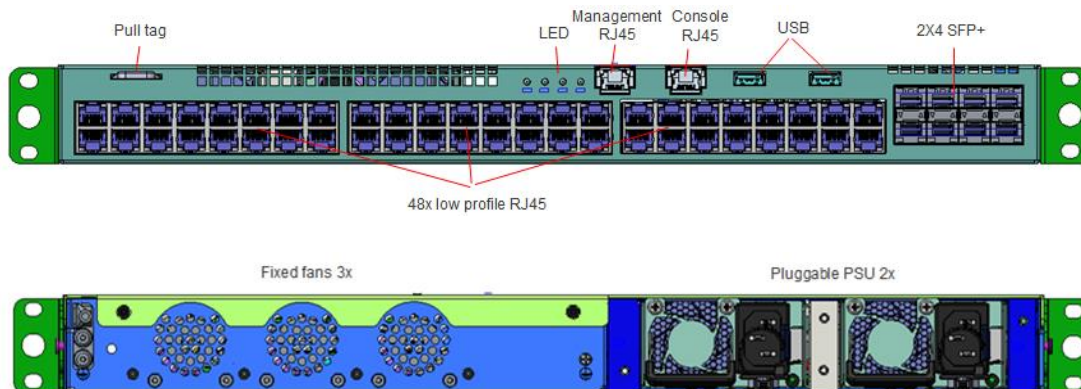
6. Rack Compatibility

DS1000 is designed to mount in a standard 19 inch equipment rack which can be accomplished by rack standard mounting “ears” or a snap in rail kit

7. Physical Specifications

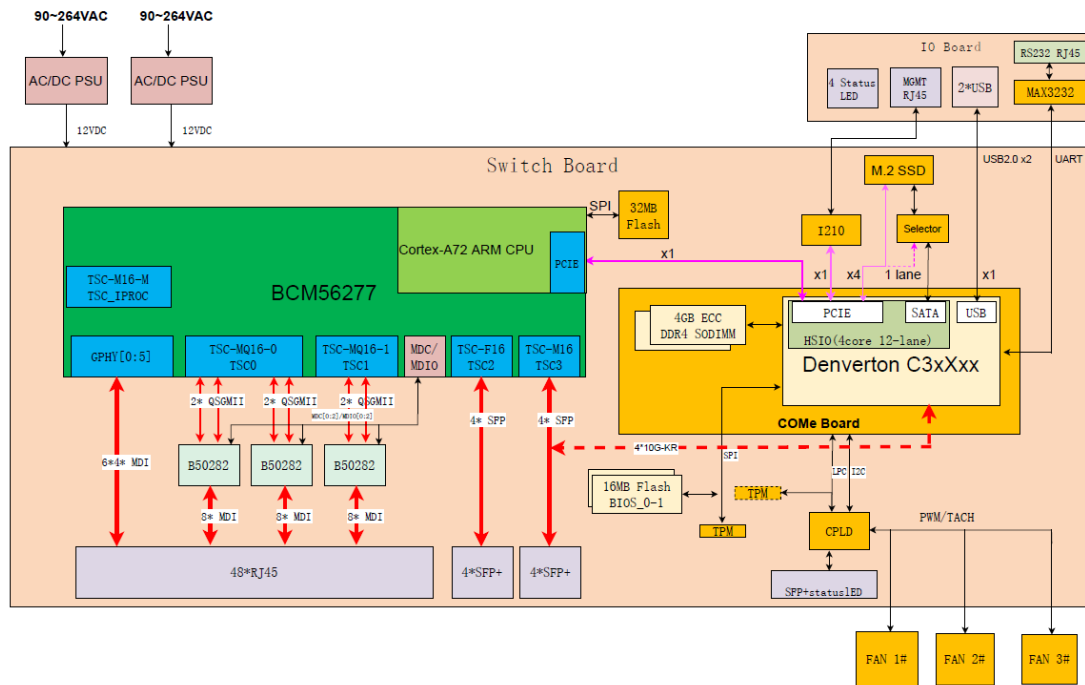
DS1000 front panel and rear panel views are shown below

Feature	Description
Dimension	438.5mm (W) X 43.6mm (1RU) (H) X 370mm (D)
Port	48 x 10/100/1000Base-T RJ45 Copper ports 8 x SFP+ 10Gigabit fiber ports 1 x Console Port base on RJ45 1 x Out of band management port base on 10/100/1000M RJ45 2 x Type A USB 2.0 ports



DS1000 Front Panel and Rear Panel

DS1000 Block Diagram



DS1000 System PCB overview

The DS1000 system is composed of three PCB assemblies as follows:

- Switch Board which includes the switching silicon, networking ports, power supply connections, and system fan connections
- COM-E Board supporting an Intel x86 Denverton CPU
- I/O Board supporting the front panel management ports and system LEDs

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Switch Board Stack up

Stackup Control Table

...	Structure		Material					Vendor proposed				Celestica Proposed				Vendor Proposed			
Layer	Type	Thickness (mil)	2-Ply Required	PCB Material	Fibre Type	Copper Weight (oz)	DK (for Simulation)	Fibre Type/Copper Weight (oz)	Thickness (mil)	copper foil type	DK (@25G)	Impedance spec (Ohms)	Reference layer	Width (/space) mil	Sim Z0	Impedance spec (Ohms)	Reference layer	Width (/space) mil	Sim Z0
	SM	0.50			SM		4.25		4.50										
1	TOP	1.90				0.5 oz + plating (HTE +plating)		8.50	1.90	HTE		S50±10%	2	6.2	50.3	S50±10%	2	6	50.0
												D85±10%	2	6/5.5	85.4	D85±10%	2	6/5.5	85.0
												D92±10%	2	5.2/6	92.1	D92±10%	2	5.2/6	92.0
												D100±10%	2	4.2/6	99.8	D100±10%	2	4.2/6	100.0
												D100±10%/Neckdown	2	3.5/4.7	99.8	D100±10%/Neckdown	2	3.5/4.7	101.0
	Prepreg	4.00	N	S100K-2 / IT-400A	Vendor Proposal		4.00	2112*1	3.54		4.16								
2	GND1	1.20				1 oz(RTF)		1.20	1.20	HTE									
	Core	6.00	N	S100K-2 / IT-400A	Vendor Proposal		4.00	2116*1	5.12		3.93								
3	SIG1	1.20				1 oz(RTF)		1.20	1.20	HTE		S50±10%	284	5	49.73	S50±10%	284	4.7	50
												D85±10%	284	6/7.5	84.92	D85±10%	284	5.7/7.8	85.2
												D92±10%	284	5.2/8.4	91.97	D92±10%	284	4.9/8.7	92.3
												D100±10%	284	4.2/8	99.88	D100±10%	284	3.9/8.3	100.3
												D92±10%/Neckdown	284	3.4/4.4	95.7				
												D100±10%/Neckdown	284	3.5/5.5	99.83	D100±10%/Neckdown	284	3.2/5.8	100.4
	Prepreg	6.00	Y	S100K-2 / IT-400A	Vendor Proposal		4.00	2112*2	7.60		4.16								
4	GND2	1.20				1 oz(RTF)		1.20	1.20	HTE									
	Core	6.00	Y	S100K-2 / IT-400A	Vendor Proposal		4.00	2116*2	17.9		4.55								
5	PWR1	1.20				1 oz(RTF)		1.20	1.20	HTE									
	Prepreg	15.00	Y	S100K-2 / IT-400A	Vendor Proposal		4.00	2116*3	15.33		4.18								
6	PWR2	1.20				1 oz(RTF)		1.20	1.20	HTE									
	Core	6.00	Y	S100K-2 / IT-400A	Vendor Proposal		4.00	2116*2	17.9		4.55								
7	GND3	1.20				1 oz(RTF)		1.20	1.20	HTE									
	Prepreg	6.00	Y	S100K-2 / IT-400A	Vendor Proposal		4.00	2112*2	7.60		4.16								
8	SIG2	1.20				1 oz(RTF)		1.20	1.20	HTE		S50±10%	789	5	49.73	S50±10%	789	4.7	50
												D85±10%	789	6/7.5	84.92	D85±10%	789	5.7/7.8	85.2
												D92±10%	789	5.2/8.4	91.97	D92±10%	789	4.9/8.7	92.3
												D100±10%	789	4.2/8	99.88	D100±10%	789	3.9/8.3	100.3
												D92±10%/Neckdown	789	3.4/4.4	95.7				
												D100±10%/Neckdown	789	3.5/5.5	99.83	D100±10%/Neckdown	789	3.2/5.8	100.4
	Core	6.00	N	S100K-2 / IT-400A	Vendor Proposal		4.00	2116*1	5.12		3.93								
9	GND4	1.20				1 oz(RTF)		1.20	1.20	HTE									
	Prepreg	4.00	N	S100K-2 / IT-400A	Vendor Proposal		4.00	2112*1	3.54		4.16								
10	BOTTOM	1.90				0.5 oz + plating (HTE +plating)		8.50	1.90	HTE		S50±10%	9	6.2	50.3	S50±10%	9	6	50.0
												D85±10%	9	6/5.5	85.4	D85±10%	9	6/5.5	85.0
												D92±10%	9	5.2/6	92.1	D92±10%	9	5.2/6	92.0
												D100±10%	9	4.2/6	99.8	D100±10%	9	4.2/6	100.0
												D100±10%/Neckdown	9	3.5/4.7	99.8	D100±10%/Neckdown	9	3.5/4.7	101.0
	SM	0.50			SM		4.25												
	Board Thickness:	77.40							77.71										
		1.97							1.97										

This is a detailed architectural floor plan of the first floor of a building. The plan is oriented with North at the top. It features a large central hall with a grid of rooms, a long corridor on the left, and a complex arrangement of rooms and service areas on the right. Rooms are numbered 1 through 22. The plan includes walls, doors, windows, and furniture like desks and chairs. A scale bar at the bottom indicates dimensions in meters.

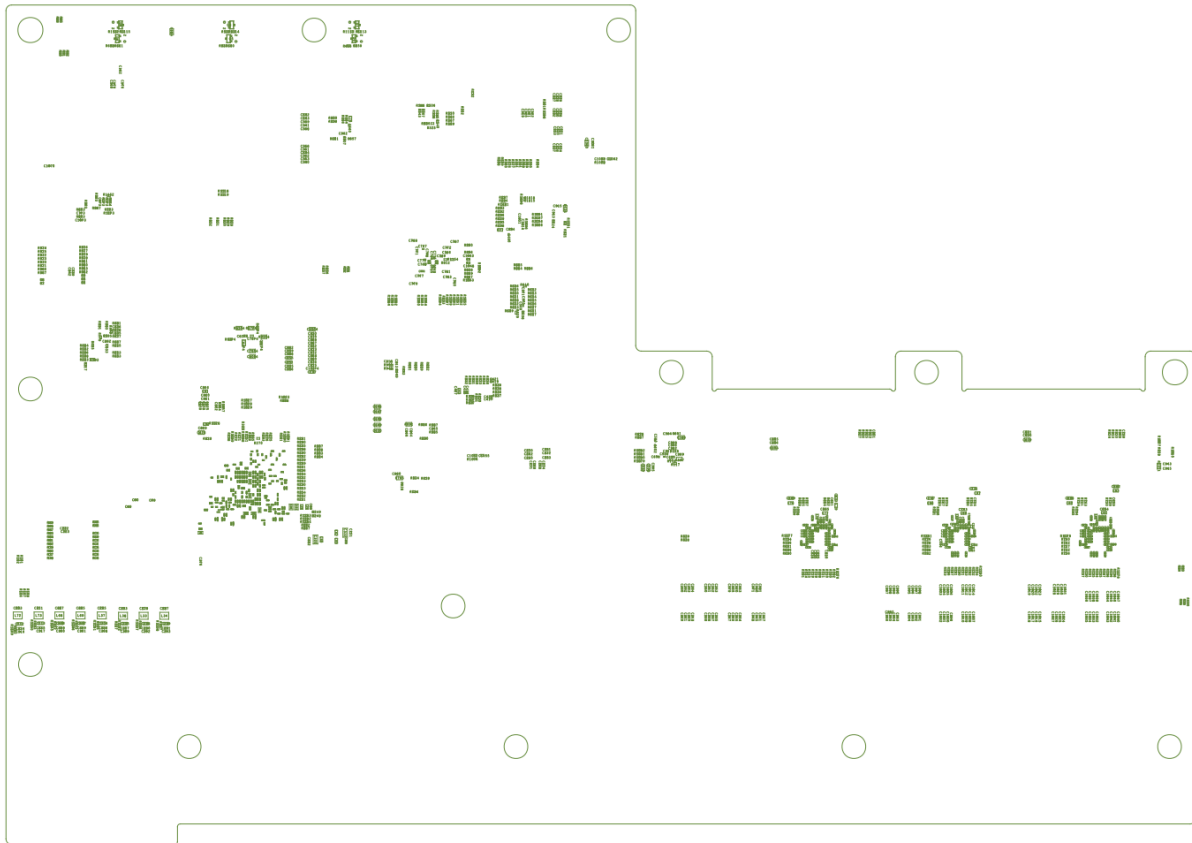
Room Numbers and Locations:

- 1: Large central hall
- 2: Room at the top left
- 3: Room at the top center
- 4: Room at the top right
- 5: Room at the middle left
- 6: Room at the middle center
- 7: Room at the middle right
- 8: Room at the bottom left
- 9: Room at the bottom center
- 10: Room at the bottom right
- 11: Room at the top left (smaller)
- 12: Room at the top center (smaller)
- 13: Room at the top right (smaller)
- 14: Room at the middle left (smaller)
- 15: Room at the middle center (smaller)
- 16: Room at the middle right (smaller)
- 17: Room at the bottom left (smaller)
- 18: Room at the bottom center (smaller)
- 19: Room at the bottom right (smaller)
- 20: Room at the top left (smaller)
- 21: Room at the top center (smaller)
- 22: Room at the top right (smaller)

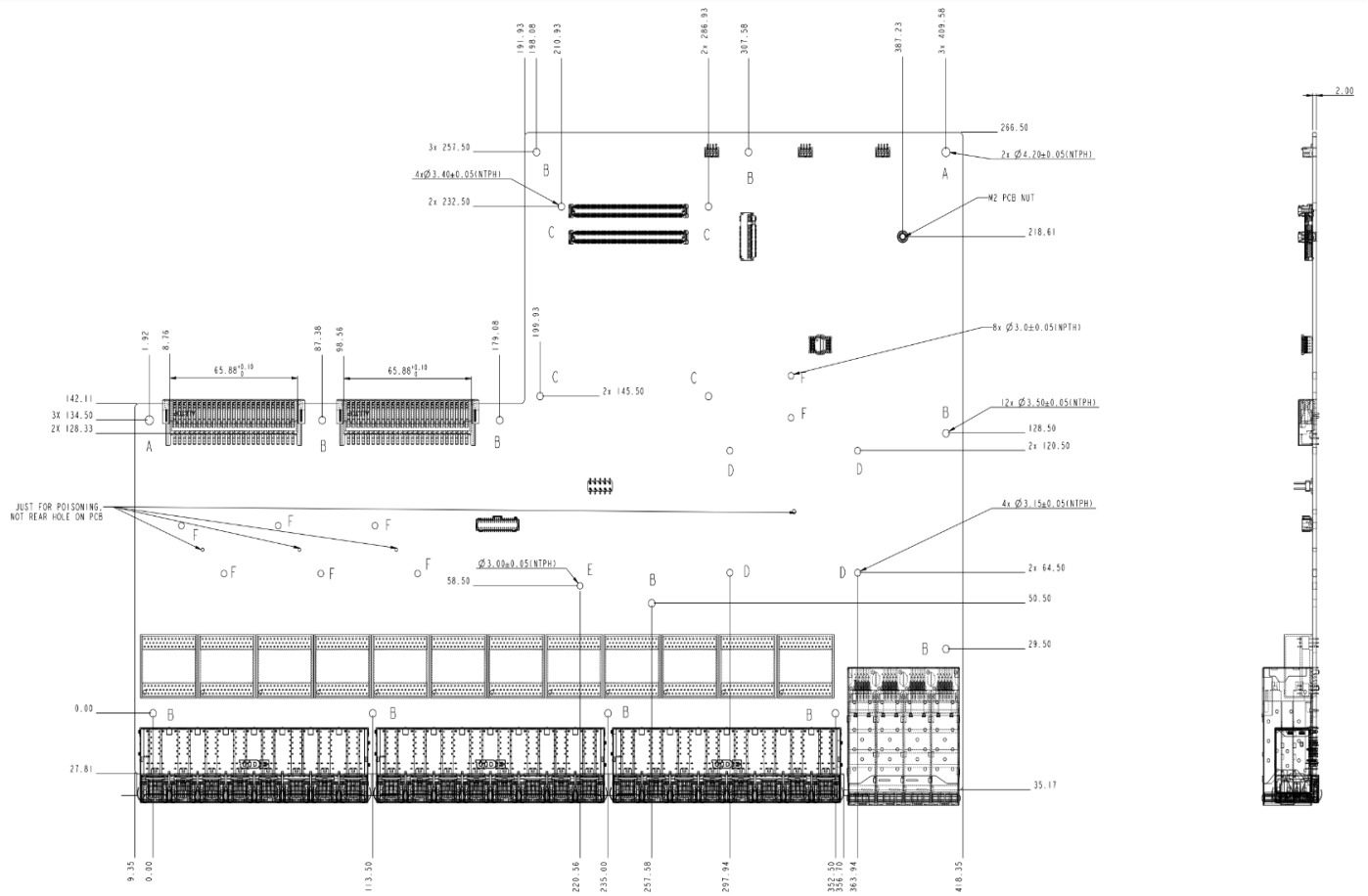
Scale Bar:

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

Switch Board Placement Bottom Side

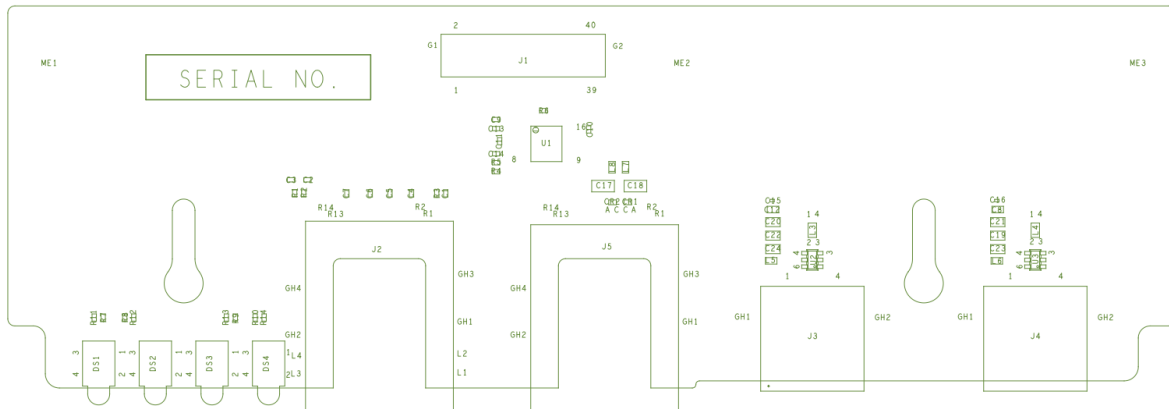


Switch Board Mechanical

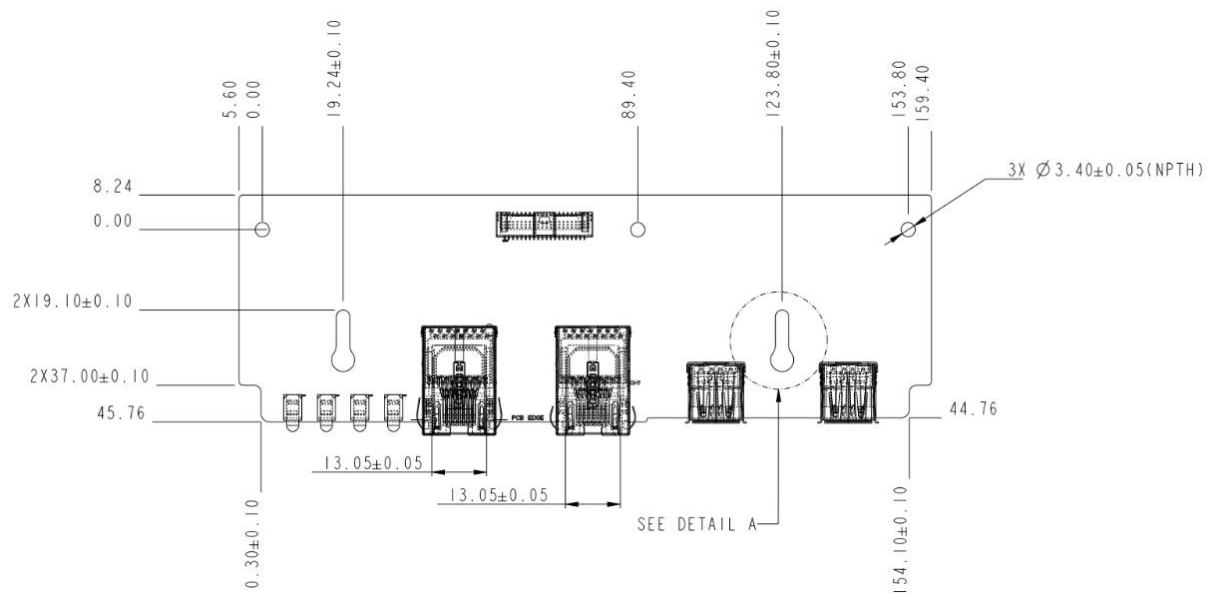


I/O Module Stack UP

I/O Board Placement



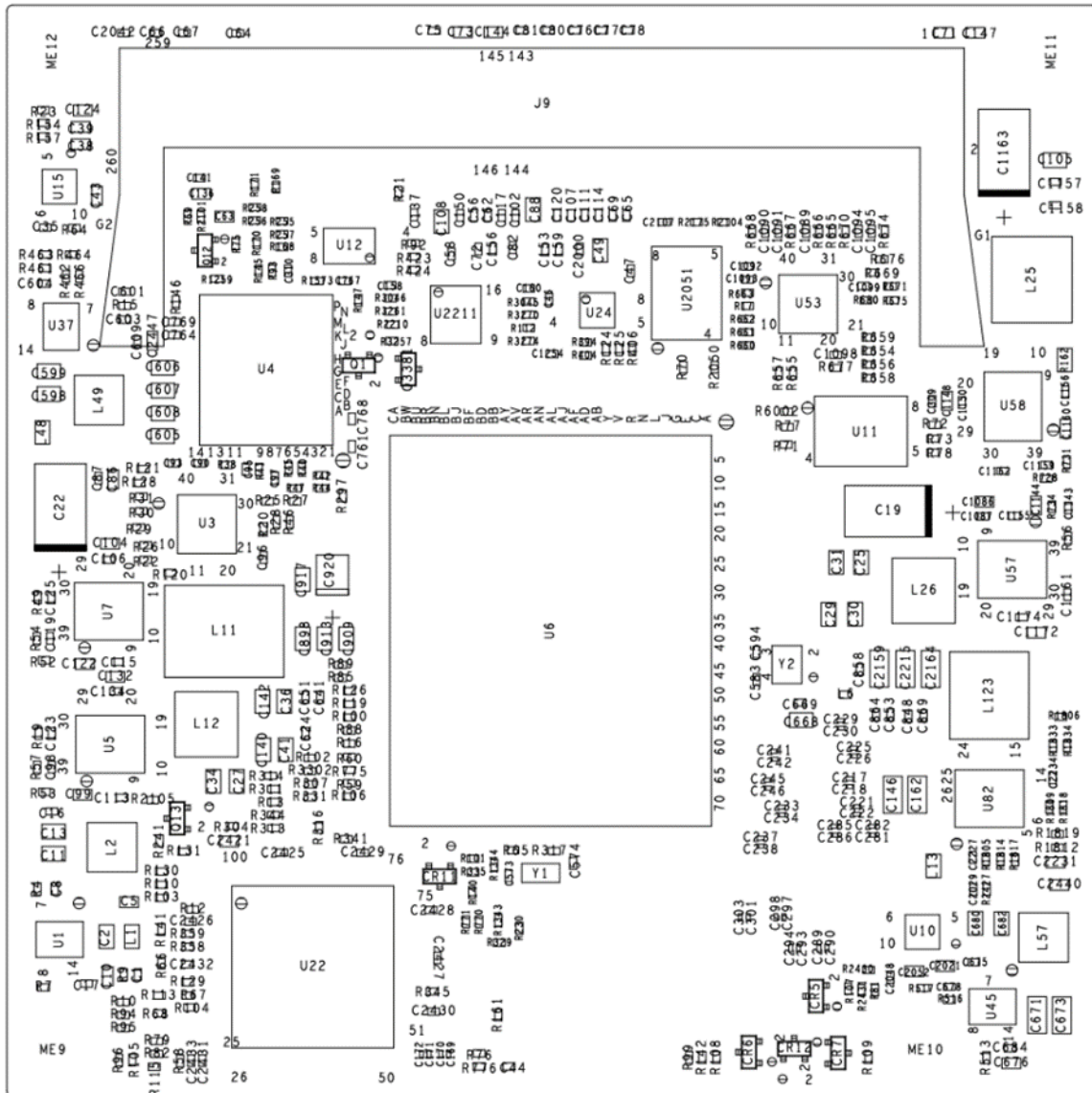
I/O Board Mechanical



CPU Module Stack UP

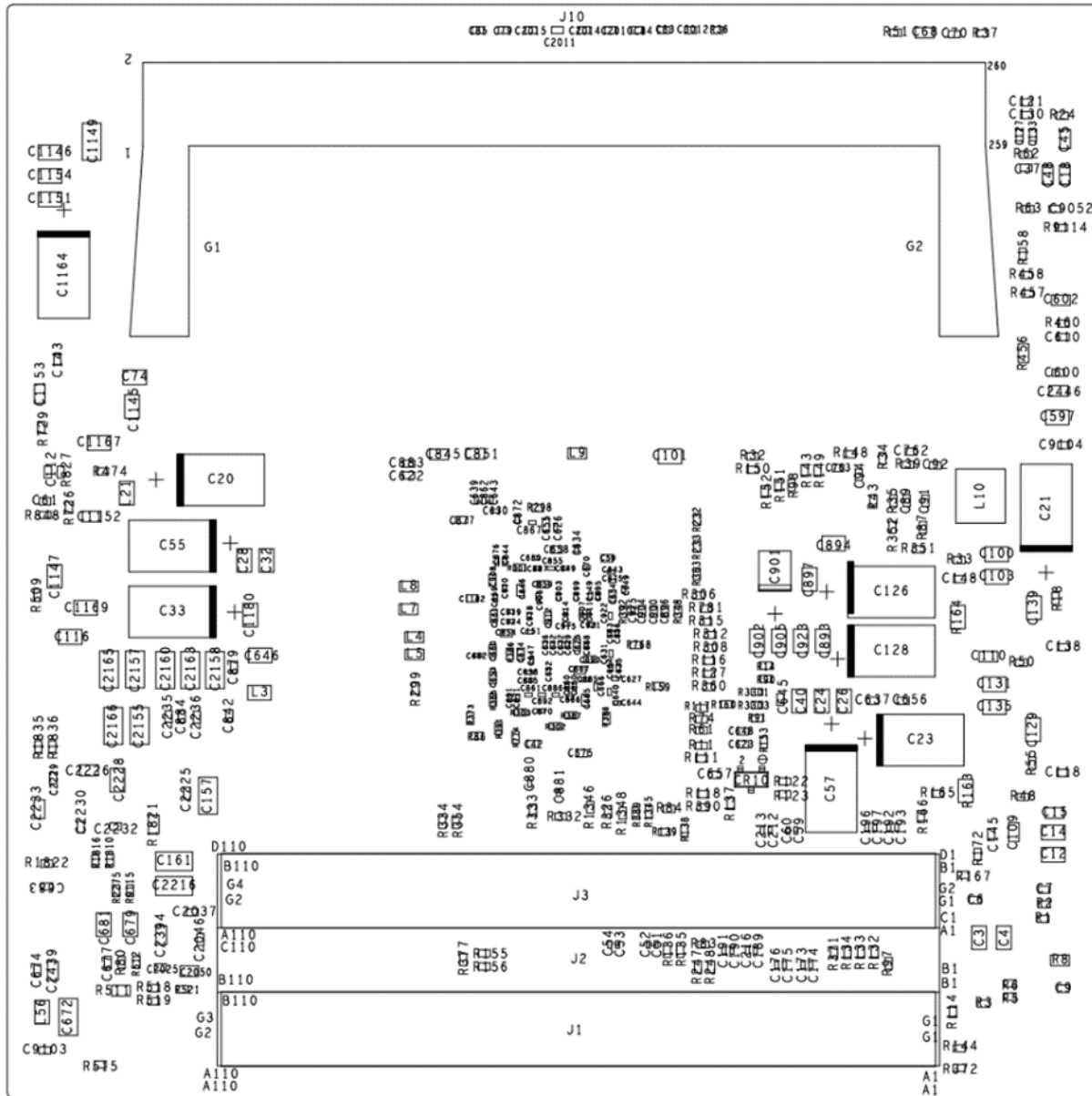
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CPU Board Placement Top Side



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CPU Board Placement Bottom Side

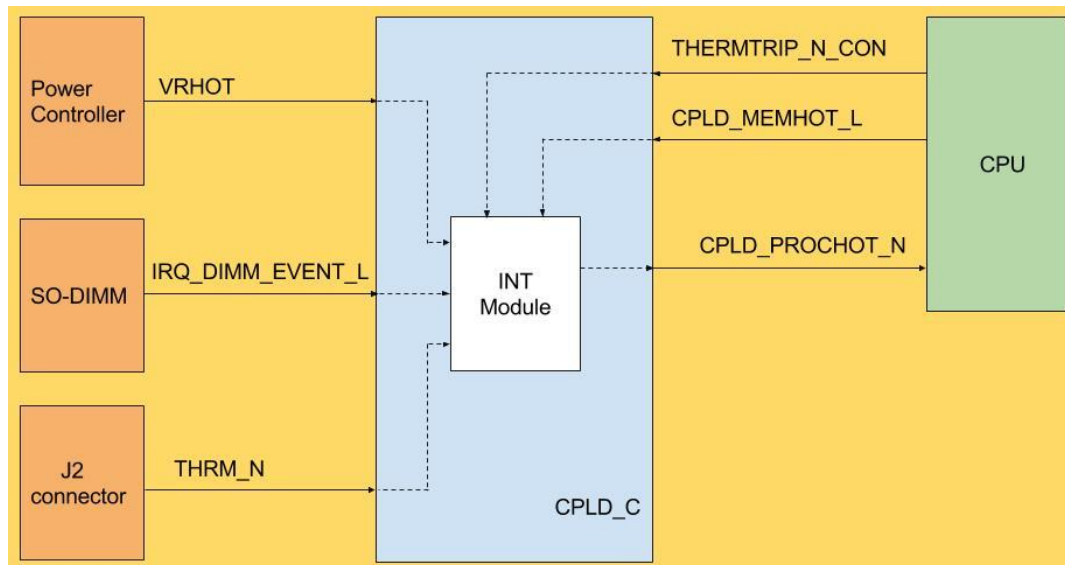


8. Thermal Design Requirements

DS1000 is designed to operate in a temperature controlled environment ranging from 0-45C. The following sections outline the thermal management capabilities of DS1000. The DS1000 is offered with front to back airflow and back to front airflow options.

Thermal Control

A CPLD will report thermal information to CPU based on the following figure.

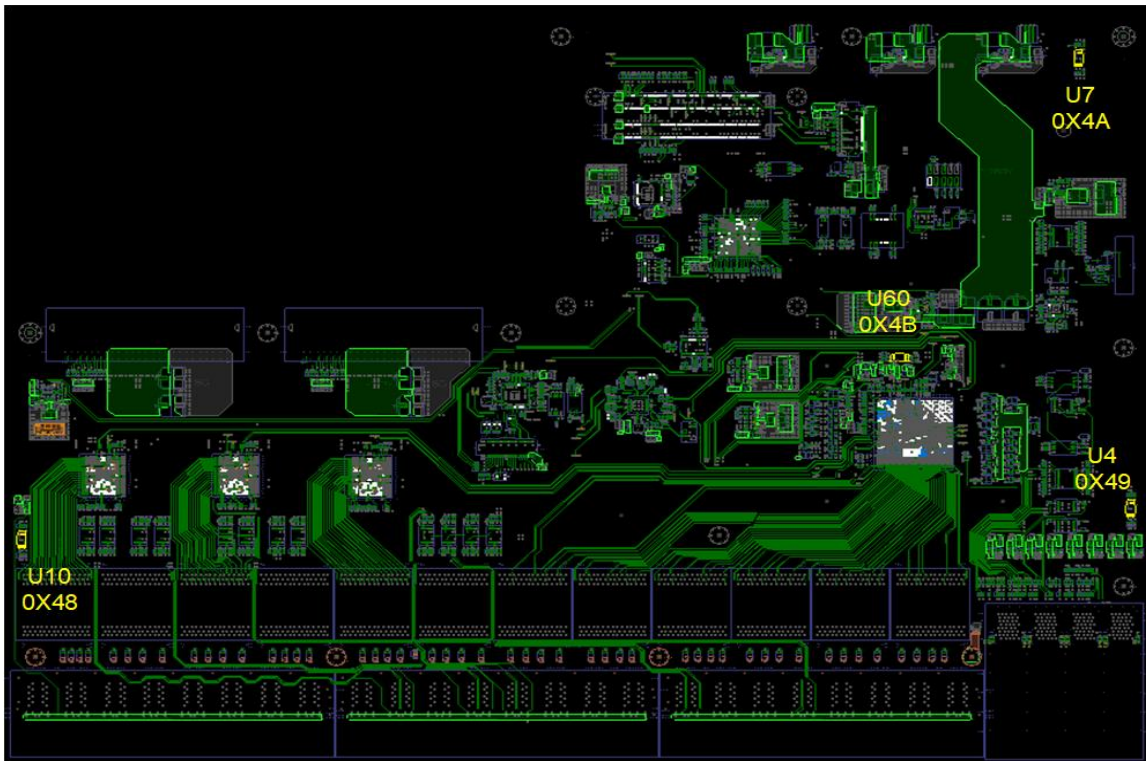


Thermal logic

CPLD manages the following thermal source,

- 'VRHOT' from memory power controller PXE1110JPM
- 'VRHOT' from CPU Core power controller PXE1110JPM
- 'CPLD_MEMHOT_L' from CPU
- 'THERMTRIP_N' from CPU
- 'THRM_N' from Carrier board
- 'IRQ_DIMM_EVENT_L' from DDR4 SO-DIMM

DS1000 supports four temperature sensors located on the main switch PCB that are used to determine temperature status of the system. The four temperature sensor locations are shown in the following diagram.



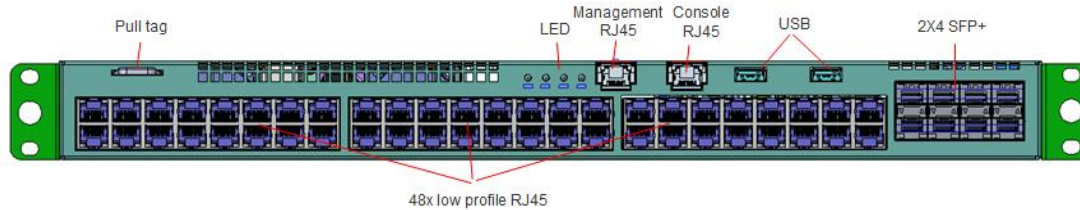
Sensor Location on Switch board

When any one of the thermal threshold values are exceeded, a fault condition shall be alerted, and the fan speed will go up to full speed immediately.

Temperature Threshold

	Item	Description	Low Warning	High Warning	Soft Shutdown	Hard Shutdown
SwitchBoard(F2R)	1	Inlet sensor (the lower temperature of U4 and U10)	-5	50	N/A	N/A
Switch Board(R2F)	2	Inlet sensor U7	-5	50	N/A	N/A
COMe Board	3	CPU Internal Sensor	N/A	88	91	94
Switch Board	4	BCM56277 Inlet Sensor	N/A	100	105	110

9. I/O System



COM-E CPU Module

DS1000 supports a modular CPU following the COM-E type 7 module standard. The CPU module supports an Intel Denverton C3538 x86 CPU and associated circuitry.

CPU Module Major Components

The COM-E CPU module supports the following major components

Description	Vendor	Part Number
System CPU	Intel	C3538
CPLD	Lattice	LCMXO2-1200HC-4TG100C
I2C EEPROM 64Kbit	Giantec	GT24C64A-2ZLI-TR
Connector SODIMM	Lotus	ADDR0206-P001A
Connector SODIMM	Foxconn	AS0A821-H2SB-7H
Connector 220P	TE Connectivity LTD	3-6318490-6

CPU Module Connector Pinout

Usage in COM-E	Type 7 Pin name	Type 6 Pin name	Pin No	Pin No	Type 6 Pin name	Type 7 Pin name	Usage in COM-E
GND	GND(FIXED)	GND	A1	B1	GND	GND(FIXED)	GND
NC	GBE0_MDI3-	GBE0_MDI3-	A2	B2	GBE0_ACT#	GBE0_ACT#	NC
NC	GBE0_MDI3+	GBE0_MDI3+	A3	B3	LPC_FRAME#	LPC_FRAME#/ESPI_CS0#	Connect to CPU LPC_FRAME# AND CPLD
NC	GBE0_LINK100#	GBE0_LINK100#	A4	B4	LPC_AD0	LPC_AD0/ESPI_IO_0	Connect to CPU LPC_AD0 AND CPLD
NC	GBE0_LINK1000#	GBE0_LINK1000#	A5	B5	LPC_AD1	LPC_AD1/ESPI_IO_1	Connect to CPU LPC_AD1 AND CPLD
NC	GBE0_MDI2-	GBE0_MDI2-	A6	B6	LPC_AD2	LPC_AD2/ESPI_IO_2	Connect to CPU LPC_AD2 AND CPLD
NC	GBE0_MDI2+	GBE0_MDI2+	A7	B7	LPC_AD3	LPC_AD3/ESPI_IO_3	Connect to CPU LPC_AD3 AND CPLD
NC	GBE0_LINK#	GBE0_LINK#	A8	B8	LPC_DRQ0#	LPC_DRQ0#/ESPI_ALERT0#	NC
NC	GBE0_MDI1-	GBE0_MDI1-	A9	B9	LPC_DRQ1#	LPC_DRQ1#/ESPI_ALERT1#	NC
NC	GBE0_MDI1+	GBE0_MDI1+	A10	B10	LPC_LCK	LPC_CLK/ESPI_CK	TO CPU ESPI_CLK AND CPLD
GND	GND(FIXED)	GND	A11	B11	GND	GND(FIXED)	GND
NC	GBE0_MDI0-	GBE0_MDI0-	A12	B12	PWRBTN#	PWRBTN#	Connect to CPU PWRBTN# AND CPLD
NC	GBE0_MDI0+	GBE0_MDI0+	A13	B13	SMB_CK	SMB_CK	Connect to CPU SMB_CK

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NC	GBE0_CTREF	GBE0_CTREF	A14	B14	SMB_DAT	SMB_DAT	Connect to CPU SMB_DAT
SUS_S3# TO CPU AND CPLD	SUS_S3#	SUS_S3#	A15	B15	SMB_ALERT#	SMB_ALERT#	Connect to CPU SMB_ALERT#
CPU Sata 0	SATA0_TX+	SATA0_TX+	A16	B16	SATA1_TX+	SATA1_TX+	CPU Sata 1
CPU Sata 0	SATA0_TX-	SATA0_TX-	A17	B17	SATA1_TX-	SATA1_TX-	CPU Sata 1
SUS_S4# AND A24, TO CPU AND CPLD	SUS_S4#	SUS_S4#	A18	B18	SUS_STAT#	SUS_STAT#/ESPI_RESET#	SUS_STAT# TO CPU AND CPLD
CPU Sata 0	SATA0_RX+	SATA0_RX+	A19	B19	SATA1_RX+	SATA1_RX+	CPU Sata 1
CPU Sata 0	SATA0_RX-	SATA0_RX-	A20	B20	SATA1_RX-	SATA1_RX-	CPU Sata 1
GND	GND(FIXED)	GND	A21	B21	GND	GND(FIXED)	GND
NC	PCIE_TX15+	SATA2_TX+	A22	B22	SATA3_TX+	PCIE_RX15+	NC
NC	PCIE_TX15-	SATA2_TX-	A23	B23	SATA3_TX-	PCIE_RX15-	NC
SUS_S5# AND A18, TO CPU AND CPLD	SUS_S5#	SUS_S5#	A24	B24	PWR_OK	PWR_OK	Connect to CPLD
NC	PCIE_TX14+	SATA2_RX+	A25	B25	SATA3_RX+	PCIE_RX14+	NC
NC	PCIE_TX14-	SATA2_RX-	A26	B26	SATA3_RX-	PCIE_RX14-	NC
NC	BATLOW#	BATLOW#	A27	B27	WDT	WDT	Connect to CPLD
SATA LED	(S)ATA_ACT#	SATA_ACT#	A28	B28	HDA_SDIN2	RSVD	NC
NC	RSVD	HDA_SYNC	A29	B29	HDA_SDIN1	RSVD	NC
NC	RSVD	HDA_RST#	A30	B30	HDA_SDIN0	RSVD	NC
GND	GND(FIXED)	GND	A31	B31	GND	GND(FIXED)	GND
NC	RSVD	HDA_BITCLK	A32	B32	SPKR	SPKR	NC
NC	RSVD	HAD_SDOUT	A33	B33	I2C_CK	I2C_CK	I2C_CK TO CPU AND CPLD
To CPLD ,select BIOS entry	BIOS_DIS0#/ESPI_SAFS	BIOS_DIS0#	A34	B34	I2C_DAT	I2C_DAT	I2C_DAT TO CPU AND CPLD
THRMTRIP# TO CPU AND CPLD	THRMTRIP#	THRMTRIP#	A35	B35	THRM#	THRM#	Connect to CPLD
NC	PCIE_TX13+	USB6-	A36	B36	USB7-	PCIE_RX13+	NC
NC	PCIE_TX13-	USB6+	A37	B37	USB7+	PCIE_RX13-	NC
NC	GND	USB_6_7_OC#	A38	B38	USB_4_5_OC#	GND	NC
NC	PCIE_TX12+	USB4-	A39	B39	USB5-	PCIE_RX12+	NC
NC	PCIE_TX12-	USB4+	A40	B40	USB5+	PCIE_RX12-	NC
GND	GND(FIXED)	GND	A41	B41	GND	GND(FIXED)	GND
USB2	USB2-	USB2-	A42	B42	USB3-	USB3-	USB3
USB2	USB2+	USB2+	A43	B43	USB3+	USB3+	USB3
Connect to CPU OC0	USB_2_3_OC#	USB_2_3_OC#	A44	B44	USB_0_1_OC#	USB_0_1_OC#	Connect to CPU OC0
USB0	USB0-	USB0-	A45	B45	USB1-	USB1-	USB1
USB0	USB0+	USB0+	A46	B46	USB1+	USB1+	USB1
P3V_BAT	VCC_RTC	VCC_RTC	A47	B47	EXCD1_PERST#	ESPI_EN	Connect to CPLD
Connect to CPLD	RSVD	EXCD0_PERST#	A48	B48	EXCD1_CPPE#	RSVD	Connect to CPLD
Connect to CPLD	RSVD	EXCD0_CPPE#	A49	B49	SYS_RESET#	SYS_RESET#	TO CPU PMU_RESETBUTTON AND CPLD
Connect to CPU LPC_SERIRQ AND CPLD	LPC_SERIRQ/ESPI_CS1#	LPC_SERIRQ	A50	B50	CB_RESET#	CB_RESET#	CB_RESET# TO CPLD
GND	GND(FIXED)	GND	A51	B51	GND	GND(FIXED)	GND
Connect to CPU PCIe6	PCIE_TX5+	PCIE_TX5+	A52	B52	PCIE_RX5+	PCIE_RX5+	Connect to CPU PCIe6
Connect to CPU PCIe6	PCIE_TX5-	PCIE_TX5-	A53	B53	PCIE_RX5-	PCIE_RX5-	Connect to CPU PCIe6
Connect to CPU GPIO5	GPI0	GPI0	A54	B54	GPO1	GPO1	Connect to CPU GPIO1
Connect to CPU PCIe4	PCIE_TX4+	PCIE_TX4+	A55	B55	PCIE_RX4+	PCIE_RX4+	Connect to CPU PCIe4
Connect to CPU PCIe4	PCIE_TX4-	PCIE_TX4-	A56	B56	PCIE_RX4-	PCIE_RX4-	Connect to CPU PCIe4
GND	GND	GND	A57	B57	GPO2	GPO2	Connect to CPU GPIO2
Connect to CPU PCIe3	PCIE_TX3+	PCIE_TX3+	A58	B58	PCIE_RX3+	PCIE_RX3+	Connect to CPU PCIe3
Connect to CPU PCIe3	PCIE_TX3-	PCIE_TX3-	A59	B59	PCIE_RX3-	PCIE_RX3-	Connect to CPU PCIe3
GND	GND(FIXED)	GND	A60	B60	GND	GND(FIXED)	GND
Connect to CPU PCIe2	PCIE_TX2+	PCIE_TX2+	A61	B61	PCIE_RX2+	PCIE_RX2+	Connect to CPU PCIe2
Connect to CPU PCIe2	PCIE_TX2-	PCIE_TX2-	A62	B62	PCIE_RX2-	PCIE_RX2-	Connect to CPU PCIe2
Connect to CPU GPIO6	GPI1	GPI1	A63	B63	GPO3	GPO3	Connect to CPU GPIO4
Connect to CPU PCIe1	PCIE_TX1+	PCIE_TX1+	A64	B64	PCIE_RX1+	PCIE_RX1+	Connect to CPU PCIe1
Connect to CPU PCIe1	PCIE_TX1-	PCIE_TX1-	A65	B65	PCIE_RX1-	PCIE_RX1-	Connect to CPU PCIe1
GND	GND	GND	A66	B66	WAKE0#	WAKE0#	Wake0,Connect to CPLD
Connect to CPU GPIO7	GPI2	GPI2	A67	B67	WAKE1#	WAKE1#	Wake1,Connect to CPLD
Connect to CPU PCIe0	PCIE_TX0+	PCIE_TX0+	A68	B68	PCIE_RX0+	PCIE_RX0+	Connect to CPU PCIe0
Connect to CPU PCIe0	PCIE_TX0-	PCIE_TX0-	A69	B69	PCIE_RX0-	PCIE_RX0-	Connect to CPU PCIe0
GND	GND(FIXED)	GND	A70	B70	GND	GND(FIXED)	GND
NC	PCIE_TX8+	LVDS_A0+	A71	B71	LVDS_B0+	PCIE_RX8+	NC
NC	PCIE_TX8-	LVDS_A0-	A72	B72	LVDS_B0-	PCIE_RX8-	NC

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NC	GND	LVDS_A1+	A73	B73	LVDS_B1+	GND	NC
NC	PCIE_TX9+	LVDS_A1-	A74	B74	LVDS_B1-	PCIE_RX9+	NC
NC	PCIE_TX9-	LVDS_A2+	A75	B75	LVDS_B2+	PCIE_RX9-	NC
NC	GND	LVDS_A2-	A76	B76	LVDS_B2-	GND	NC
NC	PCIE_TX10+	LVDS_VDD_EN	A77	B77	LVDS_B3+	PCIE_RX10+	NC
NC	PCIE_TX10-	LVDS_A3+	A78	B78	LVDS_B3-	PCIE_RX10-	NC
NC	GND	LVDS_A3-	A79	B79	LVDS_BKLT_EN	GND	NC
GND	GND(FIXED)	GND	A80	B80	GND	GND(FIXED)	GND
NC	PCIE_TX11+	LVDS_A_CK+	A81	B81	LVDS_B_CK+	PCIE_RX11+	NC
NC	PCIE_TX11-	LVDS_A_CK-	A82	B82	LVDS_B_CK-	PCIE_RX11-	NC
NC	GND	LVDS_I2C_CK	A83	B83	LVDS_BKLT_CTRL	GND	NC
NCSI_TX_EN TO CPU	NCSI_TX_EN	LVDS_I2C_DAT	A84	B84	VCC_5V_SBY	VCC_5V_SBY	XP5R0V
Connect to CPU GPIO8	GPI3	GPI3	A85	B85	VCC_5V_SBY	VCC_5V_SBY	XP5R0V
CPLD_TMS	RSVD	RSVD	A86	B86	VCC_5V_SBY	VCC_5V_SBY	XP5R0V
TO CPU RTEST AND SRTCRST	RSVD	eDP_HPD	A87	B87	VCC_5V_SBY	VCC_5V_SBY	XP5R0V
Connect to CPU CLKOUT_PCIE0	PCIE_CLK_REF+	PCIE_CLK_REF+	A88	B88	BIOS_DIS1#	BIOS_DIS1#/ESPI_BBS	To CPLD ,select BIOS entry
Connect to CPU CLKOUT_PCIE0	PCIE_CLK_REF-	PCIE_CLK_REF-	A89	B89	VGA_RED	NCSI_RX_ER	NC
GND	GND(FIXED)	GND	A90	B90	GND	GND(FIXED)	GND
Connect to 3.3V	SPI_POWER	SPI_POWER	A91	B91	VGA_GRN	NCSI_CLK_IN	NCSI_CLK_IN
Connect to CPU SPI_MISO	SPI_MISO	SPI_MISO	A92	B92	VGA_BLU	NCSI_RXD1	NCSI_RXD1
Connect to CPU GPIO0	GPO0	GPO0	A93	B93	VGA_HSYNC	NCSI_RXD0	NCSI_RXD0
Connect to CPU SPI_CLK	SPI_CLK	SPI_CLK	A94	B94	VGA_VSYNC	NCSI_CRS_DV	NCSI_CRS_DV
Connect to CPU SPI_MOSI	SPI_MOSI	SPI_MOSI	A95	B95	VGA_I2C_CK	NCSI_TXD1	NCSI_TXD1
NC	TPM_PP	TPM_PP	A96	B96	VGA_I2C_DAT	NCSI_TXD0	NCSI_TXD0
NC	TYPE10#	TYPE10#	A97	B97	SPI_CS#	SPI_CS#	TO CPLD
Connect to CPU UART0	SER0_TX	SER0_TX	A98	B98	RSVD	NCSI_ARB_IN	NCSI_ARB_IN
Connect to CPU UART0	SER0_RX	SER0_RX	A99	B99	RSVD	NCSI_ARB_OUT	NCSI_ARB_OUT
GND	GND(FIXED)	GND	A100	B100	GND	GND(FIXED)	GND
Connect to CPU UART1	CAN0/SER1_TX	SER1_TX	A101	B101	FAN_PWMOUT	FAN_PWMOUT	NC
Connect to CPU UART1	CAN0/SER1_RX	SER1_RX	A102	B102	FAN_TACHIN	FAN_TACHIN	NC
INTRUDER_N TO CPU	LID#	LID#	A103	B103	SLEEP#	SLEEP#	SLEEP# TO CPLD
XP12R0V	VCC_12V	VCC_12V	A104	B104	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	A105	B105	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	A106	B106	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	A107	B107	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	A108	B108	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	A109	B109	VCC_12V	VCC_12V	XP12R0V
GND	GND(FIXED)	GND	A110	B110	GND	GND(FIXED)	GND
GND	GND(FIXED)	GND	C1	D1	GND	GND(FIXED)	GND
GND	GND	GND	C2	D2	GND	GND	GND
Connect to CPU USB_SS0	USB_SSRX0-	USB_SSRX0-	C3	D3	USB_SSTX0-	USB_SSTX0-	Connect to CPU USB_SS0
Connect to CPU USB_SS0	USB_SSRX0+	USB_SSRX0+	C4	D4	USB_SSTX0+	USB_SSTX0+	Connect to CPU USB_SS0
GND	GND	GND	C5	D5	GND	GND	GND
Connect to CPU USB_SS1	USB_SSRX1-	USB_SSRX1-	C6	D6	USB_SSTX1-	USB_SSTX1-	Connect to CPU USB_SS1
Connect to CPU USB_SS1	USB_SSRX1+	USB_SSRX1+	C7	D7	USB_SSTX1+	USB_SSTX1+	Connect to CPU USB_SS1
GND	GND	GND	C8	D8	GND	GND	GND
NC	USB_SSRX2-	USB_SSRX2-	C9	D9	USB_SSTX2-	USB_SSTX2-	NC
NC	USB_SSRX2+	USB_SSRX2+	C10	D10	USB_SSTX2+	USB_SSTX2+	NC
GND	GND(FIXED)	GND	C11	D11	GND	GND(FIXED)	GND
NC	USB_SSRX3-	USB_SSRX3-	C12	D12	USB_SSTX3-	USB_SSTX3-	NC
NC	USB_SSRX3+	USB_SSRX3+	C13	D13	USB_SSTX3+	USB_SSTX3+	NC
GND	GND	GND	C14	D14	GND	GND	GND
NC	10G_PHY_MDC_SCL3	DDI1_PAIR6+	C15	D15	DDI1_CTRLCLK_AUX+	10G_PHY_MDIO_SDA3	NC
NC	10G_PHY_MDC_SCL2	DDI1_PAIR6-	C16	D16	DDI1_CTRLDATA_AUX-	10G_PHY_MDIO_SDA2	NC
NC	10G_SDP2	RSVD	C17	D17	RSVD	10G_SDP3	NC
GND	GND	RSVD	C18	D18	RSVD	GND	GND
Connect to CPU PCIe12	PCIE_RX6+	PCIE_RX6+	C19	D19	PCIE_TX6+	PCIE_TX6+	Connect to CPU PCIe12
Connect to CPU PCIe12	PCIE_RX6-	PCIE_RX6-	C20	D20	PCIE_TX6-	PCIE_TX6-	Connect to CPU PCIe12
GND	GND(FIXED)	GND	C21	D21	GND	GND(FIXED)	GND
Connect to CPU PCIe14	PCIE_RX7+	PCIE_RX7+	C22	D22	PCIE_TX7+	PCIE_TX7+	Connect to CPU PCIe14
Connect to CPU PCIe14	PCIE_RX7-	PCIE_RX7-	C23	D23	PCIE_TX7-	PCIE_TX7-	Connect to CPU PCIe14
NC	10G_INT2	DDI1_HPD	C24	D24	RSVD	10G_INT3	NC

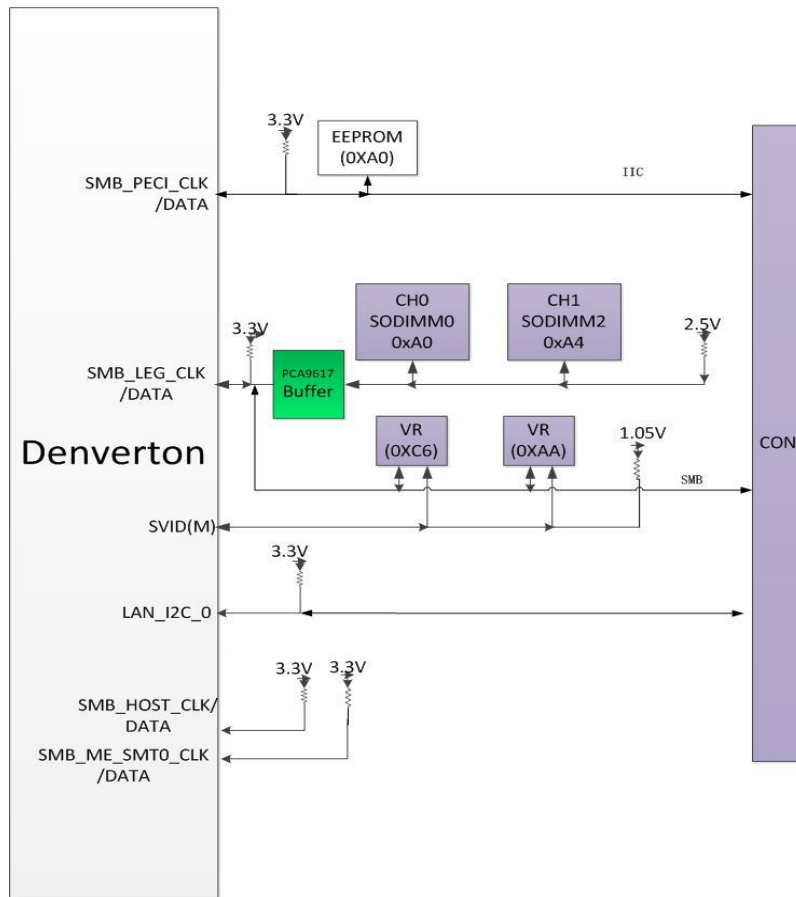
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GND	GND	DDI1_PAIR4+	C25	D25	RSVD	GND	GND
Connect to CPU KR3	10G_KR_RX3+	DDI1_PAIR4-	C26	D26	DDI1_PAIR0+	10G_KR_TX3+	Connect to CPU KR3
Connect to CPU KR3	10G_KR_RX3-	RSVD	C27	D27	DDI1_PAIR0-	10G_KR_TX3-	Connect to CPU KR3
GND	GND	RSVD	C28	D28	RSVD	GND	GND
Connect to CPU KR2	10G_KR_RX2+	DDI1_PAIR5+	C29	D29	DDI1_PAIR1+	10G_KR_TX2+	Connect to CPU KR2
Connect to CPU KR2	10G_KR_RX2-	DDI1_PAIR5-	C30	D30	DDI1_PAIR1-	10G_KR_TX2-	Connect to CPU KR2
GND	GND(FIXED)	GND	C31	D31	GND	GND(FIXED)	GND
LAN0_PORT1_I2C_DATA TO CPU	10G_SFP_SDA3	DDI2_CTRLCLK_AUX+	C32	D32	DDI1_PAIR2+	10G_SFP_SCL3	LAN0_PORT1_I2C_CLK TO CPU
LAN0_PORT0_I2C_DATA TO CPU	10G_SFP_SDA2	DDI2_CTRLCLK_AUX-	C33	D33	DDI1_PAIR2-	10G_SFP_SCL2	LAN0_PORT0_I2C_CLK TO CPU
NC	10G_PHY_RST_23	DDI2_DDC_AUX_SEL	C34	D34	DDI1_DDC_AUX_SEL	10G_PHY_SEL_23	NC
NC	10G_PHY_RST_01	RSVD	C35	D35	RSVD	10G_PHY_SEL_01	NC
SMB_GBE_DATA TO CPU	10G_LED_SDA	DDI3_CTRLCLK_AUX+	C36	D36	DDI1_PAIR3+	RSVD	NC
SMB_GBE_CLK TO CPU	10G_LED_SCL	DDI3_CTRLCLK_AUX-	C37	D37	DDI1_PAIR3-	RSVD	NC
LAN1_PORT1_I2C_DATA TO CPU	10G_SFP_SDA1	DDI3_DDC_AUX_SEL	C38	D38	RSVD	10G_SFP_SCL1	LAN1_PORT1_I2C_CLK TO CPU
LAN1_PORT0_I2C_DATA TO CPU	10G_SFP_SDA0	DDI3_PAIR0+	C39	D39	DDI2_PAIR0+	10G_SFP_SCL0	LAN1_PORT0_I2C_CLK TO CPU
NC	10G_SDP0	DDI3_PAIR0-	C40	D40	DDI2_PAIR0-	10G_SDP1	NC
GND	GND(FIXED)	GND	C41	D41	GND	GND(FIXED)	GND
Connect to CPU KR1	10G_KR_RX1+	DDI3_PAIR1+	C42	D42	DDI2_PAIR1+	10G_KR_TX1+	Connect to CPU KR1
Connect to CPU KR1	10G_KR_RX1-	DDI3_PAIR1-	C43	D43	DDI2_PAIR1-	10G_KR_TX1-	Connect to CPU KR1
NC	GND	DDI3_HPD	C44	D44	DDI2_HPD	GND	NC
NC	10G_PHY_MDC_SCL1	RSVD	C45	D45	RSVD	10G_PHY_MDIO_SDA1	NC
NC	10G_PHY_MDC_SCL0	DDI3_PAIR2+	C46	D46	DDI2_PAIR2+	10G_PHY_MDIO_SDA0	NC
NC	10G_INT0	DDI3_PAIR2-	C47	D47	DDI2_PAIR2-	10G_INT1	NC
GND	GND	RSVD	C48	D48	RSVD	GND	GND
Connect to CPU KR0	10G_KR_RX0+	DDI3_PAIR3+	C49	D49	DDI2_PAIR3+	10G_KR_TX0+	Connect to CPU KR0
Connect to CPU KR0	10G_KR_RX0-	DDI3_PAIR3-	C50	D50	DDI2_PAIR3-	10G_KR_TX0-	Connect to CPU KR0
GND	GND(FIXED)	GND	C51	D51	GND	GND(FIXED)	GND
Connect to CPU PCIe5	PCIE_RX16+	PEG_RX0+	C52	D52	PEG_TX0+	PCIE_TX16+	Connect to CPU PCIe5
Connect to CPU PCIe5	PCIE_RX16-	PEG_RX0-	C53	D53	PEG_TX0-	PCIE_TX16-	Connect to CPU PCIe5
0ohm to GND	TYPE0#	TYPE0#	C54	D54	PEG_LANE_RV#	RSVD	NC
Connect to CPU PCIe7	PCIE_RX17+	PEG_RX1+	C55	D55	PEG_TX1+	PCIE_TX17+	Connect to CPU PCIe7
Connect to CPU PCIe7	PCIE_RX17-	PEG_RX1-	C56	D56	PEG_TX1-	PCIE_TX17-	Connect to CPU PCIe7
GND	TYPE1#	TYPE1#	C57	D57	TYPE2#	TYPE2#	0ohm to GND
Connect to CPU PCIe13	PCIE_RX18+	PEG_RX2+	C58	D58	PEG_TX2+	PCIE_TX18+	Connect to CPU PCIe13
Connect to CPU PCIe13	PCIE_RX18-	PEG_RX2-	C59	D59	PEG_TX2-	PCIE_TX18-	Connect to CPU PCIe13
GND	GND(FIXED)	GND	C60	D60	GND	GND(FIXED)	GND
Connect to CPU PCIe15	PCIE_RX19+	PEG_RX3+	C61	D61	PEG_TX3+	PCIE_TX19+	Connect to CPU PCIe15
Connect to CPU PCIe15	PCIE_RX19-	PEG_RX3-	C62	D62	PEG_TX3-	PCIE_TX19-	Connect to CPU PCIe15
CPLD_TDI	RSVD	RSVD	C63	D63	RSVD	RSVD	CPLD_TDO
XP3R3V	RSVD	RSVD	C64	D64	RSVD	RSVD	VDDQP
NC	PCIE_RX20+	PEG_RX4+	C65	D65	PEG_TX4+	PCIE_TX20+	NC
NC	PCIE_RX20-	PEG_RX4-	C66	D66	PEG_TX4-	PCIE_TX20-	NC
CPLD_TCK	RSVD	RSVD	C67	D67	GND	GND	GND
NC	PCIE_RX21+	PEG_RX5+	C68	D68	PEG_TX5+	PCIE_TX21+	NC
NC	PCIE_RX21-	PEG_RX5-	C69	D69	PEG_TX5-	PCIE_TX21-	NC
GND	GND(FIXED)	GND	C70	D70	GND	GND(FIXED)	GND
NC	PCIE_RX22+	PEG_RX6+	C71	D71	PEG_TX6+	PCIE_TX22+	NC
NC	PCIE_RX22-	PEG_RX6-	C72	D72	PEG_TX6-	PCIE_TX22-	NC
GND	GND	GND	C73	D73	GND	GND	GND
NC	PCIE_RX23+	PEG_RX7+	C74	D74	PEG_TX7+	PCIE_TX23+	NC
NC	PCIE_RX23-	PEG_RX7-	C75	D75	PEG_TX7-	PCIE_TX23-	NC
GND	GND	GND	C76	D76	GND	GND	GND
VNNP	RSVD	RSVD	C77	D77	RSVD	RSVD	VCCP
Connect to CPU PCIe8	PCIE_RX24+	PEG_RX8+	C78	D78	PEG_TX8+	PCIE_TX24+	Connect to CPU PCIe8
Connect to CPU PCIe8	PCIE_RX24-	PEG_RX8-	C79	D79	PEG_TX8-	PCIE_TX24-	Connect to CPU PCIe8
GND	GND(FIXED)	GND	C80	D80	GND	GND(FIXED)	GND
Connect to CPU PCIe9	PCIE_RX25+	PEG_RX9+	C81	D81	PEG_TX9+	PCIE_TX25+	Connect to CPU PCIe9
Connect to CPU PCIe9	PCIE_RX25-	PEG_RX9-	C82	D82	PEG_TX9-	PCIE_TX25-	Connect to CPU PCIe9
XP1R05V	RSVD	RSVD	C83	D83	RSVD	RSVD	XP1R24V
GND	GND	GND	C84	D84	GND	GND	GND
Connect to CPU PCIe10	PCIE_RX26+	PEG_RX10+	C85	D85	PEG_TX10+	PCIE_TX26+	Connect to CPU PCIe10
Connect to CPU PCIe10	PCIE_RX26-	PEG_RX10-	C86	D86	PEG_TX10-	PCIE_TX26-	Connect to CPU PCIe10
GND	GND	GND	C87	D87	GND	GND	GND
Connect to CPU PCIe11	PCIE_RX27+	PEG_RX11+	C88	D88	PEG_TX11+	PCIE_TX27+	Connect to CPU PCIe11
Connect to CPU PCIe11	PCIE_RX27-	PEG_RX11-	C89	D89	PEG_TX11-	PCIE_TX27-	Connect to CPU PCIe11
GND	GND(FIXED)	GND	C90	D90	GND	GND(FIXED)	GND

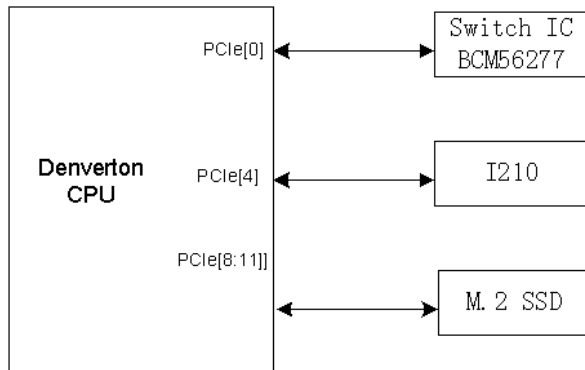
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NC	PCIE_RX28+	PEG_RX12+	C91	D91	PEG_TX12+	PCIE_TX28+	NC
NC	PCIE_RX28-	PEG_RX12-	C92	D92	PEG_TX12-	PCIE_TX28-	NC
GND	GND	GND	C93	D93	GND	GND	GND
NC	PCIE_RX29+	PEG_RX13+	C94	D94	PEG_TX13+	PCIE_TX29+	NC
NC	PCIE_RX29-	PEG_RX13-	C95	D95	PEG_TX13-	PCIE_TX29-	NC
GND	GND	GND	C96	D96	GND	GND	GND
XP1R8V	RSVD	RSVD	C97	D97	RSVD	RSVD	XP2R5V
NC	PCIE_RX30+	PEG_RX14+	C98	D98	PEG_TX14+	PCIE_TX30+	NC
NC	PCIE_RX30-	PEG_RX14-	C99	D99	PEG_TX14-	PCIE_TX30-	NC
GND	GND(FIXED)	GND	C100	D100	GND	GND(FIXED)	GND
NC	PCIE_RX31+	PEG_RX15+	C101	D101	PEG_TX15+	PCIE_TX31+	NC
NC	PCIE_RX31-	PEG_RX15-	C102	D102	PEG_TX15-	PCIE_TX31-	NC
GND	GND	GND	C103	D103	GND	GND	GND
XP12R0V	VCC_12V	VCC_12V	C104	D104	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	C105	D105	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	C106	D106	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	C107	D107	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	C108	D108	VCC_12V	VCC_12V	XP12R0V
XP12R0V	VCC_12V	VCC_12V	C109	D109	VCC_12V	VCC_12V	XP12R0V
GND	GND(FIXED)	GND	C110	D110	GND	GND(FIXED)	GND

CPU I2C Topology



PCIe Topology



PCIe Allocation

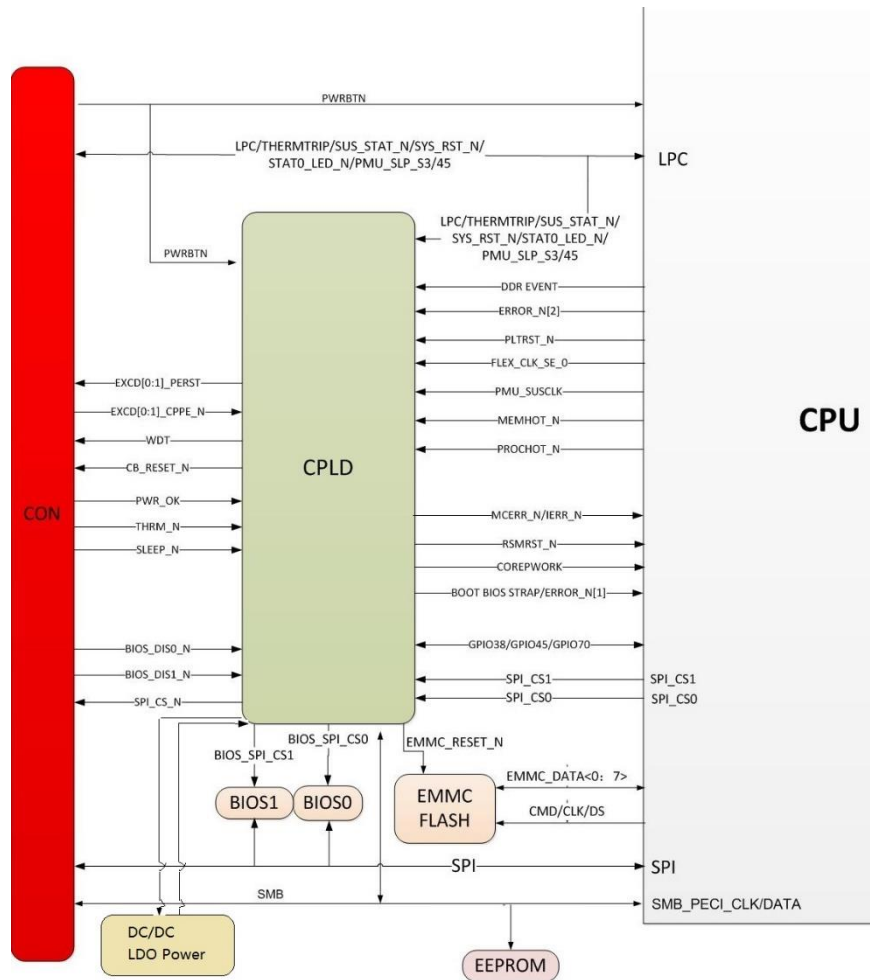
TYPE 6	Type 7	To Where	Usage	Lane No.	Speed/ BW
PCIe0	PCIe0	SWITCH Board	SWITCH IC	PCIe0	Gen3 x1
PCIe4	PCIe4		I210	PCIe4	Gen2 x1
PEG8	PCIe24		M.2 SSD	PCIe8	Gen3 x4
PEG9	PCIe25			PCIe9	
PEG10	PCIe26			PCIe10	
PEG11	PCIe27			PCIe11	

COM-E CPU Module CPLD

A CPLD is included on the COM-E CPU Module and provides the following functions

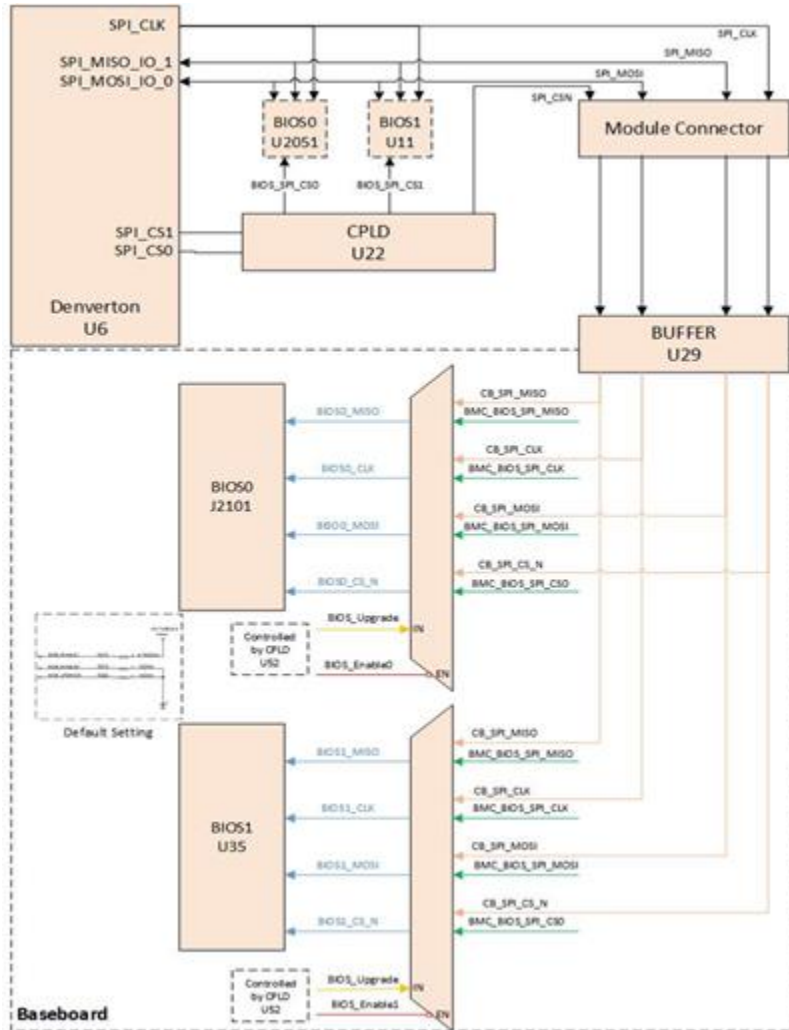
- Power sequence controlling
- On-board glue logic
- LPC accessed by CPU
- CPU BIOS Select
- Thermal merge
- Reset and Interrupt
- Watchdog

COM-E CPU Module CPLD Functional diagram



COM-E CPU Module BIOS Flash Diagram

The COM-E CPU module supports a primary and backup BIOS image each stored in a separate FLASH device located on the Switch PCB



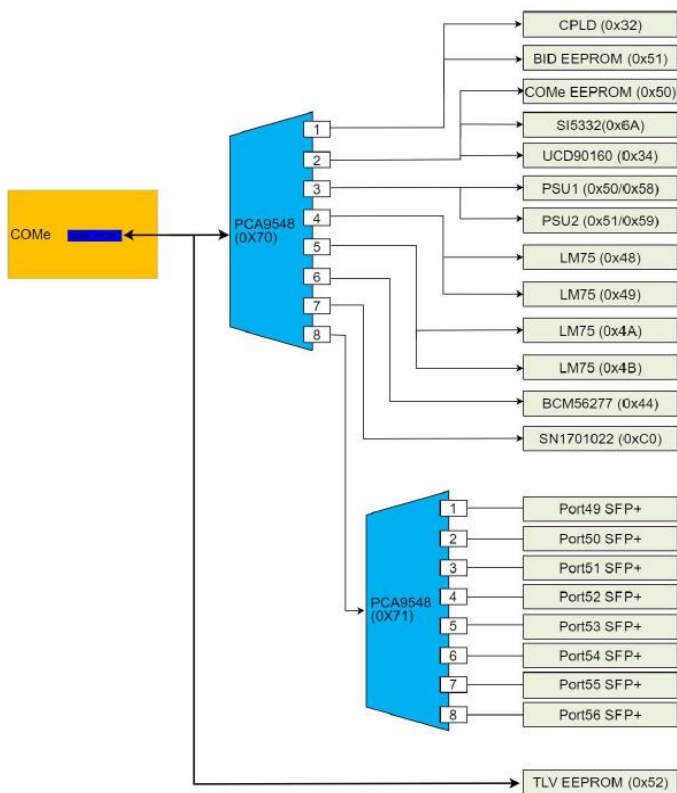
Main Switch PCB

The Main switch PCB includes the system switching silicon, external networking connections, connections to the system power supply modules and fans, and various memory systems used by the COM-E CPU Module.

Main Switch PCB major components

Description	Vendor	Part Number
Switching Silicon	Broadcom	BCM56277A1KFSBG
Octal QSGMII PHY	Broadcom	B50282C1KFBG
CPLD	Lattice	LCMXO2-2000HC-4FTG256C
BIOS SPI FLASH	Winbound	W25Q128JVS1Q-T
64GB SSD	INNODISK CORPORATION	DHM28-64GM41BC1DC-B039B
4GB,DDR4-2666,SODIMM	INNODISK CORPORATION	M4D0-4GSSPCIK-B039
Connector RJ45 2x8	UDE	M8A-CT-0001
PSU Connector	Alltop	C210N3-15031-Y
Connector COM-E	TE Connectivity	3-5353652-6
TPM (build time option)	ST MICROELECTRONICS	ST33HTPH2X28AHD4

I2C Allocation

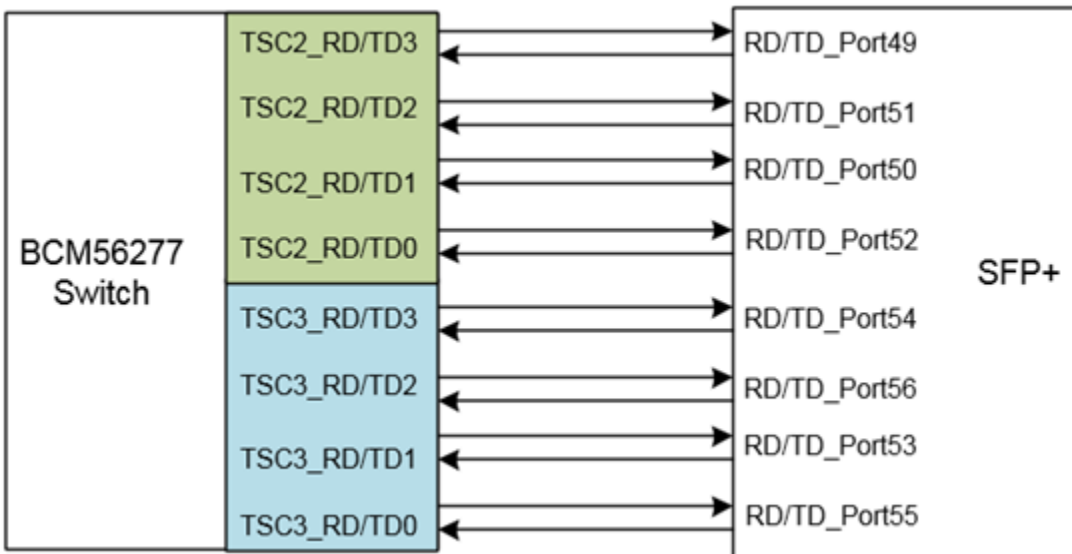


Switch Board CPLD

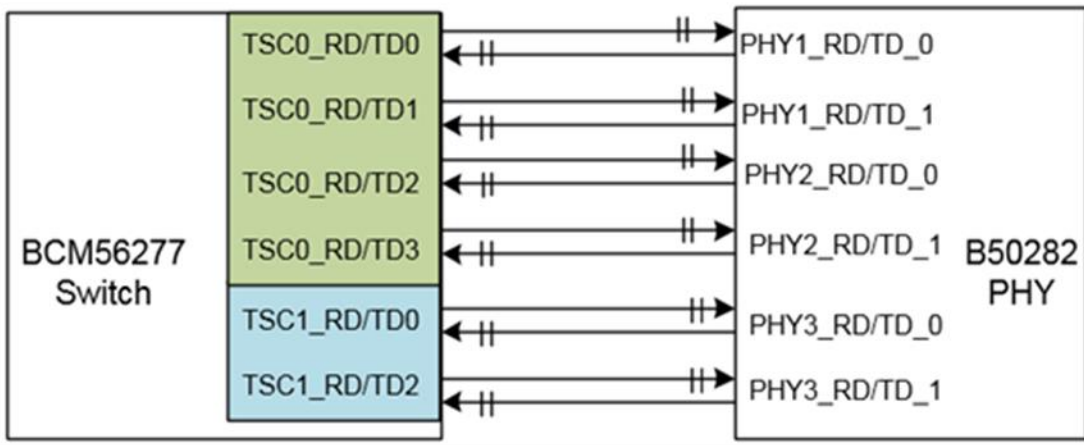
The CPLD on Switch board is LCMXO2-1200UHC-4FTG256C from Lattice. It is used as a management module including the functions below:

- Power sequence controlling
- On-board glue logic
- LPC accessed by CPU
- I2C bus
- CPU BIOS Select
- Thermal merge
- Reset and Interrupt
- Watchdog
- SFP+ status monitor and controlling
- System status LED control

Switch connections to SFP+ ports



Switch Connections to PHYs



Switch Board LEDs

48X RJ45Gb Ethernet port LEDs

Each port has one Green LED on the left and one right Yellow LED on the right.

Port Link/ Activity Status LED is provided for each RJ45 port (Left: Green, Right Yellow)
• Solid Green = 48x1000M Link up
• Flashing Green = 48x1000M Activity
• Solid Amber = 48x10/100M Link up
• Flashing Amber = 48x10/100M Activity
• Off = Link down

8xSFP+ LEDs

Each SFP+ port has one dual color Green/Amber LED

One Port Link/ Activity Status Green/Amber bi-color LED is provided for each front panel port
• Solid Green = 10G Link on SFP+ port
• Flashing Green = 10G Activity on SFP+ port
• Solid Amber = 1G Link on SFP+ port
• Flashing Amber = 1G Activity on SFP+ port
• Off = No link

IO Board

The IO board supports the four system LEDs, RJ45 Console Port, RJ45 Ethernet Management port, and two USB ports.

IO Board LEDs

Single RJ45 Management Port LED

The Management port has one Green LED on the left and one right Yellow LED on the right.

Port Link/ Activity Status LED is provided for each RJ45 port (Left dual color : Green/Amber, Right single color: Green)
Left dual color LED (Green/Amber):
• Solid Green = 1000M Link active • Solid Amber = 10/100M Link active
• Off = Link down
Right single color Green LED:
• Solid Green = Port link active and has traffic. • Off = no traffic

System Status LEDs

There are four dual color LED on front panel, used for system status indication. One system LED, one alarm LED, one PSU LED and one FAN status LED.

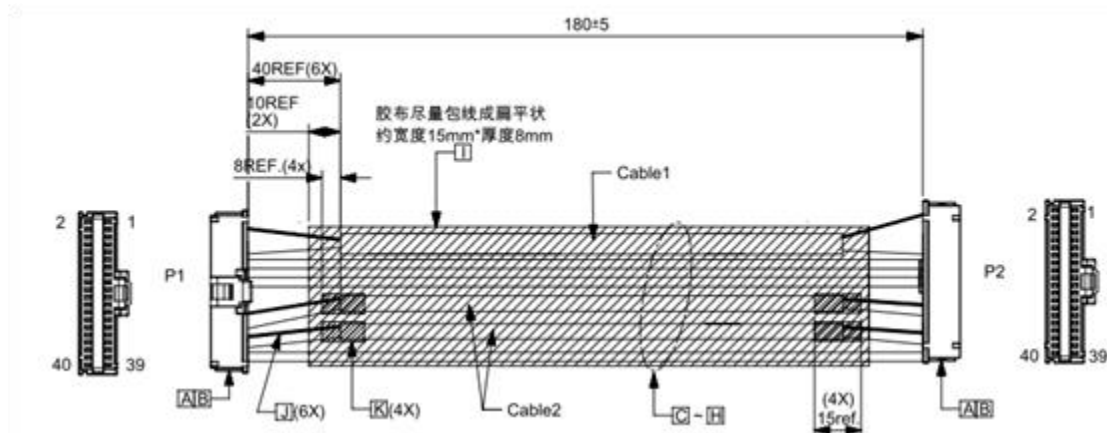
System Status LED [on front panel]			
LED	Status	Function	Note
System Led	Off	Controlled by NOS	See note1
	Green LED on	Controlled by NOS	
	Yellow LED on	Controlled by NOS	
	Green LED 1Hz Blinking	Controlled by NOS	
	Yellow LED 1Hz Blinking	Controlled by NOS	
	Green LED 4Hz Blinking	Controlled by NOS	
	Yellow LED 4Hz Blinking	Controlled by NOS	
	Green and Yellow LED Alternate 1Hz Blinking	For ONIE installed system, after ONIE boot success	
	Green And Yellow LED Alternate 4Hz Blinking	Default setting in CPLD	
PSU Status	Solid Green	PSU is present and status (PWOK and ALERT_N) are correct.	
	Solid Yellow	One PSU Absent or any one of the PSU status (PWOK or ALERT_N) is incorrect	CPLD provide register to CPU/BMC force set the PSU Status LED to Amber on
	off	PSU Status LED Off is not allowed	
Alarm LED	Off	Default	
	Solid Green	No alarm	
	Solid Yellow	Critical alarm	
	Yellow	Major alarm: 4Hz blinking	
	Blinking	Minor alarm: 1Hz blinking	
FAN LED	Solid Green	All FAN Present and status are normal	CPLD provide HW & SW control logic for FAN Status LED
	Solid Yellow	Any one of the FAN is absent, or any of the FAN status is abnormal	
		All FAN tray are absent, Fan Status LED Off.	
	off		

Switch Board to IO board connection

Switch Board Connector - Vendor: Molex MPN: 2035664007

IO Board Connector - Vendor: Molex MPN: 0686030389

Switch Board to IO Board Cable - Vendor: Molex MPN: 0686030389



Switch Board to IO Board Cable Pinout

Wire to Board Connector (Calbe /connector/header pin)						
Pin Number	Signal	Diff Impedance	Wire Color	Pin Number	Signal	Wire Color
1	GND	/	Black	2	XP3R3V	Red
3	MDIO_P	Diff 100ohm	Brown	4	XP3R3V	Red
5	MDIO_N		Brown/White mix	6	FAN_LED_Green	Black
7	GND	/	Black	8	FAN_LED_Amber	Black
9	MDI1_P	Diff 100ohm	Green	10	SYS_LED_Green	Black
11	MDI1_N		Green/White mix	12	SYS_LED_Amber	Black
13	GND	/	Black	14	PSU_LED_Green	Black
15	MDI2_P	Diff 100ohm	Blue	16	PSU_LED_Amber	Black
17	MDI2_N		Blue/White mix	18	ALARM_LED_Green	Black
19	GND	/	Black	20	ALARM_LED_Amber	Black
21	MDI3_P	Diff 100ohm	Orange	22	GND	Black
23	MDI3_N		Orange/White mix	24	TXD	White
25	GND	/	Black	26	RXD	Green
27	USB1_D+	Diff 90ohm for USB2.0	Green	28	XP5R0V_1	Red
29	USB1_D-		White	30	MGMT_LINK	Black
31	GND	/	Black	32	MGMT_LED_Amber	Black
33	USB2_D+	Diff 90ohm for USB2.0	Green	34	MGMT_LED_Green	Black
35	USB2_D-		White	36	XP5R0V_2	Red
37	GND	/	Black	38	GND	Black
39	GND	/	Black	40	GND	Black

10. Rear Side Power, I/O and Midplane



The rear side of the DS1000 includes two field replaceable power supply units and three fixed system fans.

Power Supply Modules

The DS1000 support two 550W load sharing power supply modules.

PSU Vendor: FSP GROUP Part #: FSP550-20FM

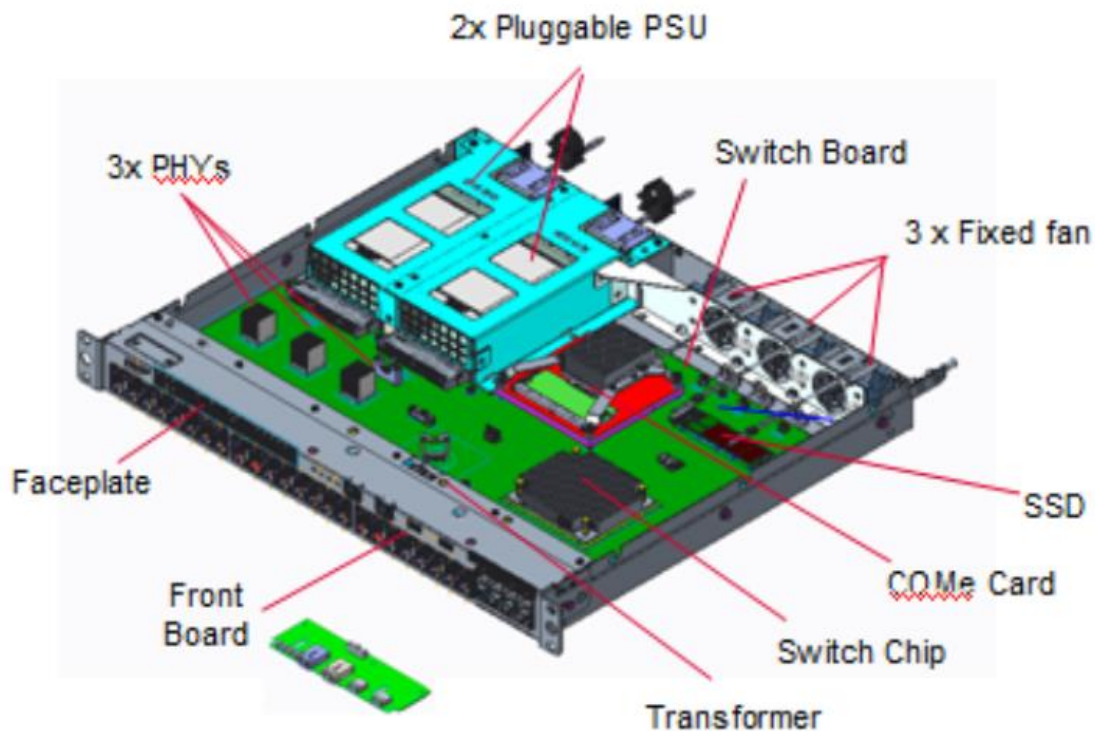
System fans

The DS1000 supports three system fans 40mmx40mmx28mm

Fan Vendor Sunronwealth Electric part # VF40281BX-Q84C-S9H

11. Mechanical

DS1000 assembly drawing is shown below



DS1000 Assembly Drawing

The main assemblies of DS1000 are listed below:

- 1. Main Switch PCB board
- 2. Denverton COM-E PCB board
- 3. Front panel IO PCB board
- 4. 2+1 Fixed Fan tray
- 5. 1+1 Hot swappable PSU Modules

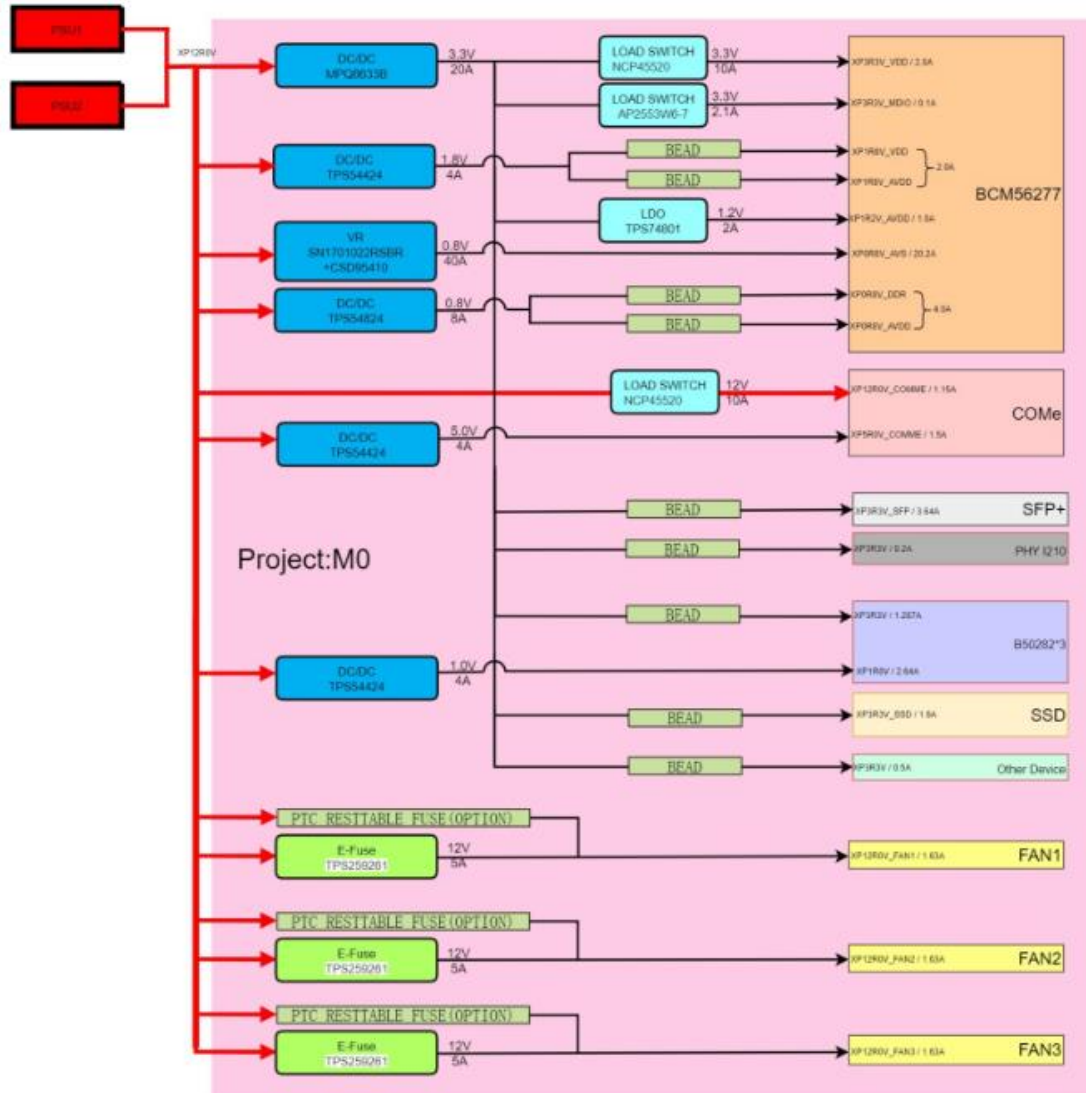
12. Motherboard Power System

DS1000 supports dual AC input load sharing power supplies which connect to the main switch PCB. The power supplies are sized so that one power supply can support the entire power load of the system and with two power supplies installed power redundancy is achieved.

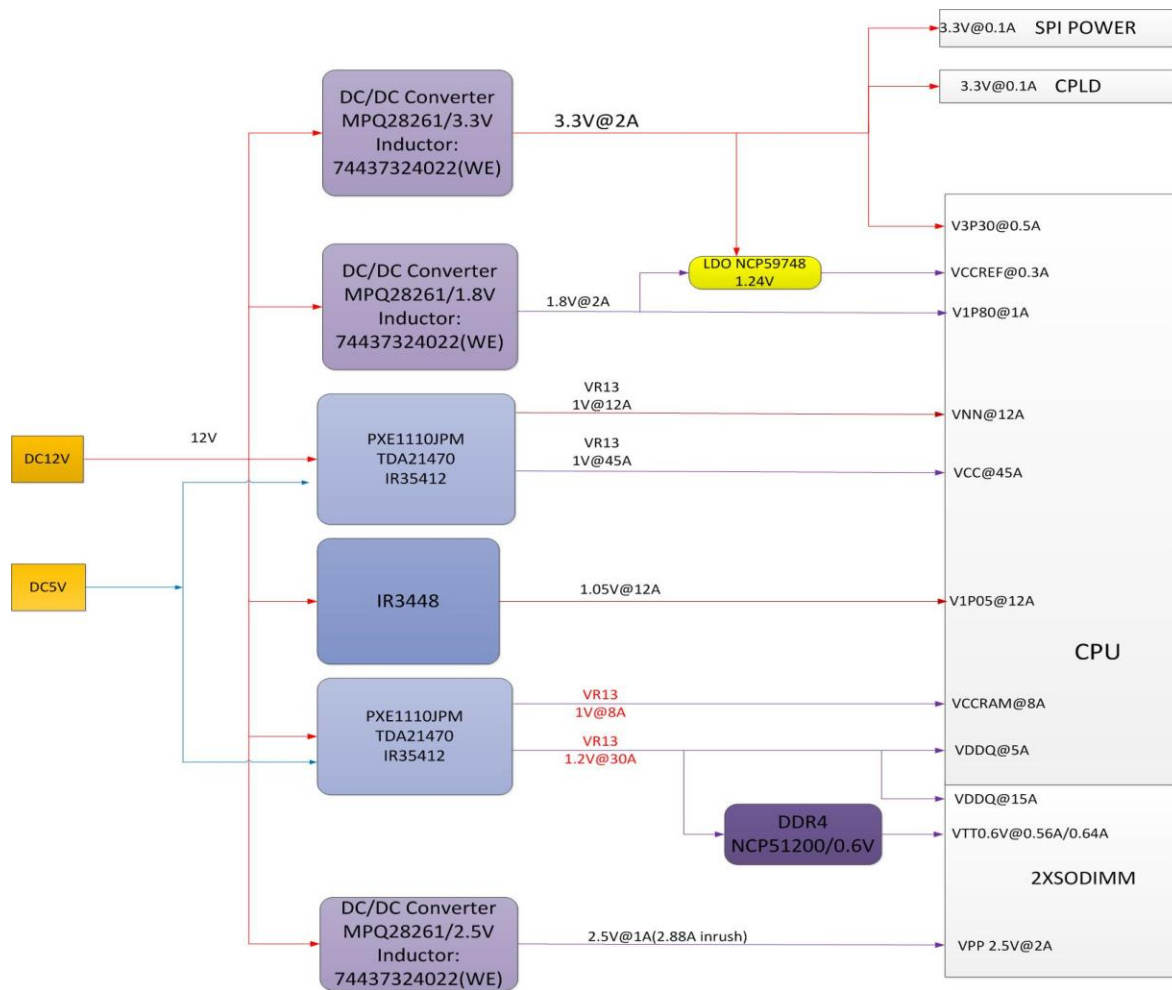
DS1000 Power Consumption

Module	Device	Qty	Power(W)	Total Power(W)	Module Power(W)
CPU Board (COMe)	Deventon CPU 8 core C3758	1	25	25	44.88
	32GB DDR4 SODIMM	2	8.69	17.38	
	CPLD	1	0.5	0.5	
	MISC1	1	2	2	
Switch Board	TD3.X2 BMC56277	1	25	25	50.61
	PHY B50282	3	2.296	6.888	
	PHY I210	1	0.626	0.626	
	1TB MLC M.2 SSD SATA3	1	4.6	4.6	
	2x4 SFP+	1	8	8	
	CPLD	1	0.5	0.5	
	MISC2	1	5	5	
FAN Tray	FAN	3	19.6	58.8	58.80
Total					154.29
Total / 0.9 (from 12V)					171.44

DS1000 Switch Board DC/DC Power Diagram



DS1000 COM-E on-board DC/DC



13. Environmental Regulations / Environmental Requirements

- Acoustic: EN300753
- Waste Electrical and Electronic Equipment (WEEE):
- Directive 2012/19/E
- European Union ROHS directive: 2011/65/EU&
- 2015/863
- SVHC requirements of REACH directive:
- (EC) No. 1907/2006
- EMC: Class A - USA, Canada, Europe, China,
- Japan, Korea, Australia, Brazil, South Africa
- Safety: UL/CSA/IEC/EN 60950-1/62368-1
- PSU: CE, CCC, KC, TUV, UL/cUL, BIS and BSMI

14. Software Support

ONIE

The DS1000 supports the Open Compute Open Network Install Environment (ONIE)

<https://github.com/opencomputeproject/onie>

Open Network Linux

The DS1000 supports Open Network Linux

<https://github.com/opencomputeproject/OpenNetworkLinux>

15. System Firmware

The DS1000 Supports a commercial BIOS package AMI Aptio

16. Hardware Management

17.1 Compliance

The DS1000 is compliant to the Usage Guide and Requirements for the OCP Baseline Hardware Management API v1.0.1

<https://www.opencompute.org/documents/usage-guide-for-baseline-hw-mgmt-api-v1-0-1-final-pdf>

17. Security

The DS1000 hardware design supports the population of an optional TPM chip if desired.

Appendix A - Requirements for IC Approval (to be completed Contributor(s) of this Spec)

List all the requirements in one summary table with links from the sections.

Requirements	Details	Link to which Section in Spec
Contribution License Agreement	OWF-CLA	1.1. OPTION B: Open Web Foundation (OWF) CLA
Are All Contributors listed in Sec 1: License?	Yes	1. License
Did All the Contributors sign the appropriate license for this spec? Final Spec Agreement/HW License?	Yes	
Which 3 of the 4 OCP Tenets are supported by this Spec?	Openness Efficiency Impact Scale	2. OCP Tenets Compliance
Is there a Supplier(s) that is building a product based on this Spec?	Yes	Celestica
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	Please have each Supplier fill out Appendix B.

Appendix B - OCP Supplier Information

Company: Celestica

Contact Info: Jeff Catlin

Product Name: DS1000

Product SKU#: DS1000

Link to Product Landing Page: <https://landing.celestica.com/ds1000/>

Please complete the following [2021 Supplier Requirements](#). This link will allow you to create a copy for your product-specific requirements.

For OCP Inspired™,

- All Suppliers must be a OCP Solution Provider.
- All Suppliers must run the Hardware Management Conformance Checks and all products must meet the [OCP Hardware Baseline Profile v1.0.0](#).
- All Suppliers must fill out a Security Profile (No Badge Level) for their product.

For OCP Accepted™, Supplier details are required.

- All Suppliers must be a OCP Solution Provider.
- All Suppliers must run the Hardware Management Conformance Checks and all products must meet the [OCP Hardware Baseline Profile v1.0.0](#).
- All Suppliers must fill out a Security Profile (No Badge Level) for their product.
- All Products must meet the Open System Firmware requirements.
- All Products must have source code for BMC, if applicable. This must be in the OCP Github repository.

List all the requirements in one summary table with links from the sections.

Requirements	Details	Links
Which Product recognition?	OCP Accepted™	
If OCP Accepted™, who provided the Design Package?	Celestica the supplier	
2021 Supplier Requirements for your product(s)		