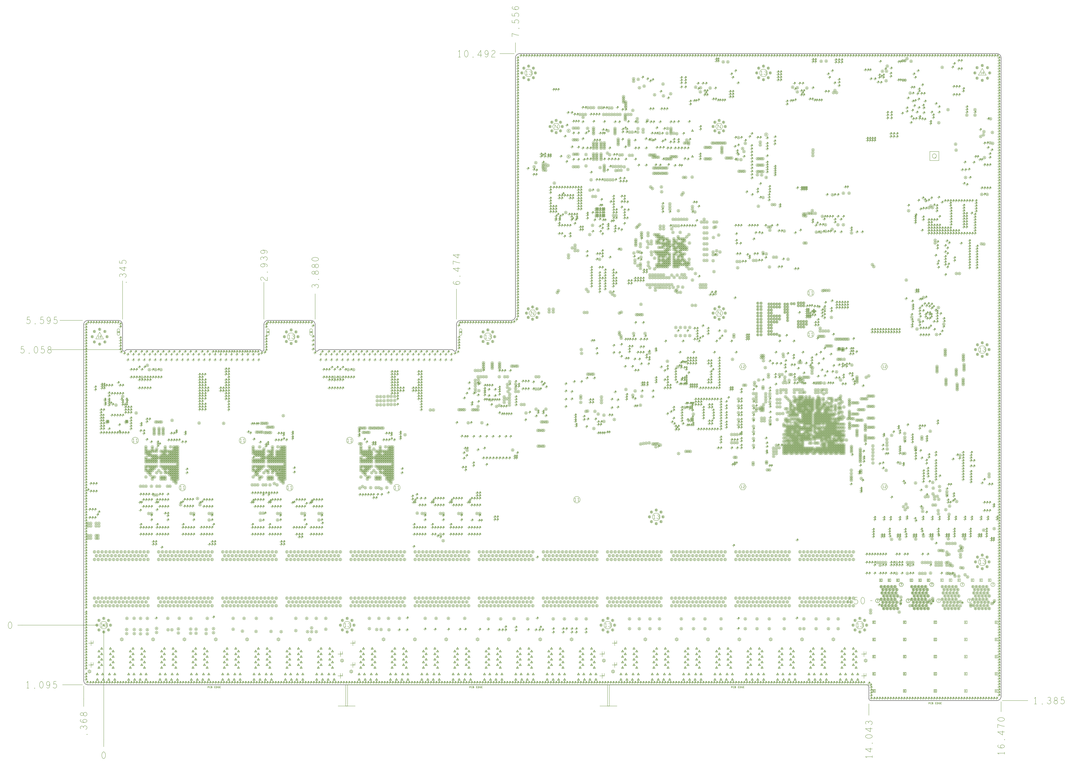
ART FILM - FAB

REL FOR ASM	QTY	TECHNICAL APPROVAL				DATE	EC NO.		DATE		PART NO.	REV
		ELECTRICAL									R3059-B0001-02	R01
		MATERIAL									DEVELOPMENT NO.	Q/M



NOTES: Unless otherwise specified

1. General Requirement:
   a. Board shall be built per IPC-A-600 and IPC6012, class II, latest revision. Plating and annular rings must meet the Class 3 specification.
   b. Board shall be electrically tested per current revision of IPC 6012 and IPC 9252 class II. Completed electrical test Boards must be marked in permanent non-conductive ink. This identification stamp or Line must be in the same location on every board, and must not encroach onto any metallic surface, tooling holes, or fiducial clearances. PCB vendor shall ensure Etest marking traceability between quality conformance test circuitry and the manufacturing history.
   c. Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the gerber data.
   d. Bow and Twist: shall not exceed .007" per inch.
   e. Fabrication Tolerances: end product trace widths and lands shall not vary more than the smaller of .001" or 20% of the trace width from the gerber data.
   f. PCB fabrication process and materials must be compliant with the Hazardous Substances (RoHS) Directive and compatible with Pb Free assembly process.
   g. Thieving is allowed all layers with 0.050" squares on 0.100" pitch and 0.100"min away from any designed features (i.e. vias, pads, traces, etc.).
   h. Unless specified otherwise, average copper thickness in plated through holes shall not be less than 0.001", with no single measurement less than 0.0008". measurement shall be taken per the IPC 6012 latest revision
   i. Non functional pads may be removed from internal layers.
   j. The entire assembly must be IEC/EN60950 compliant and be RoHS 6 compliant.

2. Via: a. Tangency is allowed on via size 8mil, 10 mils and 12 mils provided. Tear dropping is applied to the entry of the trace to the pad.

3. Drilling:
   a. All hole symbols may not be shown in the drawing. See Drill chart for details.
   b. Diameters in the drill table are finished hole sizes with +/-0.003" tolerance unless otherwise specified in the drill table.
   c. All press-fit hole size with +/-2mil tolerance

4. Marking:
   a. Soldermask:photo-imaged liquid polymer on both sides of boards in accordance with IPC-SM-840, Type B, Class 2, over bare copper. Soldermask color to be GREEN. matte finish materials preferred.
   b. Component Marking: Silkscreen both sides with white, non-conductive epoxy ink. Lands and exposed plated areas to be free of ink.
   c. Identification: PCB part number to be etched on component side. Fab vendor logo,UL marking(UL94V-0&UL file number),PWB UL type or model, date code to be placed on silkscreen solder side.

5. Backdrill legend:
   BOT SIDE: bd_10-4. Must not cut layer L03 (Stub length 6+/-4 mil tolerance)
   **Note* Backdrill Legend is system generated from Cadence layout tool. The intergrity of connection to must not cut layers must be maintained. The vendor is requested to adjust backdrill plunge depths accordingly. Our NC drill documentation will include XX backdrill files for bottom layer up plunges and XX backdrill files for top layer down plunges.

7. Please provide drill bit size selected for all press-fit holes and average plating thickness in press-fit holes in DFM report.

8. All the dimensions in the drawing will statistically monitor the ongoing process quality control and require a minimal process control value of Cpk >=1.33. There are specified requirement about critical to function marked as CTF in the drawing, require a minimal process control value of Cpk >=1.67.

9. Please provide actual residual copper rate for each layer in DFM report.

10. All BGA package sites of 47.5 MM(1.87 inches) and above are required to have not more than 0.004 inches of planar variation when measured diagonally across the silkscreen corners. For all shipments, flatness data is required.

11. Please provide actual hole measurement report for press-fit holes and non-PTH holes in a board. Send soft copy to GDS engineer, who release Gerber package. Hard copy is required in delivery report.

12. Please follow our stack-up in the gerber package.

13. For SI requirements,please refer the files in gerber package.

14. Please provide PCB working panel utilization in TQ report.

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	ROTATION	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	QTY
*	8.0	-	+0.0/-8.0	-	PLATED	2923
*	10.0	-	+0.0/-10.0	-	PLATED	3901
*	12.0	-	+0.0/-12.0	-	PLATED	231
*	18.0	-	+2.0/-2.0	-	PLATED	240
*	33.0	-	+3.0/-3.0	-	PLATED	1056
*	35.0	-	+3.0/-3.0	-	PLATED	576
*	40.0	-	+3.0/-3.0	-	PLATED	100
*	41.0	-	+2.0/-2.0	-	PLATED	58
*	62.0	-	+3.0/-3.0	-	PLATED	27
*	90.0	-	+3.0/-3.0	-	PLATED	12
*	134.0	-	+3.0/-3.0	-	PLATED	4
*	166.0	-	+3.0/-3.0	-	PLATED	1
*	35.0	-	+2.0/-2.0	-	NON-PLATED	2
*	43.0	-	+2.0/-2.0	-	NON-PLATED	1
*	63.0	-	+2.0/-2.0	-	NON-PLATED	3
*	73.0	-	+2.0/-2.0	-	NON-PLATED	12
*	118.0	-	+2.0/-2.0	-	NON-PLATED	9
*	124.0	-	+2.0/-2.0	-	NON-PLATED	4
*	138.0	-	+2.0/-2.0	-	NON-PLATED	11
*	165.0	-	+2.0/-2.0	-	NON-PLATED	2
*	122.0x47.0	90.000	+3.0/-3.0	+3.0/-3.0	PLATED	4

CTF Press-Fit

CTF Press-Fit

MATERIAL NO.		MUST CONFORM TO ENG SPEC:		SCALE:	PART NO.	REV	Celestica
				0 INCH 1	R3059-B0001-02	R01	
MAT'L ALTERNATE NO.		TOLERANCES UNLESS NOTED		THIRD ANGLE PROJECTION	TITLE	Belgite SW Board	
		LINEAR ±	0.005"		FAB		
CASE DEPTH		ANGLES ±	5 Degree		DESIGNER	May Tang	2021-08-13
HARDNESS		RADII UNLESS NOTED		THIS DOCUMENT IS THE PROPERTY OF CELESTICA INC. ITS USE IS AUTHORIZED FOR RESPONDING TO A REQUEST FOR QUOTATION OR FOR THE PERFORMANCE OF WORK FOR CELESTICA. ALL QUESTIONS MUST BE REFERRED TO THE CELESTICA PURCHASING DEPARTMENT.	CHECKED	Robinson Ouyang	2021-08-13
SURFACE TREATMENT	CODE NO.	EDGE/CORNER BREAKS	OUTSIDE MAX		APPROVED	Felix Wei	2021-08-13
			INSIDE MAX		CLASS		

PART NO. R3059-B0001-02 REV R01

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