

OPEN
Compute Project

SYSTEM IN PACKAGE TESTING

Authors :

Mike Bartley	Tessolve
James Wong	Palo Alto Electron
BoonChong Ang	Intel
Madhumita Sanyal	Synopsys

Contributors :

Anand Muthaiah	Tessolve
Aparna Tarde	Synopsys
Rajesh Pendurkar	Capgemini
Frank Mielke	Advantest

Date: November, 2024

Executive Summary

Chiplets are a new way to build highly integrated circuits (IC's) that can both improve yields and reduce costs by more than 45%. Chiplet-based products partition the IC into discrete chiplets and then assembles them within a package and connects them with a standardized interface to create a System-in-Package (SiP). This helps designers to meet performance, efficiency, power, size, and cost challenges in the 5/6G, AI, and VR era. However, with multi-die packages, one bad die can result in the failure of the whole package. Heterogeneous integration within the package involves complexities that drive the need for effective inspection for high yields and long-term reliability. Product defects need to be caught early in the production phase. This paper focuses on how best to achieve this. Specifically, it focuses on best-practice strategies including DFT, Known-Good-Chiplet (KGC)[16] testing and assembly, yield recovery and test-time reduction, and how best to reduce overall test cost.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Table of Contents

1. Introduction 6
2. Problem Statement 7
3. Status of Chiplet Test 12
4. Chiplet Based SIPs-2.5D -> 3D 15
5. DFT Strategies 21
6. Accelerating Test 23
7. System Level and Functional Tests 29
8. KGC Testing and Assembly Yield Recovery 32
9. Test Cost 37
    Wafer Sort Testing 37
    Assembly and Package Testing 39
    Board Level System Testing 40
    Test Economics Modeling 41
10. Comparison of Test Costs 45
    Wafer/Die Level Testing 46
    Module/Package Level Testing 46
    Test Cost Impact Of Higher Yield 47
    Routing Optimization for Test Cost Reduction 48
    DFT Reuse Across System Levels 48
11. Chiplet Versus Monolithic Comparison 49
12. Standard Testing and Integration 50
    Standard Workflow 53
    Standard Format 53
13. Conclusion 55
14. References 55
17. License 58
18. About Open Compute Foundation 59
Appendix A. [Title] 60

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

1. Introduction

Chiplets are a new way to build highly integrated circuits (IC's) that can both improve yields and reduce costs by more than 45%. Instead of integration of several IPs into one System-on-Chip (SoC), chiplet-based products partition the IC into discrete chiplets and then assemble them within a package and connect them with a standardized interface to create a System-in-Package (SiP). This helps designers to meet performance, efficiency, power, size, and cost challenges in the 5/6G, AI, and VR era. However, with multi-die packages, one bad die can result in the failure of the whole package. Heterogeneous integration within the package involves complexities that drive the need for effective inspection for high yields and long-term reliability. Product defects need to be caught early in the production phase. This paper focuses on how best to achieve this, starting with a problem statement to set the context.

The paper then considers the status of SiP test best-practice strategies including DFT, Known-Good-Chiplet (KGC)[16] testing and assembly, yield recovery and test-time reduction, and how these might affect overall test cost by considering how they might impact the tests at wafer sort, assembly and packaging and board-level. We do this using test economics modeling which includes the potential impact of the test for higher yields, how routing optimization and DFT reuse across system levels can reduce overall test cost. The paper sets this within the context of current industry test standards regarding workflow and test formats. The paper concludes with a set of recommendations and suggested next steps.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

2. Problem Statement

In multi-die packages, one bad die can result in the failure of the whole package. Heterogeneous integration within the package involves complexities that drive the need for effective inspection for high yields and long-term reliability. Product defects need to be caught early in the production phase. The high-performance computing system-in-package (SiP) in the hyperscale data center, networking, and AI applications cannot tolerate product defects, which can have catastrophic impact on AI workloads or data processing. Test methodologies need to be in place to improve the speed and coverage of production tests and need to be standardized to improve efficiency by using common testing metrics and interfaces at different stages of the end-product manufacturing – from wafer testing to chip testing to board-level testing. The challenges of chiplet testing are:

- **DFT Standard Challenges:**
  - **IEEE Standards:** Chiplet testing faces challenges in adhering to DFT standards such as IEEE 1500, IEEE 1687, and IEEE 1149. These standards provide guidelines for test access, scan chains, and built-in self-test (BIST) features. However, integrating these standards across heterogeneous chiplets with varying architectures and interfaces can be complex.
  - **Interoperability:** Ensuring DFT interoperability across chiplets from different vendors or with different manufacturing processes requires standardized interfaces, test wrappers, and protocols. Achieving seamless integration while maintaining test coverage and fault detection is a significant challenge.
- **Architecture Challenges:**
  - **Hierarchical Testing:** Chiplet architectures often comprise multiple layers of hierarchy, with functional blocks, IPs, and interconnects distributed across chiplets. Testing at each

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

level while ensuring overall system functionality and performance poses challenges in test planning, resource allocation, and fault isolation.

- ❖ **Inter-chip Communication Testing:** Verifying inter-chip communication protocols, data integrity, latency, and bandwidth across chiplets is critical for system reliability. Testing these aspects requires sophisticated test scenarios, emulation platforms, and real-time monitoring tools.

- **Functional Test Challenges:**

  - ❖ **IP Integration:** Chiplets integrate diverse IPs such as CPUs, GPUs, memory controllers, and custom accelerators. Functional testing involves verifying correct functionality, interface compatibility, and performance metrics for each IP block within and across chiplets.

  - ❖ **Coherency and Synchronization:** Ensuring data coherency, cache coherence, and synchronization mechanisms between chiplets is essential for distributed computing and shared memory architectures. Functional tests must validate these aspects under varying workloads and operating conditions.

  - ❖ **Fault Isolation:** Identifying and isolating faults or failures in chiplet-based systems require efficient diagnostic tools, debug interfaces, and fault-tolerant architectures. Quick turnaround time in diagnosing and rectifying issues during production testing is crucial for yield optimization and time-to-market goals.

- **Exploding Test Conditions:**

  - ❖ **Test voltages**: Chiplets from different process nodes may have distinct operating voltage ranges. For example, 7nm process nodes might operate at lower voltages than

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

28nm, and providing a unified test voltage across chiplets can result in unrealistic or misleading test results.

- **Test temperatures**: Some chiplets might be more sensitive to temperature fluctuations, especially memory components (e.g., **SRAM**), which may show increased leakage at higher temperatures. Conversely, others may exhibit inverse temperature effects, where lower temperatures worsen performance. Proper thermal stress testing is needed across all chiplets to account for these variations.

- **Test frequencies**: Different chiplets could have varying maximum operating frequencies. For instance, high-frequency test conditions for one chiplet may not be applicable for another, especially if the chiplets are of different process nodes or utilize different kinds of logic.

- **High-Voltage Stress Tests:**

  - **High-voltage stress testing:** It is crucial for ensuring that components can tolerate voltage spikes that might occur in real-world applications or during power-up/down transitions. In addition stress-tests are used to accelerate failures so that a detection is possible to avoid early life failures. However, this can be problematic when chiplets from different technology nodes are integrated. Each node has different tolerance levels for high-voltage stress, and applying a generic high-voltage stress test might damage one of the chiplets or fail to stress the other appropriately.

- **Low-Speed Testing for SRAM (Leakage-Driven Faults):**

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **SRAM** is highly susceptible to leakage currents, which can cause **retention faults** at lower speeds or under certain voltage conditions. This is particularly important in the context of **low-speed tests** where SRAM cells might exhibit **bit errors** that aren't observable during high-speed operation. Since different chiplets (from different nodes or with different IPs) could have varying SRAM implementations, each one might need distinct low-speed stress tests focused on these leakage-driven faults.

- **Retention Tests for DRAM, MRAM, SRAM:**

  - **Retention testing:** It is crucial for ensuring data integrity in memory-based chiplets like DRAM, MRAM, and SRAM. These tests check whether the memory retains data under stress conditions like temperature fluctuations, voltage fluctuations, or extended periods of inactivity. As each memory technology has different retention characteristics, chiplets with DRAM will require different tests compared to those with SRAM or MRAM. For example, DRAM is more prone to refresh issues and leakage, while MRAM might need tests to ensure magnetic stability. Testing these different memory types under diverse conditions adds significant complexity.

- **Inverse Temperature Effect:**

  - **The inverse temperature effect**: It is a phenomenon where a component's performance might worsen at either high or low temperatures, depending on its underlying physical properties. For example, certain memory components like SRAM may show increased leakage at high temperatures, while MRAM might suffer from reduced magnetic performance. These effects must be considered during temperature stress tests, especially in heterogeneous chiplet-based systems, where different components might behave differently under varying temperature conditions. A unified test condition might

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

not be sufficient to account for the different behaviors of the integrated chiplets, and each chiplet might require independent temperature testing.

- **Dynamic Voltage and Frequency Scaling (DVFS) Challenges:**

  - **Voltage and frequency mismatches**: Some chiplets may have different voltage-frequency scaling capabilities or thresholds, making it difficult to find a common operating range that works for all chiplets. This could lead to scenarios where a chiplet operates outside of its optimal voltage/frequency range, resulting in performance degradation or increased power consumption.

  - **Power delivery and distribution**: Integrating chiplets with different power requirements in a single package requires a sophisticated power delivery network (PDN) that can manage varying power needs for each chiplet. Inconsistent or inefficient power distribution can lead to voltage droops or clock skew, exacerbating the DVFS-related challenges.

  - **Clock synchronization**: Coordinating clock speeds across chiplets operating under DVFS can lead to clock skew and timing issues. Each chiplet may need its own clock tree or PLL (Phase-Locked Loop), and ensuring proper synchronization can become increasingly difficult as more chiplets are added to the system.

Addressing these chiplet testing challenges requires a holistic approach encompassing DFT standards compliance, robust test architectures, advanced functional testing methodologies, and collaboration among chiplet vendors, designers, and test engineers. Embracing innovative test technologies, simulation platforms, and automated test generation tools can streamline chiplet testing processes and improve overall system quality and reliability. The goal of this whitepaper is to define the highlights chiplet testing consideration, challenges, and available

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

solutions framework to enable efficient production test of system-in-packages (SiPs) using die-to-die interfaces and ensuring high production yield.

3. Status of Chiplet Test

There are a variety of approaches and resources available for evaluating chiplet-based systems for functional correctness, performance, Interconnect, functional, and reliability testing are just a few of the many facets of chiplet testing cover. Existing chiplet test access as follows:

- **IEEE P1838 + IEEE 1149.1**:

  - One existing solution for chiplet testing combines the capabilities of IEEE 1838 and IEEE 1149.1 standards. IEEE 1838 provides a standardized test access architecture for 3D ICs, while IEEE 1149.1 (JTAG) enables the test access for each individual chiplet. This could be boundary-scan testing for the interconnects but also all other kinds of design-for-testability (DFT) driven tests like Scan or BISTs. By integrating these standards, the solution offers comprehensive testing coverage for chiplet interconnects and internal functionalities.

  - IEEE 1838 test access architecture for testing separate Die, Packaged Dies and System-In-Package test scenarios are depicted in Figure 1:

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

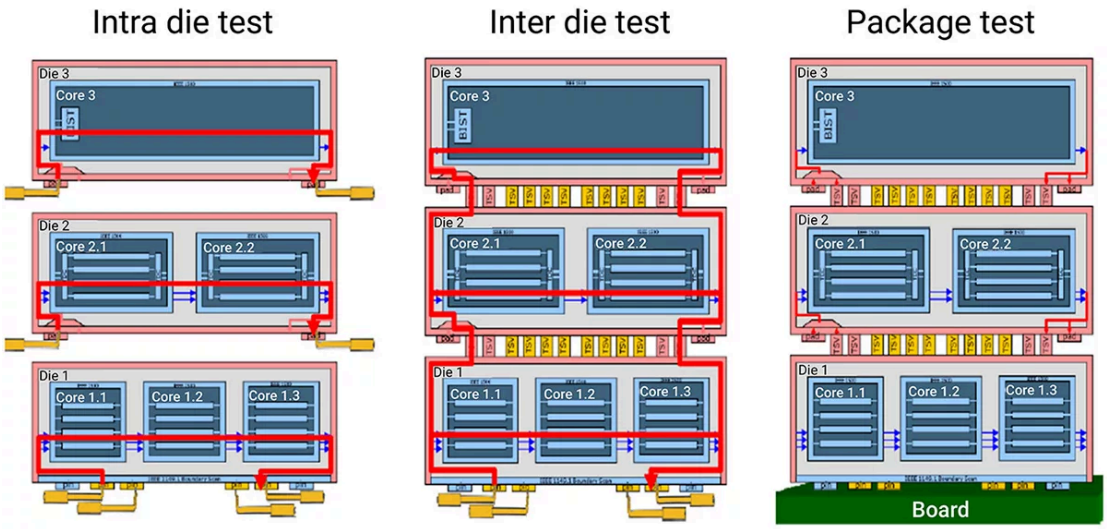


Figure 1. P1838 Test Access

There are existing test standards such as IEEE 1149.1, IEEE 1500, and IEEE 1838 , to define a test architecture that manages both Die-to-Die testing and separate Die testing, achieving functional blocks test coverage with minimal additional test circuitry. A serial port for test control and low-speed test data access (based in IEEE 1149.1) is implemented in each die and is accessible even after the final assembly, and IEEE also defines an optional parallel test access port (may not be accessible after assembly). In this architecture, both Intra and inter Die testing are covered. These ports use a reduced set of test-bumps for individual die testing or are seamlessly attached to the corresponding port in the other die.

A chiplet test infrastructure can be defined to incorporate IEEE 1838-compliant access points within the 3D IC stack, allowing for hierarchical access to embedded instruments. IEEE 1149.1 boundary-scan cells can be strategically placed on chiplets to facilitate interconnect testing and fault detection.

- **Scan Traffic over Native PCIe/USB Protocol**:

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- ❖ Another example solution leverages the native PCIe or USB protocol to facilitate scan traffic for chiplet testing. In this approach, test data and control signals are encapsulated within PCIe or USB transactions, allowing for efficient communication between the test controller and chiplets.

- ❖ For instance, a test controller connected to a chiplet via PCIe can send scan traffic using PCIe transactions, utilizing the high-speed data transfer capabilities of PCIe to accelerate test execution. Similarly, USB can be utilized for chiplet testing in scenarios where PCIe is not available or suitable.

- **Mux'ed with PCIe/USB/Other HSIO PHY**:

  - ❖ Some chiplet testing solutions integrate the test interface with high-speed input/output (HSIO) physical layer interfaces such as PCIe, USB, or other custom protocols. This integration allows for multiplexing the test signals with regular data traffic, optimizing the use of physical interconnect resources.

  - ❖ For example, a chiplet can share its HSIO PHY with both regular data communication and test access. Multiplexing techniques ensure that test signals do not interfere with normal data transmission and vice versa, enabling seamless integration of testing into chiplet operation.

- **Direct IOs through Active Interposer with Isolation Mode**:

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- An advanced solution involves utilizing an active interposer with isolation mode to enable direct I/O access for chiplet testing as illustrated in the Figure 2. The active interposer acts as an intermediary between the chiplet and the test controller, providing programmable signal routing and isolation capabilities.

- In this approach, the test controller can directly access the I/O pins of the chiplet through the active interposer, bypassing the need for complex protocol conversions or multiplexing schemes. Isolation mode ensures that test signals do not interfere with the normal operation of the chiplet, enhancing test reliability and accuracy.

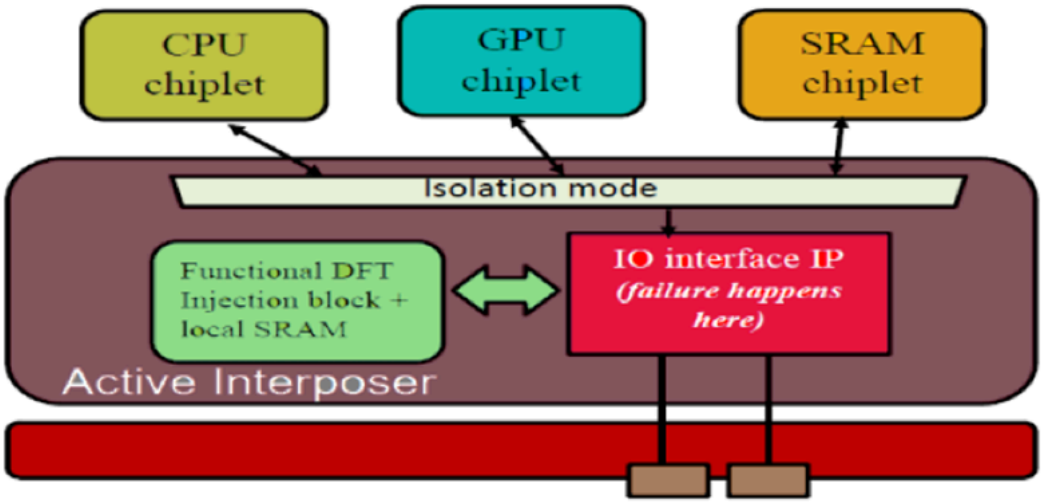


Figure 2. Direct IOs through Active Interposer with Isolation Model

These example solutions demonstrate different approaches to addressing the challenges of chiplet testing, leveraging standards such as IEEE 1838 and IEEE 1149.1, integrating with native high-speed protocols, multiplexing test signals with data traffic, and utilizing advanced interposer technologies for direct I/O access. Depending on the specific requirements and constraints of the chiplet system, one or more of these solutions may be suitable for efficient and effective chiplet testing.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

4. Chiplet Based SIPs-2.5D -> 3D

It is expected that requirements for speed and power will be significantly higher than the current state. Significant advancement to the integration of massive, high performance, low power die will be required for the future versions of application specific integrated devices also. Test will be significantly challenged.

While the current state of 2.5D/3D seems to be maturing, new enabling and supporting technologies will require advances in test access, capabilities, and costs. These emerging technologies will provide significant challenges for testing 2.5D and 3D technologies, The challenges below represent potential impacts to test, including increased costs, test times, and reduced yields and reliability.

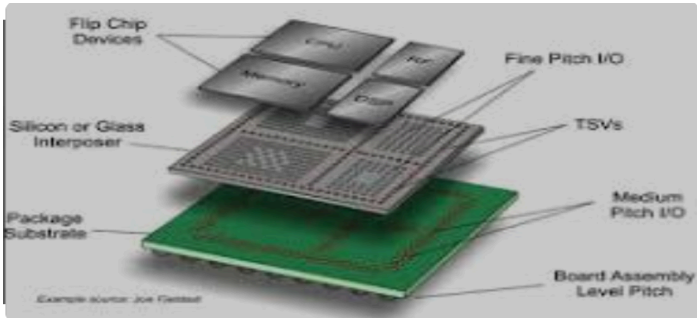


Figure 3. 2.5D Technology

Challenges when moving from 2.5D to 3D:

- **Known Good Chiplet Test (near term):** While logic blocks in the die can be partitioned and effectively tested, testing interactions between the logic blocks requires an application-based test.

- **Known Good Chiplet Test (long term):** From ITRS predictions, the number of flops per KGC are significantly higher (exponential) over time. Speed, power and thermal scale with logic. Device cooling during test will become critical. Timing may be an issue through the stack. Test time may be significant.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **System level test/diagnosis/repair (near term):** Emulating a system-level test environment (full chip model) can be considerably costly and time consuming. Complex integration can produce new and challenging defects for test. Cross domain frequency and voltage domain crossing tests can only be tested in a System environment.

- **System level test/diagnosis/repair (long term):** System test requires higher speeds. Longer test times due to significantly more logic in the die. IEEE 1149 protocols will be obsolete or antiquated at best. Optical protocols using IEEE P1838 test access protocols will replace current test protocols.

- **Access to the individual die in the 2.5D assembly:** Access may include multiple protocols: IEEE1149 based (including IEEE 1687.1 and IEEE P1838 proposed standards), photonics, various component, and system-level protocols, including I2C,I3C and SPI.

- **Interposer testing:** Point to Point testing can be accomplished primarily by probing, Multipoint interposer testing requires significantly more probing (more time and higher costs) and requires embedded logic to coordinate point-to-multipoint connections. Due to high speeds of signal just contact test may not be sufficient, some signal integrity or TDR tests at multiple temperatures may be needed. Probing will cause deformities on the pad that could result in assembly yield challenges so touchdowns should be minimal.

- **Discrete components:** More specific to high-speed interconnects through the interposer. Point to point, high speed interconnects may compromise probe-based connectivity test.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

❖ **Impact of emerging technologies with respect to test:** New technologies can impose new defects on the 2.5D. A table presented by Bayraktaroglu[14] describes the relationship to the new technologies (Die thinning, TSV, C2C connection, BS-RDL, micro-bumps, large volume of copper, increased power density and large thermal gradients, removal of IO structure) and the failure/defect mechanisms.

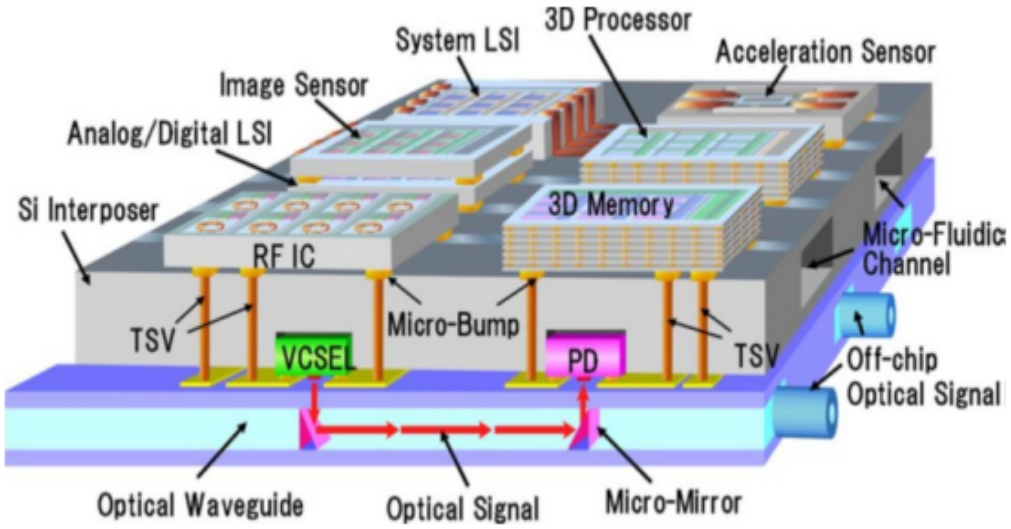


Figure 4. 3D technology

❖ **Known Good Chiplet test (near term):** Known good chiplet testing becomes more important in a stack integration, where a defective logic die could compromise the entire die stack. System/application-level testing at the die level has significant challenges. Significant Design-for-Test and Built-in Self-Test features are required to complement and simplify system/application-level test. Cost of test ($$ and time) are significant.

❖ **Known Good Chiplet(s) (long term):** similar to the 2.5D section, logic per die is increasing over time. Speed, power and thermal are scaling with increasing logic/flops. Heterogeneous die become more and more exotic, making test more challenging, and determining when the die becomes “known good”.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **System level test/diagnosis/repair (near term):** System and application-level test of a 3D die stack may require significant test/tester resources to emulate the component/test environment. These resources may consume significant time and money. Diagnosis of system level failures on the stack will have significant challenges. On a positive note, a diagnostic die may be added to the stack without significant effort. Redundant die may help as well.

- **System level test/diagnosis/repair (long term):** Test equipment cost increases significantly with respect to dollars and time. High speed signaling increases test costs and the possibility for errors/failures. Potential impact on the supply chain. With power on self-test feature and availability of redundant die In Field repair options can be used to prolong the life of the device.

- **TSV/interconnect testing:** TSV testing can be done pre-bond, micro void and pinhole defects. Mid-bond testing becomes quite challenging. Some probing could help. The interconnect test algorithm uses counting sequence patterns to test hard faults such as shorts. The algorithm gives pattern count for N interconnects equal to 2lg(N). A boundary-scan stack architecture can be utilized along with die level TAP in case of SiP using 2.5D integration where path from TDI to TDO traverses thru the interposer. The interconnect BIST controller can be designed in the case of 3D SiP where the traditional interconnect test patterns can be applied on TSV between dies. Application and/or system tests most likely will not be feasible or practical with part of the stack still missing. Test results may not be informative. Plan for Fbist, @speed testing between interconnected die at DFT architecture stage.

- **Probing 3D die stacks:** This area seems to be maturing. Companies like Tezzaron have probing figured out, since micro bumps also seem to be maturing. Stack repair: While stack repair is now possible, cost for stack repair and re-test would be prohibitive. Redundant die may simplify stack repair.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **High speed signaling/signal integrity/interconnects:** Signal integrity measurements from die to die are challenging. Design for Signal Integrity Test, at the edge of the die, may be a solution for SI measurement. Costs could be significant at the die level and higher at the stack level. There may be impact to stack level power. KGC/KGS: Known Good Chiplet is critical from a supply chain perspective. Known Good Stack also requires a stack level system/application test.

- **Mega Stack testing:** Mega Stacks address the need for high performance data processing. Stacking multiple dies becomes feasible as advances in die-to-die bonding minimize the stack size, while adding more die to the stack. Future Mega stacks may potentially have the same structural integrity as initial die stacks. Multiple redundant dies may be necessary for more probable defective die in the stack, or misconnections between die in the stack.

- **Probing die and stacks:** Advanced Probing technology will be needed as TSV's, and micro-bumps become significantly smaller. Stack repair: Primary repair will come from redundant die. Dis-assembly of the die stack becomes significantly challenging and could potentially destroy the pre-bonded die.

To enable test automation and reduce test time along with adequate test coverage is challenging for monolithic application, more challenging considering high-speed die-to-die links. The complete Die-to-Die link including the PHYs on both dies, the associated bumps, and the package link, need to be tested. This is solely relying on the test infrastructure built into the interfaces. The high-speed PHY for die-to-die connectivity must include several design-for-test (DFT) functionalities:

- Scan chains for static and at-speed detection of faults (stuck at, opens, slow path/transition) in digital circuitry.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- Built-in self-test (BIST) functionality, when possible, for specific digital and analog blocks.

- Internal loopbacks to test the individual PHY; These loopbacks can be shallow (covering the digital circuitry) or deep (covering all the transmit and receive signal path up to bump or as close to the bump as possible without avoiding mission mode performance impacts).

- Pattern generators and matcher.

- Support pseudo-random patterns or specific patterns.

- Ability to scan reference and phase to generate pass/fail eye diagrams to determine design margins.

- External loopbacks from one die to the next extending test coverage to the bumps and the die-to-die trace.

5. DFT Strategies

Design for Testability (DFT) strategies play a crucial role in ensuring the testability and manufacturability of integrated circuits, whether they are monolithic dies or chiplets within a heterogeneous integration framework. The similarities and differences in DFT strategies between chiplets and monolithic dies:

- **DFT Strategies Similarities:**

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- ❖ **Fault Coverage Goals:** Both chiplets and monolithic dies aim to achieve high fault coverage during testing to ensure that manufacturing defects, process variations, and functional faults are detected reliably.

- ❖ **Test Pattern Generation:** DFT techniques such as scan chains, built-in self-test (BIST) structures, and at-speed testing are commonly used in both chiplets and monolithic dies to generate and apply test patterns for fault detection and diagnosis.

- ❖ **Test Access Mechanisms:** Both chiplets and monolithic dies require efficient test access mechanisms (TAMs) to facilitate the application of test patterns and the capture of test responses during testing. This includes considerations for access to internal scan chains, BIST controllers, and test points.

- ❖ **Design Constraints:** DFT strategies in both cases must adhere to design constraints such as area overhead, power consumption, and test time constraints to ensure practical implementation and cost-effective testing.

- **DFT Strategy Differences:**
  - ❖ **Integration Complexity:** Chiplets often introduce additional complexity due to heterogeneous integration, where multiple chiplets are interconnected on a package or interposer. This requires novel DFT strategies for ensuring testability across chiplet boundaries and optimizing test access across different interfaces.

  - ❖ **Test Infrastructure Sharing:** In chiplet-based designs, there may be opportunities to share DFT resources (such as BIST engines, scan chains) among multiple chiplets, leading to potential optimizations in test resource utilization compared to monolithic dies.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Inter-Chiplet Communication Testing:** Chiplet designs require considerations for testing inter-chiplet communication interfaces, including high-speed serial links, parallel interfaces, or specialized protocols. DFT strategies must ensure full coverage of these communication paths during testing.

- **Fault Isolation Challenges:** Identifying and isolating faults within individual chiplets or at chiplet interfaces can be more challenging in chiplet-based designs compared to monolithic dies. Advanced DFT techniques such as hierarchical testing and debug infrastructures may be required.

- **Package-Level Testing:** Chiplet integration often involves testing at the package level, including testing interconnects, substrate connections, and overall system-level functionality. DFT strategies need to encompass package-level testing considerations in addition to chiplet-level testing.

- **For Monolithic Dies DFT Wrapper Standard Deployment:** IEEE 1500 and IEEE 1149 are commonly deployed as the DFT wrapper standard for monolithic dies. It defines a hierarchical test wrapper architecture, test access mechanisms (TAMs), and integration guidelines for enhancing testability.

- **For Chiplets DFT Wrapper Standard Deployment:** The deployment of DFT wrapper standards for chiplets may vary depending on the specific chiplet integration scheme and the interfaces involved. Standards such as IEEE 1149.1 (JTAG) and IEEE 1838 are relevant for chiplet-level testing, especially for accessing and controlling embedded instruments and inter-chiplet communication paths.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

In summary, while many DFT principles and techniques apply similarly to chiplet and monolithic die designs, chiplet integration introduces unique challenges related to test access across chiplet boundaries, inter-chiplet communication testing, fault isolation, and package-level testing. Addressing these challenges requires innovative DFT strategies tailored to the specific characteristics and requirements of chiplet-based designs.

6. Accelerating Test

There are several other test acceleration techniques and methodologies used for chiplet testing. The notable test acceleration are:

- **Built-In Self-Test (BIST):** BIST is a technique where self-testing circuitry is integrated into the design of the chip. This circuitry generates test patterns, applies them to the circuit, and analyzes the responses, all without external test equipment. BIST can accelerate testing by reducing the need for external test resources and enabling on-chip testing.

- **Scan Compression:** Scan compression techniques aim to reduce the volume of test patterns required for testing while maintaining high fault coverage. By compressing test patterns, testing time can be significantly reduced, improving overall test efficiency.

- **On-Chip Instrumentation:** On-chip instrumentation involves embedding measurement and monitoring circuitry within the chip. This allows for real-time monitoring of various parameters during operation, aiding in fault detection, diagnosis, and performance optimization.

- **Parallel Testing:** Parallel testing involves running multiple tests concurrently on different parts of the chip or across multiple chiplets. This can be achieved through parallel test access mechanisms and concurrent test execution, reducing overall test time. Example

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

of parallel testing is direct IOs through active interposer with isolation mode, as shown in Figure 2: Direct IOs through Active Interposer with Isolation Model [1] above.

- **Streaming Scan Network:** Streaming Scan Network (SSN) is a testing methodology and architecture designed to optimize the testing process for integrated circuits (ICs), especially in complex chiplet-based designs and multi-die systems. The SSN solution utilises IJTAG, which is the IEEE standard 1687, as a framework or test infrastructure. Additionally, SSN incorporates a streaming scan host (SSH) component into every design block or core. Example of SSN DFT architecture is illustrated in Figure 5.

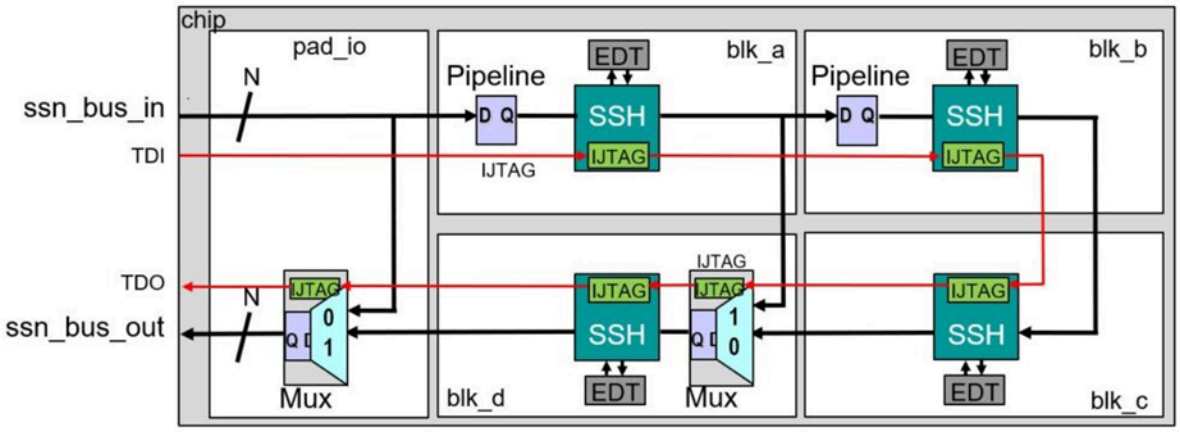


Figure 5. SSN DFT Architecture

While IEEE 1838 did establish a standard for the DFT infrastructure to facilitate inter-die integration and the hardware protocol, it failed to distinguish between 2.5D and 3D testing requirements, performance criteria for the DFT, and the test operation language. Therefore, an IEEE 1149.1 compliant IP that utilises a streaming scan network architecture based on IJTAG 1687 will enable 3DIC testing. Streaming Scan Network (SSN) offers the following benefits:

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Uniform Access Technology:** SSN serves as a uniform access technology, providing standardized and efficient access for test patterns across different IPs (Intellectual Properties) within a chiplet or die.

- **On-Die Standard Scan Pattern Delivery:** Within the chiplet, SSN ensures the delivery of standard scan patterns effectively through the scan compression network. This optimized delivery process helps in reducing test data volume and enhancing compression techniques.

- **Asynchronous Interface for Balanced Data Volume:** SSN's asynchronous interface is pivotal as it enables the delivery of balanced data volumes across various IPs on the chiplet. This feature is crucial for accommodating diverse data volume requirements across different IP blocks.

- **Universal Test Access Mechanism:** As SSN adoption grows, it is increasingly becoming a universal test access mechanism for most advanced chips. Its versatility and efficiency make it a preferred choice for ensuring comprehensive test coverage.

- **High-Speed Pattern Delivery Across Dies:** Transmitting test patterns across multiple dies is significantly improved with SSN, especially when leveraging high-speed buses like HSIO or D2D interfaces. The ability to deliver patterns at 3x to 5x speeds can be a game-changer in speeding up testing processes.

- **Standardizing Pattern Delivery with IEEE 1149.10 HSTAP:** Adopting the IEEE 1149.10 HSTAP standard is a viable solution for standardizing high-volume pattern

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

delivery at high speeds into chiplets. This involves developing corresponding IP for HSIO or D2D interfaces and additional interfaces for Automated Test Equipment (ATE).

- **Integration with SSN Network:** The 1149.10 HSTAP interface seamlessly integrates with the SSN network, facilitating the high-speed delivery of SSN patterns into each chiplet. This integration streamlines the testing process and ensures compatibility across interfaces.

- **Advantages and Efficiency:** Leveraging SSN and IEEE 1149.10 HSTAP offers several advantages, including higher-speed pattern delivery, reduced test time, and optimized utilization of test resources. The technology's compatibility with HSIO or D2D interfaces eliminates the need for additional test pins, simplifying the overall testing architecture.

In conclusion, Streaming Scan Network (SSN) coupled with standards like IEEE 1149.10 HSTAP represents a cutting-edge approach to test access and pattern delivery in complex chip designs, offering enhanced speed, efficiency, and compatibility across chiplets and dies. Example of 2.5D DFT methodology leverage SSN and 3D DFT methodology leveraging SSN is shown in Figure 6 and Figure 7.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

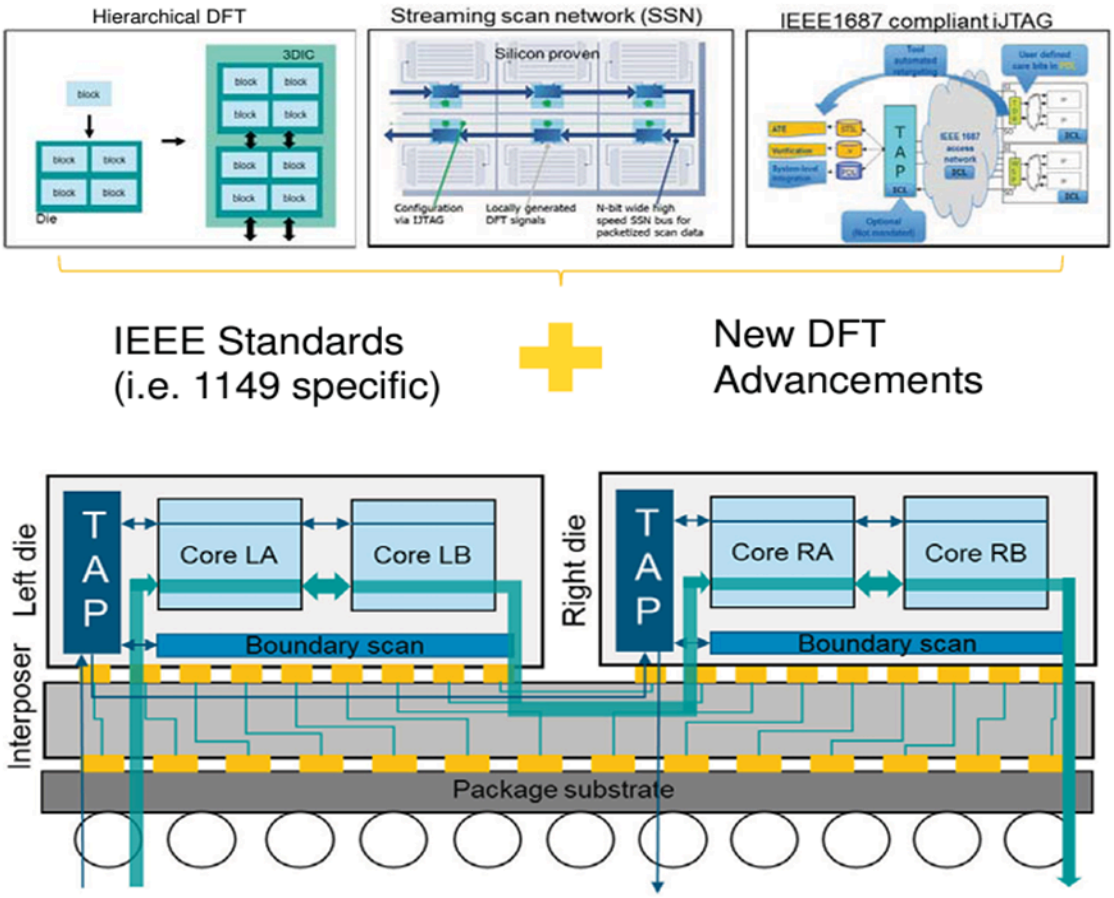


Figure 6. 2.5D DFT Methodology Leveraging SSN

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

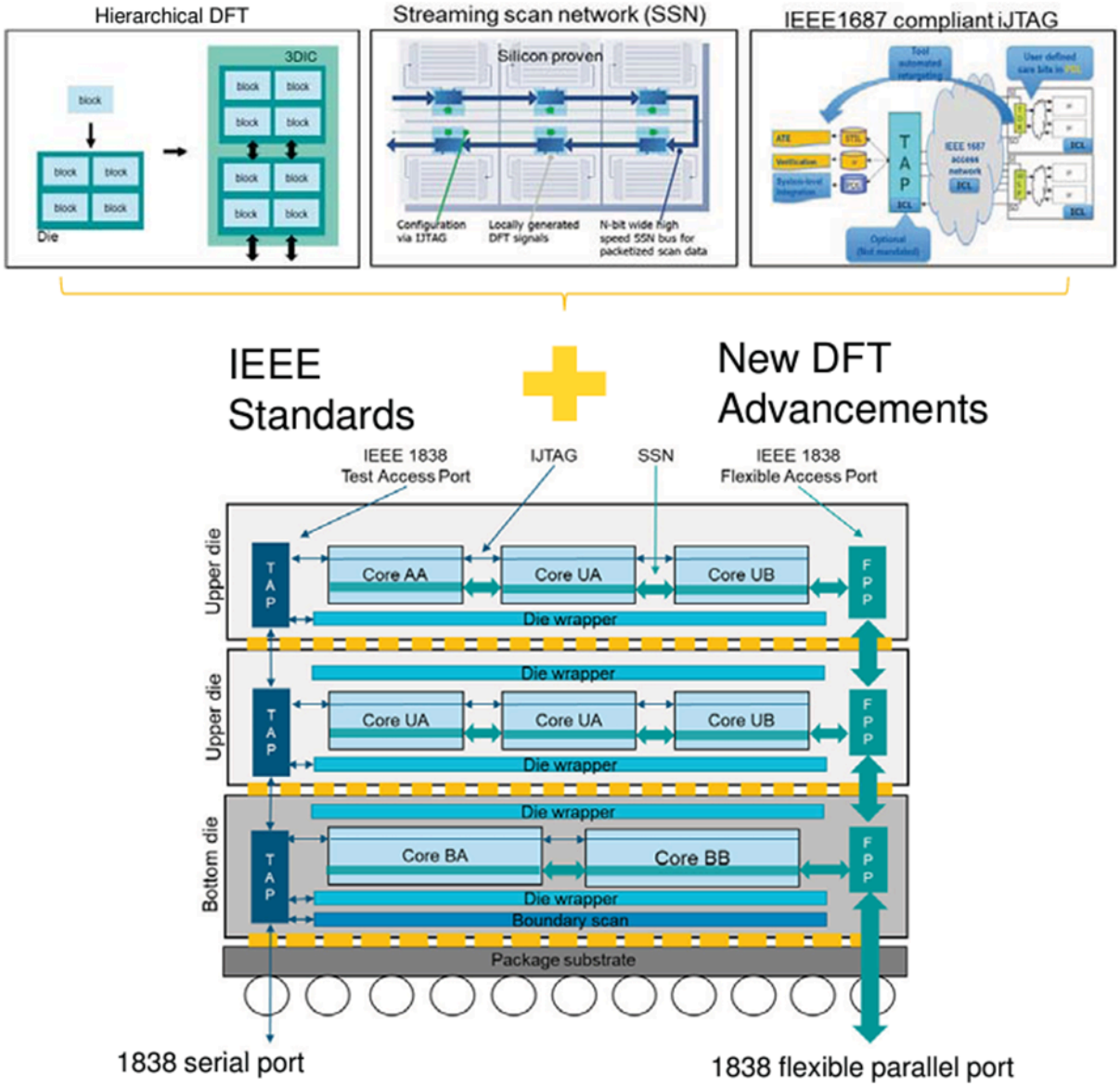


Figure 7. 3D DFT Methodology Leveraging SSN

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

7. System Level and Functional Tests

All tests performed on the devices including package test/final test are all manufacturing defect related tests; the tests are structural scan tests. Test plan could include functional test however the functional test is not a use case functional test either the tests are run tester assisted or through test cases loaded through the cache. The power is tester constrained and normally test power not mission mode power, the test path is predictable/deterministic unlike mission mode. The thermal profile at test will also not match mission mode; in test the entire device is subjected to uniform heating or cooling for a short time. In use cases there is a thermal gradient, and the heat accumulates over time and prolonged the physics of Si expansions, interface expansions, thermal impact on interconnect vias and TSV all act differently. SIP's have multiple frequency domains, during ATE testing each of these frequencies are tested independently but in the system the device internals work at different frequencies. Dynamic Voltage and frequency scaling (DVFS) is employed to optimize power and performance of modern-day devices, the di/dt impact on circuits during frequency changes cannot be created in ATE test payloads. In ATE testing all high-speed interfaces are tested for functionality with loopback configurations, these pseudo functional tests are not done under load condition. To address these, 3 types of system level tests (SLT) are needed, this is true for both SIP's and Monolithic devices.

1. One time Characterization of power, performance and electrical validation of interfaces signal under different load conditions in a user environment, these tests could include electrical tests like setup time, hold time, slew rates, eye margin, cross talk, jitter margin etc. test for protocol compliance. This could be done on reference designs with appropriate hooks for external measurement instrument hookup. This will need to be characterized at different test temperatures and also across various process corners like Fast, Typical, Slow and various combinations of these. Generating characterization samples for various corners in a multi-die SIP will be a logistical nightmare.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

2. Functional tests are done in use case environment with all device settings controlled thru BIOS, powerup thru PMICS and control by software, on booting successfully tests that include all pre-silicon design verification payloads, tests that target internal IP, tests that exercise functional data path from input to output, tests that exercise all device features. It should include the complete software stack, feature targeted test, performance indicator tests, performance per watt determination tests, tests that determine latency between different interfaces, different vendors, tests that provide maximum throughput, tests that check device safety and reliability features. Design bug fixes from roadmap devices. Tests that monitor and report health of devices, tests that identify need for self-repair and perform self-repair etc. Corner case test cases that could have escaped our HVM testing. Tests need to be run in both verification and stress mode. A one-time effort of Correlation for frequency and performance between ATE and System boards need to be performed in this step and ATE next program needs to be guard banded accordingly. These are regressions that need to be performed once for every small change in device setting, fuse setting, software change and new design revision. The hardware could be the same as the customer reference or design verification board.

3. SLT is needed in HVM also. This is the last chance to improve DPPM, before a defective part can reach the customer. The impact on DPPM from this test step can be evaluated only by testing millions of devices and analyzing data. The Payload for this insertion could be a subtest of the Functional test including powerup of each die in a SiP separately, booting of device from OS, any test cases identified by customer as test escape from ATE testing step, design/process corner case test cases, legacy test escape test cases, test cases that interact with all I/O interfaces in the user board. Hardware for this test insertion includes a system board that acts like the tester and special SLT handlers that have high parallelism. As test time is huge, high parallelism is necessary. Tools need to be developed to identify the failure mechanism in SLT and convert to ATE test case and update program at the earliest insertion where this failure could be caught.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Unlike monolithic die, for chiplet design, it posts the additional functional verification for inter-chiplet and intra-chiplet connection as illustrated in Figure 8 where additional model required from physical layer till application layer. The additional functional verification challenges for chiplet designs are:

- **Micro architecture and intra chiplet functional Layer Verification:** Validating data exchange, synchronization, and protocol adherence between chiplets, especially in heterogeneous chiplet architectures.
- **System Layer Verification:** Integrating multiple chiplets into a cohesive system, verifying inter-chip communication protocols, data routing, and ensuring seamless operation across chiplet boundaries.
- **Application Layer verification:** Validating end-to-end application workflows spanning multiple chiplets, ensuring data coherency, fault tolerance, and system-level performance.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

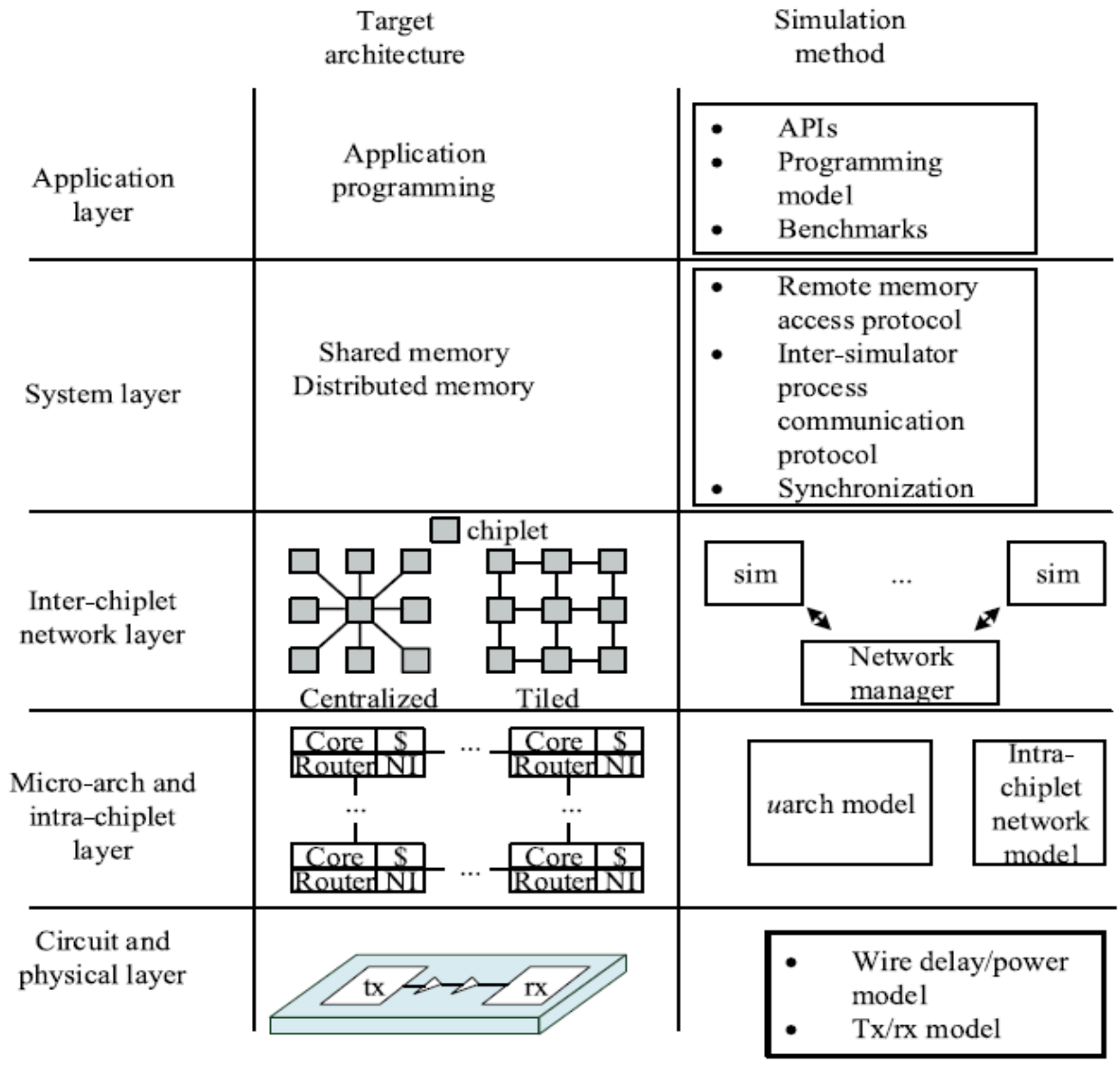


Figure 8. Chiplet Intra-chip and Inter-chiplet Design and Verification Challenges

In summary, the functional verification challenges in chiplet-based designs demand a comprehensive approach spanning from the physical layer's signal integrity to the application layer's functional correctness.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

8. KGC Testing and Assembly Yield Recovery

Known Good Chiplet (KGC) testing and assembly yield play crucial roles in chiplet-based designs and semiconductor manufacturing. The significant of KGC Testing are:

- **Quality Assurance:** KGC testing ensures that only fully functional dies are used in the assembly process, reducing the risk of defective components in the final product.
- **Yield Improvement:** Identifying and segregating defective dies early in the manufacturing process improves overall yield by preventing faulty components from entering the production line.
- **Reliability Enhancement:** KGC testing enhances the reliability and performance of assembled systems by using only verified and validated dies, reducing the likelihood of field failures.

Assembly Yield for Chiplet-Based Designs refers to the percentage of fully functional and defect-free chiplet assemblies or packages produced during manufacturing. The importance of assembly yield for chiplet designs are:

- **Complexity Management:** In chiplet-based designs, where multiple dies (chiplets) are integrated into a single package or system, achieving high assembly yield is crucial due to increased complexity and interconnect challenges.
- **Cost Efficiency:** Higher assembly yield reduces scrap and rework costs associated with defective chiplet assemblies, contributing to overall cost efficiency in semiconductor manufacturing.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Product Quality:** High assembly yield ensures that the final products meet quality standards and reliability expectations, enhancing customer satisfaction and brand reputation.

- **Time-to-Market:** Improving assembly yield accelerates production cycles and time-to-market for chiplet-based products, crucial in competitive industries.

Hence, KGC and assembly yield are important for Chiplet-Based Designs to ensure:

- **Interconnect Reliability:** Chiplet designs rely heavily on interconnects between dies. Ensuring KGC and high assembly yield mitigate risks related to interconnect failures or defects, critical for system functionality.

- **System Integration:** KGC testing and high assembly yield are prerequisites for seamless integration of chiplets into complex systems such as CPUs, GPUs, or SoCs (System-on-Chips).

- **Performance Optimization:** By incorporating only known good chiplets, manufacturers can optimize system performance, power efficiency, and thermal management, meeting performance targets reliably.

KGC testing and achieving high assembly yield are essential pillars in semiconductor manufacturing, particularly in chiplet-based designs. To ensure product quality, reliability, cost-effectiveness, and timely delivery of advanced semiconductor products in today's competitive markets for chiplet KGC testing and high assembly yield, it can be achieved with following test mechanism:

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Die-to-Die Interconnect Test and Repair Feature:** This feature involves testing and repairing the interconnects between dies in a multi-die assembly. It ensures that communication pathways between individual dies are functional and reliable. Repair mechanisms may involve rerouting connections or implementing redundant paths.

- **Naked Die Internal and External Loopback Modes**: Internal loopback mode tests the functionality of various components within a die, such as memory blocks, logic units, and I/O interfaces. External loopback mode validates the connectivity and performance of IO's with external devices or interfaces.

- **Random and Programmable Test Pattern Generation and Matching:** Random test pattern generation helps in detecting random faults or defects across the die. Programmable test patterns allow targeted testing of specific circuits or functionalities based on predefined test vectors. Matching ensures that the expected responses align with the generated test patterns.

- **IDDQ and Burn-in Test Mode:** IDDQ testing measures the quiescent current of the die to detect potential leakage or short circuits. Burn-in test mode subjects the die to prolonged operational conditions to identify early failures due to aging or stress.

- **BIST of Critical Blocks and Scan Chains:** Built-In Self-Test (BIST) mechanisms within critical blocks ensure self-testing capability for key functionalities such as memory, processor cores, or communication interfaces. Scan chains facilitate efficient testing of sequential logic elements and memory cells.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Mission Mode Health Monitoring & UCIe Repair:** Mission mode health monitoring involves continuous monitoring of die health during operational phases, enabling proactive maintenance or repair actions. Universal Chiplet Interconnect (UCIe) repair mechanisms address faults or errors in chiplet interconnects, improving overall system reliability.

- **Built-In System Integrity Monitor (SIM):** SIM continuously monitors system integrity and detects deviations from expected behavior or performance metrics. It helps in identifying and isolating faulty components or subsystems for targeted repair or maintenance.

- **Embedded and Cloud Analytics for Real-Time Control & Fleet Statistics**: Embedded analytics provide real-time monitoring and control of test processes, allowing for immediate corrective actions or adjustments. Cloud-based analytics leverage data from multiple sources to analyze fleet-wide statistics, trends, and performance metrics for predictive maintenance and yield improvement strategies.

- **Test and Repair of Individual Die Traces:** Granular testing and repair of individual traces or connections within a die ensure high interconnect reliability. Repair mechanisms may involve redundancy activation, trace rerouting, or use of spare resources.

- **Integration in On-Die and Multi-Die Hierarchical Test Solution:** Integration of these testing and repair features within hierarchical test solutions ensures comprehensive

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

coverage from individual die testing to system-level validation. Hierarchical approaches optimize test time, resource utilization, and overall assembly yield recovery.

By leveraging these advanced testing and repair features, semiconductor manufacturers can enhance yield recovery, improve product quality, and ensure the reliability of complex multi-die assemblies and hence reducing the scrap cost of chiplet system in package integration as shown in Figure 9.

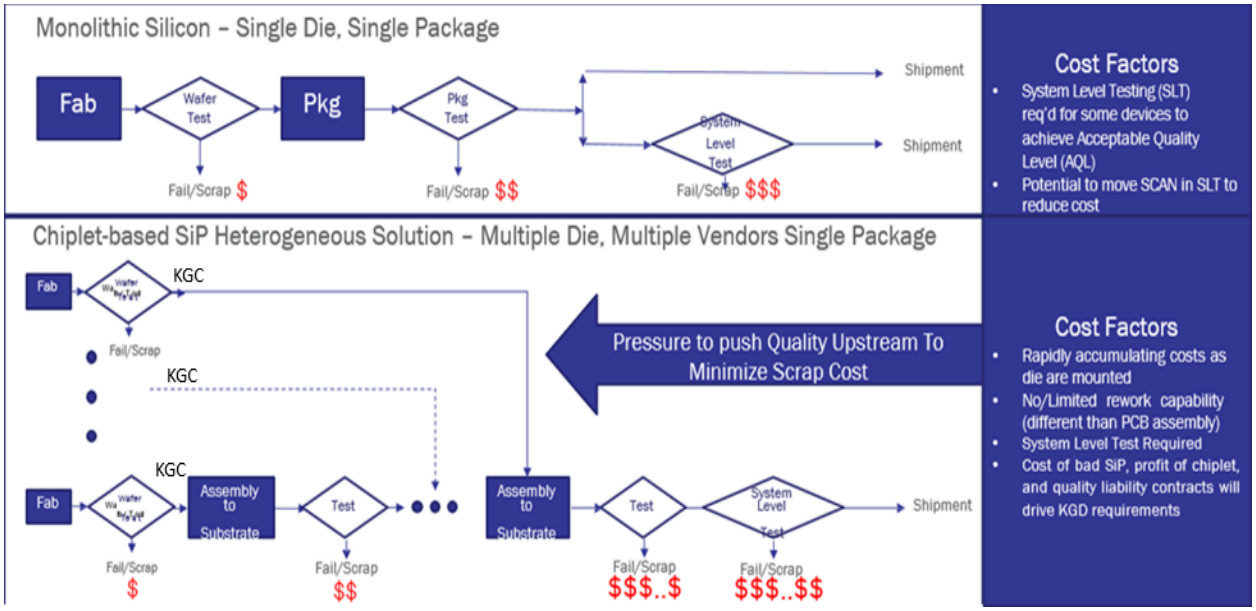


Figure 9. Significant of KGC on Chiplet SIP [12]

9. Test Cost

Testing is a crucial part of the chiplet design flow that significantly impacts cost and reliability, as outlined in the OCP white paper “Business Analysis of Chiplet-Based Systems and Technology “. Proper testing approaches must be considered throughout the design process to optimize costs while still ensuring high product quality. This section will provide an in-depth look at testing considerations, costs, and techniques that are especially relevant for chiplet-based systems.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Wafer Sort Testing

Wafer sort, or wafer probe, testing is the first step in the testing process where individual dies on a wafer are tested before dicing and packaging. This helps identify defective dies so they can be discarded before incurring additional assembly and packaging costs. For monolithic designs, wafer sort typically involves testing the full functionality of the die under test (DUT). However, for chiplet-based designs each individual chiplet must be tested separately during wafer sort. This adds testing complexity and cost overhead compared to monolithic designs for a few key reasons:

- Test programming and debugging is more complex since each chiplet may have unique test requirements and failures need to be isolated to specific chiplets.
- Test times are inherently longer since every chiplet needs to be tested rather than a single test per wafer.
- Smaller chiplet sizes result in less test parallelism, as fewer chiplets can be tested at once on a wafer prober limited footprint. This reduces throughput.
- Smaller probe bump/pad pitch increases cost of probe card exponentially.
- Die thinning to accommodate 2.5D or 3D packaging increases probability of mechanical failures.
- More tester channels and pin electronics are required to interface with all the input/outputs of the individual chiplets rather than a single large die.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- Increased complexity of test programs handling each unique chiplet design and any custom interfaces between chiplets.

- Chiplets from multiple foundries or processes may require different test conditions and equipment, increasing complexity.

To help mitigate these issues, chiplet designs should incorporate robust design for testability (DFT) techniques. Common approaches include scan chain design, built-in self-test (BIST), test compression, and shared test infrastructure. Proper DFT optimization during the design phase is critical to control wafer sort costs for chiplet designs. A thorough analysis should be performed early on to estimate test times per chiplet, and overall test costs based on the targeted fabrication volume and yields. The goal is typically to keep wafer sort costs below 15-20% of total chip costs.

Assembly and Package Testing

After wafer dicing, the next stages are chiplet assembly and package testing. Just like with wafer sort, each individual chiplet must now be tested as part of the assembly process. The specific testing steps will depend on the package type and assembly flow. Testing costs at this stage are impacted by:

- **Number of chips:** More chips mean more test handling and complexity.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Test socket/interface design:** Must support chip-level and package-level testing with minimal impact on yield.
- **Parallelism:** Ability to test multiple chips simultaneously can significantly reduce test times.
- **DFT infrastructure:** Scan, BIST and other techniques help minimize vector counts and test times.

As access to chiplet is very limited in an assembled package need to incorporate contactless functional/mission mode debug. Strategies like modular test programs, re-use of chip-level tests at the package-level, and design for testability assist in controlling assembly and package test costs. The target is typically to keep these costs below 30-40% of the total chip costs.

Board Level System Testing

Once chiplet-based modules complete assembly and package testing, the next stage is integration onto system boards and final system-level tests. At this point, the modules can be treated largely as “black box” components.

While system test costs are smaller on a per-unit basis, testing complexity increases substantially for large heterogeneous systems with many specialized chips and modules. Key factors that impact costs include:

- Hardware-in-loop testing requirements which may require expensive prototypes/emulators.
- Software debugging and validation effort which dominates overall test times.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- Test reuse with ability to leverage module/chip-level tests at the system level by treating them as self-testing components.

- Debuggability features like system-level visibility assist with troubleshooting failures in complex designs.

- Correlation where accurate test methodology to correlate for power, speed and performance between ATE and mission mode.

Targeting 75-90% re-use of lower-level tests help achieve cost-efficient validation of chiplet-based systems. Techniques like processor-in-loop testing, built-in self-test of subsystems, and modular diagnostics are commonly utilized approaches.

Test Economics Modeling

To evaluate the overall economic impact of different design, DFT, and test strategies, companies typically build cost models based on key test parameters:

- **Device technology:** Impacts complexity/testability and influences tooling costs.

- **Design size/complexity:** Larger/complex chips/systems have inherently higher costs.

- **Parametric vs. functional testing requirements:** Parametric testing is generally more expensive.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Test coverage:** Higher coverage comes at increased test cost/times.

- **Pre Si-Verification:** should cover all corner cases and if possible, done with full chip model which increases compute resources and execution cycles/time

- **Test development vs. sustaining costs:** Development costs are much higher upfront.

- **Tester/handler availability:** Constraints achievable throughput and capacity.

- **Test parallelism:** Ability to test multiple units simultaneously reduces unit costs.

- **Software validation effort:** Often a dominant cost component for system validation.

- **Defect levels:** Expected yield impacts required testing to achieve target quality levels.

- **Test re-use strategies:** Re-use across abstraction levels like chip/module/system testing.

Models can estimate costs for different program phases like development, ramp, and sustaining test. This allows evaluating tradeoffs of approaches like DFT optimization versus additional test hardware/parallelism investments upfront. Sensitivity analysis helps assess risks and impact of potential yield issues or program delays.

Proper test cost modeling and analysis is crucial for chiplet adopters to understand total cost of test, justify test program budgets, and identify opportunities for further cost reduction through

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

optimization. The end goal is achieving the necessary reliability levels to satisfy customer expectations, while keeping testing costs as a small percentage of overall product costs.

The test cost consideration at various testing stages is shown in Table 1.

Table 1. Test Cost Consideration at Different Testing Stage

Testing Stage	Key Considerations	Target Costs	Key Techniques
Wafer Sort Testing	-Additional test equipment required for individual chiplets -Increased test programming/debug complexity -Longer test times due to individual chiplet testing -Limited parallelism from small chiplet sizes -More tester channels/electronics -Complex multi-chiplet test programs -Different test requirements by fab/process -High hardware costs	Keep costs below 15-20% of total chip costs. Test cost target varies by application. Majority of soc test cost below 5% of total chip cost but performance grading chip test cost can be as high as 20%. Target is to minimize test time per chiplet through optimized DFT and test parallelism.	-Scan chains with efficient stitching across chiplet boundaries -Modular/programmable BIST circuits in each chiplet -Pattern multiplexing and response compaction in test compression -Shared clocks, reset ports and test access mechanisms

| Testing Stage | Key Considerations | Target Costs | Key Techniques |

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Assembly & Package Testing	-Number of chips impacts complexity/cost -Test socket/interface design impacts yield -Level of parallelism impacts time/cost -DFT infrastructure impacts vectors/time	Keep costs below 30-40% of total chip costs. Target is temporary test sockets/interfaces with minimal impact on yield through modular test programs and reuse of chip-level tests.	-Reusable test modules/programs for chiplet-level and package-level testing -Standard interfaces for wafer-level chiplet test and package test -Optimization of parallelism through temporary socket/interposer designs
Board-Level System Testing	-HW-in-loop testing cost -SW validation effort dominates time/cost -Debuggability impacts troubleshooting -Test re-use impacts economies -Contactless debug capability	Target is 75-90% reuse of chiplet/module level tests to maximize economies of test scale. Focus on modular diagnostics and efficient debugging.	-Processor-in-loop self-tests of board level functionality -Module level Built-In Self-Tests (BIST) with minimal board level programming -Modular Isolation and debugging using JTAG boundary scan and trace capabilities
Test Economics Modeling	-Device/design complexity -Parametric vs functional testing -Test coverage impacts cost/time -Development vs sustaining costs	-Sensitivity analysis to evaluate tradeoffs and risks	-Proper cost modeling to justify budgets and optimize costs considering DFT techniques, parallelism levels, expected yields etc.

In contrast to conventional monolithic devices, the genesis and production methodology for chiplets diverge substantially. The refuse expenses linked to the production of conventional monolithic semiconductor devices exhibit an essentially linear trend, encompassing costs for individual chips, packaging, and assembly, as shown in Figure 10.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.



Figure 10. Monolithic Device Scrap Cost

Significant variations exist between 2.5D and 3D design manufacturing processes regarding the accumulation of waste costs. Scrap expenses for multiple dies, multi-chip partial assemblies, and/or complete 2.5D/3D packages cause a precise geometric increase in these costs from fabrication to assembly as shown in Figure 11.

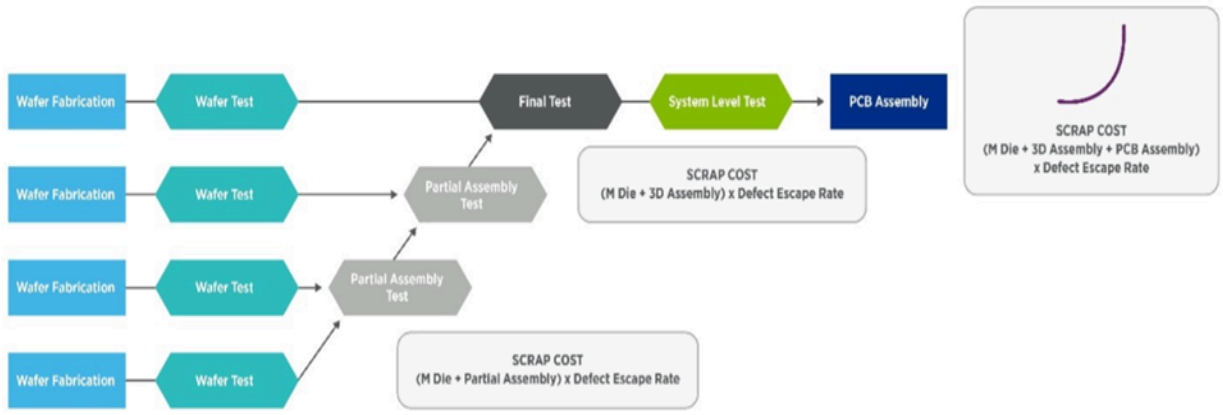


Figure 11. Chiplet Device Scrap Cost

The economic feasibility of 2.5D/3D packaging, which facilitates the advancement of Moore's Law, hinges on the reduction of defect escape rates during the initial stages of production to minimize discard expenses. By shifting tests to the left or right during the testing procedure, these objectives can be met while the overall cost of producing 2.5D/3D components is reduced. The capability to increase test coverage earlier in the manufacturing process to optimize KGC and decrease future packaging expenses is referred to as "shift left" in Figure 12.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Further tests may be incorporated into the procedure to detect and classify novel failure modes or types. Nonetheless, the advantages of shift left must be considered. An instance of this can be when, early in the manufacturing process, an increase in test intensity can have a positive effect on known excellent devices. Nevertheless, this can also lead to an increase in test expenditures that, despite the reduction in scrap costs from the optimization, is insufficient to offset.

A shift to the right entails augmenting test coverage during the later stages of production, thereby enhancing the capacity to identify flaws and uphold quality standards while striving to decrease expenses through increased parallelism in testing.

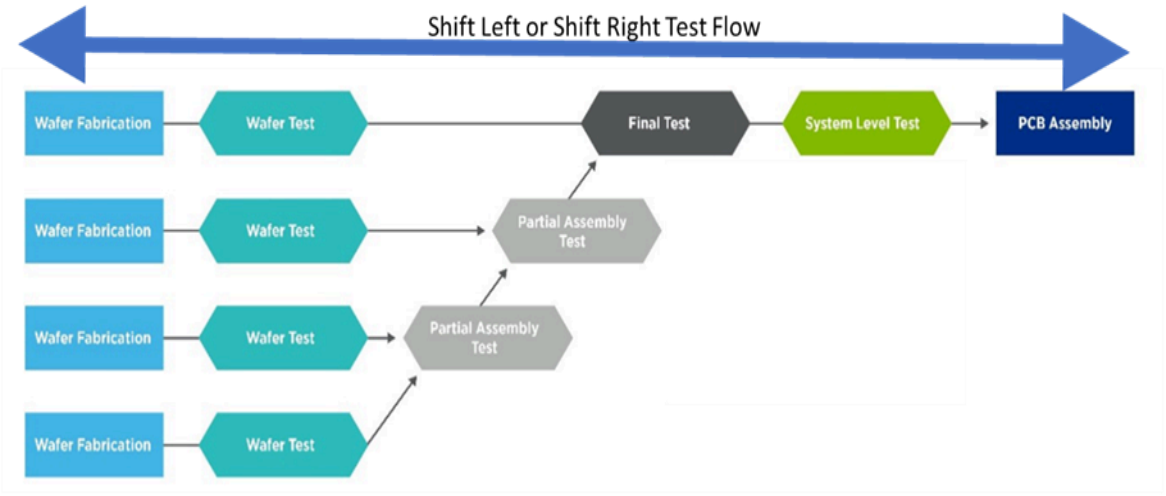


Figure 12. Chiplet Test Shift Left or Shift Right Consideration

10. Comparison of Test Costs

This section aims to do an in-depth comparison of the test costs incurred in chiplet/multi-die systems versus monolithic systems referring to insights from the OCP white paper “Business Analysis of Chiplet-Based Systems and Technology”. Test costs play a major role in determining the economic viability of adopting a chiplet-based design approach. This section will analyze test costs at various levels - wafer/die, module/package for both monolithic and chiplet-based approaches to understand the tradeoffs.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Wafer/Die Level Testing

For monolithic designs, the die undergoes wafer probe testing after fabrication. This involves using automated wafer probers to electrically test each die on the wafer using techniques like at-speed scan. Any defective dies are marked and discarded prior to dicing and packaging.

In a chiplet-based system, each individual chiplet undergoes wafer probe testing after fabrication just like a monolithic die. This is important to ensure only Known Good Chiplet (KGC) are assembled as defective chiplets could compromise the reliability of the overall module. While the per-chiplet test costs may be higher compared to a monolithic die due to smaller size, the overall yield and hence number of KGC chips is higher owing to reduced chip area.

For example, considering a monolithic design with a die size of 100mm2 with a typical yield of 70% versus 4 chiplets each of 25mm2, the total chiplet area is 100mm2. But with a yield of say 85% for each smaller chiplet, the overall number of KGC would be higher (0.85 for 4 chiplets versus 0.7 for the monolithic case). While per-chiplet test costs are higher, the overall test costs are lower due to increased KGC.

If the Chiplets are going to be used in 2.5/3D packaging, then the chiplets are assembled over a base die/interposer/active interposer called stacked die. There is a tedious process of wafer attaching to a carrier wafer, thinning and pad exposure for stacked die testing. The test content is very similar to final test content, this process doubles the cost of wafer sort.

Module/Package Level Testing

After assembly and packaging, module-level testing is performed to test the inter-chip connectivity and functionality of the overall module. For monolithic designs, this typically involves one-time testing of the packaged die.

For chiplet-based systems, module-level testing involves added complexity. Each constituent chiplet needs to be tested again after assembly in the module/package to validate intra-chip functionality as well as test the inter-chiplet connections through one or more test sessions depending on the number of chiplets.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

While more test sessions are needed for chiplet-based modules, there can be ways to optimize this using advanced DFT techniques as mentioned in the previous section. Even with such optimizations, module level test times and hence costs for chiplet systems are inevitably higher than monolithic counterparts due to multiple sessions needed. However, this overhead can be offset by higher yields and aggregate volume as discussed next.

Test Cost Impact Of Higher Yield

One of the major motivating factors behind adopting a chiplet design approach is the significant yield improvements possible due to smaller chiplet sizes. As die size scales down in advanced process nodes, yield drops dramatically with even minor defects rendering the entire die unusable in monolithic designs.

By slicing the die into smaller chiplets, the impact of localized defects is contained only to that chiplet rather than the entire die. As per the white paper, AMD reported 2X-3X yield gains for their chiplet-based CPUs. The numbers are similar or could be even higher for designs targeting leading edge nodes.

The increased number of KGC die/chips obtained from the higher chiplet-based yields directly impacts the test costs as more devices can be profitably tested and utilized. Consider a typical monolithic die with 70% yield yielding 700 KGC from 1000 total die.

For the same design split as 4 chiplets each with 85% yield, 1000 total die would yield 1000 * 0.85*4 = 3400 KGC. Though testing 4000 chiplets each cost slightly more than 1000 monolithic die individually due to smaller size, the 21% increase in KGC offsets this additional cost. The general formula for the monolithic IC test cost and chiplet test cost can be summarized in Figure 13. The technology cost is included as the mask and wafer cost for monolithic die and chiplet will be different.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

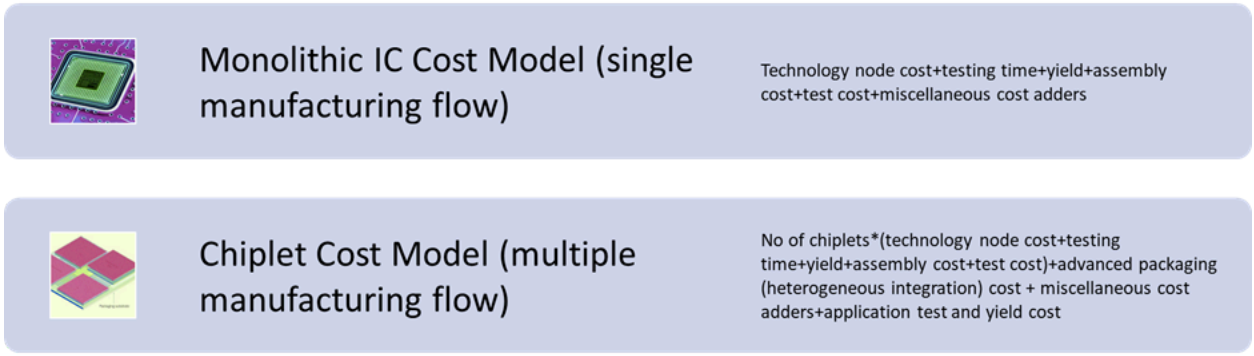


Figure 13. Monolithic IC versus Chiplet Test Cost Comparison

Routing Optimization for Test Cost Reduction

Another technique to reduce chiplet test costs is optimizing the routability between scan chains and test access ports. This deals with the routing congestion challenges encountered while integrating test wrapper logic and scan chains spread across the chiplet areas.

Congestion impacts the achievable scan chain frequencies which determines the test times directly based on the equation mentioned. Optimized routing eases the congestion allowing higher scan frequencies shortening test times substantially.

DFT Reuse Across System Levels

A key advantage for chiplets is the scope for reusing DFT infrastructure across system hierarchy levels from chiplet to module. This helps address the additional test complexities in a modular system in an efficient manner.

For example, a chiplet designed with IEEE 1500 core wrappers allows the same wrapper to be reused at module test without redesign. Boundary scan structures following IEEE 1149.1 are similarly reused at sub-system level assembly tests.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Likewise, wafer probing DFT like at-speed scan chains remain valid at module test with minor adaptations if any. Such reuse alleviates redundant DFT design effort and validation. It also enables a “plug-and-play” flavour where validated chiplet cores can be assembled with little system-level integration effort.

This design-for-reuse paradigm helps amortize the initial DFT investment over many derivative products. It optimizes the lifecycle costs while simplifying complex system test challenges associated with chiplets. The approach helps counter the higher test complexities to an extent and keeps overall test costs comparable or better than monolithic designs.

11. Chiplet Versus Monolithic Comparison

While chiplet-based designs introduce additional test complexities at module level due to multiple inter-connected dies, techniques exist to optimize this overhead. The most impactful factor is the significant yield improvements translating to higher KGC volumes justifying the test investments. The testing, yield, cost and scalability comparison of Chiplet versus monolithic is shown in Table 2.

Table 2. Comparison between Chiplet/Multi-Die Systems and Monolithic Systems

Parameter	Chiplet/Multi-Die Systems	Monolithic Systems
Die/Chip Size	Smaller individual die/chip sizes	Larger monolithic die size
Yield	Higher yields (e.g. 85% for each smaller chiplet)	Lower yields especially at advanced nodes (e.g. 70%)
Number of Known Good Chiplet/Chips	Higher number of KGC due to overall higher yield from smaller sizes	Lower number of KGC due to lower monolithic die yield

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Wafer Testing Cost	Slightly higher per-chiplet test costs but overall lower costs due to higher KGC	Lower per-die costs but higher overall costs due to lower KGC
Module/Package Testing	Multiple test sessions needed to test individual chiplets and interconnections	Single test session to test the packaged monolithic die

Parameter	Chiplet/Multi-Die Systems	Monolithic Systems
Test Time	Longer due to multiple test sessions but can be optimized using techniques like parallel testing	Shorter with single test session
DFT Reusability	DFT structures like wrappers and boundary scan can be reused across system levels	Fresh DFT effort needed at each new product/process node
Scalability	Easier to scale to advanced nodes due to modularity and yield improvements	Scaling challenges especially at advanced nodes due to low yields
Time to Market	Faster with ability to leverage existing validated IP and reuse across products	Slower due to development from scratch for each product

12. Standard Testing and Integration

The OCP whitepaper "Proposed Standardization of Chiplet Models for Heterogeneous Integration" recommends standardizing on chiplet design kits (CDKs) to facilitate chiplet design and integration. It proposes using the Chiplet Data eXchange Markup Language (CDXML) for defining and exchanging chiplet metadata.

For testing aspects, the following existing IEEE standards are recommended:

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **IEEE 1149.1 (JTAG):** IEEE 1149.1, commonly known as JTAG, provides a standard interface for testing and debugging integrated circuits. It allows for boundary-scan testing which served as foundation for IEEE 1838 chiplet testing.

- **IEEE 1687:** IEEE 1687 defines a standard for accessing and controlling instrumentation embedded within a semiconductor device. It enables the integration of on-chip instruments that can be accessed via the IEEE 1149.1 Test Access Port (TAP), facilitating comprehensive testing of chiplets through IEEE 1838.

- **IEEE 1500:** IEEE 1500 is a standard developed by the Institute of Electrical and Electronics Engineers (IEEE) that focuses on enhancing the testability of System-on-Chip (SoC) designs. The full name of the standard is "IEEE Standard Test Interface for Embedded Cores," and it is commonly referred to as the "Standard Test Interface Language (STIL)."

- **IEEE 1838:** IEEE 1838 standardizes the test access architecture for 3D ICs, which are relevant for heterogeneous chiplet systems. It provides guidelines for testing chiplets within a stacked configuration, ensuring efficient access to test points and instruments. For the details of the implementation of IEEE 1838, may refer to OCP whitepaper: Guide to Integration Workflows for Heterogeneous Chiplet Systems [2]. This standard will be further enhanced to include 3D chiplet debug and bring up.

- **IEEE 3405:** IEEE 3405 specifies a standard for chiplet interconnect test and repair, focusing on ensuring the reliability and integrity of chiplet interconnections. It provides

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

methodologies for testing the electrical characteristics of interconnects and implementing repair mechanisms if faults are detected. It is a draft in progress standard.

The summary of IEEE 1149.1, IEEE 1687, IEEE 1500, and IEEE 1838 is shown in Figure 14. IEEE 1500 and IEEE 1687 focus on enhancing testability within SoCs and managing embedded instruments, respectively. IEEE 1149 deals with boundary-scan testing, while IEEE 1838 addresses test access for 3D ICs. The comparison of the DFT wrapper of IEEE 1149.1, IEEE 1500 and IEEE 1838 is shown in Figure 15.

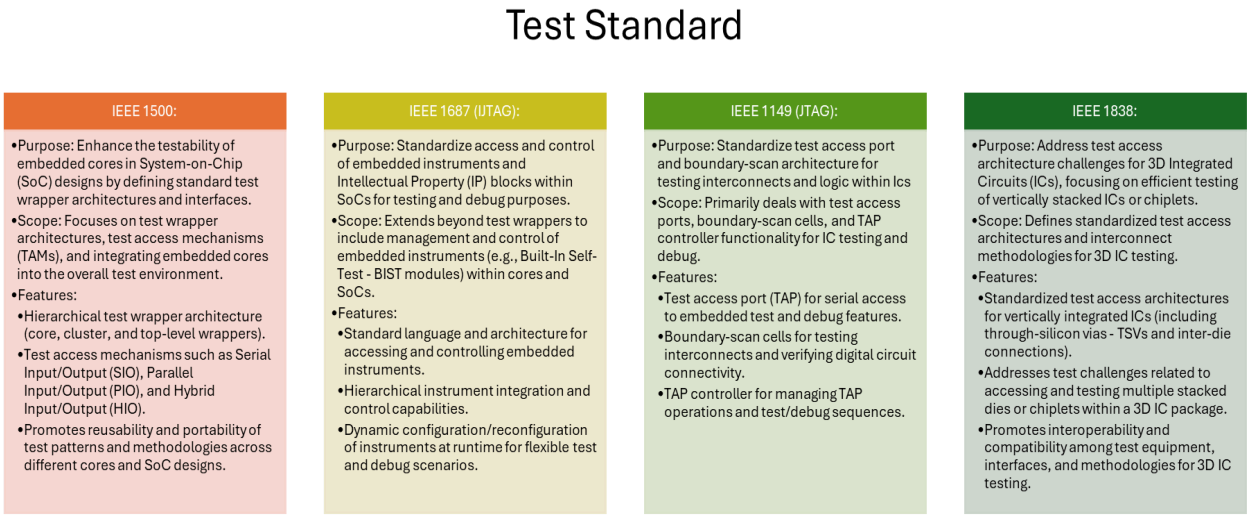


Figure 14: Summary of IEEE 1149.1, IEEE 1687, IEEE 1500 and IEEE 1838.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

	IEEE Standard 1149.1	IEEE Standard 1500	IEEE Standard 1838
Modules	Packaged chips	Embedded cores	Stacked dies and chiplets
System	Printed circuit board	SOC	3D IC, multidie packages
Focus InTest	Not applicable	Core internal circuitry	Die internal circuitry
Focus ExTest	Board-level interconnect	Top-level circuitry	Die interconnects plus "shore" logic
I/O type	Package pins (expensive)	Core terminals (cheap)	Microbumps (moderate)
Data serial	1 bit: TDI-TDO	1 bit: WSI-WSO	1 bit: TDI-TDO requires loopback
Data parallel	Not applicable	n-bit: WPI-WPO[n]"	n-bit: FPP[n]* at every stack tier
Test control	TCK, TMS, (TRSTn') plus 16-state finite-state machine	WRCK, WRSTn, SelectWIR, ShiftWR, CaptureWR, UpdateWR	TCK, TMS, TRSTn plus 16-state finite-state machine

*Optional

Figure 15. DFT Wrapper Standard Comparison

By leveraging established IEEE standards, the chiplet testing standard can address various aspects of testing in heterogeneous chiplet systems. This includes boundary-scan testing, access to embedded instrumentation, 3D IC testing, integration workflows, and interconnect testing and repair. The goal is to ensure comprehensive testing coverage and facilitate the development of reliable and interoperable chiplet-based systems.

Standard Workflow

The OCP Whitepaper “Guide to Integration Workflows for Heterogeneous Chiplet Systems” details the overall testing workflows and considerations for chiplet-based multi-die System-in-Package (SiP) designs.

The key aspects covered are:

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- **Wafer Probe Testing:** Known Good Chiplet (KGC) testing is recommended to test chiplets at wafer-level before assembling in the SiP package. However, challenges exist due to finer bump pitches and reduced power integrity during wafer probing.

- **Package Testing:** Package-level tests validate inter-chiplet connectivity and functionality of the assembled SiP. Inter-chiplet IO's need to support boundary-scan based tests. Unified BSDL is recommended to provide a single BSDL description for the whole SiP.

- **IP Testing**: Individual chiplet functionality is tested as developed using techniques like Built-In-Self-Test (BIST), scan-based testing etc. Test programs need to support both standalone and SiP-level usage.

- **Other Tests:** Additional test techniques for debugging like IDDQ testing, cell-aware ATPG are also relevant for sign-off. Thermal, signal and power integrity related tests need to validate interactions across the SiP.

Standard Format

CDXML is the XML schema defined by the OCP to standardize chiplet metadata exchange. JEDEC subsequently developed a joint effort called JEP30 to standardize on CDXML and foster its adoption.

The key aspects standardized in CDXML include:

- Logical and physical views of the chiplet including block diagrams, I/O ports, power domains.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

- Configuration and customization options supported by the chiplet.

- Performance characteristics and requirements.

- Test requirements and limitations.

- Environmental requirements and ratings.

- Regulatory and certification standards compliance.

- Foundry and assembly information.

Having a common metadata exchange format using CDXML helps in easier integration of chiplets from different providers into a System-in-Package. It provides all necessary technical information upfront to design teams for system planning, validation, and manufacturing. Following the JEP30 standard promotes wider adoption of CDXML and advanced chiplet-based design.

13. Conclusion

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Chiplet-based products partition the IC into discrete chiplets and then assembles them within a package and connect them with a standardized interface to create a System-in-Package (SiP). This helps designers to meet performance, efficiency, power, size, and cost challenges but, with multi-die packages, one bad die can result in the failure of the whole package and thus high coverage across the SiP is required which requires DFT interoperability across chiplets from different vendors, good inter-chip communication testing and complex final functional test scenarios.

The paper has considered the current status of SiP test best-practice strategies including DFT, Known-Good-Chiplet (KGC) testing and assembly, yield recovery and test-time reduction, and has discussed how these might impact the tests at wafer sort, assembly and packaging and board-level through test economics modeling which includes the potential impact of test for higher yields, how routing optimization and DFT reuse across system levels can reduce overall test cost. The paper set this all within the context of the current industry test standards regarding workflow and test formats and concluded with a set of recommendations and suggested next steps.

14. References

1. Tan, Terrence Huat Hin, “Debug and Fault Isolation Strategies as the Industry moves towards 3D-ICs”, MEPTEC, 2021. https://events.meptec.org/wpcontent/uploads/ChipletsDataTest/DataTest2021Tan.pdf
2. Boon Chong Ang, John Caka, Kevin Cameron, Lihong Cao, KK Lin, Subramanian Lalgudi, Chieh Lo, Mark Malinoski, Tony Mastroianni, Jawad Nasrullah, Rajesh Pendurkar, David Ratchkov, Joe Reynick, Satish K Surana, James Wong, “Guide to Integration Workflows for Heterogeneous Chiplet Systems”, ODSA White paper, 2024. https://www.opencompute.org/documents/chiplet-integration-workflows-1-pdf

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

3. Proposed Standardization of Chiplet Models for Heterogeneous Integration, https://www.opencompute.org/documents/ocp-odsa-cdx-proposed-standardization-of-chiplet-models-for-heterogeneous-integration-2-pdf
4. OCP CDXML, https://github.com/opencomputeproject/ODSA-CDXML
5. JEDEC JEP30, https://www.jedec.org/category/technology-focus-area/jep30
6. Business Analysis of Chiplet-Based Systems and Technology, https://www.opencompute.org/documents/odsa-whitepaper-2024-business-analysis-of-chiplet-based-systems-and-technology-pdf
7. Adam Cron, Erik Jan Marinissen, “IEEE Standard 1838 is on the move”, IEEE Computer Society, 2021. https://www.computer.org/csdl/magazine/co/2021/11/09585177/1xZlCLoy7OU
8. Bruce Swanson, “Design for Test: What is a Streaming Scan Network(SSN)?, Simens Bog, 2022. https://blogs.sw.siemens.com/xcelerator-academy/2022/03/21/design-for-test-what-is-a-streaming-scan-network-ssn/
9. Wu Yang, “3DIC Test Challenges, Trends and Solutions-An EDA Perspective”, MEPTEC, 2021. https://events.meptec.org/wp-content/uploads/ChipletsDataTest/DataTest2021Yang.pdf
10. Fisher Zhang, “Test Strategies in the Era of Heterogenous Integration”, Teradyne, 2023. https://www.teradyne.com/2023/09/05/test-strategies-in-the-era-of-heterogeneous-integration/
11. Chetan Arvind Patil, “A cost analysis of the chiplet as a SOC solution”, Commercial Micro Manufacturing, 2023. https://www.cmmmagazine.com/cmm-articles/a-cost-analysis-of-the-chiplet-as-a-soc-solution/
12. Roberto Rotili, “Known-Good-Chiplet is at the Heart of a Sustainable Open Chiplet Business Model”, OCP Global Summit 2021.
13. ChiXiao Chen, JieMing Yin, Yarui Peng,Maurizio Palesi, WenXu Cao,LeTian Huang, Amit Singh, HaoCong Zhi, XiaoHang Wang, “Design Challenges of Intra-and Inter-Chiplet Interconnection”, IEEE Design and Test, 2022

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

14. Dr. Burhan Bayraktaroglu, “Heterogenous Integration Technology”,2017 https://apps.dtic.mil/sti/tr/pdf/AD1035357.pdf

15. Vern Solberg , “2.5D and 3D Semiconductor Package Technology: Evolution and Innovation”,2016 https://www.circuitinsight.com/pdf/2.5d_3d_semiconductor_package_technology_ipc.pdf

16. Yogan Senthilkumar, “Test Challenges in KGD/Chiplets based Heterogeneous Integration”, ITC, 2023

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

17. License

OCP encourages participants to share their proposals, specifications and designs with the community. This is to promote openness and encourage continuous and open feedback. It is important to remember that by providing feedback for any such documents, whether in written or verbal form, that the contributor or the contributor's organization grants OCP and its members irrevocable right to use this feedback for any purpose without any further obligation.

It is acknowledged that any such documentation and any ancillary materials that are provided to OCP in connection with this document, including without limitation any white papers, articles, photographs, studies, diagrams, contact information (together, “Materials”) are made available under the Creative Commons Attribution-ShareAlike 4.0

International License found here: https://creativecommons.org/licenses/by-sa/4.0/, or any later version, and without limiting the foregoing, OCP may make the Materials available under such terms.

As a contributor to this document, all members represent that they have the authority to grant the rights and licenses herein. They further represent and warrant that the Materials do not and will not violate the copyrights or misappropriate the trade secret rights of any third party, including without limitation rights in intellectual property. The contributor(s) also represent that, to the extent the Materials include materials protected by copyright or trade secret rights that are owned or created by any third-party, they have obtained permission for its use consistent with the foregoing. They will provide OCP evidence of such permission upon OCP’s request. This document and any "Materials" are published on the respective project's wiki page and are open to the public in accordance with OCP's Bylaws and IP Policy. This can be found at http://www.opencompute.org/participate/legal-documents/. If you have any questions please contact OCP.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

18. About Open Compute Foundation

The Open Compute Project (OCP) is a collaborative Community of hyperscale data center operators, telecom, colocation providers and enterprise IT users, working with the product and solution vendor ecosystem to develop open innovations deployable from the cloud to the edge. The OCP Foundation is responsible for fostering and serving the OCP Community to meet the market and shape the future, taking hyperscale-led innovations to everyone. Meeting the market is accomplished through addressing challenging market obstacles with open specifications, designs and emerging market programs that showcase OCP-recognized IT equipment and data center facility best practices. Shaping the future includes investing in strategic initiatives and programs that prepare the IT ecosystem for major technology changes, such as AI & ML, optics, advanced cooling techniques, composable memory and silicon. OCP Community-developed open innovations strive to benefit all, optimized through the lens of impact, efficiency, scale and sustainability. Learn more at www.opencompute.org.

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.

Appendix A. [Title]

This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International License.