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Crater Lake 1S Server Design Specification 1v1

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3 Compliance with OCP Tenets

3.1 Openness

The Yosemite 3.5 and Crater Lake server specification describes a design which can be used to support many configuration types. It can be leveraged by other OCP partners as a standalone server, or it can drive other use cases with support for expansion options, oBMC, ORv2/ORv3.

3.2 Efficiency

Yosemite 3.5 continues to utilize shared resources such as fans, MHNIC along with support for ORv3 racks, improved thermal efficiency and 4th Gen Intel® Xeon® processors.

3.3 Impact

The Yosemite 3.5 and Crater Lake server have been designed to improve over Yv3.0 and Delta Lake in terms of compute/power density, power/thermal efficiency and IO bandwidth resulting in an overall performance/Watt gains.

3.4 Scale

The Yosemite 3.5 and Crater Lake server are designed for large scale data center deployment and operations. The system is designed with debug hooks, ease of serviceability, and reliability as a focus. YV3.5 sled design continues to be front serviceable, hot-pluggable and support service touch point indicators. The Design continues to support openBMC architecture and the OCP debug options such as OCP debug card and At Scale Debug.

3.5 Sustainability

The Yosemite 3.5 and Crater Lake server have been designed for sustainability. The spec submission will maximize transparency of environmental impacts of the contribution, with the aspiration of improvement over time.

3.6 Inclusive Terminology

This specification was written with inclusive terminology to reduce biased terms. The deprecated and new preferred terminology can be found at <https://www.opencompute.org/documents/ocp-terminology-guidelines-for-inclusion-and-openness>.

4 Version Table

Date	Version #	Author	Description
2020/8/30	0v1	Matt Bowman	Initial draft based on Delta Lake specification
2020/12/11	0v2	Matt Bowman	Significant updates in all sections based on initial feedback
2021/1/8	0v3	Matt Bowman	<p>New server block diagram 5-1 showing updated PCIe port numbering</p> <p>Preliminary power budget in section 11.2</p> <p>Fixed diagram numbering in chapter 10 to avoid repeat labels</p> <p>Removed incorrect references to LPC bus in section 12.8</p> <p>Updated description of PCIe hotplug use cases in section 13.13</p> <p>New At Scale debug diagram in section 10.3.5</p> <p>Fixed typo in USB topology diagram 9-3</p> <p>Updated SPI diagram to align with no PFR</p> <p>Misc spelling/grammar fixes</p>

Date	Version #	Author	Description
2021/1/27	0v4	Matt Bowman	Added pinout details for the expansion and baseboard connectors Added GPIO details for BIC and PCH Updated PCIe connectivity block diagrams and descriptions to reflect width and speed changes Fixed LED behavior and descriptions Removed incorrect references to SAS/SATA Fixed Class 2 USB connectivity diagram to correctly show USB switch instead of USB hub
2023/01/11	0v5	Yeshaswy Rajupalepu	Updated pinouts section 10.2.2 -10.2.3
2023/10/2	1v0	Abe Garcia	Fixed formatting Updated throttle section Updated PCIe bifur. table
2023/11/14	1v1	Abe Garcia	Formatting

5 Scope

This document describes a single socket server design based on the Intel® Xeon® Processor, Sapphire Rapids, which is referred to hereinafter as Crater Lake 1S server.

6 Overview

All processor names mentioned in this doc refer to codename SPR (Sapphire Rapids of the Eagle Stream platform). The Crater Lake platform is designed to be used with SPR MCC SKUs, supporting a TDC of 125W Max. A blade with processor installed can be seen in Figure 6-1.



Figure 6-1: Single Crater Lake blade

The Crater Lake 1S server is designed to use Intel® Xeon® Sapphire Rapids Processor utilizing the performance and advanced intelligence of Intel® Xeon® processors. It works together with Intel's Emmitsburg series Platform Controller Hub.

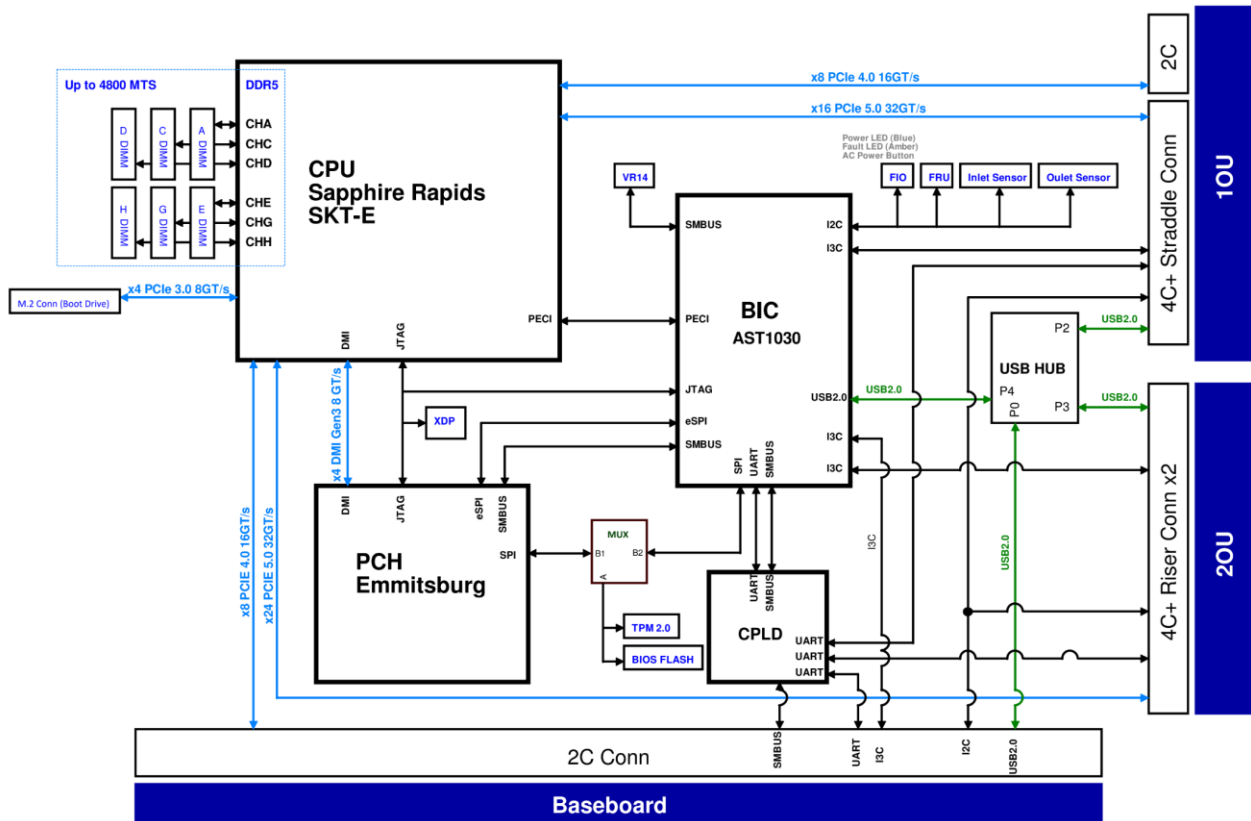


Figure 6-2: Crater Lake 1S Server Block Diagram

Here onwards we will refer to the cold air aisle as the front, and the hot air aisle as the rear, of the board. High speed and low speed signals connect to the Crater Lake 1S server through a 2C connector at the rear of the board. A cable connects the 2C connector to the Integrated Baseboard of the YV3.5 system. Signals on these connectors include:

- x8 Gen4 PCIe for the Network Interface Controller (NIC)
- A Universal Asynchronous Receiver/Transmitter (UART)
- 1x IPMB over I3C for communication between BMC (outside of Crater Lake) to BIC (Bridge IC on Crater Lake)
- A high-speed USB interface between BMC (On Baseboard) to BIC (on Crater Lake). Crater lake has a hub to enable the BMC USB to communicate with BIC on expansion boards.
- Status and control signals for power button, power enable, and power good.

Vertical PDB power connector:

- 12V is used to derive all power and is sourced from a separate power connector mating with the Vertical PDB

Crater Lake's base configuration allows one locally installed M.2 drive intended for use as the boot drive. The M.2 has a x4 PCIe Gen 4 connection to the CPU. The targeted capacity of the M.2 boot drive is 256/512GB. M.2 Connector selection and nearby component placement support double sided M.2s in the 2280 form factor.

The Crater Lake 1S server connects to a NIC on the YV3.5 platform Baseboard through the 2C connector using a x4 Gen4 capable PCIe bus. The remaining PCIe lanes are used for high bandwidth connections to 1U and 2U expansion boards (eight lanes of the SPR CPU are currently not planned). All PCIe connectivity on Crater Lake has the Sapphire Rapids CPU as the root complex. The Emmitsburg PCH communicated over a x4 DMI link to the SPR CPU. No PCIe endpoints are connected downstream to the PCH. A high level diagram of the server can be seen in Figure 6-2.

Each PCIe port of the SPR CPU supports one instance of a Compute Express Link (CXL). One x16 CXL link is routed to the 1U expansion, and one x16 CXL link goes to the 2U expansion. Section 10.2 of this document describes the options and use cases of the 1U and 2U expansions.

The PCIe lane bifurcation on the Sapphire Rapids CPU is described in Table 6-1.

Table 6-1: SPR CPU PCIe Bifurcation

Port	Bifurcation	PCIe Gen/Speed	Usage
Port 0 0:7	x8	Gen 4	Front Expansion 1U 2C
Port 0 8:15	x8	Gen 4 (Gen 5 capable)	2U Expansion x8
Port 1	x16	Gen 5 (CXL Capable)	2U Expansion x16
Port 2	x16	Gen 5 (CXL Capable)	Front Expansion 1U 4C+
Port 3	x16	N/A	Not enabled in SPR SKU
Port 4 0:4	x8	Gen 4	M.2 SSD Boot drive
Port 4 5:7	x4	N/A	Unused
Port 4 8:15	x8	Gen 3 (Gen 5 capable)	Multi-host NIC on Baseboard 2C

The Crater Lake 1S server has a dedicated hot swap controller (HSC) to enable the insertion/removal of the server blade into/from a live power bus while also providing important telemetry such as voltage, current, and power (VIP). Telemetry is used by the platform for power management purposes such as imposing power limits and triggering of throttle events to force the CPU to the lowest power state. The Crater Lake 1S server supports an Advanced Configuration Power Interface (ACPI)-compliant power button and reset signals from the platform.

A Bridge IC (BIC) is used as the management controller on the 1S server board, and it acts like the bridge between the BMC on base board to devices on Crater Lake 1S CPU motherboard. Examples for end points of the BIC include devices like the CPU and the PCH. The Bridge IC manages the 1S server, on behalf of the BMC on the platform, and bridges the BMC to the Intel® PCH internal management controller; Intel® Manageability Engine. To maximize the communication bandwidth between the BMC and the Bridge IC, a dedicated point-to-point I³C bus will be used. DMTF MCTP protocol is run on this I³C bus to allow both devices on the bus to initiate communication.

Crater Lake 1S motherboard Field Replaceable Unit (FRU) EEPROM and thermal sensors are connected to the Bridge IC's I²C buses. There are multiple General-Purpose Input/Output connections (GPIOs) between the Bridge IC and Intel® Xeon® SPR Processor for error reporting and management purposes. Details of implementation can be referred to in the Crater Lake schematics. Intel® PCH's Intel® Manageability Engine is connected to the Bridge IC via an I²C interface so that the Bridge IC can poll information from the Intel® Manageability Engine. An eSPI interface between the Bridge IC and the Intel® PCH is connected to enable in-band communications. The BMC can access the Crater Lake 1S server's thermal sensors, FRU, Intel® PCH's GPIOs and Intel® Manageability Engine via the Bridge IC with standard IPMI commands.

The BIOS and BIC firmware can be updated from in-band connectivity by the PCH or out-of-band programming through BMC. Other firmware (CPLD and VR chips) is programmable from out-of-band connectivity to the Bridge IC and BMC. All configurations of Crater Lake will use measured boot to ensure the integrity of the BIOS. Crater Lake has all hardware hooks to enable the P²OT. This is explained in more detail in Section 14.

6.1 Use Cases

This section describes major use cases of Crater Lake 1S Server motherboard in the context of Yosemite V3.5 platform. This context is to provide details for proper implementation of Crater Lake 1S server card.

- A class 1 YV3.5 configuration has the BMC on the baseboard of a sled, and all the blades in the sled share a multi-host NIC installed on the baseboard.
- A class 2 YV3.5 configuration has a dedicated BMC and single host NIC on each blade. No multi-host NIC is installed on the baseboard

Refer to the Yosemite V3.5 platform detail in Yosemite V3.5 platform Specification. The 1U and 2U Expansion Card details are covered in the expansion cards specifications. System level view and naming of major chassis components can be seen in Figure 6-3.

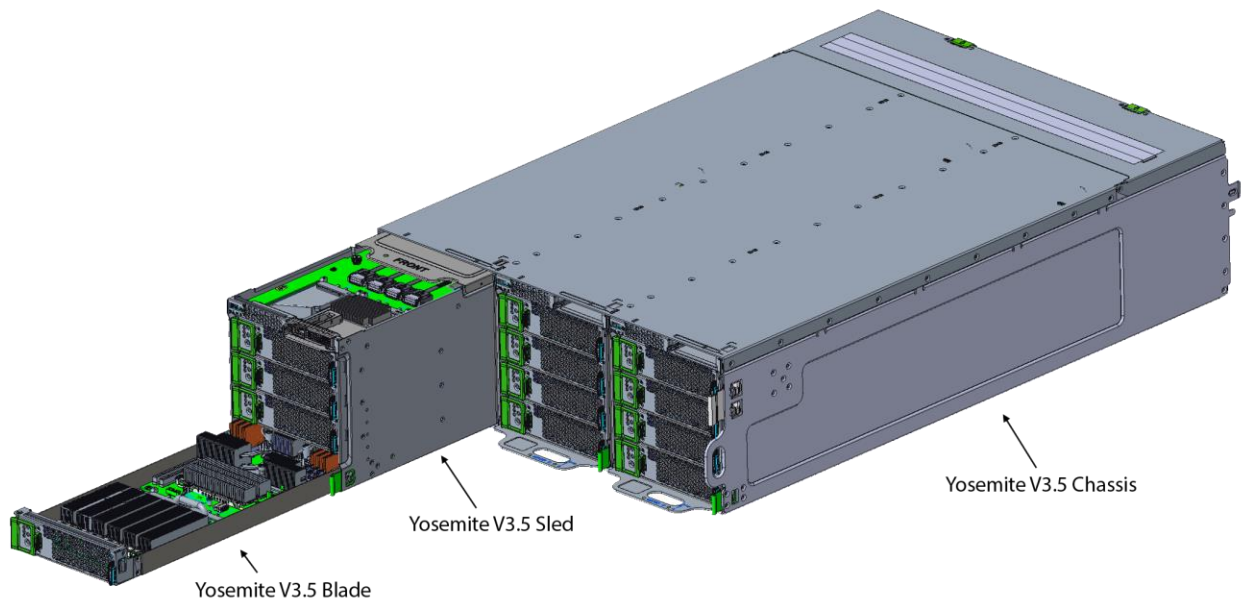


Figure 6-3 - YV3.5 System Components

6.1.1 1U/2U Multi-Host Use Cases (Class 1 Use Case)

In this class of use cases, multiple Crater Lake 1S server cards share common baseboard BMC and a multi-host NIC through baseboard. The Crater Lake 1S server can be in 1U or 2U for different use cases. The front expansion is optional in 1U use case.

Crater Lake 1S Server Design Specification

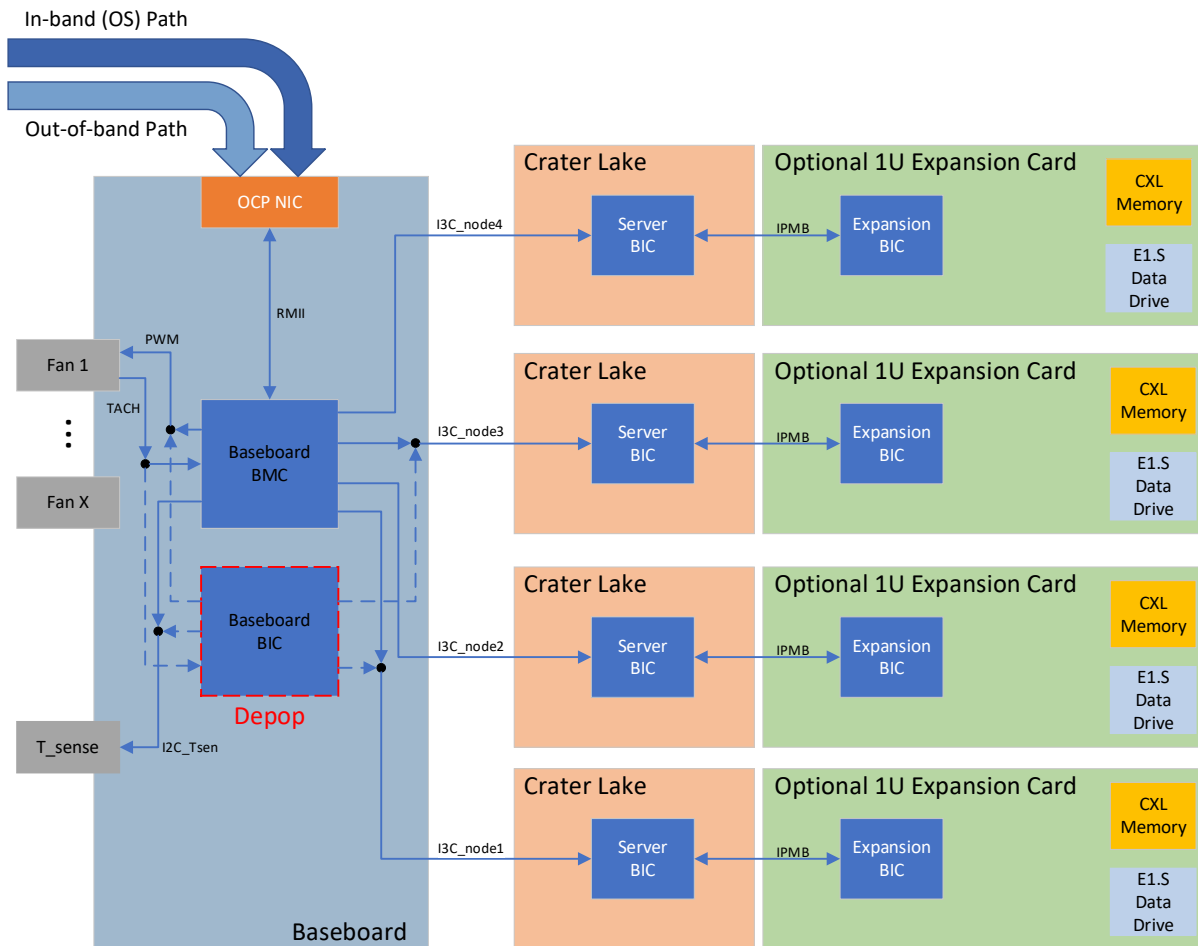


Figure 6-4: Yosemite V3.5 class 1 sled with 4 blades: Crater Lake and 1U Expansion module

Planned and potential 1U blade usages include:

- Standard compute blade with no expansion; Four compute blades per sled that make use of the multi-host NIC on the baseboard
- Extended memory compute blades with CXL based memory expansion to enable workloads with higher memory capacity requirements
- Compute blades with E1.S storage expansions for direct attached high performance storage applications

A diagram of this can be seen in Figure 6-4.

6.1.2 2U Single Host 1S Server Card (Class 2 Use Case)

In Class 2 YV3.5 configurations, each Crater Lake has its own BMC and single host NIC connection (100G is shown as an example). BMC for each Crater Lake is on a Network Expansion Card connected to Crater Lake.

The two Crater Lake server cards share the baseboard which is configured with a BIC (instead of a BMC) for chassis management purposes. No multi-host NIC is needed for management.

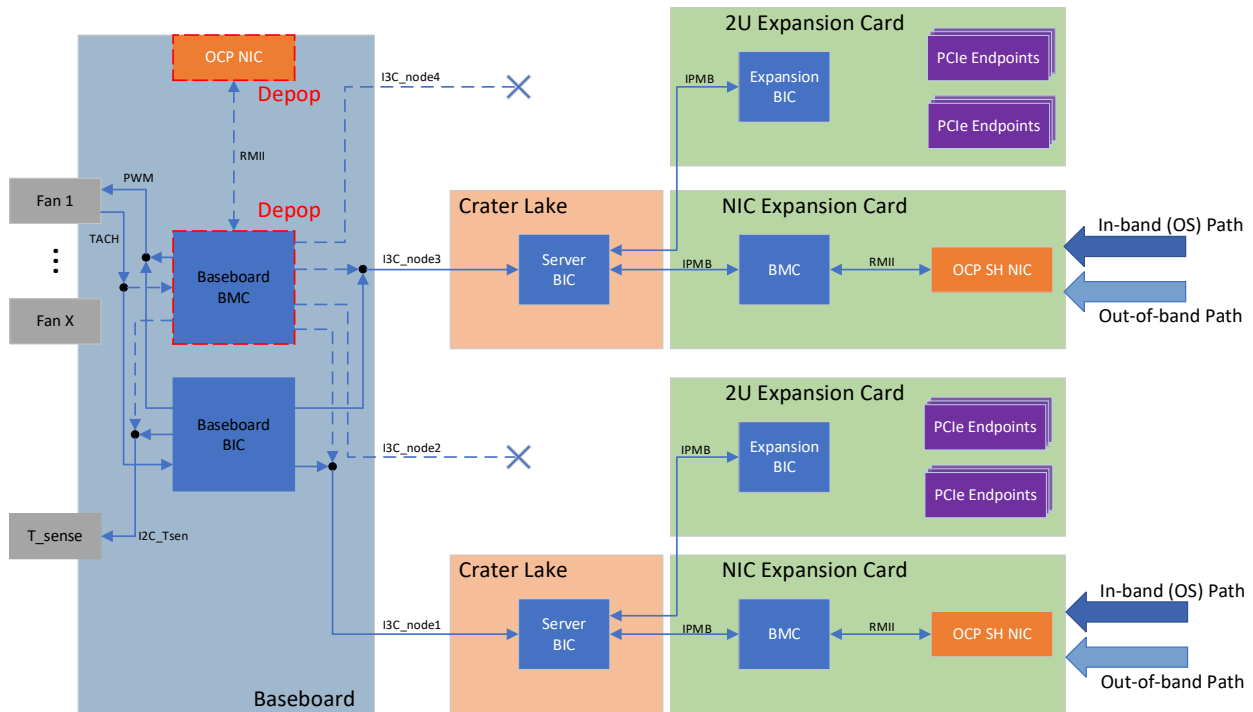


Figure 6-5: Yosemite V3.5 class 2 sled with 2 blades: Crater Lake, 2U Expansion module and single host NIC

Planned and potential 2U blade usages include:

- High-capacity disaggregated storage expansion with E1.S in the 2U expansion and a dedicated NIC in each blade
- Flexible functionality for testing, validation, or head node usage with Discovery Point v2 (CEM adapter) in the 2U expansion
- Hosting accelerator cards in M.2 or future form factors on the 2U expansion

A diagram of this can be seen in Figure 6-5.

7 Rack Compatibility

The Crater Lake 1S server board is designed to work with the YV3.5 chassis and support both ORv2 and ORv3 open rack standards. Rack density is subject to change based on IO population and workloads and they must be evaluated by adopters on a case-by-case basis.

8 Physical Specifications

8.1 CPU

Crater Lake 1S server will be built with an Intel® Xeon® Sapphire Rapids (SPR) Processor. The SPR processor is a multicore LGA part that includes memory controllers and high-speed IO interfaces. The CPU is socketed and is a Field Replaceable Unit (FRU) along with its heatsink. The SPR CPU is available in various power profiles. Crater Lake will support MCC SKUs rated for a power up to 165W, TDC.

8.2 PCH

The Emmitsburg series Platform Controller Hub (PCH) on Crater Lake works in tandem with the CPU. It provides additional IO support for the CPU that includes:

- ACPI power management Logic Support
- Integrated Serial ATA host controller
- xHCI USB controller with SuperSpeed USB 3.0 ports
- Direct Media Interface
- PCIe for peripheral and storage devices
- SPI and eSPI interface
- Flexible I/O
- GPIO
- SMBus

The Crater Lake design does not use any of the PCIe connectivity from the PCH. Crater Lake is designed to support only Emmitsburg, rated at 3W TDC.

8.3 Memory

The SPR CPU on Crater Lake 1S server has four memory controllers offering eight channels of DDR5 memory. Six channels are implemented in the Crater Lake server design. All channels will support one DIMM per socket. The memory is expected to run at 3600MT/s minimum with design target capable of a maximum speed of 4400MT/s. The memory matrix can be seen in Table 8-1.

Table 8-1: Memory Matrix

Config	Channels Used	DIMMs	Rank	DRAM
96GB	A2, A3, A6, A7	24GB	single	24Gb
128GB	A2, A3, A6, A7	32GB	dual	8Gb

8.4 Debug Headers

The Crater Lake server shall support traditional ITP/XDP debug headers.

8.5 Boot Drive

Crater Lake 1S server has one M.2 boot drive in 2280 or 22110 form factors. This drive is connected to the SPR CPU with a x4 PCIe Gen4 link. There is sufficient space around the M.2 drive to support double sided devices. The target capacity of the M.2 is 256GB/512GB.

8.6 Expansion Systems

The Crater Lake 1S server offers expansion capabilities through PCIe lanes that are routed to a riser card and front-end straddle mount connectors. The connectivity of these expansion connectors is described below. A detailed listing of the expansion capabilities can be found in the “Crater Lake 1S Expansion System” document. Expansion boards that utilize the riser or front-end straddle mount connectors are not expected to be hot swappable (e.g. there is no hot swap controller for these connectors on Crater Lake).

Riser card: (pin definition is similar to OCP NIC 3.0, but not all pins are adopted. Refer to pinout section, 10.2, in this document for details.)

- 24 lanes of PCIe split between 1x x16 and 1x x8 connectors, 2x PCIe ref clocks
- Reset (from Crater Lake CPLD)
- I2C (from BIC), Interrupts
- I3C (from BIC)
- USB (from BMC through USB hub),
- UART (from Crater Lake CPLD)
- PWRBRK
- 12V and 3.3V_STBY
- RISER CARD TYPE DETECTION (3x)

- Power Enable/Power Good

Front-end straddle mount: (to be pin-out like LFF OCP NIC 3.0 with all pins adopted)

- 24 lanes PCIe split between 1x x16 4C+ and 1x x8 2C connectors, 3x PCIe ref clocks
- Reset (from Crater Lake CPLD)
- I2C (from BIC), Interrupts
- I3C (from BIC)
- USB (from BMC through USB hub)
- UART (from Crater Lake CPLD)
- Wake, PWRBRK
- 12V and 3.3V_STBY
- Expansion PRSNT
- Expansion SLOT ID

8.7 FRU EEPROM

The Crater Lake 1S server includes a 128Kbits I²C-accessible Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM is accessible from the platform via the Bridge IC. The EEPROM contains the Field Replaceable Unit Identification (FRU ID) information and any additional configuration information, if required. The FRU ID is formatted in accordance with the IPMI Platform Management FRU Information Storage Definition document.

The EEPROM must contain the following entries:

- Board Manufacturer
- Board Name
- Board Serial Number
- Board Part Number
- Product Manufacturer
- Product Name
- Product Part Number
- Product Serial Number
- Product Asset Tag
- Product Build: e.g. EVT, DVT, PVT, MP
- Product Version: e.g. C1
- Manufacturing Date and Time
- Manufacturing Lot Code: (preferred, but optional)
- Manufacturing Work Order: (preferred, but optional)
- PCB Revision
- SoC Model Name/Number
- SoC Revision
- SoC T_{JMAX} (Maximum Junction Temperature)

9 Thermal Design Requirements

To meet thermal reliability requirements, the thermal solution should be able to adequately dissipate heat from the components when the system is operating at its maximum TDP (Thermal Design Power). The thermal solution should be found by setting a high-power target for initial design to avoid redesign of cooling solution; however, the final thermal solution should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. Thermal solution should not allow any overheating issue for any components in system. CPU or memory should not throttle due to any thermal issue under following environment.

- Inlet temperature lower than or equal to 35°C, and 0-inch H₂O datacenter pressure with all FANs in each thermal zone running properly
- Inlet temperature lower than or equal to 35°C, and 0.001-inch H₂O datacenter pressure with one FAN (or one rotor) in each thermal zone failed

9.1 Data Center Environmental Conditions

This section outlines Facebook data center operational conditions.

9.1.1 Location of Data Center/Altitude

Maximum altitude is 6,000 ft above sea level. Any variation of air properties or environmental difference due to the high altitude needs to be deliberated into the thermal design.

9.1.2 Cold-Aisle Temperature

Data centers typically maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with 3°C standard deviation. The cold aisle temperature in a data center may fluctuate minutely depending on the outside air temperature. Every component must be cooled and must maintain a temperature below its maximum specification temperature in the cold aisle.

9.1.3 Cold Aisle Pressurization

Data centers typically maintain cold aisle pressure between 0 inches H₂O and 0.005 inches H₂O. The thermal solution of the system should consider the worst operational pressurization possible, which generally is 0 inches H₂O and 0.001 inches H₂O with a single fan (or rotor) failure.

9.1.4 Relative Humidity

Data centers usually maintain a relative humidity between 10% and 90%. The thermal solution must sustain uninterrupted operation of the system across the aforementioned RH range.

9.2 Server Operational Conditions

9.2.1 System Volumetric Flow

The unit of airflow (or volumetric flow) used for this spec is cubic feet per minute (CFM). The CFM can be used to determine the thermal expenditure or to calculate the approximate Crater T of the system. The thermal expenditure is quantified by the metric CFM/W, which is calculated by the following formula:

$$\text{Thermal Expenditure} = \frac{\text{System Airflow}}{\text{Total System Power Consumption (including fans)}} \left[\frac{\text{CFM}}{\text{[W]}} \right]$$

The required airflow is 0.115 airflow per watt in the system level at sea level. The desired airflow per watt is 0.1 or lower in the system up to 35°C (95°F) ambient temperature at sea level for both 1U and 2U blade form factors. The cooling solution shall take the pre-heating effect from the expansion card into consideration if there is any.

9.2.2 Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The server blade design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 5% thermal margin for every component on the card.

9.2.3 Upper Critical Threshold

The upper critical threshold (UCR) setting should allow the detection of abnormal thermal behaviors in the system. The UCR values for the sensors that are not used in Fan Speed Control (FSC) should use a 15% thermal margin from the worst experiment data. The UCR values for the sensors used in FSC, except for CPU, inlet, and outlet sensors, should use a 20% thermal margin from the worst experiment data.

9.2.4 Thermal Testing

Thermal testing must be performed at a low inlet temperature of 15°C (59°F) and up to 35°C (95°F) inlet temperature to guarantee the design is free of thermal defect and is robust at high temperature operation. Rack-level airflow testing is recommended to evaluate rack level containment and ensure the thermal design will meet rack-level deltaT requirement.

9.3 CPU Cooling Solution

9.3.1 Passive Cooling Solution

The heatsink must be a thermally optimized design at the lowest cost. Passive cooling is desired. Heatsink installation must be uncomplicated. The heatsink fins should be aligned with the airflow direction. Heatsinks must not block debug headers or connectors and may require cutouts in order to avoid tall electrical components on the server card.

In 1U Crater Lake configuration, the heatsink must be within the footprint as shown in Figure 9-1. The heatsink solution can be with or without remote fins depending on the design requirement.

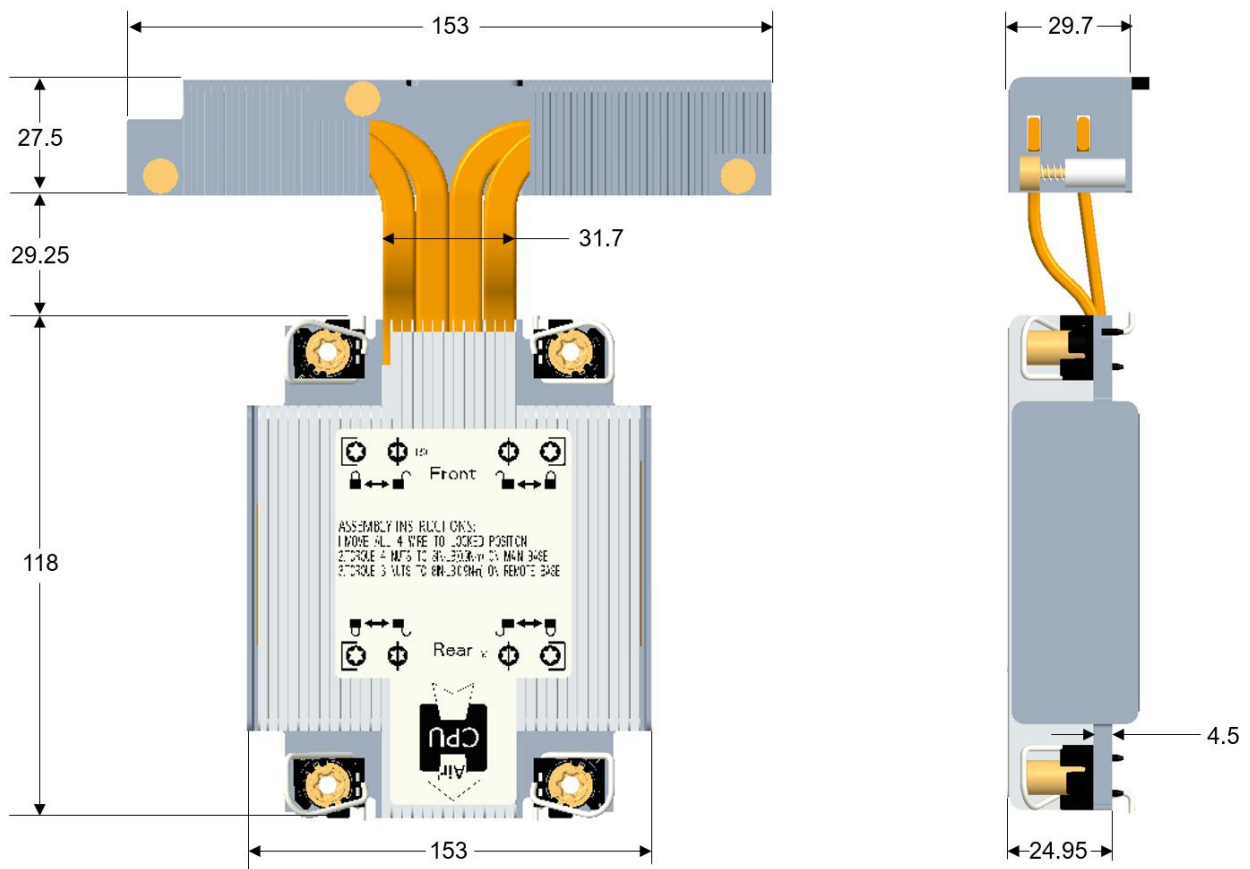


Figure 9-1: 1U Crater Lake Maximum Heatsink Footprint

9.4 Reliability Requirements

The operating life of the server card is a minimum of 3 years with target life of 5 years. All pertinent reliability data for CPU cooling solution and PCBA must be provided to meet the MTBF of 1.5 million hours.

9.5 M.2 Cooling Solution

Crater Lake 1S has a slot for one M.2 boot device.

The cooling solution for M.2 cooling must be thermally optimized design at the lowest cost. Passive cooling is required with TIM and heatsink solution being desired. Integrated heatsink is desired to enable easy serviceability. The solution must maintain all M.2 component temperatures within their operational limits during all stress conditions. 6.7mm M.2 connectors must be used to allow spacing between integrated heatsink base and server board PCB.

Components under the M.2 must follow the keepout requirement as shown in Figure 9-2.

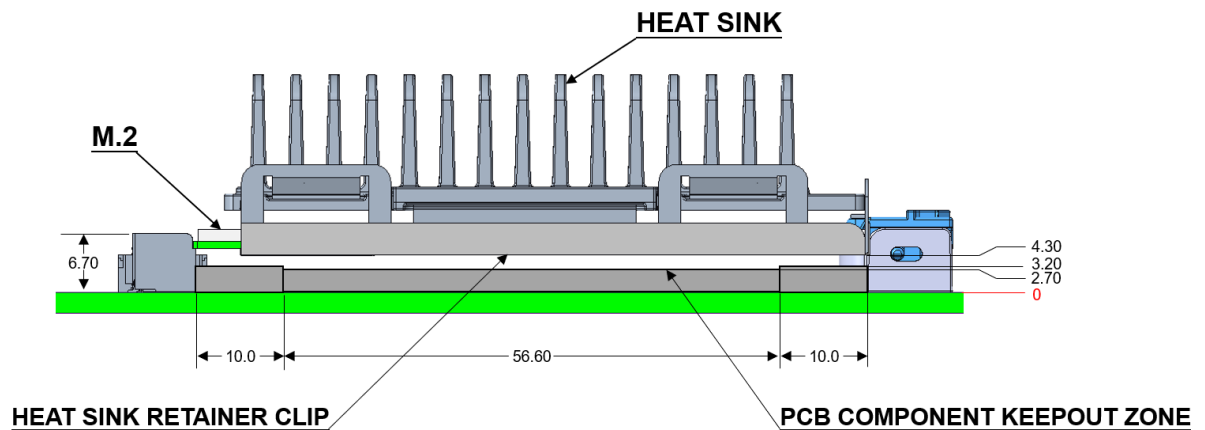


Figure 9-2: M.2 Integrated Heatsink Component Keepout

9.6 Temperature and Power Sensors

Each card must provide following sensors:

- Temperature sensors for PCH, CPU, DIMM, voltage regulators and other critical chips
- Power sensors for the PCH, CPU and the whole card
- Voltage sensors for all voltage rails
- Power/current sensors for rails providing more than 10W.

- One inlet ambient temperature sensor and one outlet ambient temperature sensor

The BMC on the platform must be able to read all these sensors via the Bridge IC. Additionally, over-temperature thresholds must be configurable, and an alert mechanism must be provided to enable thermal shutdown and/or an increase in airflow. The sensors are accurate to $\pm 2^{\circ}\text{C}$ and desired to be within 2% tolerance across whole operation temperature range. The goal sensor accuracy is $\pm 1^{\circ}\text{C}$.

9.7 Server Card Air Baffle

The card level air baffle must be designed to help maintain temperatures of all major components on the server card by reducing bypass air and increasing airflow through key components. The air baffle must be easy to service with the goal of requiring no tooling to remove. The air baffle must not have a large adverse effect on system level pressure drop. Due to height limitation, air baffle is not required for 1U blade form factor but shall be considered for 2U blade form factor.

10 I/O System

10.1 Design Guidelines

Refer to Intel® Xeon® Processor SPR CPU and Emmitsburg PCH design guide documents for implementation guidelines.

10.2 Expansion Interfaces of Crater Lake 1S Server Card

10.2.1 Straddle Mount Connector to YV3.5 Platform Integrated Baseboard (With NIC)

A straddle mount 2C connector on the Crater Lake motherboard enables the motherboard to connect to the platform integrated baseboard that houses the multi-host NIC and BIC (Class2)/BMC (Class1), depending on system class.

- A sled with four 1U blades will only route x4 PCIe and sideband to the baseboard
- A sled with two 2U blades will route all the 2C signals, including x8 PCIe and sideband to the baseboard using a cable

The list of signals on the 2C connector are as follows:

- x8 PCIe Gen 4 with 1x PCIe clock, 1x PERST#

- 1x IPMB over I3C interface for communication between management devices on Crater Lake (Bridge IC) and Yosemite V3.5 Baseboard (BMC or Bridge IC)
- 1x I2C Interface (Baseboard as Controller, for telemetry)
- 1x USB Interface (Baseboard as host for high-speed communication with Crater Lake BIC and expansion card BIC)
- 1x UART Interface for debug port to BMC
- MISC single ended signals
- Reserved for future use (RSVD)
- Signal names marked with RSVD are for future use. Vendor shall implement these functions with resistor option to isolate it from the interface where needed.

A signal list can be seen in Table 10-1

Table 10-1: Crater Lake 1S Server 2C connector to Baseboard

Crater Lake 1S 2C connector			
B1	I3C_BMC_BIC_SB_SDA	BB_BIC_READY	A1
B2	I3C_BMC_BIC_SB_SCL	SMB_BMC_CPLD_SDA	A2
B3	GND	SMB_BMC_CPLD_SCL	A3
B4	AC_ON_OFF_BTN_R	SMB_BMC_CPLD_ALT_N	A4
B5	FM_HSC_FAULT_N	GND	A5
B6	FM_BMC_HSC_EN_R	PWRBTN_R_N	A6
B7	PWRGD_SB_STBY_PWROK	RST_BMC_N	A7
B8	RST_PCIE_NIC_PERST_N	FM_BMC_RST_RTCRST_R	A8
B9	UART_REQ_R_N	SB_SLOT_ID1	A9
B10	GND	SB_SLOT_ID0	A10
B11	UART_CPLD_MUX_RXD	RSVD_2C_A11	A11
B12	UART_CPLD_MUX_R_TXD	PRSNT_SB_N	A12
B13	GND	GND	A13
B14	USB2_BMC_DN	CLK_100M_NIC_PCIE_CLK0_DN	A14
B15	USB2_BMC_DP	CLK_100M_NIC_PCIE_CLK0_DP	A15
B16	GND	GND	A16
B17	P5E_CPU_PE4_NIC_TX_C_DN_0	P5E_CPU_PE4_NIC_RX_DN_0	A17
B18	P5E_CPU_PE4_NIC_TX_C_DP_0	P5E_CPU_PE4_NIC_RX_DP_0	A18
B19	GND	GND	A19
B20	P5E_CPU_PE4_NIC_TX_C_DN_1	P5E_CPU_PE4_NIC_RX_DP_1	A20
B21	P5E_CPU_PE4_NIC_TX_C_DP_1	P5E_CPU_PE4_NIC_RX_DN_1	A21
B22	GND	GND	A22
B23	P5E_CPU_PE4_NIC_TX_C_DN_2	P5E_CPU_PE4_NIC_RX_DN_2	A23
B24	P5E_CPU_PE4_NIC_TX_C_DP_2	P5E_CPU_PE4_NIC_RX_DP_2	A24

Crater Lake 1S 2C connector			
B25	GND	GND	A25
B26	P5E_CPU_PE4_NIC_TX_C_DN_3	P5E_CPU_PE4_NIC_RX_DP_3	A26
B27	P5E_CPU_PE4_NIC_TX_C_DP_3	P5E_CPU_PE4_NIC_RX_DN_3	A27
B28	GND	GND	A28
B29	GND	GND	A29
B30	P5E_CPU_PE4_NIC_TX_C_DN_4	P5E_CPU_PE4_NIC_RX_DN_4	A30
B31	P5E_CPU_PE4_NIC_TX_C_DP_4	P5E_CPU_PE4_NIC_RX_DP_4	A31
B32	GND	GND	A32
B33	P5E_CPU_PE4_NIC_TX_C_DN_5	P5E_CPU_PE4_NIC_RX_DP_5	A33
B34	P5E_CPU_PE4_NIC_TX_C_DP_5	P5E_CPU_PE4_NIC_RX_DN_5	A34
B35	GND	GND	A35
B36	P5E_CPU_PE4_NIC_TX_C_DN_6	P5E_CPU_PE4_NIC_RX_DN_6	A36
B37	P5E_CPU_PE4_NIC_TX_C_DP_6	P5E_CPU_PE4_NIC_RX_DP_6	A37
B38	GND	GND	A38
B39	P5E_CPU_PE4_NIC_TX_C_DN_7	P5E_CPU_PE4_NIC_RX_DP_7	A39
B40	P5E_CPU_PE4_NIC_TX_C_DP_7	P5E_CPU_PE4_NIC_RX_DN_7	A40
B41	GND	GND	A41
B42	GND	GND	A42

10.2.2 Pin Definitions

Table 10-2 provides a detailed description of the pins between Crater Lake and the baseboard in class 1 and class 2 configurations. Refer to section 6.1 for more information on class 1 and class 2 differences. Class 1 and class 2 configurations use the same schematic and layout. BOM stuffing options are used to change a boards behavior to either class.

Depending on if the system configuration has four 1U blades or two 2U blades, the configuration may differ in how many PCIe lanes are connected.

- Class 1 routes all the management and sideband signals with 4 lanes of PCIe. The upper portion of the 2C connector (pins 29 – 42).
- Class 2 routes all the management and sidebands with 8 lanes of PCIe. All signals on the 2C connector are connected between Crater Lake and the Baseboard.

Unless otherwise noted, all signal directions are from the perspective of the devices on Crater Lake.

Table 10-2: Pin Description of Crater Lake <-> Baseboard Interface (Class 1)

YV3.5 Baseboard signals (class 1)		
Signal name	Direction	Description (Class 1 BMC on Baseboard)
I3C_IPMB_SDA	I/O	IPMB between Baseboard management entity (BMC) to BIC on 1S Server Card

YV3.5 Baseboard signals (class 1)		
I3C_IPMB_SCL	I/O	IPMB between Baseboard management entity (BMC) to BIC on 1S Server Card
SMB_BMC_CPLD_SDA	I/O	400KHz I2C from Baseboard to CPLD+BIC for commands
SMB_BMC_CPLD_SCL	I/O	400KHz I2C from Baseboard to CPLD+BIC for commands
SMB_BMC_CPLD_ALT_N	Output	Alert signal to baseboard, active low OD signal with PU at Baseboard
MB_PRST_N	Output	Present signal. Active low. 1S Server card to place 100 ohm to GND
FM_BMC_HSC_EN_R	Input	Signal to enable Server Card HSC Active High push pull. PD at 1S Server Card side Baseboard assert HSC_EN when: 1) 1S Server Card is fully inserted
FM_HSC_FAULT_N	Output	HSC Fault signal; low active; OD with PU on baseboard.
UART_CPLD_MUX_RXD	Input	UART input to 1S Server Card - Source is CPLD on Baseboard - Destination is CPLD on 1S Server Card
UART_CPLD_MUX_R_TXD	Output	UART TX from Server Card - Source is CPLD on 1S Server Card - Destination is CPLD on Baseboard
RST_PCIE_NIC_PERST_N	Output	PCIe reset from Server Card to Baseboard Low active , Push-Pull, 3.3V_STBY domain
PWRGD_SB_STBY_PWROK	Output	Standby Power OK of Server Card High active, push-pull
PWRBTN_R_N	Input	From Baseboard CPLD to CPU card CPLD and BIC to initiate a DC power cycle.
RST_BMC_N	Output	Signal from CPU card BIC to reset BMC on Baseboard
AC_ON_OFF_BTN_R	Output	AC button on the server module
RSVDx	N/A	Spare signals between server blade and baseboard
CLK_100M_NIC_PCIE_CLK0_DN/DP	Output	Server output of 100MHz clock; 1 clock output
PxE_*_TX*(n/p)X	Output	PCIe Gen5 RX of Server module. Class 1: X ranges from 0 to 3 Class 2: X ranges from 0 to 7

YV3.5 Baseboard signals (class 1)		
PxE_*_RX* (n/p)X	Input	PCIe Gen5 RX of Server module. Class 1: X ranges from 0 to 3 Class 2: X ranges from 0 to 7
UART_REQ_N	N/A	NC
BB_BIC_READY	Input	Indicates to CPU card CPLD that BMC is ready on Baseboard
USB2_BMC_DN/DP	I/O	USB interface between the baseboard and server Class 1: BMC on Baseboard is host Class 2: Server blade is host (e.g. NIC expansion BMC)
FM_BMC_RST_RTCSRST_R	output	0: CMOS clear 1: NA
SB_SLOT_IDx	output	Server board Slot ID strapping (1-4 server slot)
PRSNT_SB_N	Output	GNDED on Server board to indicate cable presence to Baseboard CPLD. Active Low

10.2.3 1U Front Expansion

The 1U front expansion is made up of two straddle-mount connectors at the front of the board. One connector is a 4C+, and the other is a 2C.

1U front expansion interface includes:

- 16 lanes of PCIe Gen 5 to the 4C+, and 4 lanes of PCIe Gen 4 to the 2C connector
- Two PCIe reference clocks; One is routed to the 4C+, and the other to the 2C
- I3C interface (SMBus compatible) for sideband management/thermal information
- I2C interface for additional management
- Control/alert signals such as resets, power break, present, and card ID
- 12V and 3.3V Power

A signal list can be seen in Table 10-3 and Table 10-4.

Table 10-3: Front expansion pin-out (primary 4C+)

Front 4C+ Expansion			
OB1	PWRGD_EXP_PWR_R	RST_87_PCIE_EXP_PERST2_N	OA1
OB2	FM_EXP_MAIN_PWR_EN	RST_PCIE_EXP_PERST3_N	OA2
OB3	SGPIO_LOAD_N	FM_EXP_WAKE_R_N	OA3
OB4	SGPIO_DATA_IN_R	NC	OA4

Front 4C+ Expansion			
OB5	SGPIO_DATA_OUT	NC	OA5
OB6	SGPIO_CLK	FM_EXP_SLOT_ID1	OA6
OB7	FM_EXP_SLOT_ID0	GND	OA7
OB8	NC	NC	OA8
OB9	NC	NC	OA9
OB10	GND	GND	OA10
OB11	SMB_PCIE_EXP1_SCL	SMB_PCIE_EXP1_ALT_N	OA11
OB12	SMB_PCIE_EXP1_SDA	CARD_TYPE_EXP_R	OA12
OB13	GND	GND	OA13
OB14	NC	NC	OA14
B1	P12V_STBY	GND	A1
B2	P12V_STBY	GND	A2
B3	P12V_STBY	GND	A3
B4	P12V_STBY	GND	A4
B5	P12V_STBY	GND	A5
B6	P12V_STBY	GND	A6
B7	NC	SMB_PCIE_EXP2_R_SCL	A7
B8	NC	SMB_PCIE_EXP2_R_SDA	A8
B9	NC	RST_BMC_N	A9
B10	RST_PCIE_EXP_PERSTO_N	PRSNT_PCIE_EXP1_N	A10
B11	P3V3_STBY	RST_PCIE_EXP_PERST1_N	A11
B12	FM_EXP1_AUX_PWR_R_EN	FM_EXP_PRSNT2_R_N	A12
B13	GND	GND	A13
B14	CLK_100M_EXP_PCIE_CLK0_DN	UART_PRIMARY_RX	A14
B15	CLK_100M_EXP_PCIE_CLK0_DP	UART_PRIMARY_R_TX	A15
B16	GND	GND	A16
B17	P5E_CPU_PE2_EXP_TX_DN_C_15	P5E_CPU_PE2_EXP_RX_DN_15	A17
B18	P5E_CPU_PE2_EXP_TX_DP_C_15	P5E_CPU_PE2_EXP_RX_DP_15	A18
B19	GND	GND	A19
B20	P5E_CPU_PE2_EXP_TX_DN_C_14	P5E_CPU_PE2_EXP_RX_DN_14	A20
B21	P5E_CPU_PE2_EXP_TX_DP_C_14	P5E_CPU_PE2_EXP_RX_DP_14	A21
B22	GND	GND	A22
B23	P5E_CPU_PE2_EXP_TX_DN_C_13	P5E_CPU_PE2_EXP_RX_DN_13	A23

Front 4C+ Expansion			
B24	P5E_CPU_PE2_EXP_TX_DP_C_13	P5E_CPU_PE2_EXP_RX_DP_13	A24
B25	GND	GND	A25
B26	P5E_CPU_PE2_EXP_TX_DN_C_12	P5E_CPU_PE2_EXP_RX_DN_12	A26
B27	P5E_CPU_PE2_EXP_TX_DP_C_12	P5E_CPU_PE2_EXP_RX_DP_12	A27
B28	GND	GND	A28
B29	GND	GND	A29
B30	P5E_CPU_PE2_EXP_TX_DN_C_11	P5E_CPU_PE2_EXP_RX_DN_11	A30
B31	P5E_CPU_PE2_EXP_TX_DP_C_11	P5E_CPU_PE2_EXP_RX_DP_11	A31
B32	GND	GND	A32
B33	P5E_CPU_PE2_EXP_TX_DN_C_10	P5E_CPU_PE2_EXP_RX_DN_10	A33
B34	P5E_CPU_PE2_EXP_TX_DP_C_10	P5E_CPU_PE2_EXP_RX_DP_10	A34
B35	GND	GND	A35
B36	P5E_CPU_PE2_EXP_TX_DN_C_9	31 P5E_CPU_PE2_EXP_RX_DN_9	A36
B37	P5E_CPU_PE2_EXP_TX_DP_C_9	P5E_CPU_PE2_EXP_RX_DP_9	A37
B38	GND	GND	A38
B39	P5E_CPU_PE2_EXP_TX_DN_C_8	P5E_CPU_PE2_EXP_RX_DN_8	A39
B40	P5E_CPU_PE2_EXP_TX_DP_C_8	P5E_CPU_PE2_EXP_RX_DP_8	A40
B41	GND	GND	A41
B42	FM_EXP_PRSNT0_R_N	FM_EXP_PRSNT1_R_N	A42
B43	GND	GND	A43
B44	P5E_CPU_PE2_EXP_TX_DN_C_7	P5E_CPU_PE2_EXP_RX_DN_7	A44
B45	P5E_CPU_PE2_EXP_TX_DP_C_7	P5E_CPU_PE2_EXP_RX_DP_7	A45
B46	GND	GND	A46
B47	P5E_CPU_PE2_EXP_TX_DN_C_6	P5E_CPU_PE2_EXP_RX_DN_6	A47
B48	P5E_CPU_PE2_EXP_TX_DP_C_6	P5E_CPU_PE2_EXP_RX_DP_6	A48
B49	GND	GND	A49
B50	P5E_CPU_PE2_EXP_TX_DN_C_5	P5E_CPU_PE2_EXP_RX_DN_5	A50
B51	P5E_CPU_PE2_EXP_TX_DP_C_5	P5E_CPU_PE2_EXP_RX_DP_5	A51
B52	GND	GND	A52
B53	P5E_CPU_PE2_EXP_TX_DN_C_4	P5E_CPU_PE2_EXP_RX_DN_4	A53
B54	P5E_CPU_PE2_EXP_TX_DP_C_4	P5E_CPU_PE2_EXP_RX_DP_4	A54
B55	GND	GND	A55

Front 4C+ Expansion			
B56	P5E_CPU_PE2_EXP_TX_DN_C_3	P5E_CPU_PE2_EXP_RX_DN_3	A56
B57	P5E_CPU_PE2_EXP_TX_DP_C_3	P5E_CPU_PE2_EXP_RX_DP_3	A57
B58	GND	GND	A58
B59	P5E_CPU_PE2_EXP_TX_DN_C_2	P5E_CPU_PE2_EXP_RX_DN_2	A59
B60	P5E_CPU_PE2_EXP_TX_DP_C_2	P5E_CPU_PE2_EXP_RX_DP_2	A60
B61	GND	GND	A61
B62	P5E_CPU_PE2_EXP_TX_DN_C_1	P5E_CPU_PE2_EXP_RX_DN_1	A62
B63	P5E_CPU_PE2_EXP_TX_DP_C_1	P5E_CPU_PE2_EXP_RX_DP_1	A63
B64	GND	GND	A64
B65	P5E_CPU_PE2_EXP_TX_DN_C_0	P5E_CPU_PE2_EXP_RX_DN_0	A65
B66	P5E_CPU_PE2_EXP_TX_DP_C_0	P5E_CPU_PE2_EXP_RX_DP_0	A66
B67	GND	GND	A67
B68	UART_NIC_BMC_TX_R	USB2_EXP_DN	A68
B69	UART_NIC_BMC_RX	USB2_EXP_DP	A69
B70	FM_EXP_PRSNT3_R_N	FM_PWRBRK_PRIMARY_N	A70

Table 10-4: Front expansion pin-out (secondary 2C)

B1	P12V_STBY	GND	A1
B2	P12V_STBY	GND	A2
B3	P12V_STBY	GND	A3
B4	P12V_STBY	GND	A4
B5	P12V_STBY	GND	A5
B6	P12V_STBY	GND	A6
B7	NC	NC	A7
B8	NC	NC	A8
B9	NC	NC	A9
B10	RST_PCIE_EXP2C_PERST0_N	FM_EXP2C_PRSNT2_R_N	A10
B11	P3V3_STBY	RST_PCIE_EXP2C_PERST1_N	A11
B12	NC	FM_EXP2C_PRSNT1_R_N	A12
B13	GND	GND	A13
B14	CLK_100M_FRONT_2C_CLK1_DN	CLK_100M_FRONT_2C_CLK0_DN	A14
B15	CLK_100M_FRONT_2C_CLK1_DP	CLK_100M_FRONT_2C_CLK0_DP	A15
B16	GND	GND	A16
B17	P5E_CPU_PE0_EXP2C_TX_C_DN_7	P5E_CPU_PE0_EXP2C_RX_DN_7	A17
B18	P5E_CPU_PE0_EXP2C_TX_C_DP_7	P5E_CPU_PE0_EXP2C_RX_DP_7	A18
B19	GND	GND	A19
B20	P5E_CPU_PE0_EXP2C_TX_C_DN_6	P5E_CPU_PE0_EXP2C_RX_DN_6	A20
B21	P5E_CPU_PE0_EXP2C_TX_C_DP_6	P5E_CPU_PE0_EXP2C_RX_DP_6	A21

B22	GND	GND	A22
B23	P5E_CPU_PEO_EXP2C_TX_C_DN_5	P5E_CPU_PEO_EXP2C_RX_DN_5	A23
B24	P5E_CPU_PEO_EXP2C_TX_C_DP_5	P5E_CPU_PEO_EXP2C_RX_DP_5	A24
B25	GND	GND	A25
B26	P5E_CPU_PEO_EXP2C_TX_C_DN_4	P5E_CPU_PEO_EXP2C_RX_DN_4	A26
B27	P5E_CPU_PEO_EXP2C_TX_C_DP_4	P5E_CPU_PEO_EXP2C_RX_DP_4	A27
B28	GND	GND	A28
B29	GND	GND	A29
B30	P5E_CPU_PEO_EXP2C_TX_C_DN_3	P5E_CPU_PEO_EXP2C_RX_DN_3	A30
B31	P5E_CPU_PEO_EXP2C_TX_C_DP_3	P5E_CPU_PEO_EXP2C_RX_DP_3	A31
B32	GND	GND	A32
B33	P5E_CPU_PEO_EXP2C_TX_C_DN_2	P5E_CPU_PEO_EXP2C_RX_DN_2	A33
B34	P5E_CPU_PEO_EXP2C_TX_C_DP_2	P5E_CPU_PEO_EXP2C_RX_DP_2	A34
B35	GND	GND	A35
B36	P5E_CPU_PEO_EXP2C_TX_C_DN_1	P5E_CPU_PEO_EXP2C_RX_DN_1	A36
B37	P5E_CPU_PEO_EXP2C_TX_C_DP_1	P5E_CPU_PEO_EXP2C_RX_DP_1	A37
B38	GND	GND	A38
B39	P5E_CPU_PEO_EXP2C_TX_C_DN_0	P5E_CPU_PEO_EXP2C_RX_DN_0	A39
B40	P5E_CPU_PEO_EXP2C_TX_C_DP_0	P5E_CPU_PEO_EXP2C_RX_DP_0	A40
B41	GND	GND	A41
B42	GND	GND	A42

10.2.4 2U Riser Expansion

The 2U front expansion is made up of two vertical connectors on the server board. Both connectors are 4C+.

2U front expansion interface includes:

- 16 lanes of PCIe to the first 4C+, and 8 lanes of PCIe to the second 4C+ connector; All PCIe is Gen 5 capable
- Two PCIe reference clocks: One is routed to the 4C+, and the other to the 2C
- I3C interface (SMBus compatible) for sideband management/thermal information
- I2C interface for additional management
- Control/alert signals such as resets, power break, present, and card ID
- 12V and 3.3V Power

A signal list can be seen in Table 10-5 and Table 10-6.

Table 10-5: 2U expansion pin-out (primary - 4C+)

OA1	P12V_STBY	P12V_STBY	OB1
OA2	P12V_STBY	P12V_STBY	OB2

OA3	P12V_STBY	P12V_STBY	OB3
OA4	P12V_STBY	P12V_STBY	OB4
OA5	P12V_STBY	P12V_STBY	OB5
OA6	P12V_STBY	P12V_STBY	OB6
OA7	P12V_STBY	P12V_STBY	OB7
OA8	P12V_STBY	P12V_STBY	OB8
OA9	P12V_STBY	P12V_STBY	OB9
OA10	NC, RSVD	NC, RSVD	OB10
OA11	GND	P3V3_STBY	OB11
OA12	GND	NC, RSVD	OB12
OA13	GND	GND	OB13
OA14	GND	GND	OB14
Mechanical key			
A1	GND	GND	B1
A2	GND	GND	B2
A3	GND	GND	B3
A4	GND	GND	B4
A5	GND	GND	B5
A6	GND	GND	B6
A7	GND	GND	B7
A8	FM_RISER_MAIN_PWR_R_EN	FM_PCIE_RISER_PWRBRK_N	B8
A9	PWRGD_RISER_MAIN_PWR	RISER_CARD_TYPE_DETECTION0	B9
A10	PRSNTA1_N	RISER_CARD_TYPE_DETECTION1	B10
A11	RST_PCIE_RISER_PERST1_N	RISER_CARD_TYPE_DETECTION2	B11
A12	RISER_RSVD1	FM_RISER_STBY_PWR_R_EN	B12
A13	GND	GND	B13
A14	SMB_PCIE_RISER_SCL	CLK_100M_RISER_PCIE_CLKO_DN	B14
A15	SMB_PCIE_RISER_SDA	CLK_100M_RISER_PCIE_CLKO_DP	B15
A16	GND	GND	B16
A17	NC	NC	B17
A18	NC	NC	B18
A19	GND	GND	B19
A20	NC	NC	B20
A21	NC	NC	B21
A22	GND	GND	B22
A23	NC	NC	B23
A24	NC	NC	B24
A25	GND	GND	B25
A26	NC	NC	B26

A27	NC	NC	B27
A28	GND	GND	B28
Mechanical key			
A29	GND	GND	B29
A30	NC	NC	B30
A31	NC	NC	B31
A32	GND	GND	B32
A33	NC	NC	B33
A34	NC	NC	B34
A35	GND	GND	B35
A36	NC	NC	B36
A37	NC	NC	B37
A38	GND	GND	B38
A39	NC	NC	B39
A40	NC	NC	B40
A41	GND	GND	B41
A42	NC	NC	B42
Mechanical key			
A43	GND	GND	B43
A44	P3E_CPU_RISER_RX_DN_7	P3E_CPU_RISER_TX_C_DN_7	B44
A45	P3E_CPU_RISER_RX_DP_7	P3E_CPU_RISER_TX_C_DP_7	B45
A46	GND	GND	B46
A47	P3E_CPU_RISER_RX_DN_6	P3E_CPU_RISER_TX_C_DN_6	B47
A48	P3E_CPU_RISER_RX_DP_6	P3E_CPU_RISER_TX_C_DP_6	B48
A49	GND	GND	B49
A50	P3E_CPU_RISER_RX_DN_5	P3E_CPU_RISER_TX_C_DN_5	B50
A51	P3E_CPU_RISER_RX_DP_5	P3E_CPU_RISER_TX_C_DP_5	B51
A52	GND	GND	B52
A53	P3E_CPU_RISER_RX_DN_4	P3E_CPU_RISER_TX_C_DN_4	B53
A54	P3E_CPU_RISER_RX_DP_4	P3E_CPU_RISER_TX_C_DP_4	B54
A55	GND	GND	B55
A56	P3E_CPU_RISER_RX_DN_3	P3E_CPU_RISER_TX_C_DN_3	B56
A57	P3E_CPU_RISER_RX_DP_3	P3E_CPU_RISER_TX_C_DP_3	B57
A58	GND	GND	B58
A59	P3E_CPU_RISER_RX_DN_2	P3E_CPU_RISER_TX_C_DN_2	B59
A60	P3E_CPU_RISER_RX_DP_2	P3E_CPU_RISER_TX_C_DP_2	B60
A61	GND	GND	B61
A62	P3E_CPU_RISER_RX_DN_1	P3E_CPU_RISER_TX_C_DN_1	B62
A63	P3E_CPU_RISER_RX_DP_1	P3E_CPU_RISER_TX_C_DP_1	B63

A64	GND	GND	B64
A65	P3E_CPU_RISER_RX_DN_0	P3E_CPU_RISER_TX_C_DN_0	B65
A66	P3E_CPU_RISER_RX_DP_0	P3E_CPU_RISER_TX_C_DP_0	B66
A67	GND	GND	B67
A68	USB2_RISER_DN	UART_RISER_RX	B68
A69	USB2_RISER_DP	UART_RISER_TX	B69
A70	GND	PRSNTA1_N	B70

Table 10-6: 2U Expansion Pin-Out (Secondary - 4C+)

OA1	P12V_STBY	P12V_STBY	OB1
OA2	P12V_STBY	P12V_STBY	OB2
OA3	P12V_STBY	P12V_STBY	OB3
OA4	P12V_STBY	P12V_STBY	OB4
OA5	P12V_STBY	P12V_STBY	OB5
OA6	P12V_STBY	P12V_STBY	OB6
OA7	P12V_STBY	P12V_STBY	OB7
OA8	P12V_STBY	P12V_STBY	OB8
OA9	P12V_STBY	P12V_STBY	OB9
OA10	NC, RSVD	NC, RSVD	OB10
OA11	GND	P3V3_STBY	OB11
OA12	GND	NC, RSVD	OB12
OA13	GND	GND	OB13
OA14	GND	GND	OB14
Mechanical key			
A1	GND	GND	B1
A2	GND	GND	B2
A3	GND	GND	B3
A4	GND	GND	B4
A5	GND	GND	B5
A6	GND	GND	B6
A7	GND	GND	B7
A8	SMB_RISER_ALT_N	RST_PCIE_RISER_PERST_N	B8
A9	RISER_RSVD2	RISER_LOAD_R	B9
A10	PRSNTA2_N	RISER_DATA_IN	B10
A11	RISER_RSVD3	RISER_DATA_OUT_R	B11
A12	RISER_RSVD4	RISER_CLK_R	B12
A13	GND	GND	B13

A14	IPMB_PCIE_RISER_SCL	CLK_100M_RISER_PCIE_CLK1_DN	B14
A15	IPMB_PCIE_RISER_SDA	CLK_100M_RISER_PCIE_CLK1_DP	B15
A16	GND	GND	B16
A17	P3E_CPU_RISER_RX_DN_31	P3E_CPU_RISER_TX_C_DN_31	B17
A18	P3E_CPU_RISER_RX_DP_31	P3E_CPU_RISER_TX_C_DP_31	B18
A19	GND	GND	B19
A20	P3E_CPU_RISER_RX_DN_30	P3E_CPU_RISER_TX_C_DN_30	B20
A21	P3E_CPU_RISER_RX_DP_30	P3E_CPU_RISER_TX_C_DP_30	B21
A22	GND	GND	B22
A23	P3E_CPU_RISER_RX_DN_29	P3E_CPU_RISER_TX_C_DN_29	B23
A24	P3E_CPU_RISER_RX_DP_29	P3E_CPU_RISER_TX_C_DP_29	B24
A25	GND	GND	B25
A26	P3E_CPU_RISER_RX_DN_28	P3E_CPU_RISER_TX_C_DN_28	B26
A27	P3E_CPU_RISER_RX_DP_28	P3E_CPU_RISER_TX_C_DP_28	B27
A28	GND	GND	B28
Mechanical key			
A29	GND	GND	B29
A30	P3E_CPU_RISER_RX_DN_27	P3E_CPU_RISER_TX_C_DN_27	B30
A31	P3E_CPU_RISER_RX_DP_27	P3E_CPU_RISER_TX_C_DP_27	B31
A32	GND	GND	B32
A33	P3E_CPU_RISER_RX_DN_26	P3E_CPU_RISER_TX_C_DN_26	B33
A34	P3E_CPU_RISER_RX_DP_26	P3E_CPU_RISER_TX_C_DP_26	B34
A35	GND	GND	B35
A36	P3E_CPU_RISER_RX_DN_25	P3E_CPU_RISER_TX_C_DN_25	B36
A37	P3E_CPU_RISER_RX_DP_25	P3E_CPU_RISER_TX_C_DP_25	B37
A38	GND	GND	B38
A39	P3E_CPU_RISER_RX_DN_24	P3E_CPU_RISER_TX_C_DN_24	B39
A40	P3E_CPU_RISER_RX_DP_24	P3E_CPU_RISER_TX_C_DP_24	B40
A41	GND	GND	B41
A42	NC	NC	B42
Mechanical key			
A43	GND	GND	B43
A44	P3E_CPU_RISER_RX_DN_23	P3E_CPU_RISER_TX_C_DN_23	B44
A45	P3E_CPU_RISER_RX_DP_23	P3E_CPU_RISER_TX_C_DP_23	B45
A46	GND	GND	B46
A47	P3E_CPU_RISER_RX_DN_22	P3E_CPU_RISER_TX_C_DN_22	B47
A48	P3E_CPU_RISER_RX_DP_22	P3E_CPU_RISER_TX_C_DP_22	B48
A49	GND	GND	B49
A50	P3E_CPU_RISER_RX_DN_21	P3E_CPU_RISER_TX_C_DN_21	B50

A51	P3E_CPU_RISER_RX_DP_21	P3E_CPU_RISER_TX_C_DP_21	B51
A52	GND	GND	B52
A53	P3E_CPU_RISER_RX_DN_20	P3E_CPU_RISER_TX_C_DN_20	B53
A54	P3E_CPU_RISER_RX_DP_20	P3E_CPU_RISER_TX_C_DP_20	B54
A55	GND	GND	B55
A56	P3E_CPU_RISER_RX_DN_19	P3E_CPU_RISER_TX_C_DN_19	B56
A57	P3E_CPU_RISER_RX_DP_19	P3E_CPU_RISER_TX_C_DP_19	B57
A58	GND	GND	B58
A59	P3E_CPU_RISER_RX_DN_18	P3E_CPU_RISER_TX_C_DN_18	B59
A60	P3E_CPU_RISER_RX_DP_18	P3E_CPU_RISER_TX_C_DP_18	B60
A61	GND	GND	B61
A62	P3E_CPU_RISER_RX_DN_17	P3E_CPU_RISER_TX_C_DN_17	B62
A63	P3E_CPU_RISER_RX_DP_17	P3E_CPU_RISER_TX_C_DP_17	B63
A64	GND	GND	B64
A65	P3E_CPU_RISER_RX_DN_16	P3E_CPU_RISER_TX_C_DN_16	B65
A66	P3E_CPU_RISER_RX_DP_16	P3E_CPU_RISER_TX_C_DP_16	B66
A67	GND	GND	B67
A68	RSVD_USB_DN	RSVD_UART_RX	B68
A69	RSVD_USB_DP	RSVD_UART_TX	B69
A70	GND	PRSNTA2_N	B70

10.2.5 Pin Definitions

As the connector is referenced to OCP NIC 3.0 interface, this specification will only call out pin definitions that could be different for the expansion system. Pin definitions can be seen in Table 10-7.

Table 10-7: Detailed Pin Definitions

Signal name	Direction (with respect to server blade)	Description
CARD_TYPE_N	I	Found in front expansion module. Used to determine the card type. 1.5V: Expansion with NIC 1 V: Expansion with 4 EDSFF 0.5V: Expansion with 6 M.2 0V: Direct connect for 1 EDSFF
CARD_TYPE_Detection[2:0]	I	Found in 2U expansion To identify which type of card for the riser 000 – Server Card 001 – Device Card 010 -> 111 RFU

10.3 Electrical Interface in Crater Lake 1S Server Card

10.3.1 UART

The serial port shall be routed to the BMC on the platform. Thus, the user can access the system's serial console through the BMC locally or remotely via Serial Over Lan (SOL).

10.3.2 I³C and IPMB

There is one I³C and one I²C connections from the server to Baseboard as shown in Figure 10-1

I²C connects the baseboard BMC to the server CPLD. This channel is used for the primary configuration interface. It shall support at least 400kHz while targeting operation at 1MHz. The BMC will use this channel for command and control of the CPLD.

I³C for Command will have BIC and BMC connected where its usage is generic IPMB or DMTF MCTP transactions.

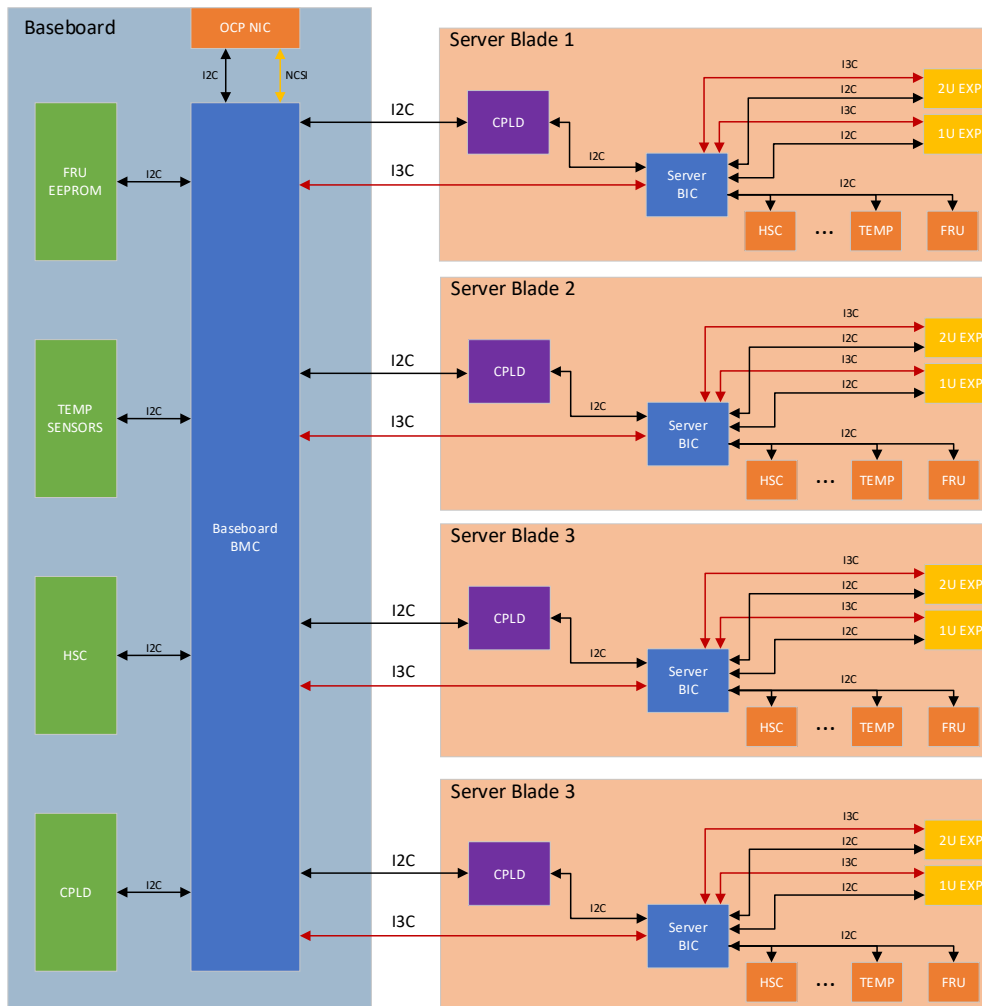


Figure 10-1: I2C/I3C connections out of server blade.

10.3.3 USB

A high-speed USB connection is provisioned from BMC to Crater Lake with BMC as host and BIC as device. There is a USB hub on Crater Lake to enable BMC to connect to the BIC on expansion cards. There is no USB connection to the CPLD on Crater Lake. The USB interface is used as a higher speed interface to perform firmware updates. Class 1 configuration can be seen in Figure 10-2.

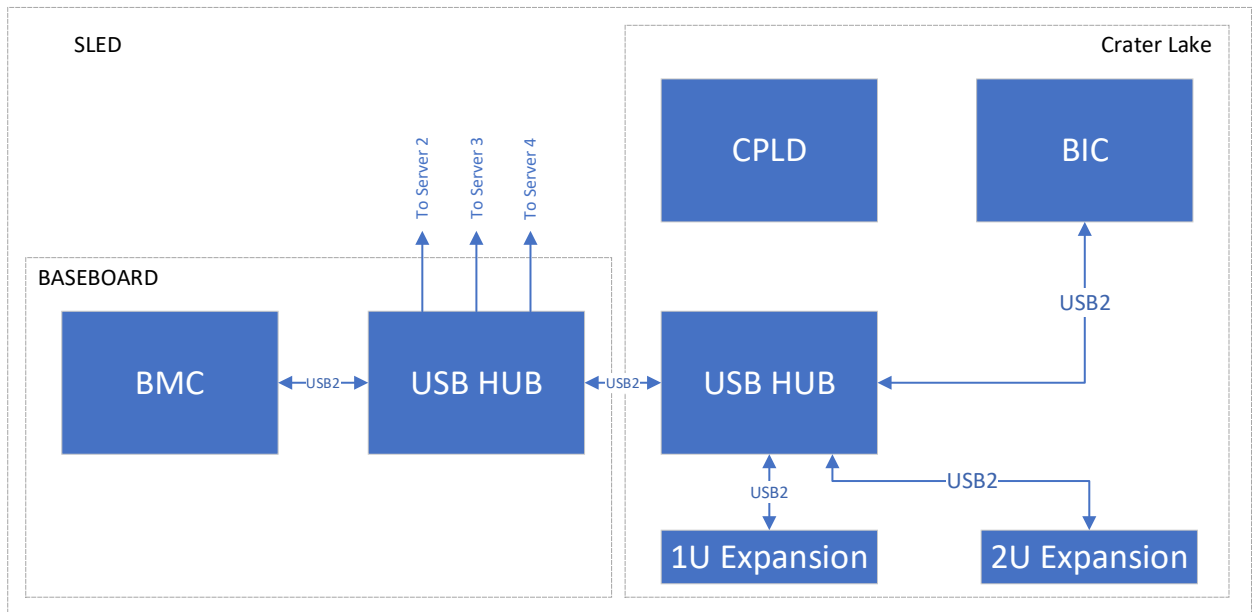


Figure 10-2: USB Connections for Class 1

In Class 2 configuration with local NIC, the BMC moves from the Baseboard to the NIC expansion board and USB is changed accordingly with BOM options. This can be seen in Figure 10-3.

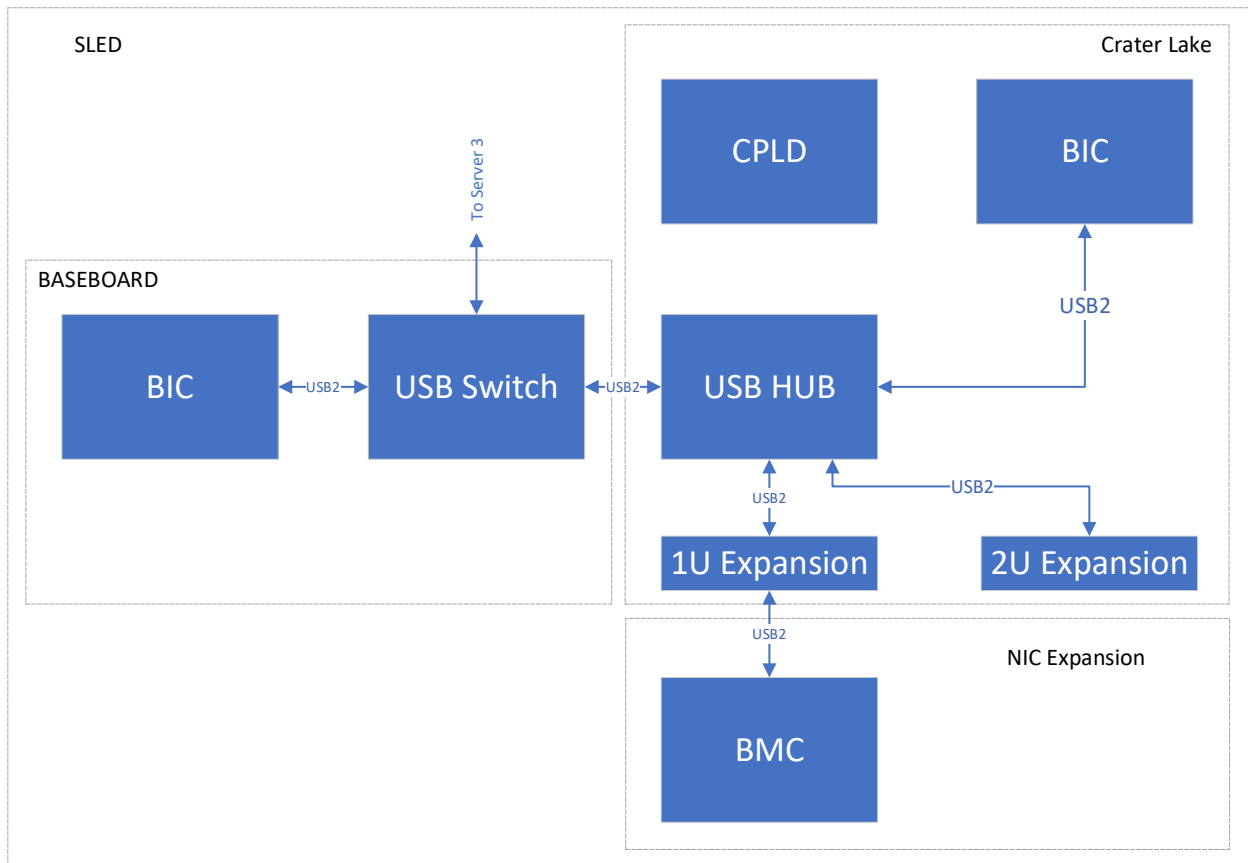


Figure 10-3: USB Connections for Class 2

10.3.4 SPI

SPI is the BIOS interface for PCH. Crater lake uses Quad SPI to load BIOS quickly. PFR is not part of the Crater Lake design. The PCH communicates directly with the boot SPI flash.

BMC can program SPI Flash Out of Band (OOB), via the BIC. To enable that, there is a mux in the CPLD that allows BIC to use the SPI path as shown in Figure 10-4.

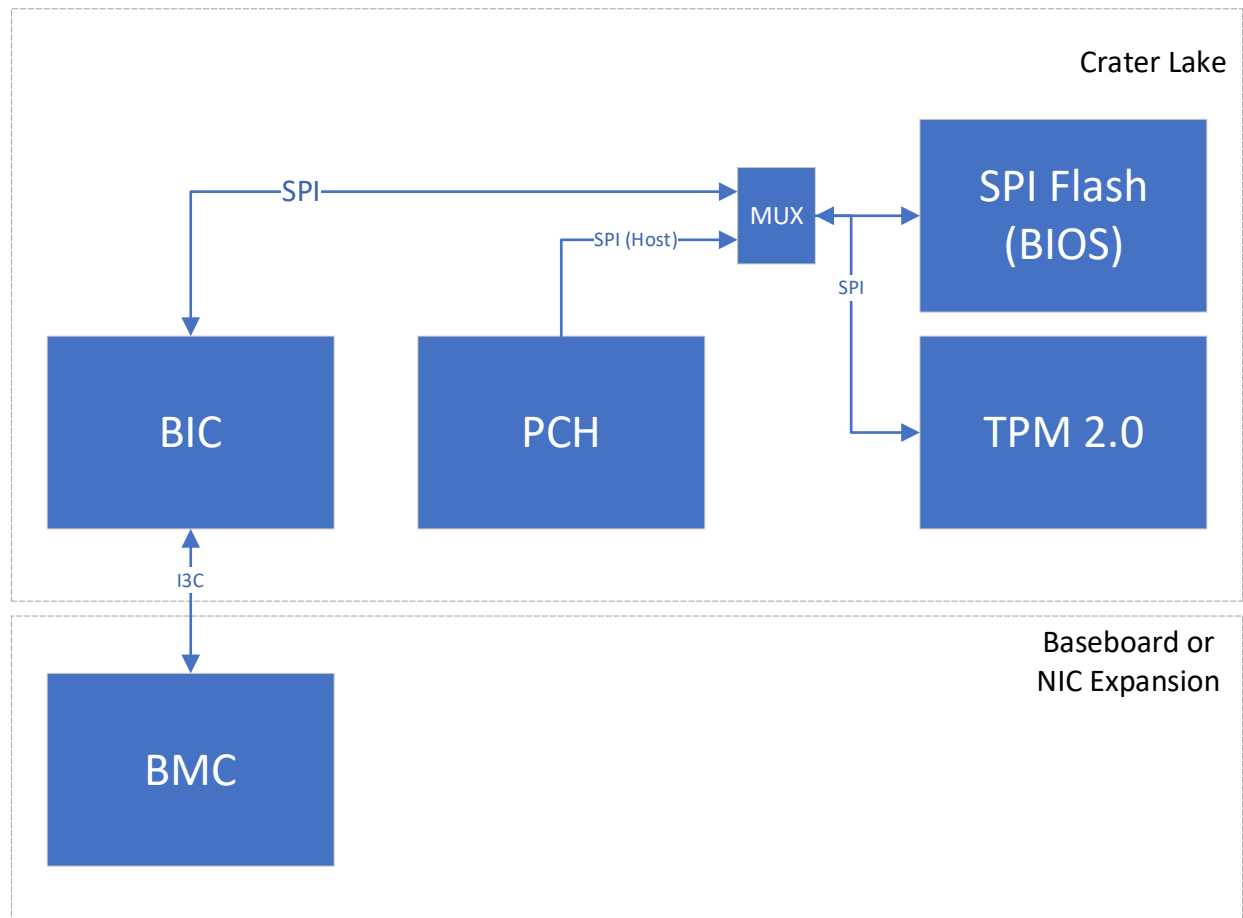


Figure 10-4: SPI Connections for Crater Lake

10.3.5 JTAG

XDP is the primary JTAG port to Crater Lake server board to communicate to PCH and CPU. The BIC is also on the bus and can take over the bus to become the controller.

There is a dedicated connector to program the CPLD.

A third JTAG connector is available to talk to BIC. CPLD is also on this bus and can take over the bus to talk to BIC.

Additionally, the BMC through the BIC, supports Intel's At-Scale Debug (ASD) to the CPU. In order to support security requirements, this ASD connection can be manually disabled by populating a jumper on Crater Lake. This way, the JTAG interface is only accessible if someone has physical access to the system.

A diagram of this implementation can be seen in Figure 10-5.

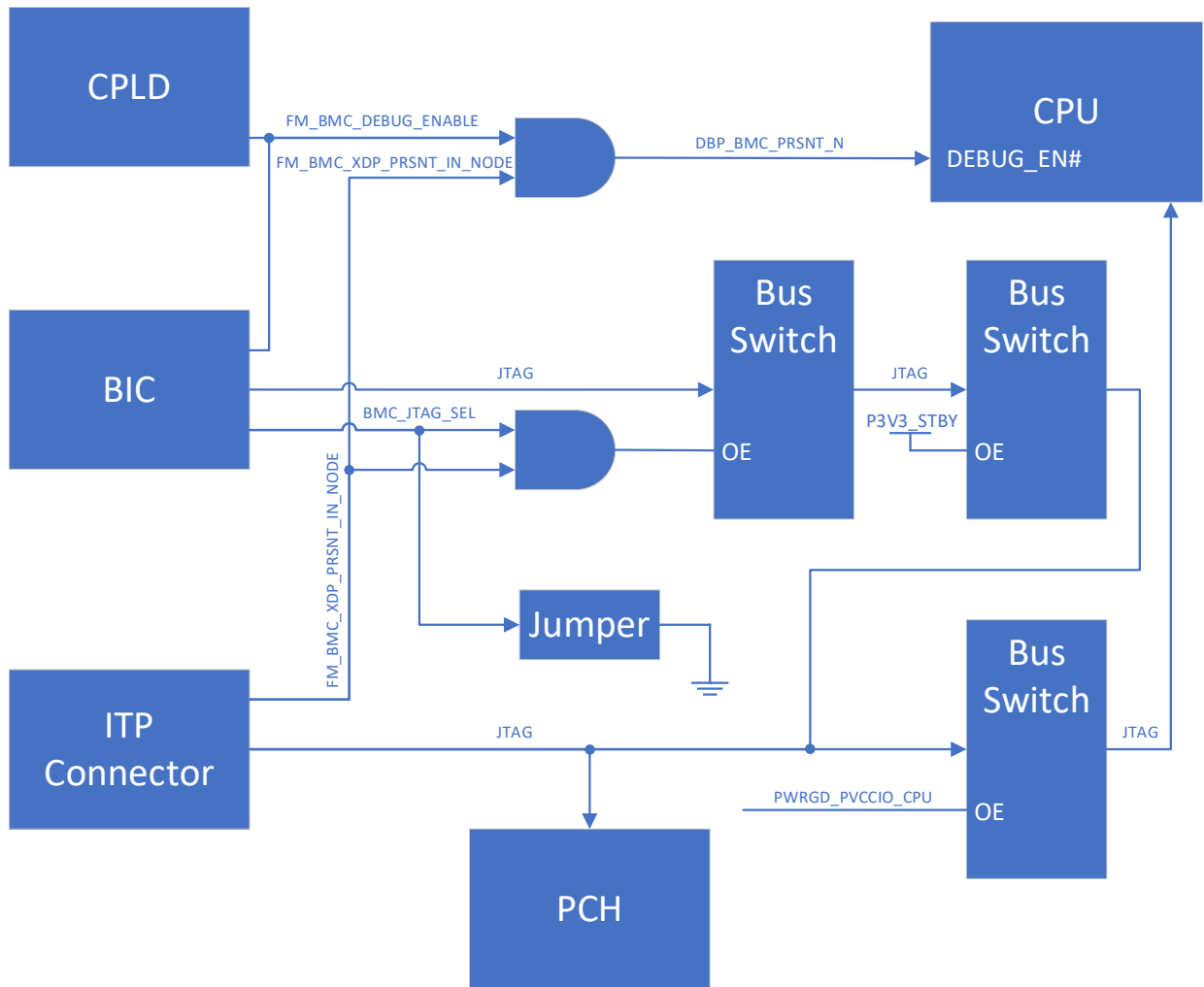


Figure 10-5 - Debug Connectivity

10.3.6 Bridge IC(BIC) GPIOs

Table 10-8 lists the GPIO assignments for BIC.

Table 10-8: BIC GPIOs

Pin	Function	Signal Name	Port Direction
B1	GPIOT1	GND	Power
B2	GPIOT0	A_P12V_STBY_SCALED	Input
B2	GPIOT2	A_P3V3_STBY_SCALED	Input
C2	GPIOT4	A_P3V_BAT_SCALED	Input
D1	GPIOT5	GND	Power

Pin	Function	Signal Name	Port Direction
D2	GPIOT6	CARD_TYPE_EXP	Input
D3	GPIOT3	A_P1V05_PCH_STBY_SENSOR	Input
E1		BIC_ADCVREFN0	Reference
E2		BIC_ADCVREFP0	Reference
E3	GPIOT7	HSC_TYPE_ADC	Input
F1		PD_BIC_ADCREXT0	Reference
F2		BIC_ADCVREFREXT0	Reference
G1		BIC_ADCVREFREXT1	Reference
G2		PD_BIC_ADCREXT1	Reference
K4	GPIOU1	A_P5V_STBY_SCALED	Input
K2	GPIOU0	GND	Power
H3		BIC_ADCVREFN1	Reference
J2	GPIOU4	GND	Power
J1	GPIOU3	A_P12V_CPU_NVDIMM_SCALED	Input
J3		BIC_ADCVREFP1	Reference
K3	GPIOU2	GND	Power
H2	GPIOU7	A_P1V8_STBY_SENSOR	Input
J4	GPIOU5	A_P1V2_STBY_SENSOR	Input
H1	GPIOU6	A_P3V3_M2A_SCALED	Input
K1	RGMII1TXCK	BIC_READY	Output
L1	RGMII1TXD3	FM_PCH_BMC_THERMTRIP_N	Output
L2	RGMII1TXD2	PWRGD_CPU_LVC3	Input
L3	RGMII1TXCTL	FM_RMCA_LVT3_N	Input
L4	RGMII1TXD0	HSC_MUX_SWITCH_R	Output
M1	RGMII1RXD0	SMB_SENSOR_LVC3_ALERT_N	Input
M2	RGMII1RXCTL	IRQ_HSC_ALERT2_N	Input
M3	RGMII1RXCK	FM_THROTTLE_R_N	Input
M4	RGMII1TXD1	FM_FORCE_ADR_N_R	Output
M5	TXD10	FM_S3M_CPU0_CD_INIT_ERROR	Input
N1	RGMII1RXD3	RST_PLTRST_BUF_N	Input
N2	RGMII1RXD2	SYS_PWRBTN_N	Input
N3	RGMII1RXD1	FM_CATERR_LVT3_N	Input
N4	PWM8	FM_BMC_PCH_SCI_LPC_R_N	Output
N5	TXD9	FM_PCHHOT_N	Input
N6	RXD12	DBP_CPU_PREQ_BIC_N	Output
P1	PWM10	FM_SLPS3_PLD_N	Input
P2	PWM12	IRQ_UV_DETECT_N	Input
P3	PWM13	FM_UV_ADR_TRIGGER_EN_R	Output

Pin	Function	Signal Name	Port Direction
P4	PWM9	FM_BIOS_POST_CMPLT_BMC_N	Input
P5	PWM11	IRQ_BMC_PCH_SMI_LPC_R_N	Output
P6	RXD9	FM_SLPS4_PLD_N	Input
P7	TXD12	IRQ_CPU0_VRHOT_N	Input
P8	TXD13	FM_CPU_THERMTRIP_LATCH_LVT3_N	Input
R1	PWM14	IRQ_SMI_ACTIVE_BMC_N	Input
R2	PWM15	HSC_SET_EN_R	Output
R3	TACH13	RST_USB_HUB_N_R	Output
R4	RXD10	PWRGD_SYS_PWROK	Input
R5	TXD11	FM_HSC_TIMER	Input
R6	THRUIN3	H_CPU_MEMHOT_OUT_LVC3_N	Input
R7		PWRBTN_N	Input
R8	MDIO1	H_BMC_PRDY_BUF_N	Input
T1	TACH12		No Connect
T2	TACH14	A_P3V_BAT_SCALED_EN_R	Output
T3	TACH15	FM_SPI_PCH_MASTER_SEL_R	Output
T4	RXD11	IRQ_SMB_IO_LVC3_STBY_ALRT_N	Input
T5	RXD13	FM_CPU_SKTOCC_LVT3_PLD_N	Input
T6	THRUOUT3	RST_PLTRST_PLD_N	Input
T7	MDC1	RST_BMC_R_N	Output
T8	MAC11LINK	BMC_READY	Output
K14	GPIOJ6		No Connect
K15	GPIOJ7		No Connect
K16	GPIOJ5	SMB_PCIE_RISER_R_SDA	Bidirectional
L14	GPIOJ2	SMB_PCIE_EXP1_R_SCL	Output
L15	GPIOJ3	SMB_PCIE_EXP1_R_SDA	Bidirectional
L16	GPIOJ4	SMB_PCIE_RISER_R_SCL	Output
M13	GPIOI4	SMB_PMBUS_SML1_STBY_LVC3_R2_SCL	Output
M14	GPIOI7	SMB_CPU_PIROM_SDA	Bidirectional
M15	GPIOJ0	SMB_I3C_BIC_BMC_SCL	Input
M16	GPIOJ1	SMB_I3C_BIC_BMC_SDA	Bidirectional
N14	GPIOH7	SMB_SENSOR_LVC3_R_SDA	Bidirectional
N15	GPIOI5	SMB_PMBUS_SML1_STBY_LVC3_R2_SDA	Bidirectional
N16	GPIOI6	SMB_CPU_PIROM_SCL	Output
P12	GPIOH5	SMB_BIC_CPLD_R_SDA	Bidirectional
P13	GPIOH6	SMB_SENSOR_LVC3_R_SCL	Output
P15	GPIOI2	SMB_HOST_STBY_BMC_LVC3_R_SCL	Output
P16	GPIOI3	SMB_HOST_STBY_BMC_LVC3_R_SDA	Bidirectional

Pin	Function	Signal Name	Port Direction
R15	GPIOH4	SMB_BIC_CPLD_R_SCL	Output
R16	GPIOI1	SMB_SMLINK0_STBY_LVC3_R_SDA	Bidirectional
T16	GPIOI0	SMB_SMLINK0_STBY_LVC3_R_SCL	Output
G15	SDA13		No Connect
G16	SDA14	I3C_SPD_DDR_CPU_BIC_R_SDA	Bidirectional
H15	SCL13		No Connect
H16	SDA12		No Connect
J13	SCL14	I3C_SPD_DDR_CPU_BIC_R_SCL	Output
J14	SCL12		No Connect
J15	SDA11	I3C1SDA_RSVD	RSVD
J16	SCL11	I3C1SCL_RSVD	RSVD
A11	TDO	JTAG_BIC_DEBUG_TDO_R	Output
A12	NTRST	JTAG_BIC_NTRST1	Input
A13	TCK2	BIC_JTAG_TCK_R	Output
B11	TMS	JTAG_BIC_DEBUG_TMS	Input
B12	TMS2	BIC_JTAG_TMS_R	Output
B13	NTRST2		No Connect
C10	TDI	JTAG_BIC_DEBUG_TDI	Input
C11	TDO2	BIC_JTAG_TDO	Input
D10	TCK	JTAG_BIC_DEBUG_TCK	Input
D11	TDI2	BIC_JTAG_TDI_R	Output
E13	ESPIRST#	RST_ESPI_RESET_R_N	Input
E14	ESPIALT#	ESPI_ALERT_N	Output
E15	ESPICS#	ESPI_CS_R_N	Input
E16	ESPICK	CLK_LPC_ESPI_R	Input
F14	ESPID3	ESPI_IO3_R2	Bidirectional
F15	ESPID2	ESPI_IO2_R2	Bidirectional
F16	ESPID1	ESPI_IO1_R2	Bidirectional
G14	ESPID0	ESPI_IO0_R2	Bidirectional
H14		PECI_BMC_R	Bidirectional
N11	GPIOF7	FBRK_N_R	Output
P10	GPIOF5	FM_FAST_PROCHOT_EN_N_R	Output
P9	GPIOF1	IRQ_SML1_PMBUS_ALERT_N	Input
R10	GPIOF4	FM_DBP_PRESENT_N	Input
R9	GPIOF2	IRQ_PCH_CPU_NMI_EVENT_N	Input
T10	GPIOF3	FM_BMC_DEBUG_ENABLE_N	Output
T11	GPIOF6	FM_SPI_MUX_OE_CTL_PLD_N	Output
T9	GPIOF0	IRQ_BMC_PCH_NMI_R	Output

Pin	Function	Signal Name	Port Direction
B14	GPION0	SGPIO_BMC_CLK_R	Output
C12	GPION3	SGPIO_BMC_DIN	Input
C13	GPION1	SGPIO_BMC_LD_R_N	Output
D12	GPION2	SGPIO_BMC_DOUT_R	Output
A10	GPIOP6	SPI_BIC_CS1_R_N	Output
A4	GPIOS1	SPI_BIC_R_IO2	Bidirectional
A5	GPIOR6	SPI_BIC_R_CLK	Output
A6	GPIOR7	SPI_BIC_R_IO0	Bidirectional
A7	GPIOR4	SPI_BIC_CS0_R_N	Output
A8	GPIOQ4	SPI_BIC_OOB1_SIO3	Bidirectional
A9	GPIOQ0	SPI_BIC_OOB1_CLK	Output
B10	GPIOP7		No Connect
B4	GPIOS2	SPI_BIC_R_IO3	Bidirectional
B5	GPIOS0	SPI_BIC_R_IO1	Bidirectional
B6	GPIOR5	BIC_SP1_CS1	Input
B9	GPIOQ1	SPI_BIC_OOB1_MOSI_SIO0	Bidirectional
C5		BIC_FWSPIMOSI	Input
C8		BIC_FWSPIMISO	Input
C9	GPIOQ2	SPI_BIC_OOB1_MISO_SIO1	Bidirectional
D5		BIC_FWSPIDQ3	Input
D8		BIC_FWSPIDQ2	Input
D9	GPIOQ3	SPI_BIC_OOB1_WP_SIO2	Bidirectional
E7		BIC_FWSPICK	Input
F7		BIC_FWSPICS1_N	Input
A2		BMC_HARTBEAT_LED_R	Output
A3		PD_BIC_ENTEST	Test Point
B3		BIC_EXTRST_N	Input
C3		RST_SRST_BMC_B_R1_N	Input
C4		BIC_RSTIND_N_R	Output
D4		CLK_25M_OSC_BIC_CLKIN	Input
M12	GPIOH1	FM_MP_PS_FAIL_N	Input
N12	GPIOH2	H_CPU_MEMTRIP_LVC3_N	Input
P11	GPIOG4	BMC_JTAG_SEL_R	Output
P14	GPIOH3	FM_CPU_BIC_PROCHOT_LVT3_N	Input
R11	GPIOG0	FM_PEHPCPU_INT	Input
R12	GPIOG2	FAST_PROCHOT_N	Input
R13	GPIOG5	H_CPU_ERR0_LVC3_N	Input
R14	GPIOH0	RST_RSMRST_BMC_N	Input

Pin	Function	Signal Name	Port Direction
T12	GPIOG1	FM_BIOS_MRC_DEBUG_MSG_DIS_R	Output
T13	GPIOG3	FM_JTAG_TCK_MUX_SEL_R	Output
T14	GPIOG6	H_CPU_ERR1_LVC3_N	Input
T15	GPIOG7	H_CPU_ERR2_LVC3_N	Input
A14		UART_BIC_R_RXD	Input
A15	GPIOM5	AUTH_PRSENT_N	Input
A16	GPIOM4	AUTH_COMPLETE	Input
B15	GPIOM0	BIC_SECUREBOOT	Input
B16	GPIOL6	BOARD_ID0	Input
C14	GPIOM3	FM_THROTTLE_IN_N	Output
C15	GPIOL5	FM_PVCCIN_CPU0_PWR_IN_ALERT_N	Input
C16	GPIOL4	IRQ_PVCCD_CPU0_VRHOT_LVC3_N	Input
D13		UART_BIC_TXD	Output
D14	GPIOM2	BIC_ESPI_SELECT	Input
D15	GPIOL2		No Connect
D16	GPIOL3	BOARD_ID2	Input
E11	GPIOM1	BOARD_ID3	Input
E12	GPIOL1	UART_HOST_R_TXD	Input
F11	GPIOL7	BOARD_ID1	Input
F12	GPIOL0	UART_HOST_RXD	Output
E4		USB2_BIC_DP	Bidirectional
F4		USB2_BIC_DN	Bidirectional
A1		GND	Power
B7		GND	Power
B8		BIC_SPI_VCC	Power
C6		GND	Power
C7		GND	Power
D6		GND	Power
D7		GND	Power
E10		P3V3_STBY	Power
E5		BIC_USB2A_1V2	Power
E6		GND	Power
E8		P3V3_STBY	Power
E9		P3V3_STBY	Power
F10		P1V2_STBY	Power
F13		P1V8_STBY	Power
F3		GND	Power
F5		BIC_USB2A_3V3	Power

Pin	Function	Signal Name	Port Direction
F6		GND	Power
F8		P1V2_STBY	Power
F9		P1V2_STBY	Power
G10		GND	Power
G11		GND	Power
G12		P3V3_STBY	Power
G13		P1V8_STBY	Power
G3		BIC_VCC_1V2_PLL	Power
G4		P3V3_STBY	Power
G5		P1V2_STBY	Power
G6		GND	Power
G7		GND	Power
G8		GND	Power
G9		GND	Power
H10		GND	Power
H11		GND	Power
H12		P1V2_STBY	Power
H13		PVNN_MAIN_CPU0	Power
H4		P3V3_STBY	Power
H5		P1V2_STBY	Power
H6		GND	Power
H7		GND	Power
H8		GND	Power
H9		GND	Power
J10		GND	Power
J11		GND	Power
J12		P1V2_STBY	Power
J5		BIC_ADCAV33	Power
J6		GND	Power
J7		GND	Power
J8		GND	Power
J9		GND	Power
K10		GND	Power
K11		GND	Power
K12		P1V2_STBY	Power
K13		P3V3_STBY	Power
K5		BIC_ADCAV33	Power
K6		GND	Power

Pin	Function	Signal Name	Port Direction
K7		GND	Power
K8		GND	Power
K9		GND	Power
L10		GND	Power
L11		GND	Power
L12		P3V3_STBY	Power
L13		P3V3_STBY	Power
L5		P3V3_STBY	Power
L6		GND	Power
L7		GND	Power
L8		GND	Power
L9		GND	Power
M10		GND	Power
M11		GND	Power
M6		P1V2_STBY	Power
M7		GND	Power
M8		GND	Power
M9		GND	Power
N10		P3V3_STBY	Power
N13		GND	Power
N7		P3V3_STBY	Power
N8		P1V2_STBY	Power
N9		P1V2_STBY	Power

10.3.7 PCH GPIOs

Table 10-9 lists the GPIO assignments for PCH.

Table 10-9: PCH GPIOs

Pin	Function	Signal Name	Port Direction
BG20	GPPC_A_0_ESPI_ALERT0_N	IRQ_PIRQA_N_ESPI_ALERT0_N	Input
BD15	GPPC_A_1_ESPI_ALERT1_N	ESPI_ALERT1_N_RCIN_N	Input
BD17	GPPC_A_10_SRCCLKREQ_N_0		No Connect
BG18	GPPC_A_11_SRCCLKREQ_N_1		No Connect
BG16	GPPC_A_12_SRCCLKREQ_N_2		No Connect
BF15	GPPC_A_13_SRCCLKREQ_N_3		No Connect
BE12	GPPC_A_14_SRCCLKREQ_N_4		No Connect

Pin	Function	Signal Name	Port Direction
BE14	GPPC_A_15_SRCCLKREQ_N_5		No Connect
BD11	GPPC_A_16_SRCCLKREQ_N_6		No Connect
BF13	GPPC_A_17_SRCCLKREQ_N_7		No Connect
BF11	GPPC_A_18_SRCCLKREQ_N_8		No Connect
BG14	GPPC_A_19_SRCCLKREQ_N_9		No Connect
BG12	GPPC_A_2_ESPI_IO_0	ESPI_IO0_R	Bidirectional
BF19	GPPC_A_3_ESPI_IO_1	ESPI_IO1_R	Bidirectional
BE18	GPPC_A_4_ESPI_IO_2	ESPI_IO2_R	Bidirectional
BD19	GPPC_A_5_ESPI_IO_3	ESPI_IO3_R	Bidirectional
BE20	GPPC_A_6_ESPI_CS0_N	LPC_LFRAME_N_ESPI_CS0_N_R	Output
BE16	GPPC_A_7_ESPI_CS1_N	IRQ_LPC_SERIRQ_ESPI_CS1_N_R	Output
BF17	GPPC_A_8_ESPI_RESET_N	RST_ESPI_RESET_R2_N	Output
BD13	GPPC_A_9_ESPI_CLK	CLK_24M_66M_LPC0_ESPI_R	Output
BD33	GPPC_B_0_GSXDOOUT	TRC_PCH_PTIO_CLK	Output
BE32	GPPC_B_1_GSXSLOAD	TRC_PCH_PTI_0	Output
BG24	GPPC_B_10_USB2_OCB_5	FM_BMC_PCH_SCI_LPC_N	Input
BG22	GPPC_B_11_USB2_OCB_6		No Connect
BD29	GPPC_B_12_HS_UART0_RXD	TRC_PCH_PTI_5	Output
BE28	GPPC_B_13_HS_UART0_TXD	TRC_PCH_PTI_6	Output
BF29	GPPC_B_14_HS_UART0_RTS_N	TRC_PCH_PTI_7	Output
BD27	GPPC_B_15_HS_UART0_CTS_N	BMC_READY_R	Input
BE26	GPPC_B_16_HS_UART1_RXD		No Connect
BF27	GPPC_B_17_HS_UART1_TXD		No Connect
BD25	GPPC_B_18_HS_UART1_RTS_N		No Connect
BF25	GPPC_B_19_HS_UART1_CTS_N	FM_BOARD_REV_ID0	Input
BF33	GPPC_B_2_GSX DIN	TRC_PCH_PTI_1	Output
BE24	GPPC_B_20	FM_BOARD_REV_ID1	Input
BF23	GPPC_B_21	FM_BOARD_REV_ID2	Input
BE22	GPPC_B_22	FM_BOARD_REV_ID3	Input
BD23	GPPC_B_23	FM_THROTTLE_R_IN_N	Input
BD31	GPPC_B_3_GSXRESET_N	TRC_PCH_PTI_2	Output
BE30	GPPC_B_4_GSXCLK	TRC_PCH_PTI_3	Output
BF31	GPPC_B_5_USB2_OCB_0	TRC_PCH_PTI_4	Output
BG32	GPPC_B_6_USB2_OCB_1	FM_OC1_USB_N	Input
BG30	GPPC_B_7_USB2_OCB_2	FM_OC2_USB_N	Input
BG28	GPPC_B_8_USB2_OCB_3	FM_OC_USB_N	Input
BG26	GPPC_B_9_USB2_OCB_4	FM_OC4_USB_N	Input
BC4	GPPC_C_0_ME_SML0CLK	SMB_PCH_SML0_SCL	Input

Pin	Function	Signal Name	Port Direction
BA4	GPPC_C_1_ME_SML0DATA	SMB_PCH_SML0_SDA	Bidirectional
AP3	GPPC_C_10_ME_SML2DATA	SMB_PMBUS_SML2_STBY_LVC3_R2_SDA	Bidirectional
AV3	GPPC_C_11_ME_SML2ALERT_N	FM_PMBUS_ALERT_B_EN_R	Output
AN4	GPPC_C_12_ME_SML3CLK	SMB_PCH_SML3_SCL	Output
AY1	GPPC_C_13_ME_SML3DATA	SMB_PCH_SML3_SDA	Bidirectional
AW2	GPPC_C_14_ME_SML3ALERT_N	FM_THROTTLE_N	Output
BA2	GPPC_C_15_ME_SML4CLK		No Connect
AV1	GPPC_C_16_ME_SML4DATA		No Connect
AL3	GPPC_C_17_ME_SML4ALERT_N	FM_BIOS_POST_CMPLT_N	Output
AL5	GPPC_C_18	FM_ADR_MODE1_R	Output
AL1	GPPC_C_19_MC_SMBCLK		No Connect
AU2	GPPC_C_2_ME_SML0ALERT_N	TP_GPPC_C_2	Test point
AT1	GPPC_C_20_MC_SMBDATA		No Connect
AN2	GPPC_C_21_MC_SMBALERT_N		No Connect
AU4	GPPC_C_3_ME_SML0BDATA		No Connect
BB3	GPPC_C_4_ME_SML0BCLK		No Connect
AT3	GPPC_C_5_ME_SML0BALERT_N		No Connect
AP1	GPPC_C_6_ME_SML1CLK	SMB_PCH_SML1_SCL	Output
AW4	GPPC_C_7_ME_SML1DATA	SMB_PCH_SML1_SDA	Bidirectional
AR4	GPPC_C_8_ME_SML1ALERT_N	IRQ_SML1_PMBUS_ALERT_N	Input
AR2	GPPC_C_9_ME_SML2CLK	SMB_PMBUS_SML2_STBY_LVC3_R2_SCL	Output
AF2	GPP_D_0_HS_SMBCLK_DMA_SMBCLK	SMB_PCH_HS_SML_SCL	Output
AE1	GPP_D_1_HS_SMBDATA_DMA_SMBDATA	SMB_PCH_HS_SML_SDA	Bidirectional
AB2	GPP_D_10_BM_BUSY_N_SX_EXIT_HOLDOFF_N	IRQ_PCH_SCI_WHEA_N	Input
AB4	GPP_D_11_PLTRST_N	RST_PLTRST_N	Output
AH2	GPP_D_12_PCHHOT_N	FM_PCHHOT_R_N	Output
AC1	GPP_D_13_ADR_COMPLETE	FM_ADR_COMPLETE	Output
AH4	GPP_D_14_ADR_TRIGGER_N	FM_ADR_TRIGGER_R_N	Input
AC3	GPP_D_15_VRALERT_N	PU_PCH_VRALERT_N	Input
AD4	GPP_D_16_ADR_ACK	FM_ADR_ACK	Input
Y2	GPP_D_17_THERMTRIP_N	FM_PLT_BMC_THERMTRIP_R_N	Output
AF4	GPP_D_18_MEMTRIP_N	FM_CPU_RMCA_CATERR_DLY_N	Input
Y4	GPP_D_19_MSMT_N	FM_BIOS_IMAGE_SWAP_N	Input
AD2	GPP_D_2_HS_SMBALERT_N_DMA_SMBALERT_N	TP_PCH_GPP_D2	Test point
AG3	GPP_D_20_CATERR_N		No Connect
AA1	GPP_D_21_GLB_RST_WARN_N	FM_PCH_GLB_RST_WARN_N	Output
AA3	GPP_D_22_USB2_OCB_7	TP_GPP_D_22	Test point
W1	GPP_D_23	FM_PCH_BOOT_BIOS_STRAP	Input

Pin	Function	Signal Name	Port Direction
AJ1	GPP_D_6	FM_FLASH_SECURITY_STRAP	Input
AG1	GPP_D_7	FM_ESPI_FLASH_MODE	Input
AE3	GPP_D_8_CRASHLOG_TRIG_N	FM_PCH_CRASHLOG_TRIG_N	Input
AJ3	GPP_D_9_PME_N	FM_LPC_PME_N	Input
BA26	GPP_E_0_SATA1_XPCIE_0		No Connect
BA23	GPP_E_1_SATA1_XPCIE_1		No Connect
AV31	GPP_E_10_SATA0_SDATAOUT_SATA0_GP		No Connect
AV34	GPP_E_11_SATA1_SCLOCK_SATA1_LED_N	TP_GPP_E_11	Test point
BB28	GPP_E_12_SATA1_SLOAD_SATA1_GP	TP_GPP_E_12	Test point
BA32	GPP_E_13_SATA1_SDATAOUT_SATA1_DEVSLEP	TP_GPP_E_13	Test point
BB34	GPP_E_14_SATA2_SCLOCK_SATA2_LED_N		No Connect
AW20	GPP_E_15_SATA2_SLOAD_SATA2_GP	IRQ_BMC_PCH_SMI_LPC_N	Input
AW29	GPP_E_16_SATA2_SDATAOUT_SATA2_DEVSLEP	IRQ_BMC_PCH_NMI	Input
BA36	GPP_E_17_ERR0_N		No Connect
BA20	GPP_E_18_ERR1_N	FM_PS_PWROK_DLY_R_SEL	Output
BB31	GPP_E_19_ERR2_N	FM_TPM_MOD_PRESENCE_N	Input
AW23	GPP_E_2_SATA1_XPCIE_2		No Connect
BB21	GPP_E_3_SATA1_XPCIE_3		No Connect
AV24	GPP_E_4_SATA0_XPCIE_2		No Connect
AV28	GPP_E_5_SATA0_XPCIE_3		No Connect
BB24	GPP_E_6_SATA0_USB3_XPCIE_0		No Connect
AW32	GPP_E_7_SATA0_USB3_XPCIE_1		No Connect
AW36	GPP_E_8_SATA0_SCLOCK_SATA0_LED_N		No Connect
BA29	GPP_E_9_SATA0_SLOAD_SATA0_DEVSLEP		No Connect
G4	GPPC_H_0	FM_PCH_VISA_DEFAULT	Input
K1	GPPC_H_1	FM_PCH_IO_EXPANDER	Input
J2	GPPC_H_15_FLEX_CLK_OUT_0	FM_BIOS_MRC_DEBUG_MSG_DIS	Input
G2	GPPC_H_16_FLEX_CLK_OUT_1	TP_PCH_RSVD_G2	Input
H3	GPPC_H_17_FLEX_CLK_OUT_2	TP_PCH_RSVD_H3	Input
J4	GPPC_H_18_PMCALERT_N		Input
L4	GPPC_H_19	FM_PCH_RSVD_L4	Input
L2	GPPC_H_6	FM_PCH_EXTERNALCLKMODE	Input
K3	GPPC_H_7	TP_PCH_RSVD_K3	Input
U3	GPP_I_12_HDA_BCLK		No Connect
N2	GPP_I_13_HDA_RST_N		No Connect
P1	GPP_I_14_HDA_SYNC		No Connect
R2	GPP_I_15_HDA_SDO		No Connect
U1	GPP_I_16_HDA_SDI_0		No Connect

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Pin	Function	Signal Name	Port Direction
V4	GPP_I_17_HDA_SDI_1		No Connect
N4	GPP_I_21	IRQ_TPM_SPI_N	Input
P3	GPP_I_22	FM_PCH_RSVD_P3	Input
R4	GPP_I_23	FM_PCH_RSVD_R4	Input
F3	CPU_THRMTRIP_N	H_THERMTRIP_LVC1_N	Input
G10	CPUPWRGD	PWRGD_CPUPWRGD_GTL	Output
M8	PLTRST_CPU_N	TP_PCH_PLTRST_CPU_N	Test point
H11	TRIGGER0_N	TP_PCH_TRIGGER0_R_N	Test point
K8	TRIGGER1_N	TP_PCH_TRIGGER1_R_N	Test point
F5	CPU_PWR_DEBUG_N	FM_PCH_CPU_PWR_DEBUG_N	Output
E4	CPU_MEMTRIP_N	TP_PCH_FM_CPU_MEMTRIP_N	Test point
F11	CPU_MSMI_N	TP_PCH_CPU_MSMI_N	Test point
J10	ME_PECI	PECI_PCH	Bidirectional
J7	CPU_ERR0_N	FM_CPU_ERR0_PCH_N	Input
G7	CPU_ERR1_N	FM_CPU_ERR1_PCH_N	Input
L7	CPU_ERR2_N	FM_CPU_ERR2_PCH_N	Input
F8	CPU_CATERR_N	TP_PCH_CPU_CATERR_N	Test point
AF8	GPP_L_0_PM_SYNC_0	H_CPU_PMSYNC_PCH_R	Output
AE7	GPP_L_1_PM_DOWN_0	H_CPU_PMDOWN_PCH	Input
AC10	GPP_L_2	FM_BIOS_USB_RECOVERY	Input
AF11	GPP_L_3	FM_BIOS_ADV_FUNCTIONS	Input
AG7	GPP_L_4	FM_ME_RCVR_N	Input
AB8	GPP_L_5	FM_PASSWORD_CLEAR_N	Input
AG10	GPP_L_6	FM_MFG_MODE	Input
AC7	GPP_L_7	TP_PCH_GPP_L_7	Test point
AE10	GPP_L_8	TP_PCH_GPP_L_8	Test point
N7	GPP_M_0		No Connect
AA13	GPP_M_1		No Connect
R7	GPP_M_11	FM_PCH_BIOS_RCVR_MODE	Test point
U7	GPP_M_12	TP_PCH_GPP_M_12	Test point
T8	GPP_M_15	TP_PCH_GPP_M_15	Test point
N10	GPP_M_16		No Connect
W13	GPP_M_17		No Connect
AA7	GPP_M_2		No Connect
AA10	GPP_M_3		No Connect
W7	GPP_M_4		No Connect
V8	GPP_M_5		No Connect
R10	GPP_M_6		No Connect

Pin	Function	Signal Name	Port Direction
AB11	GPP_M_7		No Connect
W10	GPP_M_8		No Connect
T11	GPP_N_1	TP_PCH_GPP_N_1	Test point
V11	GPP_N_4	TP_PCH_GPP_N_4	Test point
BB18	GPPC_S_0_TIME_SYNC_0	PD_XTAL_INPUT_FREQUENCY_0	Input
AU16	GPPC_S_1_SPKR_TIME_SYNC_1	FM_NO_REBOOT_SPKR	Input
AW10	GPPC_S_10	FM_JTAG_ODT_DISABLE	Input
BB8	GPPC_S_11	FM_ESPI_CS_SWIZZLE	Input
AR16	GPPC_S_2_CPU_GP_0	PD_XTAL_INPUT_FREQUENCY_1	Input
AV11	GPPC_S_3_CPU_GP_1	FM_ADR_MODE0_R	Output
AU13	GPPC_S_4_CPU_GP_2	FM_SPI_3P3_1P8_VOLTAGE	Input
AT18	GPPC_S_5_CPU_GP_3	FM_PCH_CONSENT_STRAP_N	Input
AR13	GPPC_S_6_SUSWARN_N_SUSPWRDNACK	FM_EUP_LOT6_N	Output
BA7	GPPC_S_7_SUSACK_N	FM_SUSACK_R_N	Input
AP15	GPPC_S_8_NMI_N	IRQ_PCH_CPU_NMI_EVENT_R_N	Output
AV18	GPPC_S_9_SMI_N	IRQ_SMI_ACTIVE_N	Output
AN10	GPP_O_0	FM_PCH_SPARE0	Input
AU10	GPP_O_7	TP_PCH_RSVD_AU10	Input
AN7	ACPRESENT	PU_ACPRESENT	Input
BE40	DBG_PMODE	PCH_XDP_ITP_PMODE	Output
BE8	DSW_PWROK	PWRGD_DSW_PWROK	Input
BG8	INTRUDER_N	FM_INTRUDER_HDR_PCH_N	Input
BF35	JTAG_TCK	JTAG_DBP_PCH_TCK	Input
BE38	JTAG_TDI	JTAG_DBP_TDI_PCH	Bidirectional
BE36	JTAG_TDO	JTAG_DBP_TDO_PCH	Bidirectional
BD37	JTAG_TMS	JTAG_DBP_TMS_PCH	Bidirectional
BD35	JTAGX	JTAG_DBP_CPU_GTL_TCK	Output
AU7	LAN_WAKE_N	LAN_WAKE	Input
AJ7	LANPHYPC		No Connect
BG3	NC_CGC_DUT_DETECT_N	TP_PCH_CGC_DUT_DETECTED	Test point
BE4	PCH_PWROK	PWRGD_PCH_PWROK	Input
BB37	PRDY_N	PCH_XDP_PRDY_N	Input
BF37	PREQ_N	PCH_XDP_PREQ_N	Output
AR10	PWRBTN_N	SYS_PWRBTN_N	Input
BD7	RCTRST_N	RST_RTRCRST_N	Input
BD9	RSMRST_N	RST_RSMRST_N	Input
AV21	RSVD		Reserved
AW26	RSVD		Reserved

Pin	Function	Signal Name	Port Direction
BF39	RSVD		Reserved
BG36	RSVD		Reserved
AM11	SLP_A_N	PCH_SLPSA_N	Test point
AK8	SLP_LAN_N	SLP_LAN_N	Input
AP8	SLP_S3_N	FM_SLPS3_N	Output
AL13	SLP_S4_N	FM_SLPS4_N	Output
AJ13	SLP_S5_N	PCH_SLPS5_N	Test point
AL7	SLP_SUS_N	FM_SLP_SUS_N	Output
BB15	SPI0_CLK	QSPI1_R_CLK	Output
AW13	SPI0_FLASH_0_CS_N	SPI_PCH_CS0_N	Output
BA10	SPI0_FLASH_1_CS_N	SPI_PCH_CS1_N	Output
AV15	SPI0_IO_2	SPI_PCH_IO2	Bidirectional
BA16	SPI0_IO_3	SPI_PCH_IO3	Bidirectional
BA13	SPI0_MOSI_IO_0	SPI_PCH_IO0	Bidirectional
AW16	SPI0_MISO_IO_1	SPI_PCH_IO1	Bidirectional
BB11	SPI0_TPM_CS_N	SPI_PCH_TPM_CS_N	Output
BF9	SRTCST_N	RST_SRTCST_N	Input
AR7	SUSCLK	PD_SUSCLK	Input
AL10	SYS_PWROK	PWRGD_SYS_PWROK	Input
AJ10	SYS_RESET_N	RST_BMC_RSTBTN_OUT_N	Input
AH11	WAKE_N	IRQ_LVC3_WAKE_N	Input

11 Mechanical

11.1 Mechanical Outline

Crater Lake 10U blade form factors as shown in Figure 11-1, Crater Lake server board dimensions are shown in Figure 11-2. The overall dimensions of the server card is 321.4mm x 157.0mm. The blade length measured from front panel to rear surface of the power connector is 534.12mm, blade width is 164.0mm, and front panel height (not including EMI gasket) is 40.8mm.

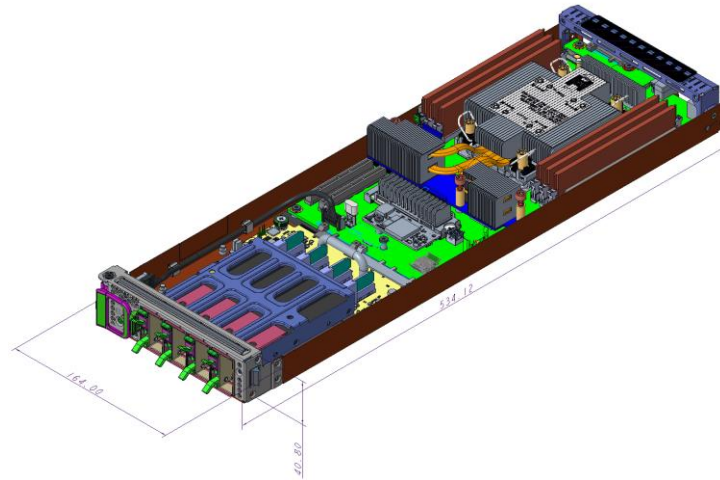


Figure 11-1: Yosemite V3.5, 1U Crater Lake, 10U Blade Form Factor

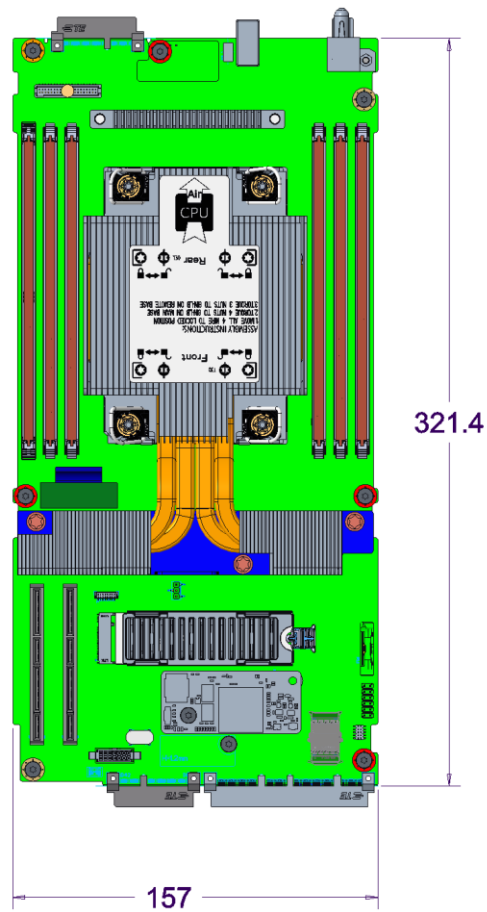


Figure 11-2: Yosemite V3.5, Crater Lake Server Board Dimension

The front of the Crater Lake blade receives the expansion module. The expansion card is defined in the OCP Yosemite V3.5 Expansion Card Specification. An example of an expansion card can be seen in Figure 11-3. In this example the expansion card serves 4x E1.S 25mm, and the blade sheet metal is also modified with E1.S slots.

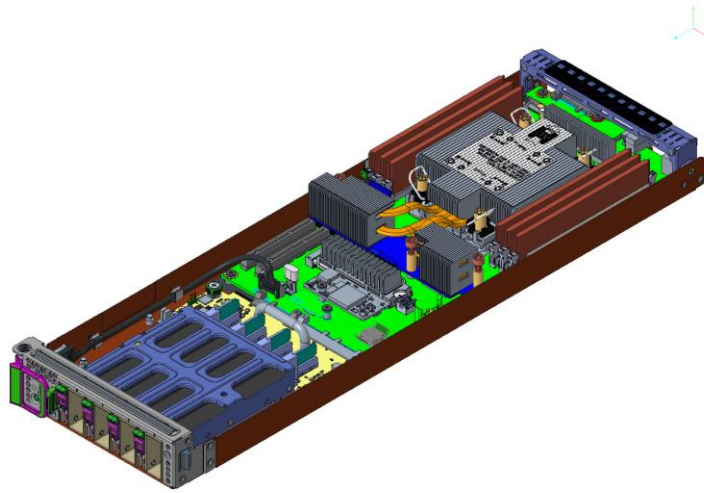


Figure 11-3: Yosemite V3.5, Crater Lake with 1OU Expansion Card for Reference

11.2 Platform Design

Platform design details are not discussed in this specification. Refer to the OCP Yosemite V3.5 Platform Design Specification for more detail.

12 Onboard Power System

12.1 Input Voltage Level

The expected nominal input voltage delivered by the Yosemite V3.5's power delivery subsystem is 12.5VDC; however, the rail has a varying range of 11.5V to 13.5V. The Crater Lake 1S server shall accept and operate normally with an input voltage range of 12.5V +/- 7%.

12.2 1S Server Power Budget (Preliminary)

The total power budget of the Crater Lake 1S Server shall not exceed the Yosemite V3.5's platform power budget that is to be allocated to each server blade. The max power budget design specs are listed below:

Server Board				
Component	Power (W)	Efficiency	Quantity	Total
CPU	165	0.9	1	165
PCH	19	0.9	1	20.9
DDR5 DIMMs	8.78	0.9	6	57.948
Boot M.2	8.25	0.9	1	9.075
CPLD	3.5	0.9	1	3.85
BIC	4.5	0.9	1	4.95
Misc	10	0.9	1	11
Total				288.723
1U Expansion				
4C+ Connector	72	1	1	72
2C Connector	72	1	1	72
Total				144
2U Expansion				
Riser Connector	150	1	2	300
Total				300
Blade Total				727.723

The Crater Lake board supports server throttle through prochot logic to ensure system workloads do not overstress the power distribution component and trigger fault conditions. To enable the above power budget, the power throttle levels on the server will be set to levels specified in Table 12-1 and Table 12-2. The TDP throttle thresholds are programmable, and all throttle thresholds are selectable by BMC between 1U and 2U configs.

To maximize transient power budget, the server implements 3 types of power limiting prochot triggers:

1. OC_Warning: Triggered by average power exceeding system TDP limits
2. HSC_Timer: Tied to Hot swap over current protection, but triggers before the overcurrent (OCP) timer expires (2ms).
3. Fast prochot: Triggers when system's instantaneous power (<20us time window) exceeds design limits, before severe OCP protection meant for short circuit protection can trigger.

Table 12-1: Power throttle thresholds for 1U config

Purpose	Throttle protection	Design value (A)	Min Time window	Calculation
Ensure protection of input cable, rack power budget and make sure no defective components run continuously	HSC generated OC_warning	35	>20ms	Current: min (120% of system TDP, rack power allocation, cable limits, thermal limits for system) Time: min (max averaging capability of HSC, TDP tau)
Ensure peak current due to soft short failure conditions or component failure trigger throttle before shutting down server	HSC generated HSC_TIMER	40A	>2ms	min (120% of system TDP with CPU in turbo assuming components in PI2=1.5x TDP, rack peak power, SOA permitted by hotswap)
Ensure Power virus conditions throttle system before shutting down server through fast OCP	Fast prohot	50.05A	<20us	Min (80% of Severe OCP, 120%*Pmax on all system components)

Table 12-2: Power throttle thresholds for 2U config

Purpose	Throttle protection	Design value	Min Time window	Calculation
Ensure protection of input cable, rack power budget and make sure no defective components run continuously	HSC generated OC_warning	50	>20ms	Current: min (120% of system TDP, rack power allocation, cable limits, thermal limits for system) Time: min (max averaging capability of HSC, TDP tau)
Ensure peak current due to soft short failure conditions or component failure trigger throttle before shutting down server	HSC generated HSC_TIMER	70A	>2ms	min (120% of system TDP with CPU in turbo assuming components in PI2=1.5x TDP, rack peak power, SOA permitted by hotswap)
Ensure Power virus conditions throttle system before shutting down server through fast OCP	Fast prohot	84.89A	<20us	Min (80% of Severe OCP, 120%*Pmax on all system components)

The Crater Lake hot swap controller is used to protect the upstream power distribution components from catastrophic faults, by triggering system power off for overcurrent conditions. System workloads are not expected to trigger these faults, throttle signaling is expected to bring down system power before fault conditions are reached. Details can be found in Table 12-3 and Table 12-4.

Table 12-3: Fault thresholds for 1U configs

HW protection	Design value (A)	Time window	Calculation
OCP fault	40A	>4ms	min (120% of system TDP with CPU in turbo assuming PI2=1.5x TDP, rack peak power, SOA permitted by hotswap)
Sever OCP fault	90A	100ns	Options fixed by HSC, select by checking voltage drop for SCP condition on neighboring blade
Sled OCP fault	62A	>4ms	min (120% of system TDP with CPU in turbo assuming PI2=1.5x TDP, rack peak power, SOA permitted by hotswap)

Table 12-4: Fault thresholds for 2U config

HW protection	Design value (A)	Time window	Calculation
OCP fault	70A	>4ms	min (110% of system TDP with CPU in turbo assuming PI2=1.5x TDP, rack peak power, SOA permitted by hotswap)
Severe OCP fault	157.5A	100ns	Options fixed by HSC, select by checking voltage drop for SCP condition on neighboring blade
Sled OCP fault	62A	>4ms	min (120% of system TDP with CPU in turbo assuming PI2=1.5x TDP, rack peak power, SOA permitted by hotswap)

12.2.1 Expansion System Power Design Consideration (WIP)

Each of the Front expansion connectors are expected to carry up to 6A and the Riser connectors for 2U expansion can carry up to 18A.

As shown in section 6.1, the Crater Lake 1S Server shall support various expansion configurations and blade chassis sizes to accommodate various future use cases. However, the expansion subsystem must adhere to specific power design requirements:

1. The sustained current draw from the front expansion shall be at most 15A (1 connector) while the 2U expansion board must be limited to 25A (2 connectors)

2. Although the power budget may allow for high power commodities, feasibility is determined by whether the cooling solution implemented is adequate and does not introduce long term reliability degradation of the hardware

Note: Detailed design requirements for server expansion use cases is defined in the separate Crater Lake 1S Server Expansion Design Specification, please refer to the corresponding document for additional guidelines that may apply.

12.3 Capacitive Load

The capacitance on the input 12V power rail for Crater Lake 1S Server shall be optimized to meet the system's power supply requirements and does not cause instability. In addition, the Crater Lake 1S Server shall be designed such that it adheres to the maximum capacitive load allowable as defined in the Yosemite V3.5 Platform Design Specification document.

12.4 Hot Swap Controller Circuit

Crater Lake 1S Server shall implement a dedicated HSC which is expected to support the following:

1. In-rush current control when motherboard is inserted and powered up
2. MOSFETs must be kept within safe operating area during all operational conditions such as power on/off and fault conditions
3. Signals that indicate power status, alerts, interrupts are expected to allow rapid response upon impending fault conditions and/or warnings
4. Current limit protection for over current and short circuit whereby overcurrent threshold should be configured to TBD without 2U expansion (TBD with 2U expansion)
5. Undervoltage and overvoltage protection shall be configured to 10.1 V and 14.3 V respectively
6. Default HSC response for fault conditions shall be latch off with retry as stuff option
7. PMBus interface that supports the following features:
 - a. Report voltage, current, and power (VIP) telemetry with accuracy of +/- 2.0% or better when operating above 10% of the maximum range
 - b. Status registers that allow the definition of upper and lower critical thresholds for VIP of which are logged upon being triggered
8. Implements a fast (<20us) overcurrent monitoring scheme that generates an alert based on a remotely selectable threshold that triggers system throttling (Fast PROCHOT#) either using the HSC itself or external circuits. The recommended threshold for Fast PROCHOT# shall be lower than the severe overcurrent limit such that there is no tolerance overlap.
 - a. Special consideration shall be taken to ensure that CPU performance is not impacted during extended peak power excursions; thus, sophisticated filter may be necessary to avoid pre-emptive throttling during such peak power events.
9. Average current limit (measured for 20ms window) protection is implemented by configuring one of the HSC Alert GPIO pins to trigger based on the programmed Overcurrent (OC) warning threshold. This is also routed to the PROCHOT logic to throttle the system if OC warn threshold is exceeded.

The voltage drop on the HSC current-sense resistor should be less than or equal to 25mV at full loading.

The power reporting of the HSC must be better than 2%, from 25W to full loading at room temperature. Further optimizations to power telemetry accuracy shall be performed through

firmware based on characterized results from multiple boards based on entire load range and operating temperature requirements.

12.5 Power Sequence and Standby Power

Since the Crater Lake 1S Server relies on a single input power source from the Yosemite V3.5, there is no power sequence requirement from the platform perspective. The PCH will also require certain standby power rails to allow for certain operations and functions. Design must avoid any leakage paths among different power subsystems (e.g. Yosemite V3.5 platform, 1S Crater Lake Server, and expansion cards).

The 3.3V is also used to power the M.2 boot drive on the Crater Lake board. The M.2 slots is power through load switches that can be controlled out of band as a method of fault remediation.

12.6 VR design and Efficiency

Crater lake utilizes universal VR controller and power stage footprints. Power VR configurations can be seed in Table 12-5.

Table 12-5: Power VR controller configuration

	Power rail	Controller	Power Stage
CPU	PVCCIN_CPU0	ISL69260/ XDPE15284D/ TPS53689	RAA221491/ TDA21590/ CSD95410
	PVCCFA_EHV_FIVRA_CP U0		RAA221340/ TDA21535/ CSD95420
	PVCCINFAON_CPU0	ISL69260/XDPE15284D/TPS536 89	RAA221340/ TDA21535/ CSD95420
	PVCCFA_EHV_CPU0		RAA221320/TDA21520/CSD954 20
	PVCCD_HV_CPU	ISL69260/XDPE15284D/TPS536 89	RAA221340/TDA21535/CSD954 20

High efficiency Voltage Regulators (VR) shall be used on Crater Lake 1S Server with at least 91% efficiency over the 30% to 90% load range. If higher efficiency VRs are available at additional cost and/or design complexity, the vendor should present the tradeoffs before implementation.

12.7 Power Reading and Capping

The Crater Lake 1S Server is responsible for actively monitoring its own power consumption through the HSC. Like the last generation of 1S Server design Delta Lake, the PCH is responsible for the calculation of a one second average based on the samples and report it upstream to the Bridge IC which is later polled by the BMC.

The Crater Lake 1S Server must have the ability to rapidly throttle itself to the lowest possible power state when the platform asserts the PRIMARY_THROTTLE signal, receives a request directly from the BMC, or power event reported by on-board power monitor.

A preferred power-capping implementation is to reduce the 1S server's power consumption gradually with fine-grained power control by steps as small as 5 watts and to reach the control target power limit within 3 seconds. This process shall be smooth but fast, and the settled power value shall be within -3% of the target power limit set by the platform.

The server card will also have circuit to generate a POWER_FAIL_N signal to inform the 1S server that the 12V input power to the server is going to be cut off in certain amount of time (which is pre-defined by the platform). The 1S server can leverage this signal to develop mechanisms to protect critical data prior to a power outage.

12.8 Configuration Support

The platform design supports up to 165W CPUs and multiple memory configurations. While the board layout supports the highest power config, the design implements 2 BOM configurations, shown in Table 12-6, one optimized for the lower power CPU + DIMMs and 2nd one supporting maximum power CPU.

Table 12-6: CPU and DIMM config for Crater Lake

BOM config	CPU	DIMM config
1	Sapphire Rapids MCC	Four 16GB DIMMs for 64GB total
2	Sapphire Rapids MCC	Six 16GB DIMMs (or potentially 4 DIMMs and CXL expansion) for 96GB total

13 Environmental Requirements

The full system with the server card installed meets the following environmental requirements:

- Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C (long-term storage) *
- Transportation temperature range: -40°C to +70°C (short-term storage) *

- Operating altitude with no de-rating to 6000 ft

13.1 Vibration and Shock

The motherboard meets shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) and IEC721-3-(*) Standard & Levels. Details can be seen in Table 13-1.

Table 13-1: Vibration and Shock Requirements

	Operating	Non-Operating
Vibration	0.3G, 5 to 500 to 5 Hz per sweep, 10 sweeps at 1 octave/minute, test along three axes 5-20Hz – 6db/Oct 20-200Hz – 0.0003 G ² /Hz 200-500 – -6db/Oct	1G, 5 to 500 to 5 Hz per sweep, 10 sweeps at 1 octave/minute, test along three axes
Shock	6G, half sine, 11ms, 5 shocks, test along three axes	12G, half sine, 11ms, 10 shocks, test along three axes

14 Prescribed Materials

14.1 Disallowed Components

The following components are not used in the design of the motherboard:

- Components disallowed by the European Union's Restriction of Hazardous Substances Directive, **RoHS 2 Directive (2011/65/EU)**
- Trimmers and/or potentiometers
- Dip switches

14.2 Capacitors and Inductors

The following limitations apply to the use of capacitors:

- Only aluminum organic polymer capacitors made by high-quality manufacturers are used; they must be rated 105°C.
- All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under the worst conditions.
- Tantalum capacitors using manganese dioxide cathodes are forbidden.
- SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 are still allowed when installed far from the PCB edge and with a correct orientation that minimizes the risk of cracking).

- X7R ceramic material for SMT capacitors should be used by default and at minimum X6S for portions of design subject to thermal hotspots such as CPU and/or DIMM cavities.
- COG or NP0 type should be used for tolerance sensitive portions of design
- Conditional usage of X5R ceramic material must be based on evaluation of worst-case thermal conditions and upon approval from Facebook

The following limitations apply to the use of inductors:

- Only SMT inductors may be used as the use of through-hole inductors is disallowed

14.3 Component De-rating

For inductors, capacitors, and FETs, derating analysis is based on at least 20% derating.

15 System Firmware (BIOS)

The card supplier is responsible for supplying and customizing the BIOS for the CPU. The requirements are outlined in this section.

15.1 Specification Compliance

- The system BIOS needs to comply with the following specification:
- UEFI Specification version 2.6
- ACPI Specification version 6.2
- SMBIOS Specification version 3.1.1

15.2 Configuration and Features

The BIOS is tuned to minimize card power consumption. It has the following features:

- Disables unused devices, including PCIe lanes, USB ports, SATA/SAS ports, etc.
- A BIOS setup menu
- The CPU settings can be tuned to achieve the optimal combination of performance and power consumption

15.3 BIOS Settings Tools

The card supplier shall provide a tool to make BIOS setting changes without requiring a BIOS re-flash. The BIOS settings update tool must also support success and failure codes so that updates can be easily scripted.

This tool has to be compatible in a Linux OS environment.

15.4 PXE Boot

The BIOS supports PXE boot and provides the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first available Ethernet device.

The default boot device priority is:

1. Network (search all configured network interfaces)
2. HDD, SSD, or flash device (local or remote)
3. CD-ROM
4. Removable Device

This process loops indefinitely and requires no user intervention.

15.5 iSCSI Boot

The BIOS shall be capable of iSCSI network boot.

15.6 BIOS Update

The BIOS can be updated from the OS under these scenarios:

- Scenario 1: Sample/Audit BIOS settings
 - Return current BIOS settings, or
 - Save/export BIOS settings in a human-readable form that can be restored/imported (as in Scenario 2)
- Scenario 2: Update BIOS with pre-configured set of BIOS settings
 - Update/change multiple BIOS settings
 - Reboot
- Scenario 3: BIOS/firmware update with a new revision
 - Load new BIOS/firmware on machine and update, retain the current BIOS settings
 - Reboot
 - BIOS needs to support both vendor proprietary upgrade tool and EFI capsule loader to upgrade BIOS image.

Additionally, the update tools have the following capabilities:

- Update from the operating system.
- Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
- No user interaction (such as prompts)

- BIOS updates and option changes do not take longer than fifteen minutes to complete

15.7 Remote BIOS Update

The BIOS can be updated remotely under these scenarios:

- Scenario 1: Sample/Audit BIOS settings
 - Return current BIOS settings, or
 - Save/export BIOS settings in a human-readable form that can be restored/imported (as in Scenario 2)
- Scenario 2: Update BIOS with a pre-configured set of BIOS settings
 - Update/change multiple BIOS settings
 - Reboot
- Scenario 3: BIOS/firmware update with a new revision
 - Load new BIOS/firmware on machine and update, retain the current BIOS settings
 - Reboot

Additionally, the update tools have the following capabilities:

- Update from the remote host over the LAN connection to BMC
- Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
- No user interaction (like prompts)
- BIOS updates and option changes do not take longer than 20 minutes to complete
- Can be scripted and propagated to multiple machines

15.8 SMBIOS Event Log

Per the SMBIOS specification Version 2.6, the BIOS implements SMBIOS Type 15 for an event log and the assigned area is large enough to hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB) and follows the SMBIOS event log organization format for the event log.

A system access interface and application software must be provided to retrieve and clear the event log from the BIOS, including, at minimum, a Linux application for the CentOS operating system and driver as needed. The event log must be retrieved and stored as a readable text file that is easy to handle by a scripting language under Linux. Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID.

15.9 Logged Errors

The following list of errors is logged by the BIOS or Bridge IC. These errors must include the date, time, and location information so that failing components can be easily identified.

- CPU/Memory errors: Both correctable ECC and uncorrectable ECC errors are logged into the event log. Error categories include DRAM, Link, and others.
- PCIe* errors: Any errors that have a status register are logged into the event log, including root complex, endpoint device, and any switch upstream/downstream ports if available. Link disable on errors are also be logged. Fatal, non-fatal, or correctable error classification follows the chipset vendor's recommendation.
- POST errors: All POST errors detected by the BIOS during POST are logged into the event log.
- System reboot events
- Sensor values exceeding warning or critical thresholds
- Power-startup sequencing failure events

The System Event Log (SEL) format and decoding scheme need to comply with the Facebook Unified SEL Format.

16 Error Thresholds

An error threshold setting must be enabled for both correctable and uncorrectable errors. Once the programmed threshold is reached, an event is triggered and logged.

- Memory Correctable ECC: The threshold default value is 1,000. When the threshold is reached, the BIOS logs the event and includes the physical DIMM location.

16.1 POST Codes

The BIOS outputs a set of Power-On Self-Test (POST) codes identifying the current initialization step and any errors encountered along the initialization. The output is provided on the serial console and errors are logged.

Errors in POST need to be sent to BMC in the form of SEL.

During the boot sequence, the BIOS shall initialize and test each DIMM module. If a module fails initialization or does not pass the BIOS test, the following POST Codes should indicate which DIMM has failed:

- The first hex character indicates which CPU interfaces the DIMM module. Since there is only one CPU, this will always be "0"
- The second hex character indicates the number of the DIMM module.
- The POST Code will also display both the error major code and minor code from the memory reference code.
- The display sequence will be "00", DIMM location, Major code and Minor code with a one second delay for every code displayed.
- The BIOS shall repeat the display sequence indefinitely to allow time for a technician to service the system.

16.2 HOTPLUG support for PCIe devices

The system (board, BIOS, and management devices) need to be configured to allow PCIe hotplug and surprise removal. Expected uses of this functionality include:

- Expansion boards with E1.S drives that will be hotplugged. Typically this will be an expected and managed event. Since the drives will be front accessible a mis-service is possible (e.g. tech pulling the wrong drive) so support for surprise removal is also needed.
- The Multihost NIC on the baseboard is typically not hotplugged but is physically capable. Surprise removal is also needed to prevent a system crash if it the wrong NIC is inadvertently removed.
- Expansion designs with PCIe endpoint-based accelerators that can be individually power cycled. This should be possible without impacting the full system.

16.3 Latency for SMI Error Handling

It is expected that the error handling of SMI should have latency no more than 20mS. It is expected that this implementation is done using unified SEL for Error/Fault report.

16.4 Support of AC Cycling of PCIe Devices

In the event of device error for PCIe devices in the expansion systems (like accelerators for example), there exists a mechanism to power cycle these PCIe devices connected using the register in PCIe config space. This mechanism would need to be made working with devices connecting directly to the Root Complex (CPU) or the PCIe switch. The procedure would generally involve control of GPIOs upon toggling the register. This GPIO could be on the PCIe switch or a CPLD connecting to the reset, power and clock control to the device. It should be noted that for the case where a PCIe switch is not involved, this may involve the following:

- CPU to issue a I2C command thru its Hot Plug SMBUS controller to server board CPLD
- Server CPLD to relay this event to the server BIC either thru interrupt, or BIC polling.
- Server BIC to transfer this information to the expansion board BIC
- Expansion board BIC to sequence the control of power/reset to the relevant device with the expansion board CPLD as a logic gate.

There should be logging of such events when they happen. And there would also be “3-tries” mechanism to try to recover the erratic device in such a manner before the system gives up.

17 Hardware Management

The primary server management functions will be provided using a BMC on the platform. The BMC on the platform uses an I3C bus as the management interface. This section identifies the required information that must be accessible from the BMC.

17.1 Overview

Figure 17-1 and Figure 17-2 give an overview of Crater Lake 1S CPU server management scheme.

There are 2x classes of use cases.

Class 1 use case is with multi-host NIC shared by 1S server cards. In this use case, 1S CPU card interfaces baseboard to the left of the diagram below, and an optional 1U front expansion card to the right of the diagram below.

Baseboard has below major components:

- Multi-host NIC
- BMC
- CPLD for glue logic, power sequence
- Front I/O

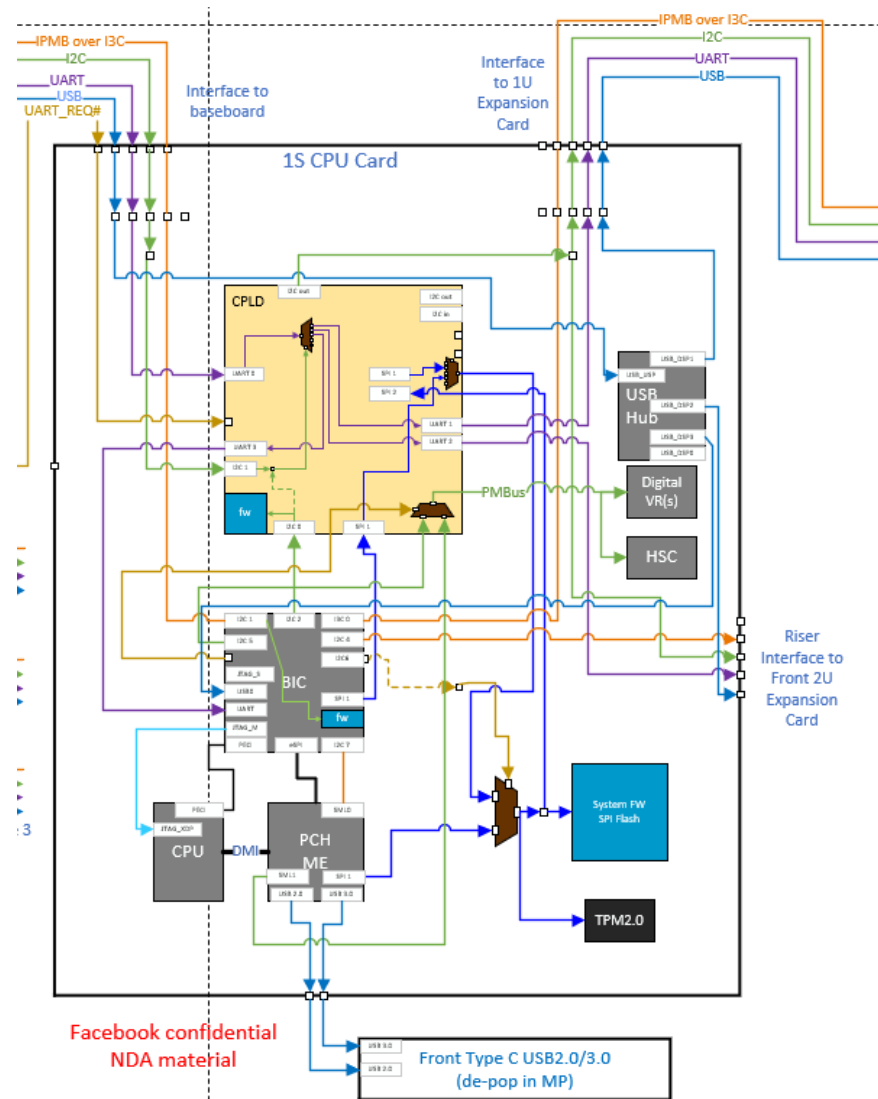


Figure 17-1: Class 1 Server management

Class 2 use case has each 1S server card with single host NIC and its own BMC. In this use case, 1S CPU card interfaces baseboard to the left of the diagram below. On the right side, the 1S CPU card interface with 1) a NIC expansion card 2) a 2U front expansion card through a riser. Note Class 1 is the primary use case for Crater Lake, but appropriate design provisions should be included to support class 2 operation if needed.

Base board has below major components:

- CPLD for glue logic, power sequence
- A bridge IC
- Front I/O

NIC expansion card has below major components:

- A single host NIC
- BMC
- CPLD (Glue logic, power sequence)

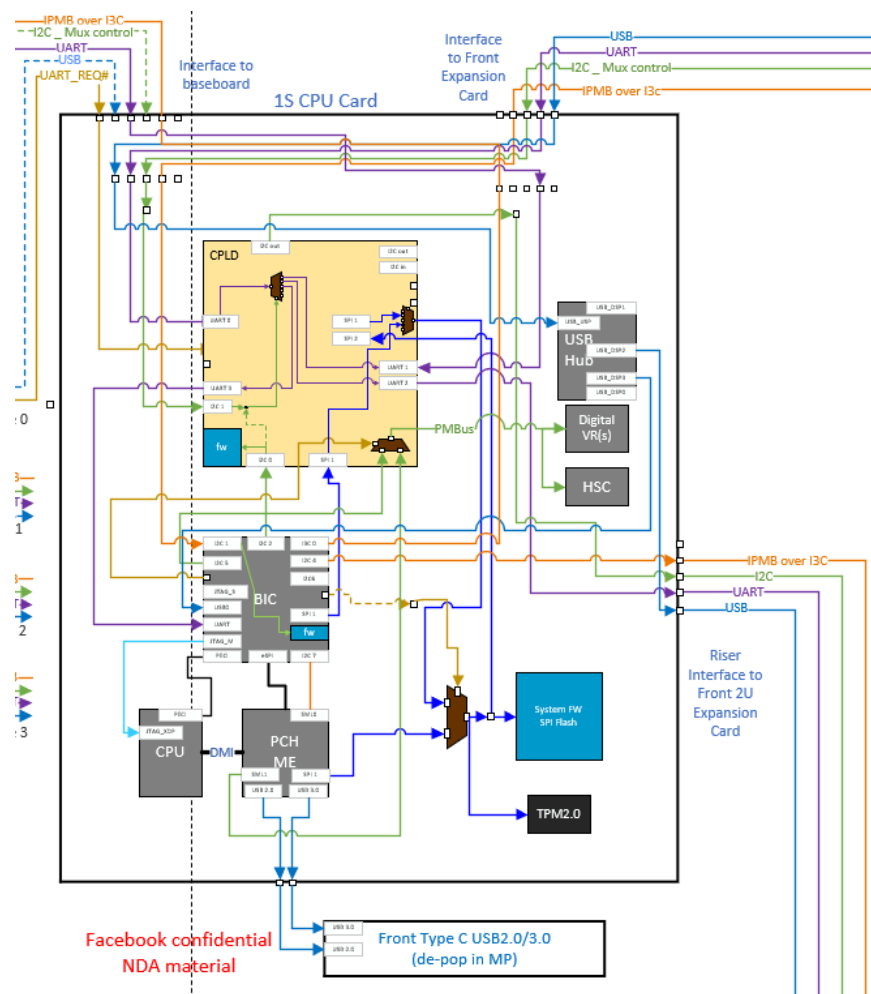


Figure 17-2: Class 2 server management

17.2 Bridge IC

The Crater Lake 1S server uses a Bridge IC, defined as the bridging device between the PCH and the BMC. The Bridge IC is on stand-by power so that it can be accessed by the BMC when the SoC is powered down.

On the platform side, the BMC and Bridge IC communicate with each other with IPMI messages and DMTF MCTP transactions over the I³C bus. To enable prompt communication, this I³C bus shall be a point-to-point link without any other devices on the same bus. The targeted speed of the I³C interface is 12.5 MHz bitrate (11 Mbps) .

On the 1S server side, the Bridge IC has FRU EEPROM and thermal sensors on a local I²C bus. The BMC can communicate with the Bridge IC to inquire the FRU and thermal data through the Intelligent Platform Management Bus (IPMB) or DMTF MCTP transactions. The FRU EEPROM's data format is defined in Section 8.7. The thermal sensors are mainly used to measure the inlet and outlet temperatures of the 1S server for the platform thermal management's algorithm.

The Bridge IC has a dedicated I²C bus to the PCH's Intel® Manageability Engine that supports IPMB. The Bridge IC now behaves as a transparent bridge to forward IPMI messages between the BMC and the PCH's Intel® Manageability Engine. With this transparent bridge, the BMC can directly work with the PCH's Intel® Manageability Engine to perform most of server management functions.

The Bridge IC also implements a PECI interface to enable in-band server manageability.

The Bridge IC monitors the Crater Lake 1S server's sensors, such as voltage sensors, power sensors, and digital sensors for critical GPIOs. The BMC can inquire about the 1S server's status by reading these sensors and taking actions via the Bridge IC.

It is recommended to use a versatile microcontroller as the Bridge IC. The microcontroller has a compact size, uses a low amount of power, and has adequate functions to support all required bridging functions. The Bridge IC on the Crater Lake 1S server is an Aspeed AST1030.

17.3 I³C

The Crater Lake 1S server and BMC communicates using DMTF MCTP transactions or IPMI 2.0 commands transmitted over the I³C connection through a Bridge IC on the 1S Server card. The static address for the Bridge IC is configured as 0x09. The BMC on the platform is configured as 0x08.

The BIC on 1U Expansion card is configured as 0x20.

The BIC on 2U Expansion card is configured as 0x20.

The I³C interface between the CPU and DIMMs is required and should be implemented per platform design guidelines. The BIC does not need access to this interface so no additional muxing logic is needed.

Although all the BICs have the same address, it does not cause a conflict as the I3C bus is point to point between the BICs and the BIC initiating the transaction does not respond to its own request. This has been tested on Yosemite V3.5 platform.

17.4 MCTP Interfaces

The Bridge IC provides a MCTP over I3C interface where IPMI commands are encapsulated in MCTP transactions between the BMC and the Bridge IC. This allows the BMC to access various resources on the Crater Lake 1S Server. To meet this requirement, the Bridge IC shall implement various standard IPMI commands. It shall implement FRUID commands to identify the 1S server, System Event Log (SEL) commands to store 1S Server specific event logs, and Sensor Data Repository (SDR) commands to identify various sensors described for the specific 1S server.

17.5 USB

Covered in section 10.3.3

17.6 SPI

Covered in section 10.3.4

17.7 JTAG

Covered in section 10.3.5

17.8 UART

The serial console of the Crater Lake server is used as the BIOS or OS serial console and will also be available as a Serial over Lan (SOL) connection via the BMC. BIC on Crater Lake talks to PCH over eSPI and sends the serial data through CPLD to BMC. The BIOS menus must be fully accessible and text-based. Any hot keys that are required must be transmittable through a serial console session.

The BIOS should default to 57,600 bps/8N1.

17.9 Message Transfer

As the bridge between the server PCH and BMC on the platform the Bridge IC provides ways to transfer messages between them via KCS interfaces.

For in-band management, the Bridge IC can forward the PCH's Keyboard Controller Style (KCS) request to the BMC and then send the received response back to the PCH.

When the BMC sends a request on the I3C bus meant for the PCH's Intel® Manageability Engine, the Bridge IC shall forward the command on the I²C bus to the CPU and send the received response back to the BMC.

It is possible to implement an alternative SOL through the Bridge IC. When the alternative SOL feature is enabled, the serial data from the PCH's serial port shall be sent to the BMC via I3C. When the BMC sends SOL data, it shall be emitted via the serial port.

17.10 Platform Discovery and Configuration

The Bridge IC provides a way for the BMC to discover platform capabilities such as electrical interface assignment. It also provides a way to discover and configure its own capabilities like enabling or disabling the SOL interface and/or POST code interface.

17.11 POST Code Access

During the power-on stage, the PCH usually sends out status/error information on the POST Code interface. The Bridge IC needs to provide a way for the BMC to access POST Code information. The Bridge IC shall keep the latest POST Code in a 230-byte buffer. Whenever the BMC is available, the Bridge shall send the POST Code as soon as it is received on the POST Code interface. Whenever the BMC is not available (such as the BMC being in a firmware update mode or during BMC boot-up) the Bridge IC shall add the latest POST Code at the top of the 230-byte buffer. The BMC shall be able to retrieve the POST Code buffer from the Bridge with the latest POST Code.

17.12 Firmware Update

The Bridge IC can update firmware of the programmable devices on the Crater Lakes 1S Server, such as BIOS, the PCH's Intel® Manageability Engine firmware, the CPLD image, various VR firmware and the Bridge IC's firmware.

Bridge IC provides a way for the BMC to access the version information and initiate update process of various firmware components on the Crater Lake 1S Server, as well as detect and retransmit corrupted firmware image packets during transit from the BMC to the Bridge IC.

17.13 GPIO Register

The Bridge IC shall provide a GPIO interface to the BMC through IPMB. In this way, the BMC can control the GPIO behind the Bridge IC (or this hardware abstraction layer) through accessing this register block.

The BMC sends IPMB set/get GPIO commands to the BIC for GPIO control of the Crater Lake BIC, in addition to BICs located on the 1OU and 2OU expansion boards.

17.14 IPMI commands

The Bridge IC supports the IPMI commands shown in Table 17-1 . These commands are encapsulated in an MCTP over I3C packet transaction between the BMC and the BIC.

Table 17-1: Bridge IC supported IPMI command Table

IPMI Command	Net Function	CMD#
Get Device ID	App	01h
Get Self Test Results	App	04h
Get System GUID	App	37h
Controller Write-Read I ² C	App	52h
Get FRU Inventory Area Info	Storage	10h
Read FRU Inventory Data	Storage	11h
Write FRU Inventory Data	Storage	12h
Get SDR Repository Info	Storage	20h
Reserve SDR Repository	Storage	22h
Get SDR	Storage	23h
Get SEL Info	Storage	40h
Get SEL Allocation Info	Storage	41h
Reserve SEL	Storage	42h
Get SEL Entry	Storage	43h
Add SEL Entry	Storage	44h
Clear SEL	Storage	47h
Get Sensor Reading	Sensor/Event	2Dh
Get Sensor Reading	Sensor/Event	2Dh
Send request message to BMC	OEM (0x38)	01h
Send request message to Bridge-IC	OEM (0x38)	02h
Get all GPIO status	OEM (0x38)	03h

IPMI Command	Net Function	CMD#
Set all GPIO status	OEM (0x38)	04h
Get GPIO configuration	OEM (0x38)	05h
Set GPIO configuration	OEM (0x38)	06h
Send interrupt to BMC	OEM (0x38)	07h
Send POST Code to BMC	OEM (0x38)	08h
Request POST Code data	OEM (0x38)	12h
Firmware Update	OEM (0x38)	09h
Firmware Verify	OEM (0x38)	0Ah
Get Firmware version	OEM (0x38)	0Bh
Enable Bridge IC update flag	OEM (0x38)	0Ch
Get NIC LED Frequency	OEM (0x38)	0Dh
Bridge IC Discovery	OEM (0x38)	0Eh
Platform Discovery	OEM (0x38)	0Fh
Set Bridge IC Configuration	OEM (0x38)	10h
Bridge IC Reset Cause	OEM (0x38)	11h
Bridge IC enter update mode	OEM (0x38)	13h
Set VR monitor Enable	OEM (0x38)	14h
Get VR monitor Enable	OEM (0x38)	15h
Reset BMC	OEM (0x38)	16h
Read BIOS image	OEM (0x38)	18h
Get Flash size	OEM (0x38)	19h
Set Pump Duty	OEM (0x38)	1Bh
Get Pump Duty	OEM (0x38)	1Ch
Set BIOS Chip Select	OEM (0x38)	1D
Get BIOS Chip Select	OEM (0x38)	1F
Set JTAG Tap State	OEM (0x38)	21
Shift JTAG Data	OEM (0x38)	22
Set System GUID	OEM (0x38)	EFh

Table 17-2 provides details of the IPMI Original Equipment Manufacturer (OEM) commands that are defined Table 17-1.

Table 17-2: Bridge IC supported IPMI command Table(WIP)

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
01h	Send request message to BMC	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Request interface 01h: Intel® Manageability Engine 02h: SOL 03h: KCS SMS 04h: KCS SMM Byte 5:X – Request data Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5 – Request interface 01h: Intel® Manageability Engine 02h: SOL 03h: KCS Byte 6:X – Response data	This command is used for Bridge IC transfer request to BMC. For example: 1. Bridge IC gets “Get Device ID” command 0x06 0x01 from KCS. 2. Bridge IC will send this command to BMC as below. 0x38 0x01 0x03 0x06 0x01 3. BMC responds Get Device ID data.
02h	Send request message to Bridge IC	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 –Receive interface 01h: Intel® Manageability Engine 02h: SOL Byte 5:X – Request data from BMC Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5 –Receive interface 01h: Intel® Manageability Engine 02h: SOL Byte 6:X – Response data	This command is used for BMC send request to Bridge IC. For example: 1. When BMC want to send “Get Device ID” command to ME. It can use this command: 0x38 0x02 0x01 0x06 0x01 2. When Bridge IC receive this command, It will send “Get Device ID”

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
			<p>command to Intel® Manageability Engine and get the response from Intel® Manageability Engine .</p> <p>3. Bridge IC responds this command to BMC.</p>
03h	Get all GPIO status	<p>Request:</p> <p>Byte 1:3 – IANA ID – 00A015h, LS byte first</p> <p>Response:</p> <p>Byte 1 – Completion Code</p> <p>00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2)</p> <p>Byte 2:4 – IANA ID – 00A015h, LS byte first</p> <p>Byte 5:8 – Get all GPIO status</p> <p>0b: Low 1b: High</p>	This command used by BMC to get GPIO status from Bridge IC. Refer to Table 8 GPIO mapping table.
04h	Set all GPIO status	<p>Request:</p> <p>Byte 1:3 – IANA ID – 00A015h, LS byte first</p> <p>Byte 4:7 – GPIO enable mask, refer to GPIO mapping table</p> <p>0b: Disable 1b: Enable</p> <p>Byte 8:11 – Set all GPIO status</p> <p>0b: Low 1b: High</p> <p>Response:</p> <p>Byte 1 – Completion Code</p> <p>00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2)</p> <p>Byte 2:4 – IANA ID – 00A015h, LS byte first</p>	This command used by BMC to set GPIO status from Bridge IC. Refer to Table 8 GPIO Mapping Table.

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
05h	Get GPIO configuration	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4:7 – GPIO enable mask, refer to GPIO mapping table 0b: Disable 1b: Enable Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5:X – GPIO configuration (one byte for one GPIO pin configuration) Bit[0] – Input/output pin 0b : Input pin 1b : Output pin Bit[1] – interrupt disable/enable 0b : Disable 1b : Enable Bit[2] – Edge trigger 0b : Edge trigger (default) Bit[3:4] – Trigger type 00b : Falling edge 01b : Rising edge 10b : Both 11b : Reserved	This command used by BMC to get GPIO configuration from Bridge IC. Refer to Table 8 GPIO Mapping Table.
06h	Set GPIO configuration	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4:7 – GPIO enable mask, refer to GPIO mapping table 0b: Disable 1b: Enable Byte 8:X – GPIO configuration (one byte for one GPIO pin configuration) Bit[0] – Input/output pin 0b : Input pin 1b : Output pin Bit[1] – interrupt disable/enable 0b : Disable 1b : Enable Bit[2] – Edge trigger 0b : Edge trigger (default) Bit[3:4] – Trigger type 00b : Falling edge	This command used by BMC to set GPIO configuration to Bridge IC. Refer to Table 8 GPIO Mapping Table.

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
		01b : Rising edge 10b : Both 11b : Reserved Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	
07h	Send interrupt to BMC	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Interrupt GPIO number, refer to GPIO mapping table Byte 5 – Trigger type 00h: Falling edge 01h: Rising edge Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	This command used for Interrupt notification from Bridge IC sends to BMC. Refer to Table 8 GPIO Mapping Table.
08h	Send POST Code to BMC	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Data length Byte 5:X – Port 80 data Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	Bridge IC support maximum 230 bytes to buffer BIOS POST Code when BMC is not ready. The POST Code data will be in FIFO manner i.e. with the first POST Code as the first byte. But in case BMC is ready, Bridge IC will send one POST Code to BMC at a time.

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
12h	Request POST Code data	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:X – Port 80 data Byte 2:4 – IANA ID – 00A015h, LS byte first	BMC can get all POST Code data by this command. Bridge IC will buffer POST Code data for last boot. The POST Code data will be in LIFO manner i.e. with the latest POST code as the first byte. Bridge IC clear buffer when system power on. The maximum buffer data length is 230 bytes.
09h	Firmware Update	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – update target 00h: BIOS 01h: CPLD - bit[7] = 1, last package for image data 02h: Bridge IC boot loader from OOB - bit[7] = 1, last package for image data 03h: Bridge IC boot loader from In-Band - bit[7] = 1, last package for image data 04h: VR - bit[7] = 1, last package for image data Byte 5:8 – Offset Byte 9:10 – Data length Byte 11:X – Update image data Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) 80h –Write flash error 81h – Power status check fail 82h – Data length error 83h – Flash erase error Byte 2:4 – IANA ID – 00A015h, LS byte first	This command is used to update BIOS and CPLD Firmware from BMC.

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
0Ah	Firmware Verify	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 –update target 00h: BIOS 01h: CPLD 02h: Bridge IC boot loader 03h: VR Byte 5:8 – Offset Byte 9:12 – Data length Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) 80h – Checksum error 82h – Data length error 84h – Read flash error Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5:8 – Checksum	This command is used to verify BIOS and CPLD Firmware from BMC.
0Bh	Get Firmware version	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 –update target 01h: CPLD 02h: Bridge IC 03h: Intel® Manageability Engine version 04h: Bridge IC Bootloader 05h: VCCIO VR 06h: VCCIN VR 07h: VCCSA VR 08h: DDR_AB VR 09h: DDR_DE VR 0Ah: VNNPCH VR 0Bh: 1V05PCH VR Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5:X – CPLD version (Hexadecimal) – CPLD user code 4 bytes.	

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
		<p>Bridge IC version (Decimal) – 2 bytes length, ex: 1.03. Return data will be 0x01 0x03.</p> <p>Intel® Manageability Engine version (Decimal) – 5 bytes length, ex: Intel® version 03.0.0.010. Return data will be 0x03 0x00 0x00 0x01 0x00.</p> <p>VR version (Hexadecimal) – VR user data, 4 bytes length. Ex: 3d 01 11 00, user data 0 : 0x3d01, user data 1 : 0x1100</p> <p>Bridge IC bootloader version (Decimal) – 2 bytes length, version 1.08 Return data will be 0x01 0x08</p>	
0Ch	Enable Bridge IC update flag	<p>Request:</p> <p>Byte 1:3 – IANA ID – 00A015h, LS byte first</p> <p>Byte 4 – Enable update interface flag</p> <p>00h: UART 01h: I2C 02h: LPC</p> <p>Response:</p> <p>Byte 1 – Completion Code</p> <p>00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2)</p> <p>Byte 2:4 – IANA ID – 00A015h, LS byte first</p>	This command is used to enable Bridge IC update flag from BMC.
0Dh	Get NIC LED frequency	<p>Request:</p> <p>Byte 1:3 – IANA ID – 00A015h, LS byte first</p> <p>Response:</p> <p>Byte 1 – Completion Code</p> <p>00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2)</p> <p>Byte 2:4 – IANA ID – 00A015h, LS byte first</p> <p>Byte 5 – LED frequency</p> <p>00h: No blinking 01h: Solid on 02h: Slow flashing 03h: Fast flashing</p>	

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
0Eh	Get Bridge IC configuration	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5 – Bit[0] – SOL interface 0b : Disable 1b : Enable Bit[1] – Port 80 0b : Disable, Bridge IC will not send post code to BMC 1b : Enable	
0Fh	Platform discovery	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5 – 0x03: A13/A14 PCIe0 RefClk Byte 6 – 0x02: A17/A18 PCIe0 Lane 0, Gen3 Byte 7 – 0x02: A21/A22 PCIe0 Lane 1, Gen3 Byte 8 – 0x02: A25/A26 PCIe0 Lane 2, Gen3 Byte 9 – 0x02: A29/A30 PCIe0 Lane 3, Gen3 Byte 10 – 0x05: A33/A34 SATA0, Gen3 Byte 11 – 0x03: A37/A38 PCIe2 RefClk Byte 12 – 0x02: A49/A50 PCIe1 Lane 0 Gen3 Byte 13 – 0x02: A53/A54 PCIe1 Lane 1 Gen3 Byte 14 – 0x02: A57/A58 PCIe1 Lane 2 Gen3 Byte 15 – 0x02: A61/A62 PCIe1 Lane 3 Gen3 Byte 16 – 0x02: A65/A66 PCIe2 Lane 0 Gen3 Byte 17 – 0x02: A69/A70 PCIe2 Lane 1 Gen3 Byte 18 – 0x02: A73/A74 PCIe2 Lane 2 Gen3 Byte 19 – 0x02: A77/A78 PCIe2 Lane 3 Gen3 Byte 20 – 0x02: B15/B16 PCIe0 Lane 0, Gen3 Byte 21 – 0x02: B19/B20 PCIe0 Lane 1, Gen3	For scalability needs, we list all configurations in this command response. If we store that information in BMC FW and check by FRU ID, we will need to modify BMC FW whenever there is a new card. We recommend storing the info on MB.

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
		Byte 22 – 0x02: B23/B24 PCIe0 Lane 2, Gen3 Byte 23 – 0x02: B27/B28 PCIe0 Lane 3, Gen3 Byte 24 – 0x05: B31/B32 SATA0, Gen3 Byte 25 – 0x03: B35/B36 PCIe1 Ref Clk Byte 26 – 0x02: B51/B52 PCIe1 Lane 0 Gen3 Byte 27 – 0x02: B55/B56 PCIe1 Lane 1 Gen3 Byte 28 – 0x02: B59/B60 PCIe1 Lane 2 Gen3 Byte 29 – 0x02: B63/B64 PCIe1 Lane 3 Gen3 Byte 30 – 0x02: B67/B68 PCIe2 Lane 0 Gen3 Byte 31 – 0x02: B71/B72 PCIe2 Lane 1 Gen3 Byte 32 – 0x02: B75/B76 PCIe2 Lane 2 Gen3 Byte 33 – 0x02: B79/B80 PCIe2 Lane 3 Gen3	
10h	Set Bridge IC configuration	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Config Bridge IC Bit[0] – SOL interface 0b : Disable 1b : Enable Bit[1] – Port 80 0b : Disable, Bridge IC will not send post code to BMC 1b : Enable Bit[2] – KCS 0b : Disable, Bridge IC will not send KCS command to BMC 1b : Enable Bit[3] – IPMB message 0b : Disable, Bridge IC will not send IPMB message to BMC 1b : Enable Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	When BMC enter update mode, BMC can use this command to disable various communication to Bridge IC.

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
11h	Bridge IC reset cause	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Reset cause 0x00 : Cold reset by Firmware update 0x01 : Watchdog timeout Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	Bridge IC will send this command to notify BMC when Bridge IC is reset.
13h	Bridge IC enter update mode	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 2 – Firmware mode 0x01 : normal mode 0x0F : update mode Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	This command is used to notify BMC, Bridge IC enter update mode and normal mode before and after Firmware update.
14h	Set VR Monitor Enable	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Enable/Disable VR Monitor 0x01 : normal mode 0x0F : update mode Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	
15h	Get VR Monitor Enable	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5 – VR Monitor	

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
		0x00: Disable 0x01: Enable	
16h	Reset BMC	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	
18h	Read BIOS image	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – update target 00h: BIOS Byte 5:8 – Offset Byte 9 – Data length Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) 81h – Power status check fail Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5:N – BIOS image data	
19h	Get Flash Size	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – target 00h: BIOS Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5:8 – flash size	

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
1Bh	Set Pump Duty	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Duty Value, range from 0 to 100 Byte 5 – Pump number, in this project it's set to 0 Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	
1Ch	Get Pump Duty	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Pump number, in this project it's set to 0 Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5 – Pump Duty	
1Dh	Set BIOS Chip Select	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – BIOS chip select index 0x00: Select SPI 0 0x01: Select SPI 1 Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	
1Fh	Get BIOS Chip Select	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – Pump number, in this project it's set to 0 Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5 – BIOS Chip Select Index	

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
		0x00: select SPI 0 0x01: select SPI 1	
21h	Set JTAG Tap State	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4 – JTAG TMS Bit length Byte 5 – JTAG TMS Bit data Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first	
22h	Shift JTAG Data	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4:5 – write data bit length Byte 5:n – write data Byte n:n+1 – read data bit length Byte n+2 – last transaction index 0x00 – not the last transaction, keep the TMS state 0x01 – last transaction, set tap state to Exit1 state Response: Byte 1 – Completion Code 00h – Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2) Byte 2:4 – IANA ID – 00A015h, LS byte first Byte 5:n – JTAG TDO response data	

Net Function = OEM (0x38), LUN = 00			
Code	Command	Request, Response Data	Description
EFh	Set System GUID	Request: Byte 1:3 – IANA ID – 00A015h, LS byte first Byte 4:19 – System GUID. See Picture 5, GUID format Response: Byte 1 – Completion Code 00h - Success (Remaining standard Completion Codes are shown in IPMI spec v2.0 table 5-2)	

17.15 Management Interface

The PCH could have its own management controller. However, this controller has to work together with the Bridge IC as well as the BMC to perform server management tasks. The management interface between the Bridge IC and the PCH consists of a supplier-agnostic interface that combines a simple register interface to abstract the card-specific details. This interface can be implemented in hardware, software, or a combination of the two.

17.16 Power Control

The BMC controls power on, off, and reset directly via the signals defined in the pin-out. If 12V to the card is lost and returns “AC Lost”, the BMC must be configurable to enable either an immediate power-on, delayed power-on, or the last power state prior to the event.

17.17 Thermal Alerts

The PCH provides a mechanism to provide thermal alerts and over temperature notifications. The BMC must be able to receive these alerts in a timely fashion to allow it take action quickly. The I²C alert signal must be used. In some cases, an over temperature condition may occur which forces the PCH to power-off immediately. This condition must be logged.

17.18 Sensors

The following list of analog and discrete sensors are provided and are reported by the Bridge IC to the BMC.

Analog sensors include:

- Outlet Temperature
- Inlet Temperature
- VR Temperature(s)

- VR Current(s)
- PCH Temperature
- CPU Thermal Margin
- DIMM Temperature(s)
- CPU Package Power
- CPU T_{jMAX}
- Voltage Sensor(s)
- Current Sensor(s)
- Power(s)

Discrete sensors include:

- CPU Thermal Trip
- System Status
- CPU Fail
- System Boot Status
- PCH/DIMM Hot
- VR Hot

Event Only Sensors Include:

- Power Threshold Event
- POST Error
- Power Error
- CPU Throttle
- Machine Check Error
- PCIe Error
- Other IO Error
- Memory ECC Error

17.19 Event Log

The vendor should implement the BMC to support storing events/logs from each 1S server, baseboard, device carrier card, and mezzanine card.

17.20 Logged Errors

17.20.1 CPU Error

Both correctable ECC errors and uncorrectable ECC errors should be logged into the Event log. Error categories include Link and L3 Cache.

17.20.2 Memory Error

Both correctable ECC errors and uncorrectable ECC errors should be logged into the Event log. The Error log should indicate the location of the DIMM (if applicable), channel #, and slot #.

17.20.3 PCIe Error

All errors, which have a status register, should be logged into the Event log, including root complex, endpoint devices, and any switch upstream/downstream ports if available. Link disable on errors should also be logged. The error classifications Fatal, Non-fatal, or Correctable follow the 1S server vendor's recommendation.

17.20.4 POST Error

All POST errors, which are detected by BIOS during POST, should be logged into the Event log.

17.20.5 Power Error

Two power errors should be logged. One is a 12.5V DC input power failure that causes all power rails on the baseboard to lose power, including standby power. The other is an unexpected system shutdown during system S0/S1 while the 12.5V DC input is still valid.

17.20.6 MEMHOT# and PROCHOT#

Memory hot errors and processor hot errors should be logged. The Error log should identify the error source as internal, coming from the processor or memory, or an external error coming from the voltage regulator.

17.21 LEDs and Buttons

As for the front panel IO for the server, the following are suggested:

1. Power LED
2. Fault/LOC/Select LED
3. AC_cycle_on/off button

The Power and Fault/LOC/Select LED behavior is as follows:

Permitted States	Separate LEDs	
	PWR (Blue)	FAULT/LOC (Amber)
System AC Off/Service Action Allowed		
System On/Status OK		
System Off + Fault	 / 	
System On + Locate		
System Off + Locate	 / 	
System On + Fault		
System DC Off		

As for the Select LED, its behavior is based on whether the server blade is selected for OCP Debug cards function. Select LED is Amber and is lit when the OCP Debug card serial port is connected to that Crater Lake through BMC.

AC_cycle button is meant to AC cycle the server blade independently by triggering the enable to its hot swap controller. This button has to be operational independent of SW state of the Crater Lake system. The enable to the hot swap controller is managed by BMC. With a powered on system, if the AC_cycle button is pressed for >4 seconds < 8 seconds, the button state is detected by BMC to trigger the AC cycling of Crater Lake. When AC_cycle button is pressed for >8 seconds, the BMC will trigger Crater Lake to turn AC off. When the system is powered off, if the AC_cycle button is pressed for <8 seconds, no action will be taken. If the AC_cycle button is pressed for >8 seconds, the server board will turn AC on.

18 Security

18.1 TPM (Trusted Platform Module)

CPU host complex (CPU+PCH) shall have access to a TPM 2.0 module on its SPI interface. This TPM will exist as a hardware TPM physically on the Crater Lake board. The TPM will be used for measured boot. It will hold image measurements until the system is fully booted and connected to the network. From there, these measurements will be used in order to attest the system during provisioning. The TPM will only be used to store measurement values and will not contain any keys used elsewhere in the system.

19 Labels and Markings

The motherboard shall include the following labels on the component side of the motherboard. The labels shall not be placed in a way which may cause them to disrupt the functionality or the airflow path of the motherboard.

Description	Type	Barcode Required?
Safety Markings	Silk Screen	No
Vendor P/N, S/N, REV (Revision would increment for any approved changes)	Adhesive label	Yes
Vendor Logo, Name & Country of Origin	Silk Screen	No
PCB Vendor Logo, Name	Silk Screen	No
Date Code (Industry Standard: WEEK / YEAR)	Adhesive label	Yes
RoHS compliance	Silk Screen	No
WEEE Symbol. The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the Manufacturer at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silk Screen	No
CE Marking	Silkscreen	No
UL Marking	Silkscreen	No