CHIPLET TEST DESIGN KIT (TDK)

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Boon Ang Chong, Intel Corporation

Rajesh Pendurkar, University of California Santa Cruz

David Ratchkov, Thrace Systems

Tony Mastroianni, Siemens

Vidya Neerkundar, Siemens

Pratyush Kamal, Siemens

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Compliance with Open Compute Project Tenets

Openness

In this white paper, experts in their fields have contributed their knowledge of chiplet DFT workflows and data exchanged.

Efficiency

This white paper strives to improve the efficiency of architects, engineers and manufactures involved in the integration of heterogenous chiplet systems by providing chiplet-level definitions of DFT modes and pin assignments.

Impact

This white paper is the first to describe a format for exchanging chiplet DFT definitions.

Sustainability

The contributors hope that this white paper, the first of its kind, will benefit anyone interested in growing the Open Chiplet Economy.

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Executive Summary

The Chiplet Test Design Kit (TDK) provides a comprehensive framework to support the planning, design, and manufacturing of chiplet-based systems, with a particular emphasis on testability. Developed as part of the Open Compute Project (OCP), the TDK aims to standardize the testing process for chiplet integration, addressing critical challenges in modern semiconductor design and manufacturing.

Key highlights of the TDK include:

- Standardized Definitions: Clear and precise definitions of terms such as "pad," "sacrificial pad," and various pad construction methods (e.g., solder balls, copper pillars, and hybrid bond pads).
- Test Flow Integration: Detailed guidelines for incorporating test requirements at every stage of the development lifecycle, from planning and design to manufacturing and final product assembly.
- Sacrificial Pads: Introduction of sacrificial pads as a pivotal element in testing. These pads are specifically designed for temporary use during testing phases and are excluded from the final product, ensuring optimal design efficiency.
- CDXML-Based Standardization: Use of the CDXML format to define pad locations, structures, and testing parameters, enabling seamless communication and integration across design and manufacturing teams.
- Support for Advanced Manufacturing Techniques: The TDK supports emerging technologies, such as backside power delivery and 3D integration, by providing robust definitions and workflows tailored to these innovations.

Organizations can adopt the Chiplet Test Design Kit to ensure a standardized, scalable, and efficient testing process, reducing development time and costs while enhancing overall product reliability. This collaborative effort aligns with the OCP's mission to foster open innovation and advance semiconductor technology.

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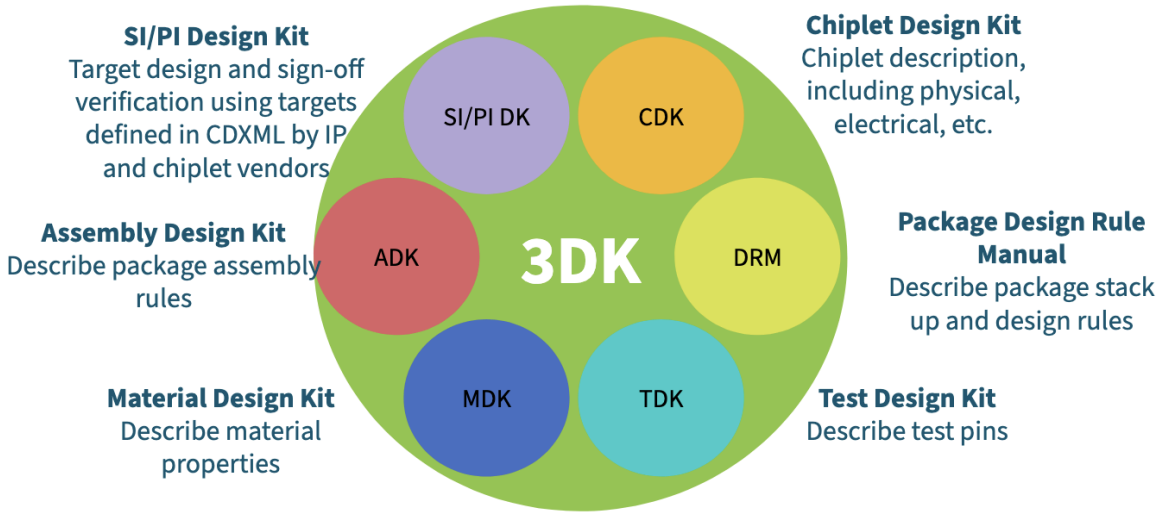
Introduction

Today CDXML defines a final product that can be integrated into more extensive chiplet systems. Recognizing the need for a standard file format to carry data through the planning, design and manufacturing stages of the product flow, this proposed extension to CDXML addresses the Test steps of the flow. This extension focuses on two main aspects: the complete definition of a “pad” and the handling of what is known as sacrificial pads. Sacrificial pads are essential because, as opposed to other pads, which may be reused for testing purposes, they exist as physical objects purely to enable test.

3D-IC Design Kits (3DK)



Architecture	Chiplet selection	CDK for choosing chiplets ADK for chiplet compatibility DRM for package technology
	Package planing	DRM for choosing a technology MDK for material properties
	System planning	ADK for physical floorplan CDK for netlist creation
	Performance analysis	SI/PI Design Kit MDK for thermal
Design	DFT	TDK for test connectivity
	Package routing	DRM for design rules
Sign-off	SI/PI analysis	SI/PI Design Kit for sign-off targets MDK for material properties
	Thermal and mechanical analysis	MDK for material properties

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Definitions

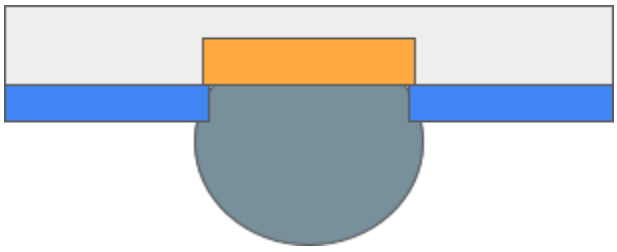
Front side vs Back side

Typically, in the manufacturing of semiconductors, the processes are referred to as Front End Of the Line (FEOL) and Back End Of the Line (BEOL). Simply put, FEOL refers to the deposition of transistors on the Silicon wafer, while BEOL refers to the deposition of wire interconnect. With the advent of Back Side Power (BSP), wiring is being deposited on both sides of the wafer, where connectivity between both sides is accomplished by Through Silicon Vias (TSV). BSP is a key enabling technology for Silicon interposers and three-dimensional die stacking. Having connections on both sides of a Silicon die necessitates a clear distinction between pads placed on each side. To maintain familiarity with the existing terms mentioned above, pads placed on the FEOL side will be referred to as “front-side pads”, while pads placed on the BSP side will be referred to as “back-side pads”.

Pad construction

A “pad” is a generic reference to an exposed physical connection. Below are the ways to construct a “pad.”

Ball



Also referred to as a solder ball, solder bump, C4 bump, or just bump, a solder ball is a roughly spherical object made of a material with a height and a diameter.

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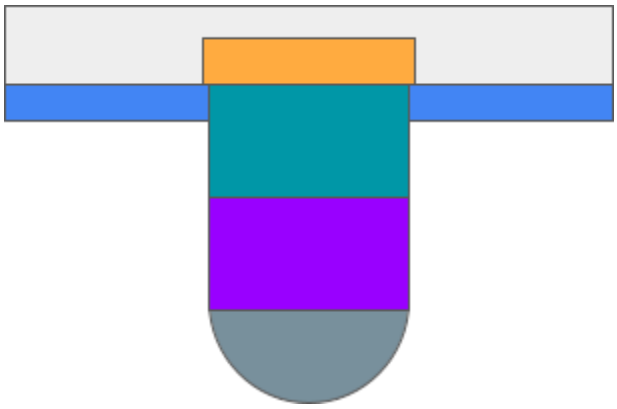
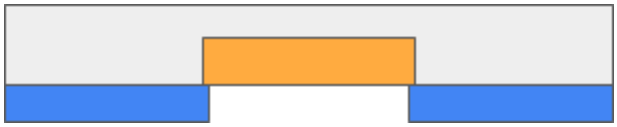
Micro-bump and Pillar



Typically referred to as a Copper Pillar, it is manufactured as part of the BEOL process. It has a two_dimension shape, height, multiple layers of deposited material, and may or may not have a solder cap.

Pad



Pads are areas of exposed metal on top of a die. These pads are typically used as a base for depositing balls, pillars, or micro bumps, commonly called bumping. Although a final fully assembled product will never have dies with just pads and without Balls, Pillars or Micro bumps, a separate definition is necessary to accommodate the manufacturing process - wafer probing will be done before any bumping; and to accommodate dies sold as chiplets before bumping, so their location, shape, and material composition need to be defined.

Hybrid bond pad

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These pads are exposed BEOL metal, typically Copper, and are used for direct connection to another Hybrid bond pad. These pads are described by their two_dimension shape and

Pad vs Pin vs Net

This document assumed the following definitions:

- Pad - denotes a physical two-dimensional object on the die. Pads are described by their two_dimension shape.
- Pin - denotes the logical name of the pad; this name is used when defining connectivity outside of the die.
- Net - typically, this is the same as the pin, as pins are nets internal to the die but brought to the boundary.

Test modes

An IC undergoing a test will go through different tests called test modes. There are several ways to control an IC to put it into a test mode:

- Low pin count test mode - a single pin is used to put the device in a test mode
- Internal control of test modes - internal registers are set through JTAG
- External control of test mode - external pins are user to control

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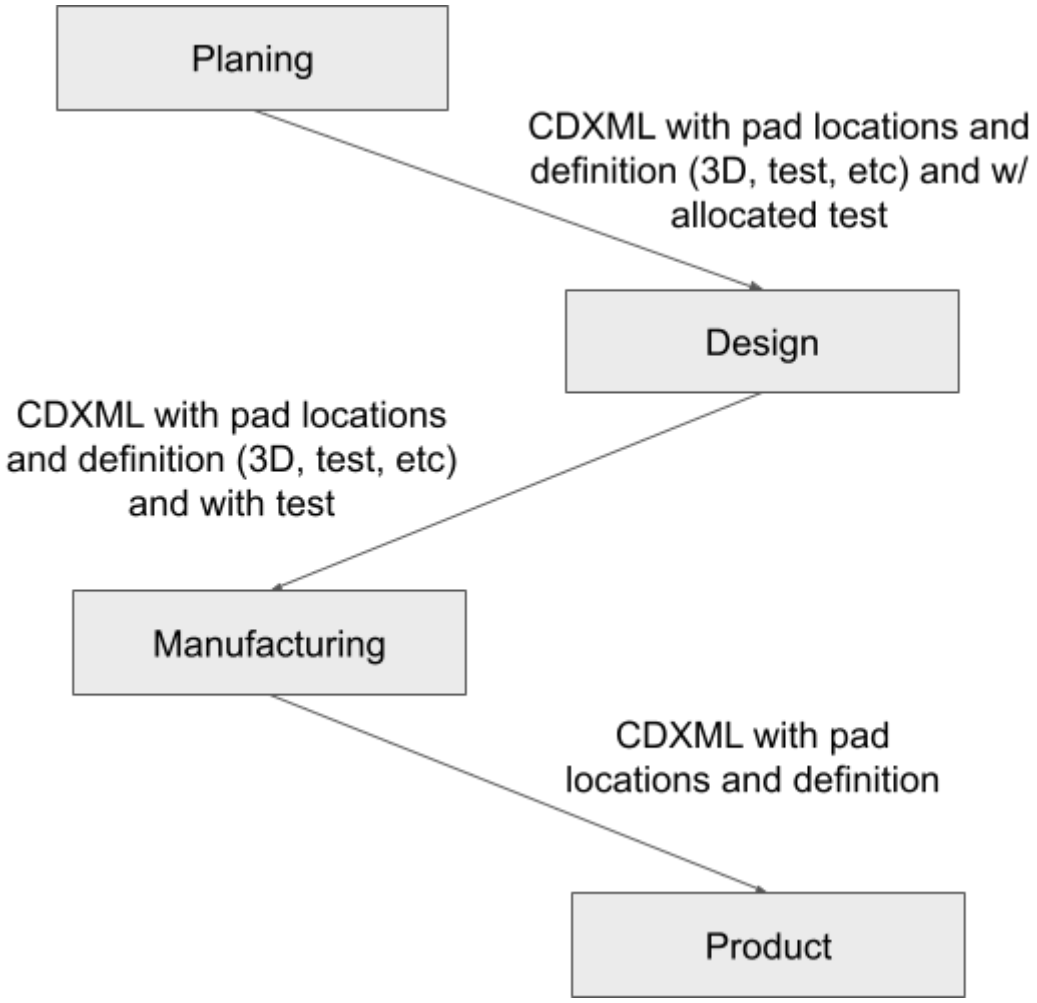
Flows



Planning step

In this step, the location and structure of the pads are defined. Specifically, test only, specifically sacrificial pads, are identified. The pad definitions may include internal layers to help with the design flow in this step. For example, a pad definition may consist of UBM shape and thickness but also include a passivation opening and the top metal layer of the BEOL layer stackup.

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Design step

The design flow will use the incoming pad definitions. Additionally, it is expected that the design flow will additionally mark pads as test-related during the test insertion process. Most importantly, at this step, sacrificial test pads cannot be unmarked, nor can pads be added or removed.

Manufacturing step

This step will use the incoming pad definitions to develop test hardware.

Product step

The final product will contain all necessary pads. Most notable, however, it may or may not contain all test-only pads. For example, sacrificial pads are expected not to be excluded as the end customer cannot use them.

Existing CDXML definitions

This document assumes CDXML has definitions of the following items:
Pad areas that define the coordinates of each pad/pin.
Net names are attached to each pin. These nets match a Verilog netlist or Schematic.

CDXML Structure

Below is high-level description of the structure of CDXML with TDK, where the TDK related entries are highlighted.

CDXML
- **Pad/bump Definitions**
  - **Hybrid bond pad**

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    - **Reference two_dimension shape**
    - **Reference material**
  - **Pad**
    - **Reference two_dimension shape**
    - **Reference material**
    - **Height above the die surface**
  - **Pillar/uBump**
    - **Reference pad**
    - **Reference two_dimension shape**
    - **Layers**
      - **Thickness**
      - **Material**
      - **Height**
    - **Solder cap (optional)**
      - **Material**
      - **Height**
    - **Total height above the die surface**
  - **Solder bump**
    - **Reference pad**
    - **Diameter**
    - **Height**
    - **Material**
- **Test mode definitions**
- IO definition
  - **Pad type reference**
  - Pin definition
    - **Pad type reference**
    - X,y
    - Pin name
    - **Test definition (optional)**
      - **Direction**
      - **Test only flag**
      - **Sacrificial flag**
      - **Direction**
      - **Test pin type**

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Test Design Kit CDXML Examples

Pad definitions

```
<cdxml>
      <mpn></mpn>
      <pad_structure>
            <name>Pad1</name>
            <library_reference>PAD20R</library_reference>
            <two_dimension>
                  <circle radius=”22.5”>
            </two_dimension>
            <three_dimension>
                  <layer>
                        <name>bump</name>
                        <material>SnPb</material>
                        <semi_sphere>
                              <height>20</height>
                        </semi_sphere>
                  </layer>
            </three_dimension>
      </pad_structure>
      <pad_structure>
            <name>Pad1</name>
            <library_reference>PAD20R</library_reference>
            <two_dimension>
                  <oval width=”22.5” height=”10.75”>
            </two_dimension>
            <three_dimension>
                  <layer>
                        <name>Cu</name>
                        <material>Cu</material>
                        <thickness>10</thickness>
```

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```
            </layer>
            <layer>
                  <name>Cap</name>
                  <material>SnPb</material>
                  <semi_sphere>
                        <height>5</height>
                  </semi_sphere>
            </layer>
      </three_dimension>
</pad_structure>
<pad_structure>
      <name>Pad2</name>
      <two_dimension>
            <square dimension=”22.5”>
      </two_dimension>
      <three_dimension></three_dimension>
      </pad_structure>
      <pad_structure>
      <name>Pad2</name>
                  <two_dimension>
            <rectangle width=”22.5” height=”10.75”>
      </two_dimension>
      <three_dimension></three_dimension>
</pad_structure>
<pad_structure>
      <name>Pad2</name>
      <two_dimension>
            <polygon>
                  <point x=”0” y=”0”/>
                  <point x=”10” y=”0”/>
                  <point x=”5” y=”10”/>
            </polygon>

      </two_dimension>
```

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```
            <three_dimension></three_dimension>
      </pad_structure>
      <io>
            <mech_type rotation="45">Pad1</mech_type>
            <pin>
                  <mech_type>pad1</mech_type>
                  <sig_type>Power</sig_type>
                  <test only="true|false" sacrificial="true|false">
                        <direction>in|out</direction>
                        <group>Group Name 1</group>
                              <type>clock_in|clock_out|data_in|data_out|
                        enable|test_mode</type>
                  </test>
            </pin>
      </io>
</cdxml>
```

Test modes

```
<cdxml>
      <test_mode name="<mode name 1>" type="internal|external">
            <pin name="<pin name 1>" state="Logic0|Logic1"/>
            <pin name="<pin name 2>" state="Logic0|Logic1"/>
      </test mode>
      <test_mode name="<mode name 2>" type="internal|external">
            <pin name="<pin name 1>" state="Logic0|Logic1"/>
            <pin name="<pin name 2>" state="Logic0|Logic1"/>
      </test mode>
</cdxml>
```

Functional mode pin not used for test.

```
<cdxml>
      <mpn></mpn>
```

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```
      <pad_structure>
            <name>Pad1</name>
            <two_dimension></two_dimension>
            <three_dimension></three_dimension>
      </pad_structure>
      <io>
            <mech_type>Pad1</mech_type>
            <pin>
                  <mech_type>Pad1</mech_type>
                  <sig_type>Power</sig_type>
            </pin>
      </io>
</cdxml>
```

Shared pin used for functional and test modes

```
<cdxml>
      <mpn></mpn>
      <pad_structure>
                  <name>Pad1</name>
                  <two_dimension></two_dimension>
                  <three_dimension></three_dimension>
      </pad_structure>
      <io>
            <mech_type>Pad1</mech_type>
            <pin>
                  <mech_type>Pad1</mech_type>
                  <sig_type>Power</sig_type>
                  <test>
                        <direction>in|out|inout</direction>
                        <group>Group Name 1</group>
```

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```
      <type>clock_in|clock_out|data_in|data_out|enable|test_mode</typ
      e>
                  </test>
            </pin>
      </io>
</cdxml>
```

Test mode only pin without tie-off

```
<cdxml>
      <mpn></mpn>
      <pad_structure>
                  <name>Pad1</name>
                  <two_dimension></two_dimension>
                  <three_dimension></three_dimension>
      </pad_structure>
      <io>
            <mech_type>Pad1</mech_type>
            <pin>
                  <mech_type>pad1</mech_type>
                  <test only=”true”>
                        <direction>in|out</direction>
                        <group>Group Name 1</group>

      <type>clock_in|clock_out|data_in|data_out|enable|test_mode</typ
      e>
                  </test>
            </pin>
      </io>
</cdxml>
```

Test mode only pin with tie-off

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```
<cdxml>
      <mpn></mpn>
      <pad_structure>
                <name>Pad1</name>
                <two_dimension></two_dimension>
                <three_dimension></three_dimension>
      </pad_structure>
      <io>
            <mech_type>Pad1</mech_type>
            <pin>
                  <mech_type>pad1</mech_type>
                  <sig_type>Power</sig_type>
                  <test only=”true” mode=”<test mode name 1>”>
                        <direction>in|out</direction>
                        <group>Group Name 1</group>

      <type>clock_in|clock_out|data_in|data_out|enable|test_mode</typ
      e>
                  </test>
                  <test only=”true” mode=”<test mode name 2>”>
                        <direction>in|out</direction>
                        <group>Group Name 1</group>

      <type>clock_in|clock_out|data_in|data_out|enable|test_mode</typ
      e>
                  </test>
            </pin>
      </io>
</cdxml>
```

Sacrificial pad

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```
<cdxml>
      <mpn></mpn>
      <pad_structure>
                  <name>Pad1</name>
                  <two_dimension></two_dimension>
                  <three_dimension></three_dimension>
      </pad_structure>
      <io>
            <mech_type>Pad1</mech_type>
            <pin>
                  <mech_type>pad1</mech_type>
                  <test only=”true” sacrificial=”true”>
                        <direction>in|out</direction>
                        <group>Group Name 1</group>

      <type>clock_in|clock_out|data_in|data_out|enable|test_mode</typ
      e>
                  </test>
            </pin>
      </io>
</cdxml>
```

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