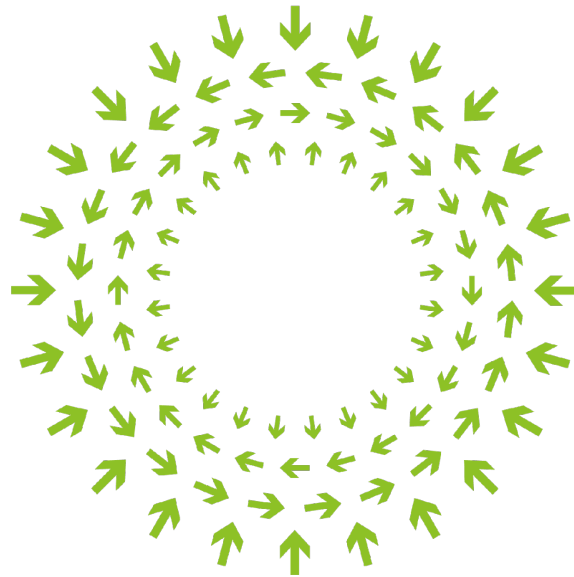




OPEN

Compute Project

Catalina: PCIe Gen5 EDSFF NVMe SSD Reference Designs

1.0.1

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Version History

Date	Version #	Author	Description
05 SEP 24	1.0.0	Xiaochun Wang Kaiqiang Zhao Keith McKay	Initial Release
16 SEP 24	1.0.1	Xiaochun Wang Kaiqiang Zhao Keith McKay	Corrected some minor typographic errors.

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1. License

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Notes:

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2. Compliance with OCP Tenets

The OCP core tenets can be seen [here](#). Adherence to these tenets is described in the following sections.

2.1. Openness

All design files required to enable 3rd party manufacturing are available for download. This specification can also be used as the basis for derivative designs, such as the implementation of additional form factors.

2.2. Efficiency

Performance per Watt is a key operational efficiency metric for an SSD. A variety of power modes operating per the OCP Datacenter SSD Specification provide flexibility to achieve the most appropriate balance of power and performance for the intended application.

2.3. Impact

Enabling alternative hardware providers will improve supply chain resiliency. Hardware providers are able to optimize the BOM for their supply chain.

2.4. Scale

Implementing key features of the OCP Datacenter SSD Specification, including telemetry and latency monitoring, help manage deployments of SSDs at scale.

2.5. Sustainability

Manufacturers have the flexibility to modify the design to meet their goals. Components that are not needed for the intended application can be removed, such as the EEPROM. This could save many components from being wasted in applications where they are not needed. Furthermore, the use of local supply chains reduces transportation related emissions.

3. Scope

This document includes the Base, Design and Product Specifications for PCIe Gen5 NVMe SSDs in EDSFF (Enterprise and Datacenter Standard Form Factor).

4. Overview

The Catalina contribution is intended to enable manufacturers to produce SSDs optimized for their supply chain or produce derivative designs with alternate components or form factors. Two designs are included: an E1.S with a 15mm enclosure and an E3.S with a 7.5mm 1T enclosure.

5. Base Specifications

5.1. Environmental Regulatory Compliance and Requirements

Catalina is designed to comply with the following regulations:

- RoHS: Restriction of Hazardous Substances Directive compliance.
- WEEE: Waste Electrical and Electronic Equipment Directive compliance.
- FCC: Federal Communications Commission's regulations for electromagnetic interference in the United States.
- UL: Underwriters Laboratories (UL) product safety.
- cULus: Underwriters Laboratories (UL) product safety for both the U.S. (UL) and Canada (cUL).
- CE: Health, safety, and environmental protection standards for products sold within the European Economic Area (EEA).
- CAN ICES-3(B)/NMB-3(B): Industry Canada's standards for radio interference.
- RCM: Australian and New Zealand regulatory requirements for electrical safety, electromagnetic compatibility, and telecommunications.
- UKCA: United Kingdom Conformity Assessment.
- VCCI: Voluntary Control Council for Interference by Information Technology Equipment standards in Japan.
- ICES: Canadian ICES-003 standard for electromagnetic interference.
- KCC: South Korean safety and electromagnetic compatibility standards.
- NVMe: Non-Volatile Memory Express standards compliance.
- PCIe: PCI Express interface standard compliance.

It is the responsibility of the manufacturer to obtain the necessary or desired certifications.

The recommended limits on environmental conditions are outlined in the following table.

Environmental Conditions (Operating and Non-Operating)

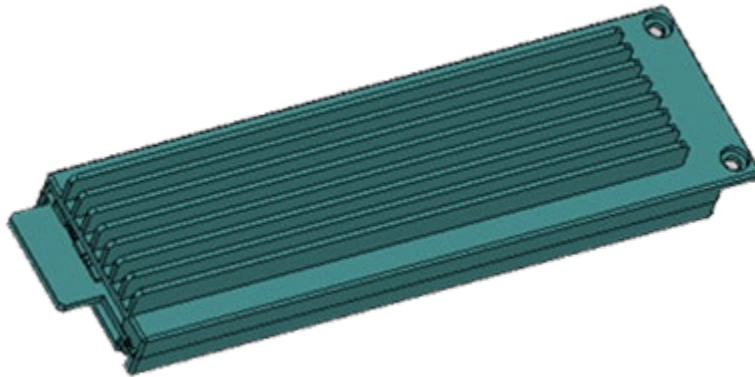
Parameter	Unit	Value
Max Operating Temperature	°C	77
Max Ambient Operating Temperature	°C	35
Min Ambient Operating Temperature	°C	0
Max Operating Relative Humidity (Non-Condensing)	%	90
Min Operating Relative Humidity (Non-Condensing)	%	10

Max Ambient Thermal Gradient	C/Hour	20
Max Non-Operating Temperature	°C	85
Min Non-Operating Temperature	°C	-40
Max Non-Operating Relative Humidity (Non-Condensing)	%	95
Min Non-Operating Relative Humidity (Non-Condensing)	%	5
Max Non-Operating Shock (Half-Sine)	G	700
Max Non-Operating Vibration (5-800Hz)	GRMS	3.13
Minimum Altitude	Feet	-1000
Maximum Altitude	Feet	10000

5.2. Physical Specifications

Catalina conforms to the E1.S (SFF-TA-1006: Enterprise and Datacenter 1U Short Device Form Factor) and E3.S (SFF-TA-1008: Enterprise and Datacenter Standard Form Factor) specifications. Renderings of these form factors are shown in the following figures.

E1.S Enclosure with 15mm Heatsink



Please describe the physical requirements for your contribution. This may be the limitations of the physical envelope.

E3.S Enclosure in 1T Thickness



All EDSFF devices connect to the system through the same card edge connector standard (SFF-TA-1002 1C). The following table outlines the overall dimensions in selected thickness variations:

Enclosure Measurements

Form Factor	Height	Length	Thickness
E3.S 1T	76mm	112.75mm	7.5mm
E1.S 15mm	33.75mm	118.75mm	15mm

5.3. Mechanical

Enclosure latch designs are outside the scope of this specification.

5.4. Electrical Requirements

The power supply tolerances for the 12V and 3.3V AUX PCIe supply rails are provided in the following table.

Power Supply Tolerances

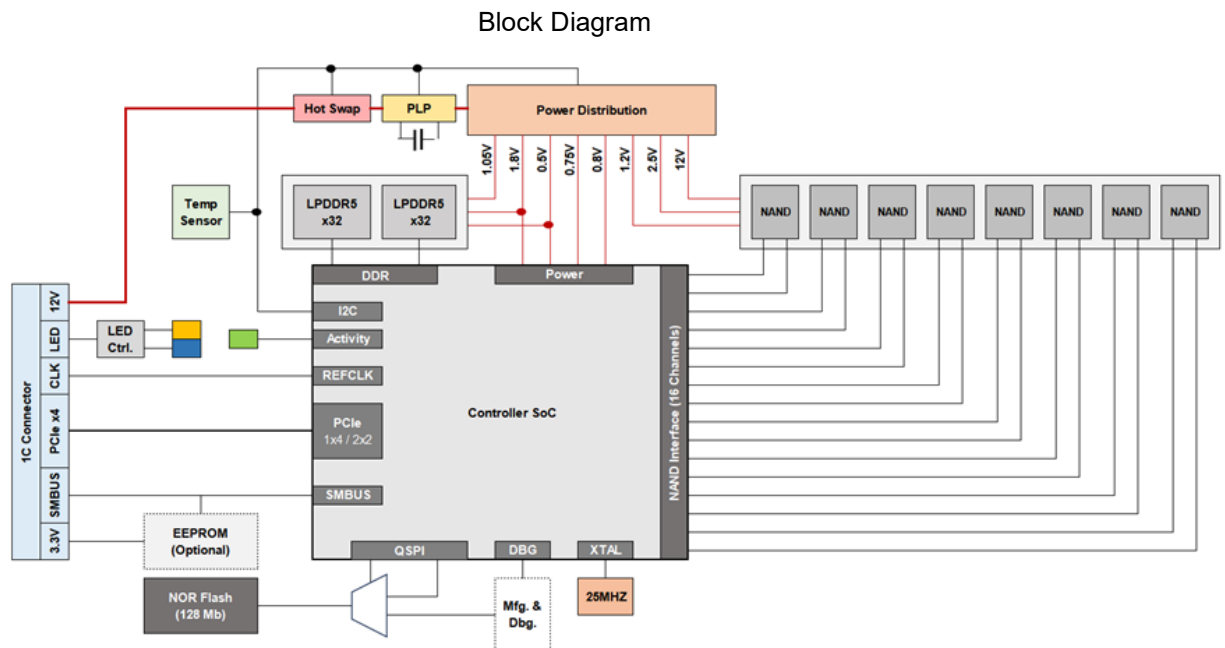
Parameter	Unit	Value	Comment
12V Supply Tolerance	V	10.8 - 13.2	Including supply ripple.
3.3V AUX Supply Tolerance	V	2.97 - 3.465	

5.5. Thermal Design Requirements

The enclosures included in the Catalina reference designs are generally designed to dissipate the rated power limit for each form factor with 1.5 LFM of airflow at the maximum operating air temperature. Thermal parameters should be modeled for any designs based on this specification to ensure that they meet the intended design constraints.

5.6. Interfaces

A top-level diagram of the Catalina reference designs is presented below. The SFF-TA-1002 1C connector provides a PCI Express and SMBus external host interface. Manufacturing interfaces include a JTAG and a UART interface.



5.6.1. Signal List

Both E1.S and E3.S designs utilize the 1C connector defined in the SFF-TA-1002 specification. The signal assignments of the connector are listed in the table below. The connector contains 56 contacts with up to 18 differential pairs of data signals in a GSSGSSG configuration.

Host Interface Signal List

Pin	Connection Sequence	B-Side Signal	A-Side Signal	Connection Sequence	Pin
B1	2nd mate	12V	GND	1st mate	A1
B2	2nd mate	12V	GND	1st mate	A2
B3	2nd mate	12V	GND	1st mate	A3
B4	2nd mate	12V	GND	1st mate	A4
B5	2nd mate	12V	GND	1st mate	A5
B6	2nd mate	12V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDAT	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMBRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28

5.6.2. Sideband Interfaces

There are two I2C and two SMBus interfaces: I2C0 is used for the power management IC and temperature sensor monitoring and control, while I2C1 is reserved for future use. An EEPROM connected on SMBus0 for VPD data is optional. A QSPI interface is available for storing boot images and metadata in NOR Flash.

5.7. Onboard Power System

The on-board power system consists of several components:

1. A hot-swap controller to manage hot-add and hot-remove
 2. A power loss detection and protection system designed to provide sufficient hold-up power to safely persist all volatile host data to non-volatile storage.
 3. A DC-DC conversion network to satisfy the component power supply rail requirements.
-

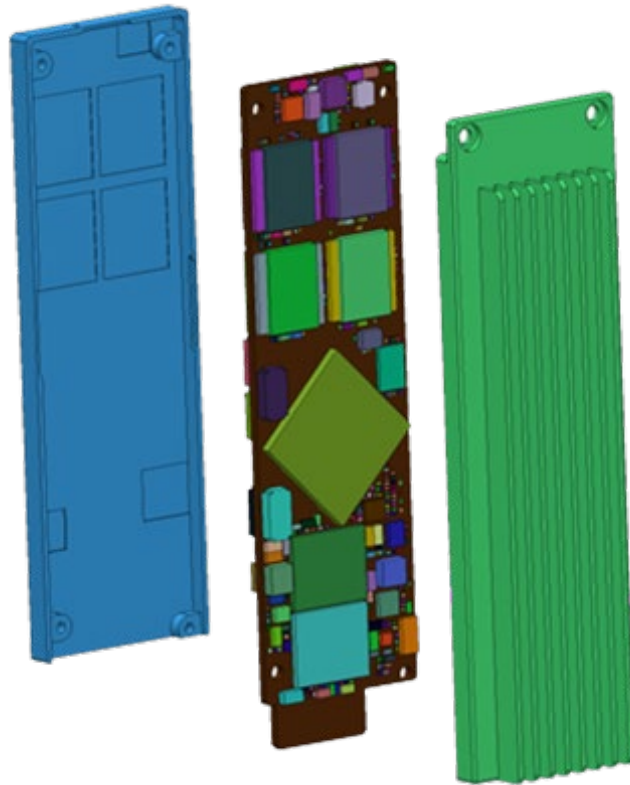
6. Design Specifications

6.1. Physical Specifications

6.1.1. E1.S Form Factor

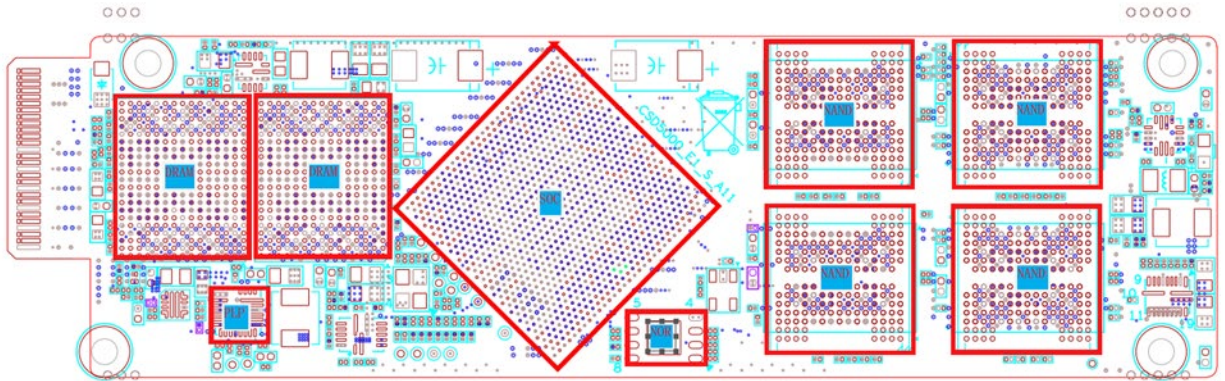
An internal view of the E1.S 15mm design is presented below:

E1.S Internal View

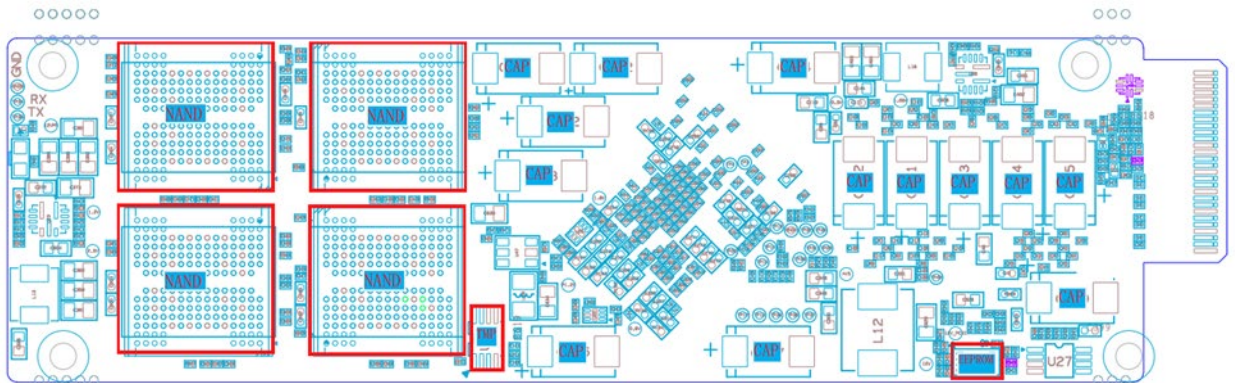


PCB views from the top and bottom are shown below:

E1.S PCB Top

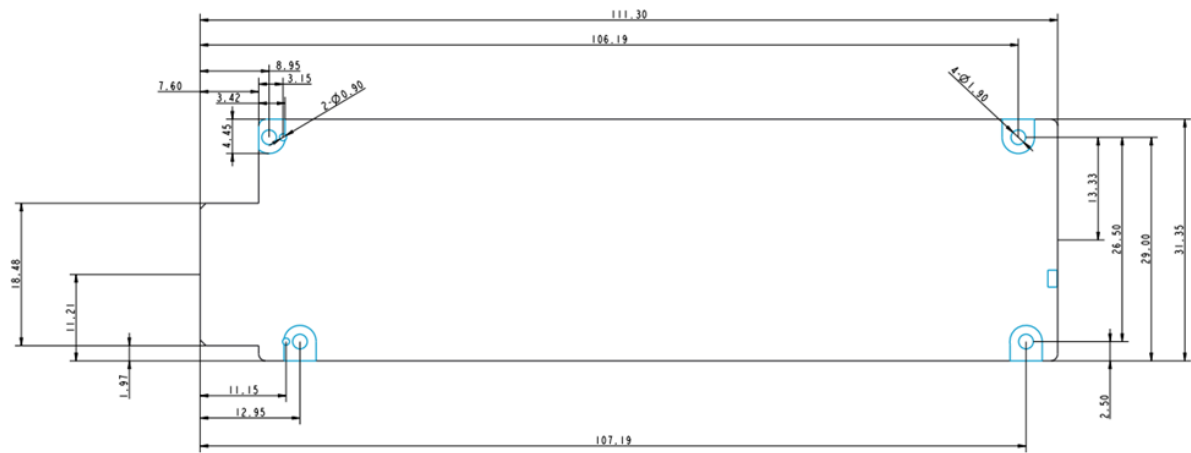


E1.S PCB Bottom



The E1.S form factor utilizes a single PCB design. The PCB is a fourteen-layer board. The internal PCB measurements are described as follows:

E1.S PCB Dimensions

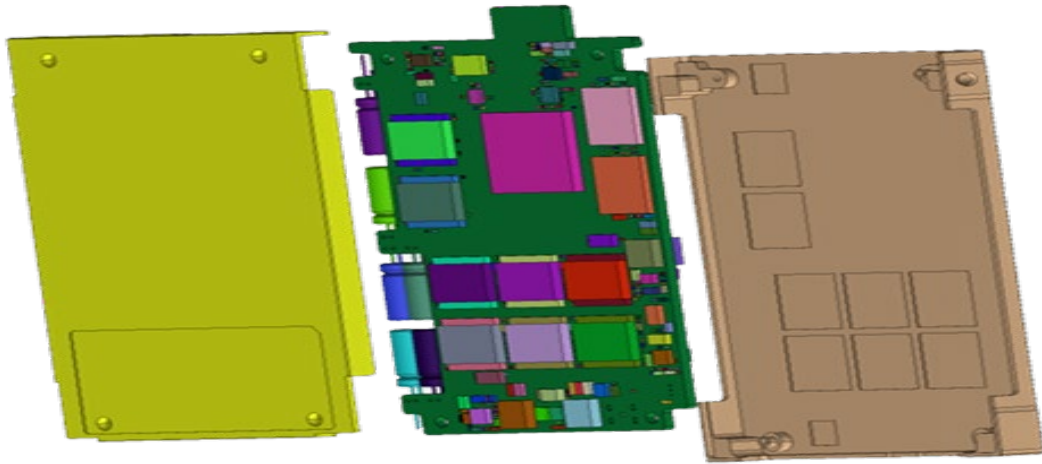


PCB Dimension	Inches	Millimeters
Length	4.37	111
Width	1.23	31.35
Thickness	0.062	1.57

6.1.2. E3.S Form Factor

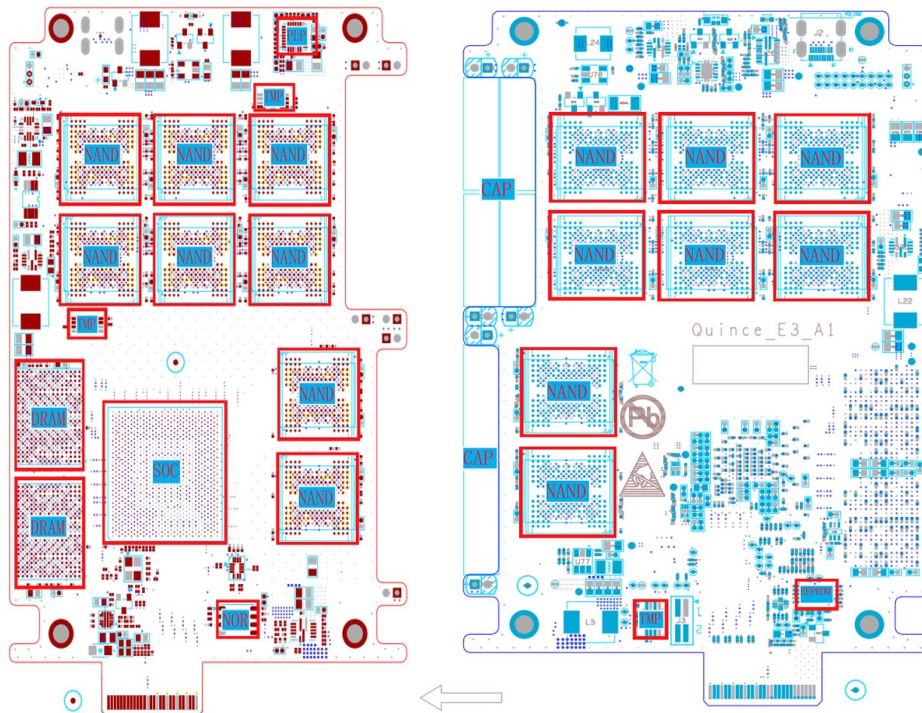
An internal view of the E3.S 15mm design is presented below:

E3.S Internal View

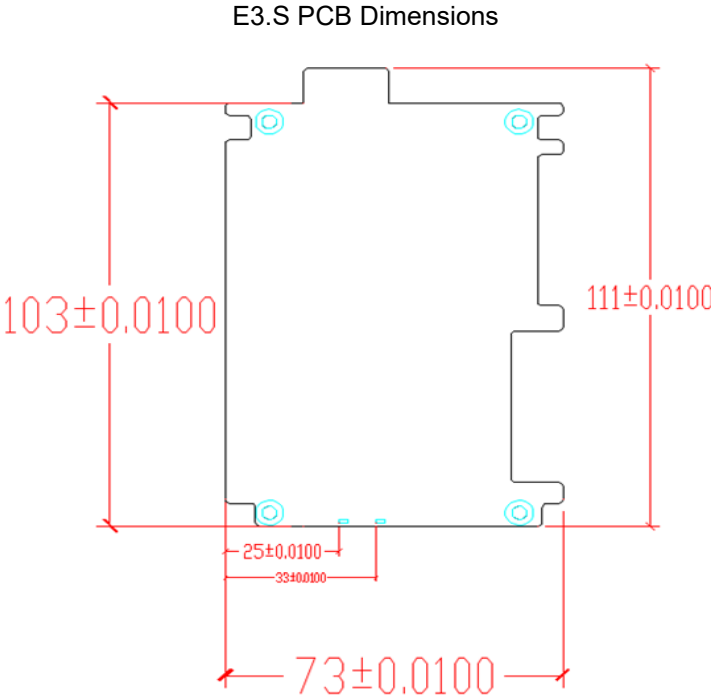


PCB views from the top and bottom are shown below:

E3.S Top and Bottom PCBs



The E3.S form factor utilizes a single PCB design. The PCB is a fourteen-layer board. The internal PCB measurements are described as follows:



PCB Dimension	Inches	Millimeters
Length	4.37	111
Width	2.874	73
Thickness	0.062	1.57

6.2. Electrical Requirements

The E1.S and E3.S designs share the same electrical requirements. These are presented in the following tables for the 12V and 3.3V AUX host supplies.

12V Power Supply Requirements

Parameter	Unit	Value	Comment
Maximum Sustained Power	W	25	Maximum power averaged over any 1s period. A device shall not consume more power than the slot power limit regardless of other settings.
Maximum Burst Power	W	37.5	Maximum power averaged over any 100 μ s period.
Maximum Slew Rate	A/ μ s	0.3	Maximum slew rate for any step current as measured at the connector. This does not include hot plug.
Maximum Inrush Current	A	2	Maximum current load drawn by the device 12V supply at the host receptacle averaged over any 5us period during the initial power-up ramp to 90% of the device operating voltage.
Maximum Inrush Capacitance	μ F	5	Capacitance system sees during the initial power-up ramp to 90% of the device operating voltage.

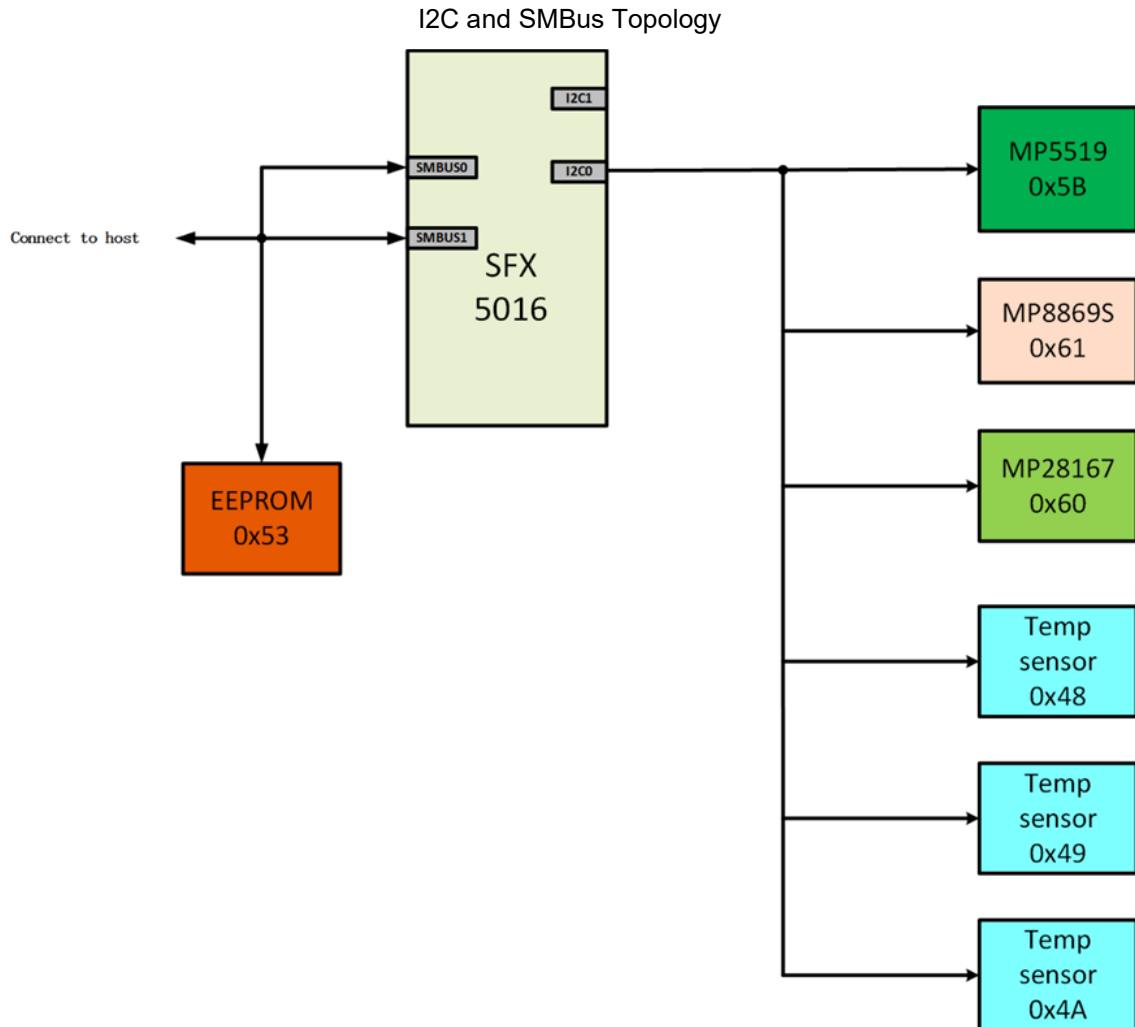
3.3V Power Supply Requirements

Parameter	Unit	Value	Comment
Supply Tolerance	V	2.97 - 3.465	Including supply ripple.
Maximum Current	mA	25	Maximum average current measured over any 100 μ s period after the supply voltage reaches its operating range.
Maximum Slew Rate	A/ μ s	0.3	Maximum slew rate for any step current as measured at the connector. This does not include hot plug.
Maximum Inrush Capacitance	μ F	5	Capacitance system sees during the initial power-up ramp to 90% of the device operating voltage.

6.3. Interfaces

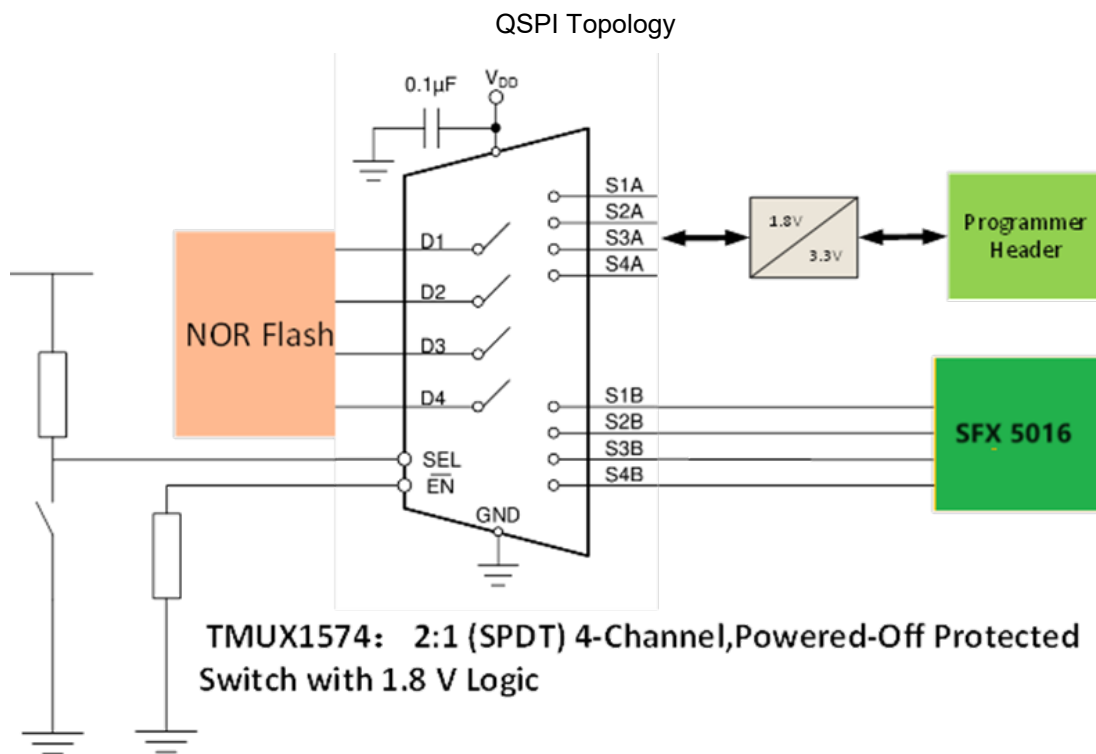
6.3.1. I2C and SMBus Interfaces

The I2C0 and SMBus topology is illustrated below with default addresses and part numbers of the connected components:



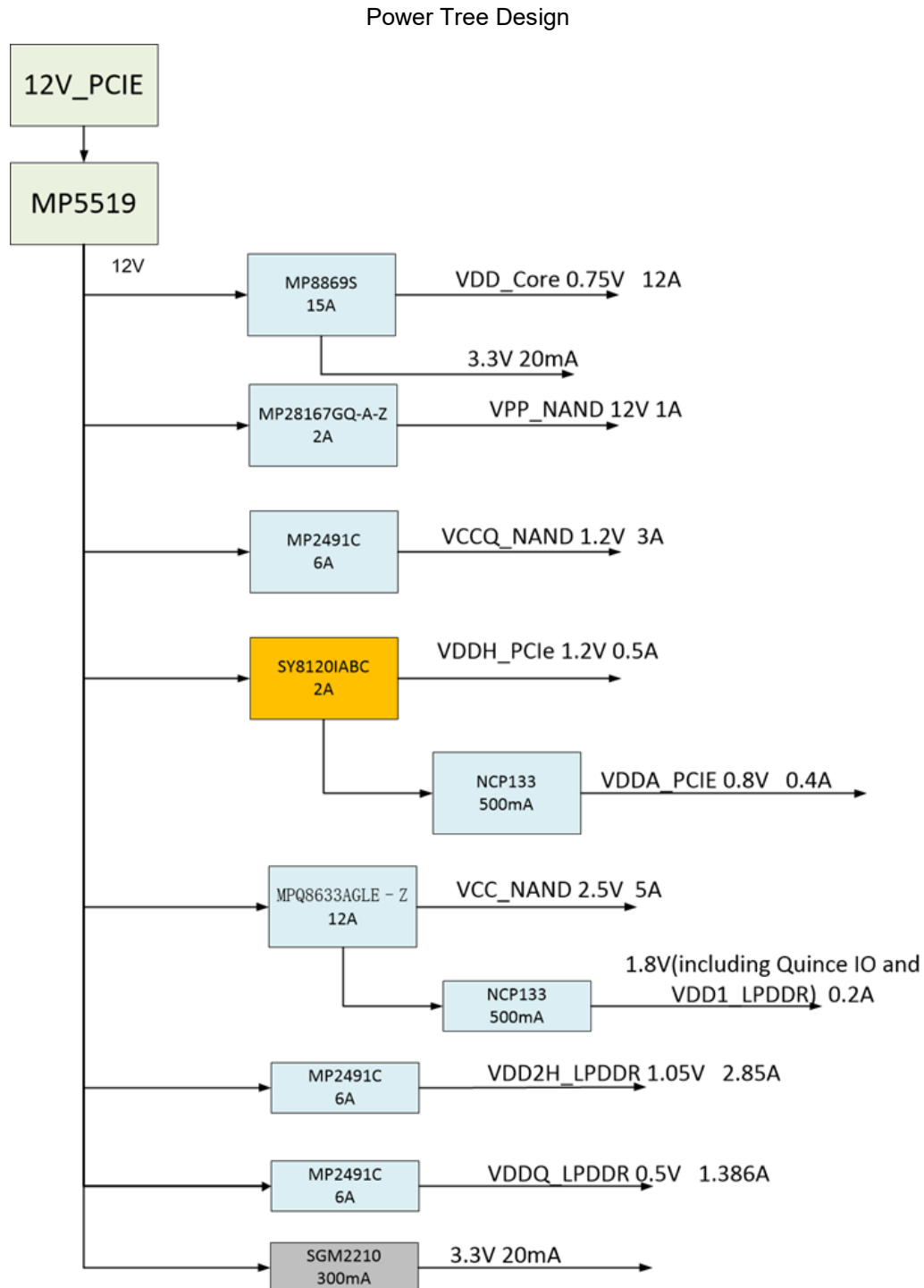
6.3.2. QSPI Interface

A QSPI interface is connected to a 128Mbit NOR flash for booting. The system design supports in-system NOR flash programming for the design phase. By default, the NOR flash is connected to a FX5016 controller. When programming is needed, the SEL signal is set low and the MUX will switch the NOR interface to the programming header (on a debug board) for NOR programming. Designs may choose to disable this feature or remove the MUX for a variety of reasons. The following figure illustrates the NOR Flash topology.

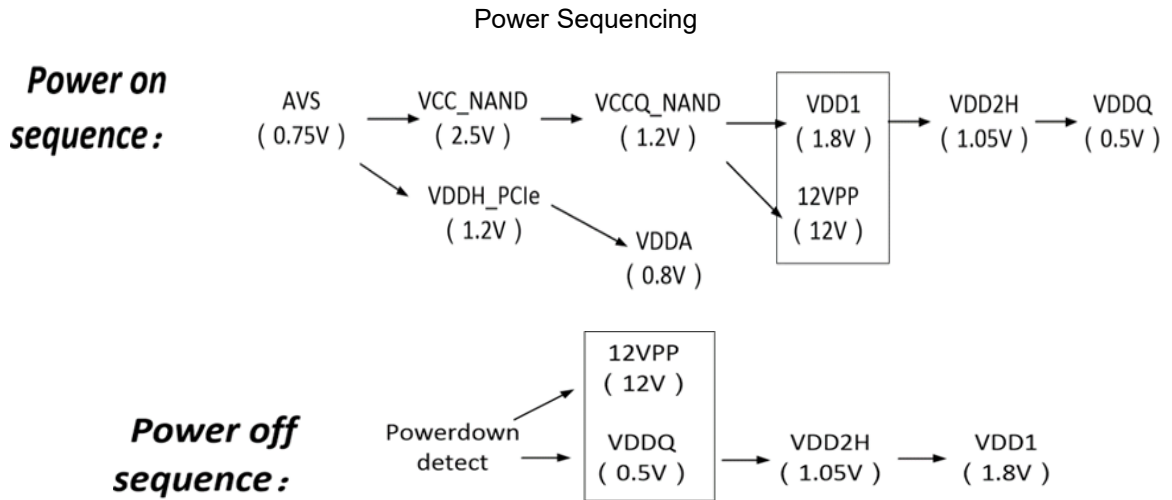


6.4. Onboard Power System

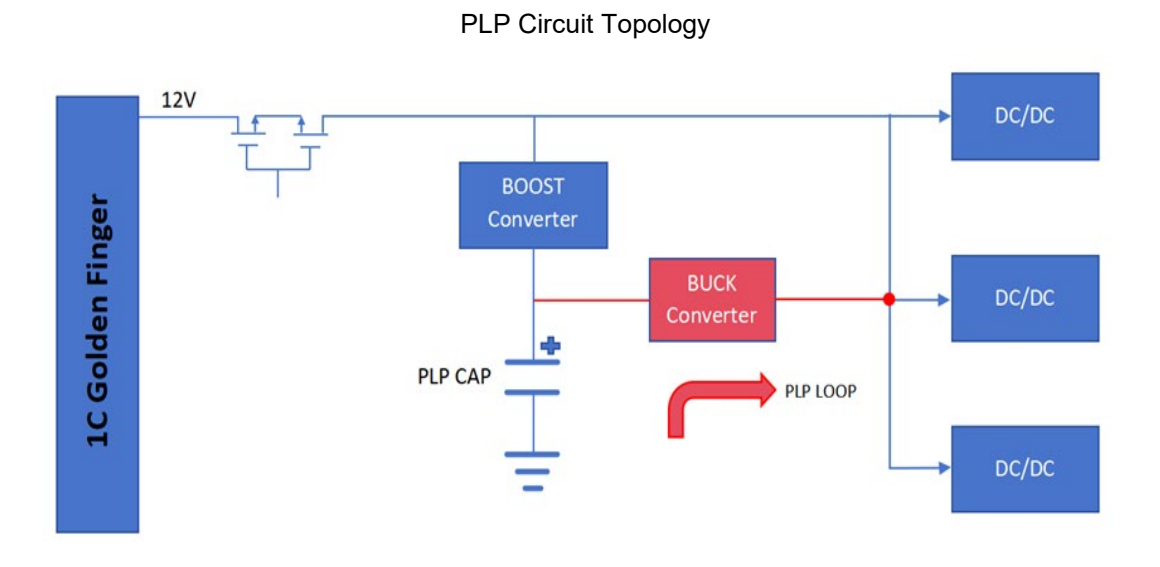
The power tree of the system is illustrated below. The power tree contains output voltage and maximum output current values.



Per each component's power up/down requirements, the system power sequence should follow the sequences illustrated as follows:



During the use of the device, unexpected power failures such as server power failure or hot swap may occur. Therefore, power loss protection (PLP) is a very important feature to secure any in-flight data. The PLP design for Catalina uses the MP5519 scheme. The basic principle is shown in the figure below. A large capacitance will be charged through a boost converter circuit in normal operation mode. If the host power supply becomes abnormal, the MOSFET will be disconnected, and the large capacitance supplies power to the DC/DC converter through a buck converter.



7. Product Specifications

All design files are included alongside this specification. The major components used in the design are described in the following table:

Major Components

Description	Manufacturer	Part Number
SOC	ScaleFlux	SFX 5016/DF02-010M-0H0
DRAM	SK hynix	H58G78BK8BX114N
NAND	KIOXIA	TH58LKT3Y48BA8S
Nor Flash	Macronix	MX25U12832FZNI02
Temperature Sensor	TI	TMP75CIDGKT
EEPROM	ST	M34E04
PLP	MPS	MP5519GR-0014-Z
Description	Manufacturer	Part Number
SOC	ScaleFlux	SFX 5016/DF02-010M-0H0

7.1. Included Design Materials

The Catalina reference design includes the following design materials for each form factor:

- Bill of Materials (BOM)
- PCB Layout [.brd]
- Component Placement Map
- Gerber Files
- Schematics [.dsn]
- 3D Models [.stp]

Appendix A - List of Related Specifications

1. NVM Express Base Specification 2.0
<https://nvmexpress.org/specifications/>
2. NVM Express NVM Command Set Specification 1.0
<https://nvmexpress.org/specifications/>
3. PCI Express Base Specification Revision 5.0, Version 1.0
<https://pcisig.com/specifications/pciexpress>
4. SFF-TA-1006 Enterprise and Datacenter 1U Short Device Form Factor (E1.S)
<https://members.snia.org/document/dl/26956>
5. SFF-TA-1008 Enterprise and Datacenter Standard Form Factor (E3)
<https://members.snia.org/document/dl/26716>
6. SFF-TA-1002 Protocol Agnostic Multi-Lane High Speed Connector
<https://members.snia.org/document/dl/27231>
7. SFF-TA-1009 Enterprise/Datacenter Standard Form Factor Pin & Signal Specification
<https://members.snia.org/document/dl/26837>
8. SFF-TA-1023 Thermal Characterization Specification for EDSFF Devices
<https://members.snia.org/document/dl/34947>
9. System Management Bus (SMBus) Specification, Version 3.1
<https://smbus.org/specs/>
10. Open NAND Flash Interface Specification, Version 5.0
<https://onfi.org/specs.html>
11. Low Power Double Data Rate (LPDDR) 5/5X (JESD209-5C)
<https://www.jedec.org/standards-documents/docs/jesd209-5c>