IM2972B CPLDs

Altera EPM2210F324
Revision 0.3
Aug 16, 2013

1.0 Overview

The IM2972 board uses two Altera MAX II CPLD to allow the main CPU to control the basic functionality of the board. Some of the features controlled by the CPLDs are: Resets, Power Sequencing, MDIO/MDC and I2C interfaces.

2.0 Internal Registers

The address maps of the CPLDs internal registers as well as register descriptions are given below.
The registers are accessed from the Host CPU thru a serial bus.
They are also accessible from a Debug port thru the SPI protocol.

Primary CPLD Registers

Table 1. Primary CPLD Registers Address Map. Selected when CARD_SEL[4:0] = 11101

Register Name	Address Offset	Host Access
P_CPLD_SIG_L	0	RO
P_CPLD_SIG_H	1	RO
P_CPLD_REV	2	RO
reserved	3	-
RST_CTL	4	R/W
MI_MX_SL	5	R/W
reserved	6 - 13	-
SYS_LED_CTL	14 (0x0E)	R/W
PWR_LED_CTL	15 (0x0F)	R/W
reserved	16 - 26	-
RS232_MUX_SELECT	27 (0x1B)	R/W
BA_CTL	28 (0x1C)	R/W
SPI_BSL	29 (0x1D)	R/W
reserved	30 (0x1E)	-
I2C_BSL	31 (0x1F)	R/W
reserved	32 – 63	-
User Flash Memory (UFM) Interface		
UFM_CTL	64 (0x40)	R/W
UFM_ADDR	65 (0x41)	R/W
UFM_DATAIN_L	66 (0x42)	R/W
UFM_DATAIN_H	67 (0x43)	R/W
UFM_DATAOUT_L	68 (0x44)	RO
UFM_DATAOUT_H	69 (0x45)	RO
reserved	70 - 71	-
LED Control Registers		
LED_CFG	72 (0x48)	R/W
reserved	73 (0x49)	-
WC0_LDAT_A	74 (0x4A)	R/W
WC0_LDAT_B	75 (0x4B)	R/W
WC1_LDAT_A	76 (0x4C)	R/W
WC1_LDAT_B	77 (0x4D)	R/W

WC2_LDAT_A	78 (0x4E)	R/W
WC2_LDAT_B	79 (0x4F)	R/W
WC3_LDAT_A	80 (0x50)	R/W
WC3_LDAT_B	81 (0x51)	R/W
WC4_LDAT_A	82 (0x52)	R/W
WC4_LDAT_B	83 (0x53)	R/W
WC5_LDAT_A	84 (0x54)	R/W
WC5_LDAT_B	85 (0x55)	R/W
WC6_LDAT_A	86 (0x56)	R/W
WC6_LDAT_B	87 (0x57)	R/W
WC7_LDAT_A	88 (0x58)	R/W
WC7_LDAT_B	89 (0x59)	R/W
WC8_LDAT_A	90 (0x5A)	R/W
WC8_LDAT_B	91 (0x5B)	R/W
WC9_LDAT_A	92 (0x5C)	R/W
WC9_LDAT_B	93 (0x5D)	R/W
WC10_LDAT_A	94 (0x5E)	R/W
WC10_LDAT_B	95 (0x5F)	R/W
WC11_LDAT_A	96 (0x60)	R/W
WC11_LDAT_B	97 (0x61)	R/W
WC12_DAT_A	98 (0x62)	R/W
WC12_LDAT_B	99 (0x63)	R/W
WC13_LDAT_A	100 (0x64)	R/W
WC13_LDAT_B	101 (0x65)	R/W
WC14_LDAT_A	102 (0x66)	R/W
WC14_LDAT_B	103 (0x67)	R/W
WC15_LDAT_A	104 (0x68)	R/W
WC15_LDAT_B	105 (0x69)	R/W
WC16_LDAT_A	106 (0x6A)	R/W
WC16_LDAT_B	107 (0x6B)	R/W
WC17_LDAT_A	108 (0x6C)	R/W
WC17_LDAT_B	109 (0x6D)	R/W
WC18_LDAT_A	110 (0x6E)	R/W
WC18_LDAT_B	111 (0x6F)	R/W
WC19_LDAT_A	112 (0x70)	R/W
WC19_LDAT_B	113 (0x71)	R/W
WC20_LDAT_A	114 (0x72)	R/W
WC20_LDAT_B	115 (0x73)	R/W
WC21_LDAT_A	116 (0x74)	R/W
WC21_LDAT_B	117 (0x75)	R/W
WC22_LDAT_A	118 (0x76)	R/W
WC22_LDAT_B	119 (0x77)	R/W
WC23_LDAT_A	120 (0x78)	R/W
WC23_LDAT_B	121 (0x79)	R/W
reserved	122 - 127	-

P_CPLD_SIG_L – CPLD Signature Low Byte, read only
This register returns the value 0x89.

P_CPLD_SIG_H – CPLD Signature High Byte, read only
This register returns the value 0.

P_CPLD_REV – CPLD Revision, read only

7	6 4	3 0
reserved	BRD_REV[2:0]	CPLD_REV[3:0]

bit 7 reserved

bits 6:4 BRD_REV[2:0] – Returns the Board Revision Level

bits 3:0 CPLD_REV[3:0] – Returns the CPLD Revision Level

RST_CTL – Reset Control

7	6	5	4	3	2	1	0
S_RST	res	res	res	res	res	res	res

bit 7 S_RST – CPLD Reset
Writing a 1 into this bit position sets all the CPLD registers to the default state.
This bit is self-clearing.

bits 6:0 reserved

MI_MX_SL – MDIO/MDC Select

7	6	5	4	3	2	1	0
res	res	res	res	res	res	MSL[1]	MSL[0]

bits 7:2 reserved

bits 1:0 MSL[1:0] – MDIO/MDC Bus Select
Selects which MI bus, from segments D, E or F, connects to the BCM56850 MI bus 3.

SYS_LED_CTL – System Status LED Control Register
Upon reset, bits 3:2 are set to 0 and bits 1:0 are set to 1.
Therefore, the status LED will be blinking green.

7	6	5	4	3	2	1	0
res	res	res	res	COL[1]	COL[0]	LC[1]	LC[0]

bits 7:4 reserved

bit 3:2 COL [1:0] – LED Color
These bits control the LED color as shown in the table below.

COL [1:0]	LED Color
00	Green
01	Yellow
10	Orange
11	Red

bits 1:0 LC[1:0] – LED ON/OFF Control

These bits control the LED state as shown in the table below.

LC[1:0]	LED ON/OFF State
00	OFF
01	ON
10	reserved
11	BLINKING

PWR_LED_CTL – Power Status LEDs Control register
Upon reset all bits are set to 0.

7	6	5	4	3	2	1	0
COL_1[1]	COL_1[0]	LC_1[1]	LC_1[0]	COL_0[1]	COL_0[0]	LC_0[1]	LC_0[0]

bits 7:6 COL_1[1:0] – LED 1 Color Control
These bits control the LED color as shown in the table below.

COL_0/1[1:0]	LED Color
00	Green
01	Yellow
10	Orange
11	Red

bits 5:4 LC_1[1:0] – LED ON/OFF Control
These bits control the LED state as shown in the table below.

LC_0/1[1:0]	LED ON/OFF State
00	OFF
01	ON
10	reserved
11	BLINKING

bits 3:2 COL_0[1:0] – LED 0 Color Control
These bits control the LED color as shown in the table above.

bits 1:0 LC_0[1:0] – LED ON/OFF Control
These bits control the LED state as shown in the table above.

RS232_MUX_SELECT –

7	6	5	4	3	2	1	0
VLD	res	res	res	res	SP_SL[2]	SP_SL[1]	SP_SL[0]

bit 7 VLD – Valid Bit
This bit must be 1 for the serial mux to be enabled.
When it is 0, the serial mux is disabled and the TX outputs are driven high.

bits 6:3 reserved

bits 2:0 SP_SL[3:0] – Serial Port Select

VLD	SP_SL[2:0]	Selected RS232 Port
1	000	Offload Board
1	001	Trident UART 0
1	010	Trident UART 1
x	011 - 110	reserved
1	111	Loop Back Mode
0	xxx	Mux disabled

BA_CTL – Bus Allocation Control (used for testing only)
This register controls the SPI, MDIO/MDC and I2C bus associations

7	6	5	4 0
EB_EN	B_MD[1]	B_MD[0]	SA_SL[4:0]

bit 7 EB_EN – Extended Bus Enable
When set to 1, the extended serial bus can be accessed thru the the SPI debug port if bypass mode is selected.

bits 6:5 B_MD[2:0] – Bus Mode
These bits determine which bus (SPI, I2C or MDIO/MDC) is associated with the debug SPI port in bypass mode (SPI_FS high)

SPI_FS	EB_EN	B_MD[1:0]	Access Initiator	Target Accessed by Serial Bus
1	0	00	Debug SPI Port	none
1	0	01	Debug SPI Port	none
1	0	10	Debug SPI Port	I2C Peripherals on IM2972 Board
1	0	11	Debug SPI Port	MDIO/MDC Peripherals on IM2972 Board
1	1	00	Debug SPI Port	Slave Cards CPLD Registers
1	1	01	Debug SPI Port	Slave Cards SPI Peripherals
1	1	10	Debug SPI Port	Slave Cards I2C Peripherals
1	1	11	Debug SPI Port	Slave Cards MDIO/MDC Peripherals

bits 4:0 SA_SL[4:0] – Slave Agent Select
Select the slave Agent to be accessed via the debug SPI port

SA_SL[4:0]	Selected Agent
00000 - 10001	IO Cards A0 to F2
10010 - 10111	reserved
11000	Offload Board
11001 - 11011	reserved
11100	IM2972 Secondary CPLD Registers
11101	IM2972 Primary CPLD Registers
11110	FAN Card
11111	Management Card

SPI_BSL – SPI Bus Select
The SPI buses are accessed only from the Debug SPI Port in bypass mode (SPI_FS high).

7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	SPI_SL[0]

bits 7:1 reserved

bit 0 SPI_SL[0] – SPI Bus select

SPI_SL[1:0]	SPI Bus Selected
0	Reserved
1	TRIDENT

I2C_BSL – I2C Bus Select

7	6	5	4	3	2	1	0
res	res	res	res	res	I2C_SL[2]	I2C_SL[1]	I2C_SL[0]

bits 7:3 reserved

bits 2:0 I2C_SL – I2C Bus select

I2C_SL[2:0]	I2C Bus Selected
000	BCM56850
001	External Power Supplies
010	reserved
011	Temperature Monitor
100	VCC_CORE regulator 0
101	VCC_CORE regulator 1
110	VCC_CORE regulator 2
111	VCC_1.0 Regulator

User Flash Memory Interface

The CPLD has an internal User Flash Memory (UFM) that can be used to store any information that needs to be retained after being reset or powered off. The UFM consists of 2 sectors, and each sector has 4096 bits of memory, organized in a 256 x 16 bit fashion. Each data word field can be written a word at a time, but it can only be written to once before any erase operation. The erase functionality of the UFM can only erase the entire sector, not a specific word.

UFM_CTL – User Flash Memory Control

7	6	5	4	3	2	1	0
res	res	OP[1]	OP[0]	SEC_SEL	DATA_VLD	OP_STOP	OP_START

bits 7:6 reserved

bits 5:4 OP[1:0] - Operation Code
This field specifies the operation to be performed.
Encodings are shown in the table below.
The software should not change this field while an operation is in progress (ST = 1).
Upon reset, all bits are set to 0.

OP[1:0]	CPLD Operation
00	UFM Read
01	UFM Write
10	UFM Sector Erase All words in the selected sector will be set to the value of 0xFFFF
11	reserved

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bit 3 SEC_SEL – Sector Select.
This bit selects either sector 0 or sector 1 of the UFM.

bit 2 DATA_VLD – UFM Data Valid, read-only
This bit is set to 1 when the data to be read is valid after a read operation completes.
This bit is provided for testing and can be ignored.

bit 1 OP-STOP
Writing a 1 into this bit position stops any operation in progress.
This bit is provided to reset the UFM access logic in case the operation does not terminate.
It is not used in normal operation.
This bit is self clearing..

bit 0 OP-START
Writing a 1 into this bit position starts an operation as specified by the OP field.
Cleared automatically when the operation is completed.

Note: When an operation is started, the host software must wait until the operation is completed (OP_START bit cleared) before reading any result or before starting another operation.

UFM_ADDR – User Flash Memory Address
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_ADDR[7:0]							

bits 7:0 UFM_ADDR – UFM Address.
This register holds the UFM address of the memory location to be accessed in a read or write operation.

UFM_DATAIN_L – User Flash Memory Data-in, Low-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_DATAIN_L[7:0]							

bits 7:0 UFM_DATAIN_L – UFM Data-in Low-Byte.
This register holds the lower byte of the data word to be written to the UFM in a write operation.

UFM_DATAIN_H – User Flash Memory Data-in, High-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0

UFM_DATAIN_H[7:0]

bits 7:0 UFM_DATAIN_H – UFM Data-in, High-Byte.
This register holds the upper byte of the data word to be written to the UFM in a write operation.

UFM_DATAOUT_L – User Flash Memory Data-out, Low-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_DATAOUT_L[7:0]							

bits 7:0 UFM_DATAOUT_L – UFM Data-out, Low-Byte.
This register holds the lower byte of the data word returned after a read operation.

UFM_DATAOUT_H – User Flash Memory Data-out, High-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_DATAOUT_H[7:0]							

bits 7:0 UFM_DATAOUT_H – UFM Data-out, High-Byte.
This register holds the upper byte of the data word returned after a read operation.

LED Control registers

LED_CFG – Led Configuration
Determines if the bits in the Cn_LDATA registers are loaded from the Trident LED data stream or if they must be loaded by software.
If bit 0 is 1, the Cn_LDATA registers must be loaded by the software.

7	6	5	4	3	2	1	0
res	res	res	res	res]	res	LD_COL	LD_ACT

bits 7:2 reserved

bit 1 LD_COL – Color Bit Load Control
If this bit is 0, the speed indication bits in the WCn_LDAT_A and WCn_LDAT_B registers are loaded from the Trident LED data stream.
If it is 1, the speed indication bits must be loaded by the software.

bit 0 LD_ACT – Activity Bit Load Control
If this bit is 0, the activity bits in the WCn_LDATA and WCn_LDAT_B registers are loaded from the Trident LED data stream.
If it is 1, the activity bits must be loaded by the software.

WC0_LDAT_A – LED Data WC0 Ports 0 and 1
This register stores the link up, activity status and speed indicator bits for ports 0 and 1 of the Trident WC0 port group.

7	6	5	4	3	2	1	0
P1_COL[1]	P1_COL[0]	P1_ACT	P1_LUP	P0_COL[1]	P0_COL[0]	P0_ACT	P0_LUP

bits 7:6 and 3:2 P1/0_COL[1:0] – Speed Indicator bits for ports 1 and 0
These bits can be loaded either from the Trident LED data stream or by software

bits 5 and 1 P1/0_ACT – Link Activity Status for Ports 1 and 0
These bits can be loaded either from the Trident LED data stream or by software

bits 4 and 0 P1/0_LUP – Link Up Status for Ports 1 and 0
These bits must be loaded by software

WC0_LDAT_B – LED Data WC0 Ports 2 and 3
This register stores the link up, activity status and speed indicator bits for ports 2 and 3 of the Trident WC0 port group.

7	6	5	4	3	2	1	0
P3_COL[1]	P3_COL[0]	P3_ACT	P3_LUP	P2_COL[1]	P2_COL[0]	P2_ACT	P2_LUP

WC1...23_LDAT_A/B – LED Data Registers for Port Groups WC1 to WC23
These registers store the link up, activity status and speed indicator bits for ports 0 to 3 of the Trident WC1 to WC23 port groups.
Their format is the same as WC0_LDAT_A and WC0_LDAT_B registers.

Secondary CPLD Registers

Table 2. Secondary CPLD Registers Address Map. Selected when CARD_SEL[4:0] = 11100

Register Name	Address Offset	Host Access
S_CPLD_SIG_L	0	RO
S_CPLD_SIG_H	1	RO
S_CPLD_REV	2	RO
reserved	3	-
RST_CTL_0	4	R/W
RST_CTL_1	5	R/W
RST_CTL_2	6	R/W
reserved	7 - 10	-
PS_CSR	11 (0x0B)	R/W
MISC_CSR	12 (0x0C)	R/W
INT_STAT_0	13 (0x0D)	RO
INT_EN_0	14 (0x0E)	R/W
INT_STAT_1	15 (0x0F)	RO
INT_EN_1	16 (0x10)	R/W
INT_STAT_2	17 (0x11)	R/W
INT_EN_2	18 (0x12)	R/W
reserved	19 - 20	-
IOC_PRES_0	21 (0x15)	RO
IOC_PRES_1	22 (0x16)	RO
IOC_PRES_2	23 (0x17)	RO
P_CTL	24 (0x18)	R/W
reserved	25 - 127	-

S_CPLD_SIG_L – CPLD Signature Low Byte, read only
This register returns the value 0x8A.
Writing any value into this register causes a reload of the Watch Dog timer.

S_CPLD_SIG_H – CPLD Signature High Byte, read only
This register returns the value 0.

S_CPLD_REV – CPLD Revision, read only

7	6 4	3 0
reserved	BRD_REV[2:0]	CPLD_REV[3:0]

bit 7 reserved

bits 6:4 BRD_REV[2:0] – Returns the Board Revision Level

bits 3:0 CPLD_REV[3:0] – Returns the CPLD Revision Level

RST_CTL_0 – Reset Control Register 0

7	6	5	4	3	2	1	0
IO_RST_C1	IO_RST_C0	IO _RST_B2	IO_RST_B1	IO_RST_B0	IO_RST_A2	IO_RST_A1	IO_RST_A0

bit 7 IO_RST_C1 – IO Card C1 reset
When this bit is set to 1, the IO card C1 is reset.
These bits must be set to 0 for normal operation.

bit 6 IO_RST_C0 – IO Card C0 reset
When this bit is set to 1, the IO card C0 is reset.
These bits must be set to 0 for normal operation.

bit 5 IO_RST_B2 – IO Card B2 reset
When this bit is set to 1, the IO card B2 is reset.
These bits must be set to 0 for normal operation.

bit 4 IO_RST_B1 – IO Card B1 reset
When this bit is set to 1, the IO card B1 is reset.
These bits must be set to 0 for normal operation.

bit 3 IO_RST_B0 – IO Card B0 reset
When this bit is set to 1, the IO card B0 is reset.
These bits must be set to 0 for normal operation.

bit 2 IO_RST_A2 – IO Card A2 reset
When this bit is set to 1, the IO card A2 is reset.
These bits must be set to 0 for normal operation.

bit 1 IO_RST_A1 – IO Card A1 reset
When this bit is set to 1, the IO card A1 is reset.
These bits must be set to 0 for normal operation.

bit 0 IO_RST_A0 – IO Card A0 reset
When this bit is set to 1, the IO card A0 is reset.

These bits must be set to 0 for normal operation.

RST_CTL_1 – Reset Control Register 1

7	6	5	4	3	2	1	0
IO_RST_F0	IO_RST_E2	IO_RST_E1	IO_RST_E0	IO_RST_D2	IO_RST_D1	IO_RST_D0	IO_RST_C2

bit 7 IO_RST_F0 – IO Card F0 reset
When this bit is set to 1, the IO card F0 is reset.
These bits must be set to 0 for normal operation.

bit 6 IO_RST_E2 – IO Card E2 reset
When this bit is set to 1, the IO card E2 is reset.
These bits must be set to 0 for normal operation.

bit 5 IO_RST_E1 – IO Card E1 reset
When this bit is set to 1, the IO card E1 is reset.
These bits must be set to 0 for normal operation.

bit 4 IO_RST_E0 – IO Card E0 reset
When this bit is set to 1, the IO card E0 is reset.
These bits must be set to 0 for normal operation.

bit 3 IO_RST_D2 – IO Card D2 reset
When this bit is set to 1, the IO card D2 is reset.
These bits must be set to 0 for normal operation.

bit 2 IO_RST_D1 – IO Card D1 reset
When this bit is set to 1, the IO card D1 is reset.
These bits must be set to 0 for normal operation.

bit 1 IO_RST_D0 – IO Card D0 reset
When this bit is set to 1, the IO card D0 is reset.
These bits must be set to 0 for normal operation.

bit 0 IO_RST_C2 – IO Card C2 reset
When this bit is set to 1, the IO card C2 is reset.
These bits must be set to 0 for normal operation.

RST_CTL_2 – Reset Control Register 2

7	6	5	4	3	2	1	0
BSC	OL_PERST	OL _RST	MPHY_RST	res	res	IO_RST_F2	IO_RST_F1

bit 7 BSC – Trident Reset
When set to 1, the Trident device is reset.
This bit must be set to 0 for normal operation.

bit 6 OL_PERST – Offload Board PCIE Reset.
When set to 1, the Offload board PERST_N signal is asserted.
This bit must be set to 0 for normal operation.

bit 5 OL_RST – Offload Board Reset.
When set to 1, the Offload board is reset.
This bit must be set to 0 for normal operation.

bit 4 MPHY_RST– management PHY Reset.
When set to 1, the management PHY device is reset.
This bit must be set to 0 for normal operation.

bits 3:2 reserved

bit 1 IO_RST_F2 – IO Card F2 reset
When this bit is set to 1, the IO card F2 is reset.
These bits must be set to 0 for normal operation.

bit 0 IO_RST_F1 – IO Card F1 reset
When this bit is set to 1, the IO card F1 is reset.
These bits must be set to 0 for normal operation.

MISC_CSR - Miscellaneous Control and Status

7	6	5	4	3	2	1	0
1V0R_ALRT	CR2_ALRT	CR1_ALRT	CR0_ALRT	TM_OVERT	TM_ALERT	PWR_SD	PWR_OFF

bit 7 1V0R_ALRT – VCC 1.0V Regulator Alert

bit 6 CR2_ALRT – VCC Core Regulator 2 Alert

bit 5 CR1_ALRT – VCC Core Regulator 1 Alert

bit 4 CR0_ALRT – VCC Core Regulator 0 Alert

bit 3 TM_OVERT – Over temperature status from Temperature Monitor.
Returns a 1 when the OVERT signal from the temperature monitor is active.

bit 2 TM_ALERT – Alert Status from Temperature Monitor
Returns a 1 when the ALERT signal from the temperature monitor is active.

bit 1 PWR _SD – Power shut down
When a 1 is written into this bit position, the power regulators are turned OFF and then ON again.

bit 0 PWR_OFF – Power OFF
Writing a 1 into this bit position turns OFF the power modules

PS_CSR – Pluggable Power Supply Control and Status Register 0.

7	6	5	4	3	2	1	0
PS1_PRSNT	PS1_OK	PS1_INT	PS1_OFF	PS0_PRSNT	PS0_OK	PS0_INT	PS0_OFF

bit 7 PS1_PRSNT- Pluggable Power Supply 1 Present.
If this bit is 0, then bits 6:5 are meaningless.

bit 6 PS1_OK – PS 1 Power OK
This bit returns a 1 when AC input power & DC output power from Power Supply 1 is ok.

bit 5 PS1_INT – PS 1 Interrupt
This bit is 1 when Power Supply 1 interrupt signal is asserted.

bit 4 PS1_OFF – Power Supply 1 ON/OFF Control
This bit is effective only when the pluggable Emerson power supplies are used.

Power Supply 1 is ON when this bit is 0; setting it to 1 turns it OFF.
Upon reset, it is set to 0.

bit 3 PS0_PRSNT - Pluggable Power Supply 0 Present.
If this bit is 0, then bits 2:1 are meaningless.

bit 2 PS0_OK – PS 0 Power OK
This bit returns a 1 when AC input power & DC output power from Power Supply 0 is ok.

bit 1 PS0_INT – PS 0 Interrupt
This bit is 1 when Power Supply 0 interrupt signal is asserted.

bit 0 PS0_OFF – Power Supply 0 ON/OFF Control
This bit is effective only when the pluggable Emerson power supplies are used.
Power Supply 0 is ON when this bit is 0; setting it to 1 turns it OFF.
Upon reset, it is set to 0.

INT_EN_0 – Interrupt Enable Register 0
When any bit is set to 1 and the corresponding bit in the INT_STAT_0 register is 1, the interrupt signal to the Host CPU board is asserted.

INT_STAT_0 – Interrupt Status 0, read-only

7	6	5	4	3	2	1	0
IO_C1	IO_C0	IO_B2	IO_B1	IO_B0	IO_A2	IO_A1	IO_A0

bits 7:0 IO_xy – IO Interrupt Status
Each bit returns a 1 when the interrupt signal from the corresponding IO card is active.

INT_EN_0 – Interrupt Enable Register 0
When any bit is set to 1 and the corresponding bit in the INT_STAT_1 register is 1, the interrupt signal to the Host CPU board is asserted.

INT_STAT_1 – Interrupt Status 1, read-only

7	6	5	4	3	2	1	0
IO_F0	IO_E2	IO_E1	IO_E0	IO_D2	IO_D1	IO_D0	IO_C2

bits 7:0 IO_xy – IO Interrupt Status
Each bit returns a 1 when the interrupt signal from the corresponding IO card is active.

INT_EN_1 – Interrupt Enable Register 1
When any bit is set to 1 and the corresponding bit in the INT_STAT_1 register is 1, the interrupt signal to the Host CPU board is asserted.

INT_STAT_2 – Interrupt Status 2, read-only

7	6	5	4	3	2	1	0
ON_OFF_INT	PS_INT	MGT	FAN_EV	OL_INT	TEMP_EV	IO_F2	IO_F1

bit 7 ON_OFF_INT - ON-OFF Push Button Pressed

Set to 1 when the system is powered and the ON-OFF switch is pressed for 3 seconds.
Cleared by writing a 1 into this bit position.

bit 6 PS_INT – Power Supply Interrupt
Returns a 1 when the INT signal from an external power supply module (bits 1,5 of PS_CSR) or the ALERT signal from a High Power regulator (bits 4,5,6,7 of MISC_CSR) is active

bit 5 MGT – Management PHY Interrupt
Returns a 1 when the Management PHY Interrupt signal is active.

bit 4 FAN_EV– FAN Event
Returns a 1 when the FAN_EV signal from the FAN card is active

bit 3 OL_INT – Offload Board Interrupt
Returns a 1 when the Interrupt signal from the Offload board is active

bit 2 TEMP_EV – Temperature Event from Temperature Monitor.
Returns a 1 when either the ALERT or the OVERT signal from the temperature monitor is active.

bits 1:0 IO_Fn – IO Interrupt Status
Each bit returns a 1 when the interrupt signal from the corresponding IO card is active.

INT_EN_2 – Interrupt Enable Register 2
When any bit is set to 1 and the corresponding bit in the INT_STAT_2 register is 1, the interrupt signal to the Host CPU board is asserted.

IOC_PRES_0 – IO Card Presence Status 0
A bit returns a 1 when the corresponding card is inserted in the bus slot.

7	6	5	4	3	2	1	0
PRES_C1	PRES_C0	PRES_B2	PRES_B1	PRES_B0	PRES_A2	PRES_A1	PRES_A0

bits 7:0 PRES_xy
A bit returns a 1 when the corresponding IO card is present

IOC_PRES_1 – IO Card Presence Status 1
A bit returns a 1 when the corresponding card is inserted in the bus slot.

7	6	5	4	3	2	1	0
PRES_F0	PRES_E2	PRES_E1	PRES_E0	PRES_D2	PRES_D1	PRES_D0	PRES_C2

bits 7:0 PRES_xy
A bit returns a 1 when the corresponding IO card is present

IOC_PRES_2 – IO Card Presence Status 2
A bit returns a 1 when the corresponding card is inserted in the bus slot.

7	6	5	4	3	2	1	0
res	res	res	res	res	res	PRES_F2	PRES_F1

bits 7:2 reserved

bits 1:0 PRES_xy
A bit returns a 1 when the corresponding IO card is present

The following register is used for testing the power regulators.

P_CTL – Power Control
This register controls all the power regulators when the Byte Blaster is connected to the SPI debug port.
If bit 0 is set to 1, the CPLD will perform the power up sequence.
If it is 0, bits 1 to 3 of this register control the enable pins of the
individual power regulators.
bits 7:4 reserved
bit 3 en_1v0_td
bit 2 en_core_td
bit 1 en_3v3
bit 0 en_pwr_seq

4.0 Timing Diagrams

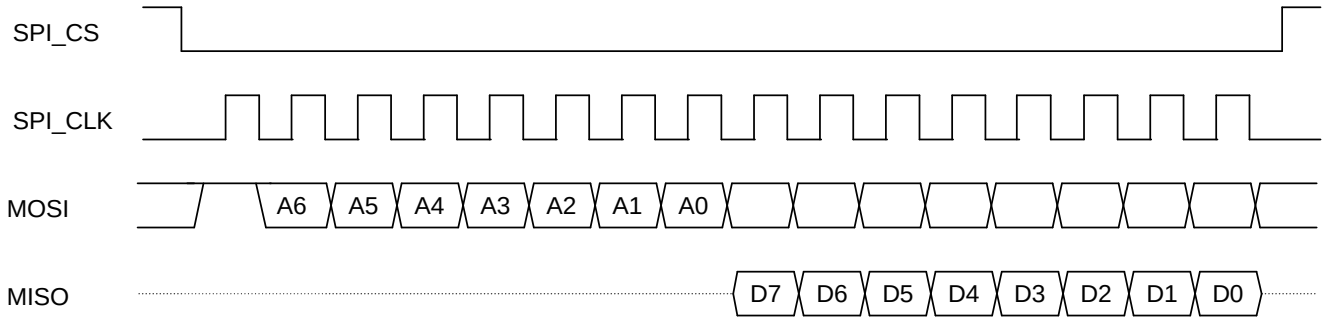


Figure 3-1. Debug SPI Port Read Access, 7-bit Address, 8-bit Data

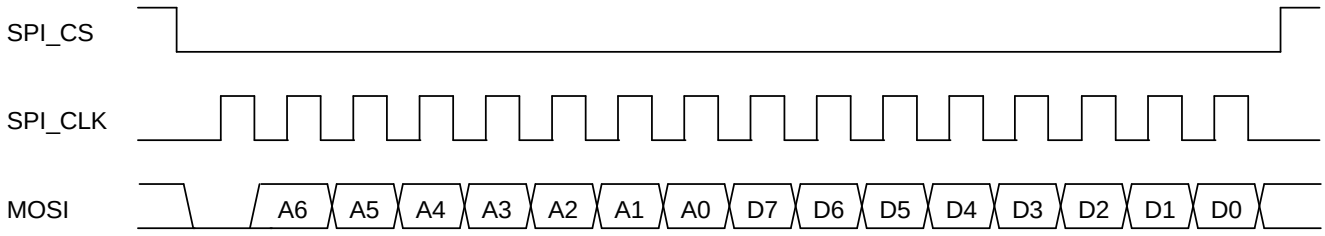


Figure 3-2. Debug SPI Port Write Access, 7-bit Address, 8-bit Data

4.0 History

Document Rev	Changes
0.2	LED registers format

0.3	