IM13042A

Table of Contents

Page 01 ..... Table of Contents
Page 02 ..... Block Diagram
Page 03 ..... IO Connectors
Page 04 ..... COMX connector
Page 05 ..... Winbond I/O
Page 06 ..... RJ45, VGA & FAN
Page 07 ..... CPLD
Page 08 ..... Power Regulation
Page 09 ..... Power Sequence & consumption
Page 10 ..... History

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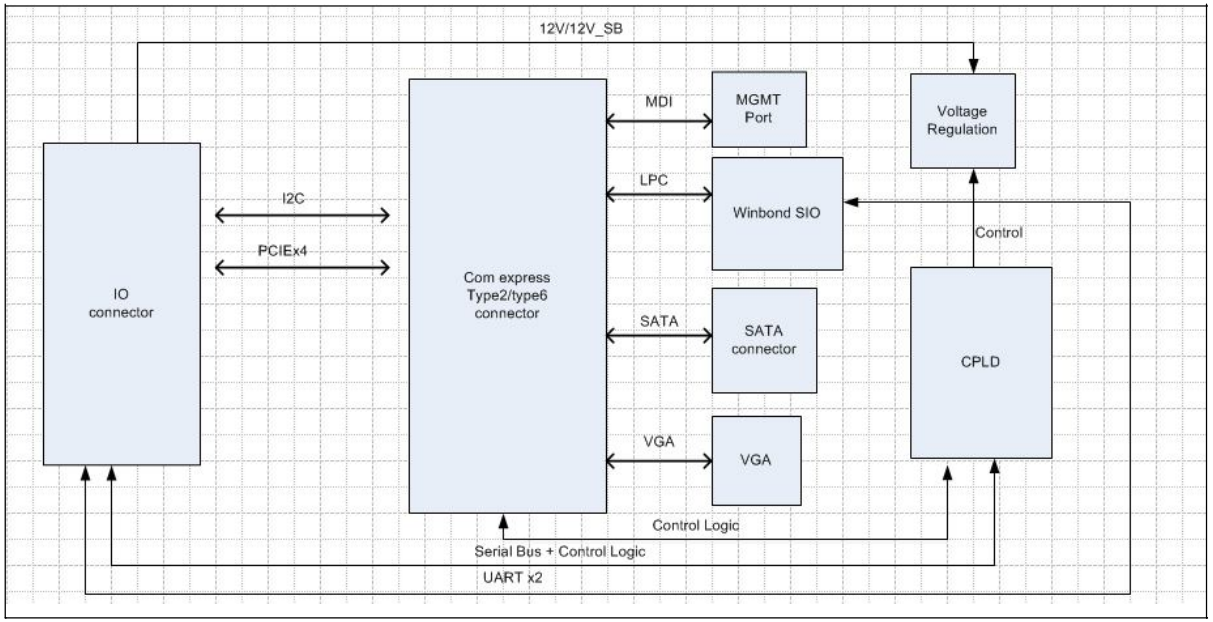
Interface Masters, Inc.
150 East Brokaw Road
San Jose, CA 95112
www.interfacemasters.com

Title: Table of Contents

Customer Name: **Interface Masters**

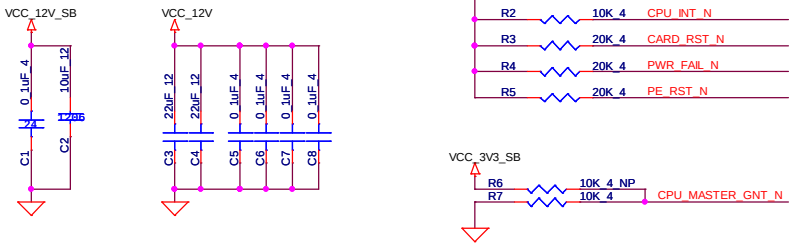
Size	DWG NO	Rev
	IM13042A	13

Scale	Date	Sheet
None	Thursday, July 11, 2013	1 of 10



Interface Masters, Inc.		
Title: Block Diagram		
Size: Custom	Document Number: IM13042A	Rev: 13
Date: Thursday, July 11, 2013	Sheet 2 of 10	

Even pins are on the component side.
Odd pins are on the solder side.



All PCIE pairs are 85 ohm differential pairs.

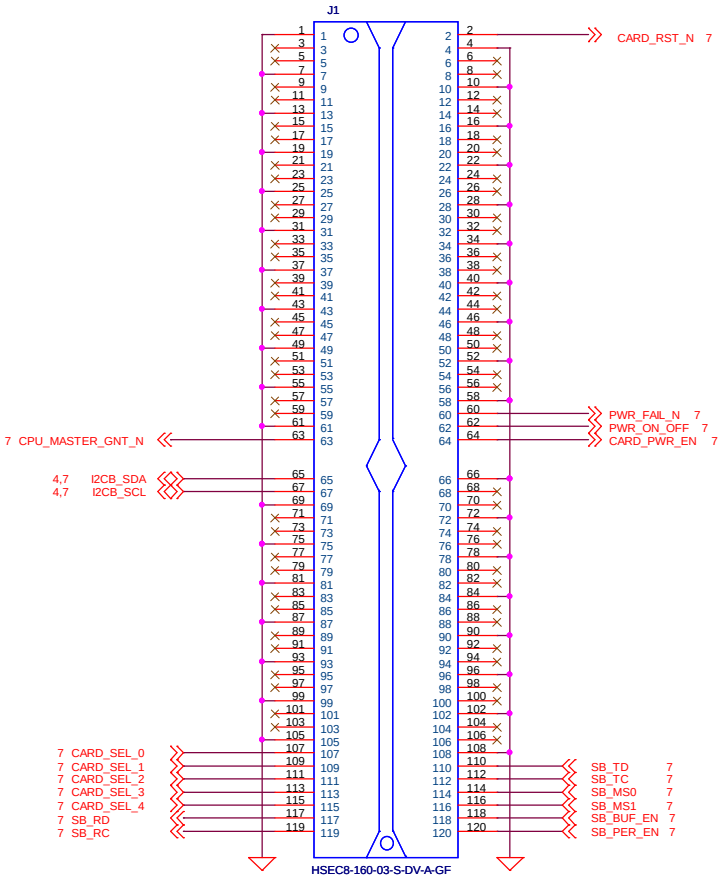
PCIE clock pairs are 100 ohm differential pairs.

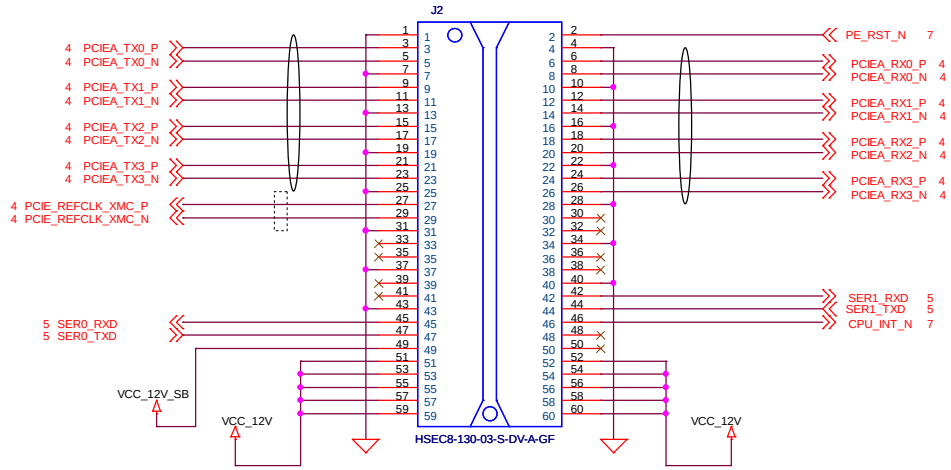
- CARD_PWR_EN enables the card power-up sequencing when the card is a slave

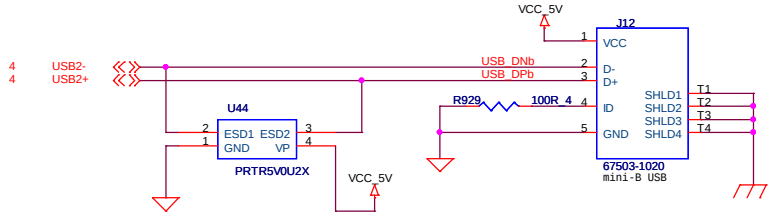
High = Enabled, Low = Disabled

- PWR_ON_OFF can be used to control the main power supply. It is pulled low temporarily to either turn ON or turn OFF the power supply.

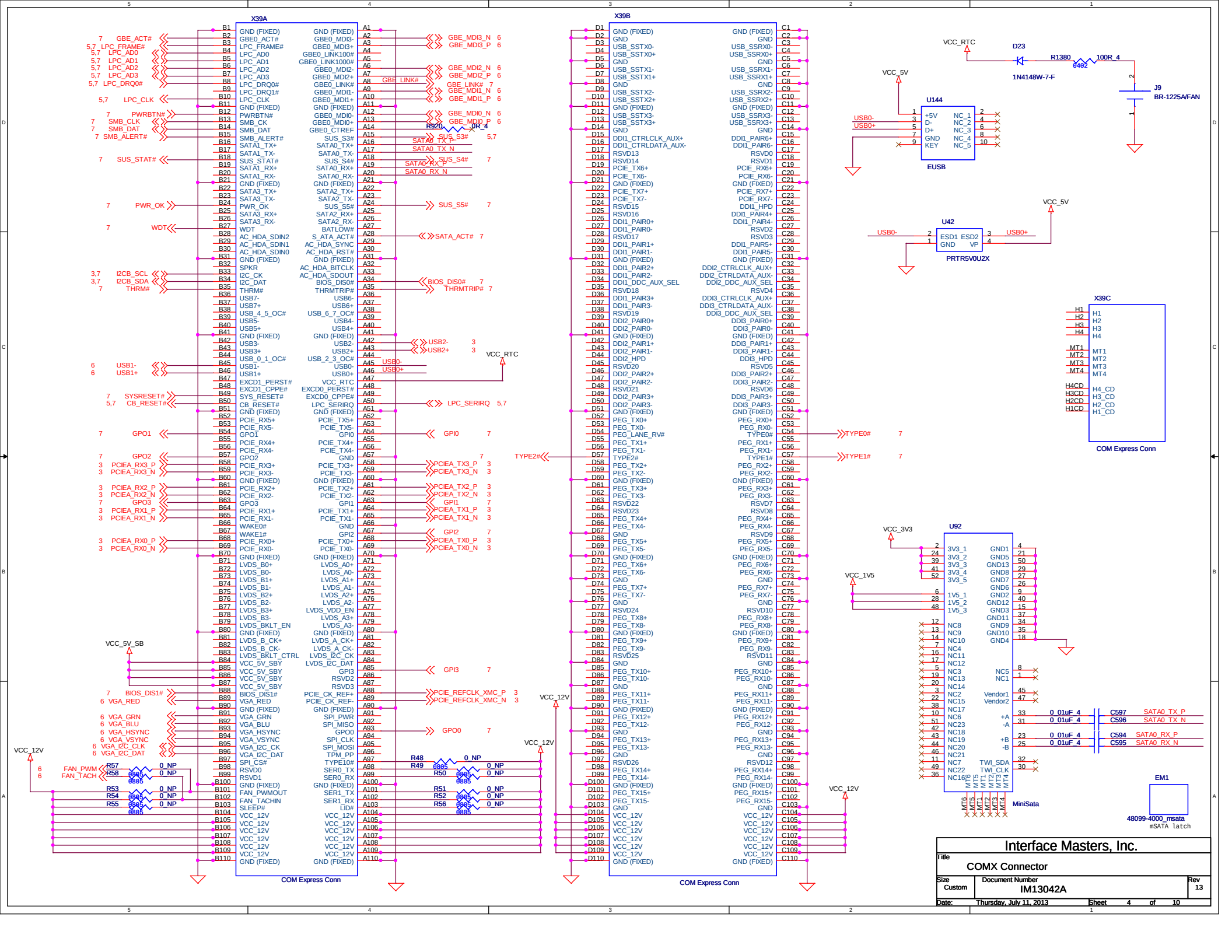
- MASTER_GNT_N indicates that the request to be master has been granted.

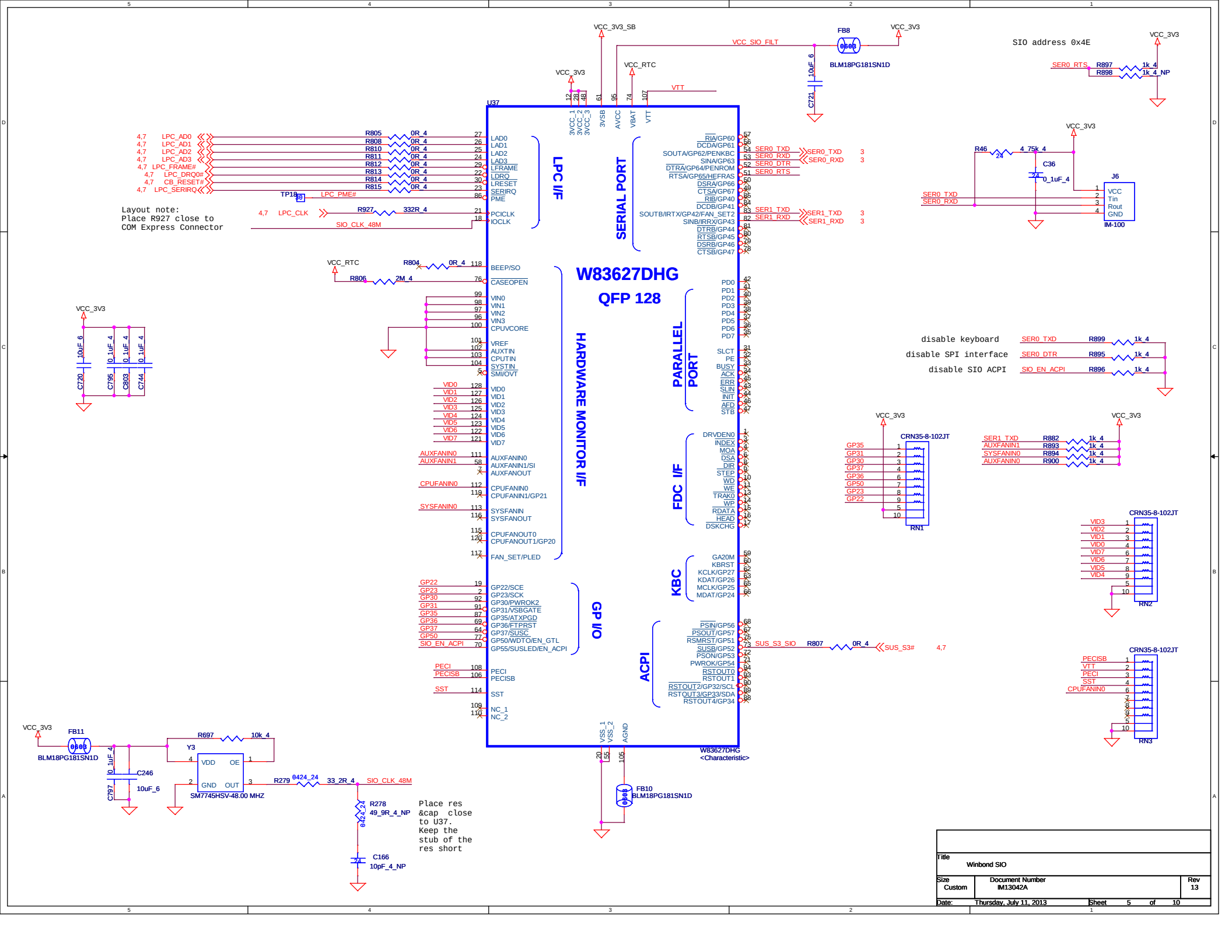


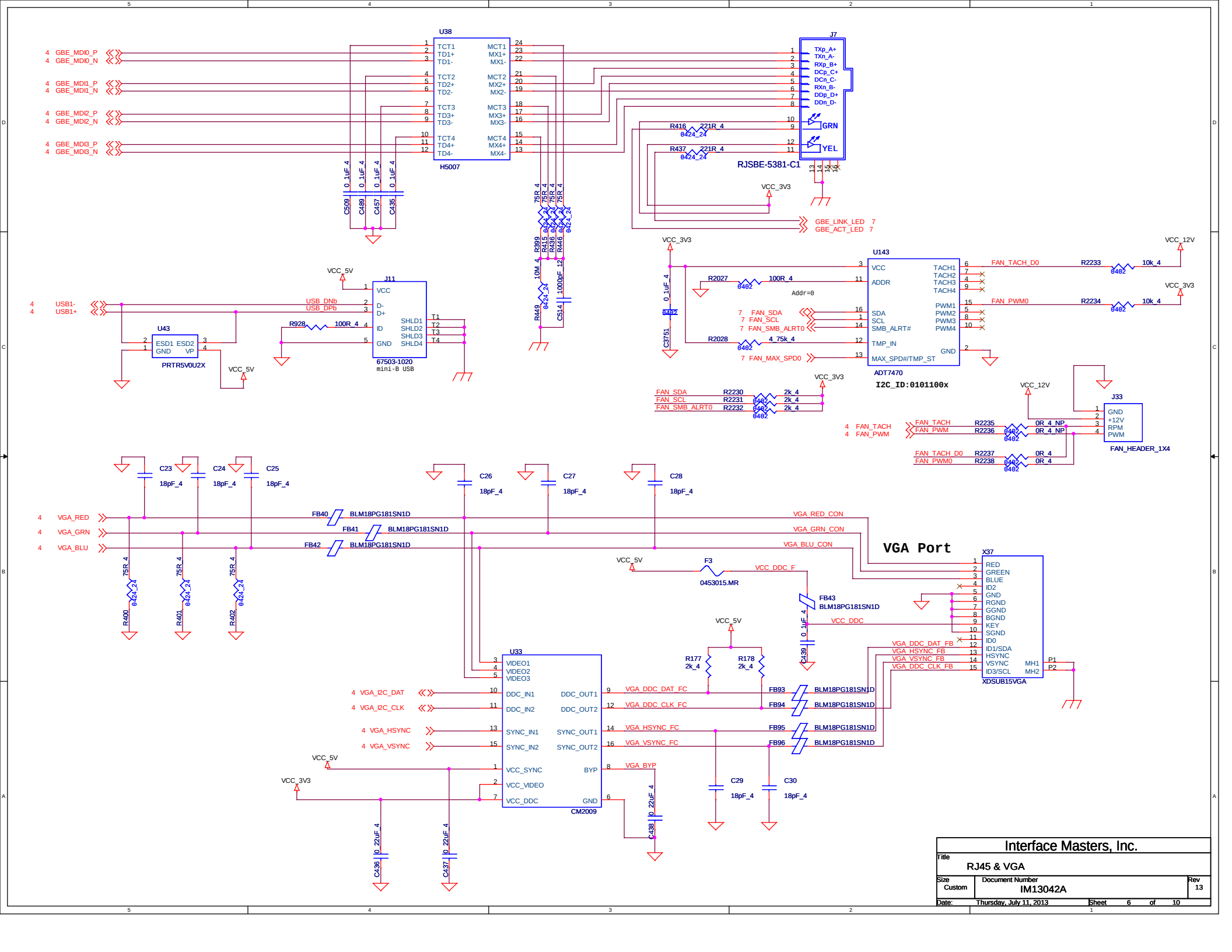


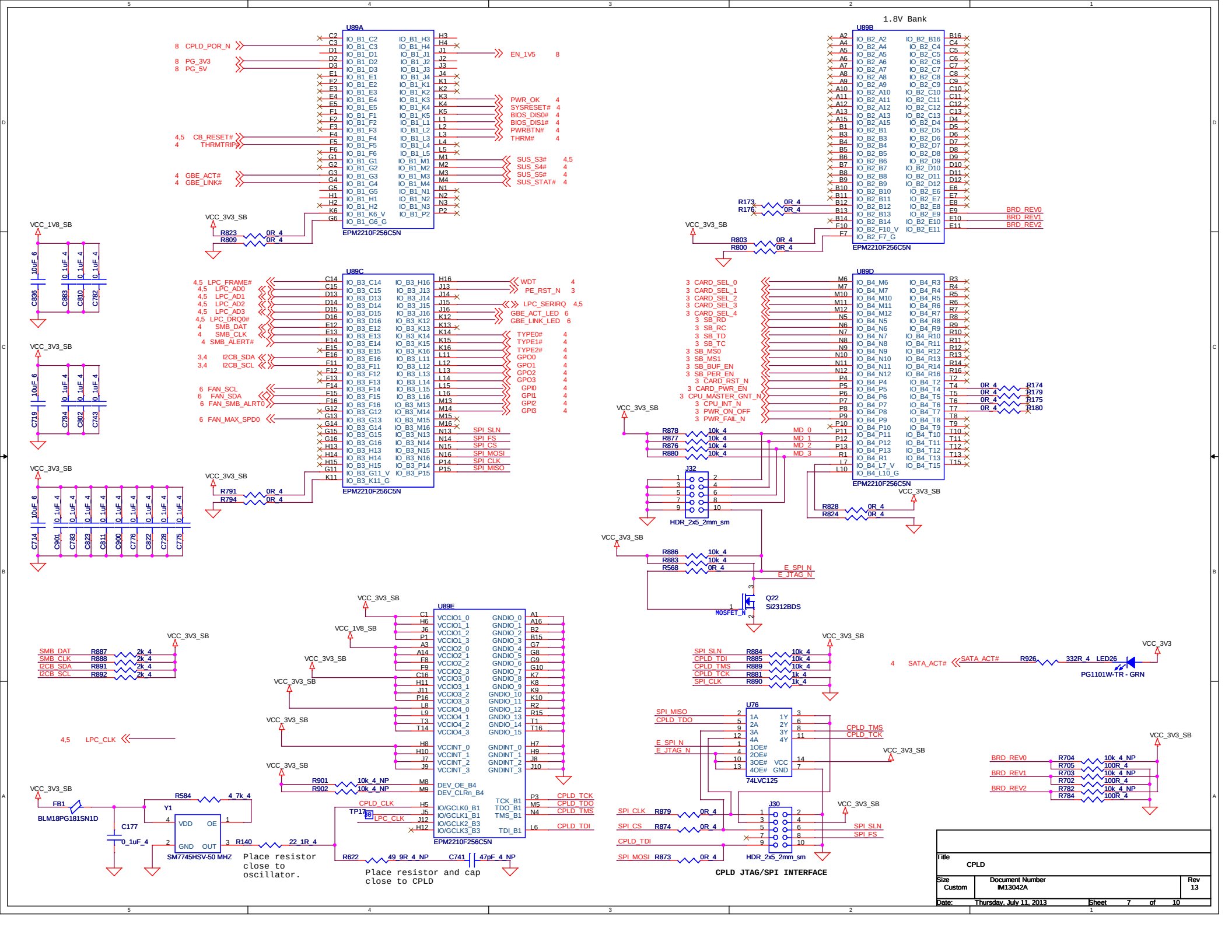


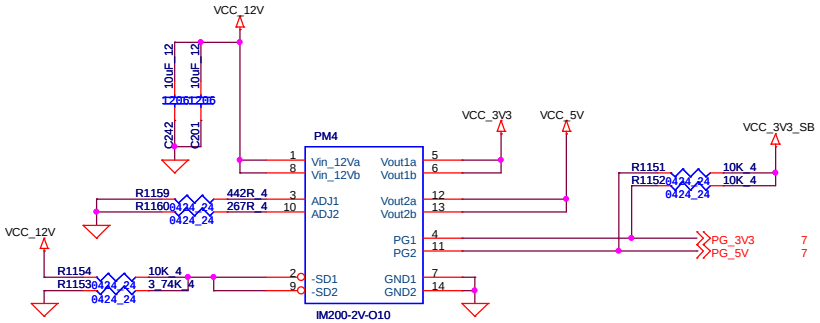
Interface Masters, Inc.		
Title: Gold Finger		
Size: Custom	Document Number: IM13042A	Rev: 13
Date: Thursday, July 11, 2013	Sheet 3 of 10	

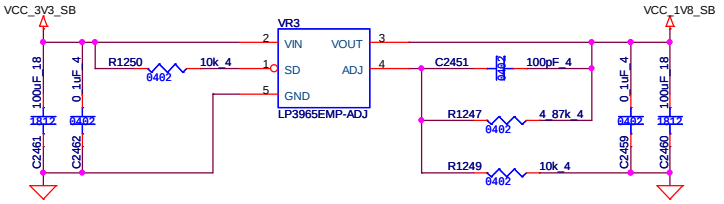

X39A
X39B
X39C
COM Express Conn
COM Express Conn
COM Express Conn
VCC_RTC
VCC_5V
VCC_5V_SB
VCC_12V
VCC_3V3
VCC_1V5
D23
1N4148W-7-F
R1380
100R_4
0402
J9
BR-1225A/FAN
U144
EUSB
U42
PRTR5V0U2X
U92
MiniSata
EM1
48099-4000_msata
mSATA latch
R920
0R_4
R48
R49
R50
R51
R52
R56
R57
R58
R53
R54
R55
0_NP
0805
C597
C596
C594
C595
0_01uF_4
SATA0_TX_P
SATA0_TX_N
SATA0_RX_P
SATA0_RX_N
GBE_MDI3_N
GBE_MDI3_P
GBE_MDI2_N
GBE_MDI2_P
GBE_MDI1_N
GBE_MDI1_P
GBE_MDI0_N
GBE_MDI0_P
GBE_LINK#
SUS_S3#
SUS_S4#
SUS_S5#
SATA_ACT#
BIOS_DIS0#
THRMTRIP#
USB2-
USB2+
USB0-
USB0+
LPC_SERIRQ
GPI0
GPI1
GPI2
GPI3
GPO0
PCIEA_TX3_P
PCIEA_TX3_N
PCIEA_TX2_P
PCIEA_TX2_N
PCIEA_TX1_P
PCIEA_TX1_N
PCIEA_TX0_P
PCIEA_TX0_N
PCIE_REFCLK_XMC_P
PCIE_REFCLK_XMC_N
TYPE0#
TYPE1#
TYPE2#
GBE_ACT#
LPC_FRAME#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ0#
LPC_CLK
PWRBTN#
SMB_CLK
SMB_DAT
SMB_ALERT#
SUS_STAT#
PWR_OK
WDT
I2CB_SCL
I2CB_SDA
THRM#
USB1-
USB1+
SYSRESET#
CB_RESET#
GPO1
GPO2
PCIEA_RX3_P
PCIEA_RX3_N
PCIEA_RX2_P
PCIEA_RX2_N
GPO3
PCIEA_RX1_P
PCIEA_RX1_N
PCIEA_RX0_P
PCIEA_RX0_N
BIOS_DIS1#
VGA_RED
VGA_GRN
VGA_BLU
VGA_HSYNC
VGA_VSYNC
VGA_I2C_CLK
VGA_I2C_DAT
FAN_PWM
FAN_TACH
Interface Masters, Inc.
Title
COMX Connector
Size
Custom
Document Number
IM13042A
Rev
13
Date:
Thursday, July 11, 2013
Sheet
4
of
10

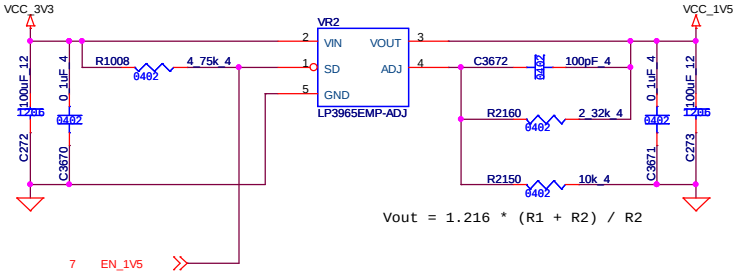

W83627DHG
QFP 128
W83627DHG
<Characteristic>
U37
LPC I/F
SERIAL PORT
HARDWARE MONITOR I/F
PARALLEL PORT
FDC I/F
KBC
GP IO
ACPI
Layout note:
Place R927 close to
COM Express Connector
SIO address 0x4E
disable keyboard
disable SPI interface
disable SIO ACPI
Place res
&cap close
to U37.
Keep the
stub of the
res short
SM7745HSV-48.00 MHZ
BLM18PG181SN1D
CRN35-8-102JT
IM-100
Winbond SIO
Size
Custom
Document Number
IM13042A
Rev
13
Date:
Thursday, July 11, 2013
Sheet
5
of
10

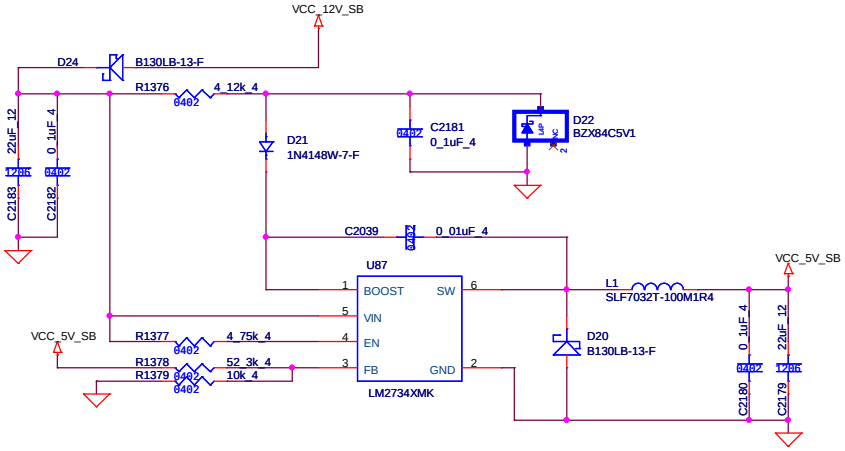

U38
H5007
J7
RJSBE-5381-C1
GRN
YEL
GBE_MDI0_P
GBE_MDI0_N
GBE_MDI1_P
GBE_MDI1_N
GBE_MDI2_P
GBE_MDI2_N
GBE_MDI3_P
GBE_MDI3_N
GBE_LINK_LED
GBE_ACT_LED
VCC_3V3
U143
ADT7470
I2C_ID:0101100x
Addr=0
FAN_TACH_D0
FAN_PWM0
FAN_SDA
FAN_SCL
FAN_SMB_ALRT0
FAN_MAX_SPD0
FAN_TACH
FAN_PWM
J33
FAN_HEADER_1X4
VCC_12V
VCC_5V
J11
67503-1020
mini-B USB
U43
PRTR5V0U2X
USB1-
USB1+
USB_DNb
USB_DPb
VGA Port
X37
XDSUB15VGA
VGA_RED
VGA_GRN
VGA_BLU
VGA_RED_CON
VGA_GRN_CON
VGA_BLU_CON
BLM18PG181SN1D
VCC_DDC_F
0453015.MR
VCC_DDC
VGA_DDC_DAT_FB
VGA_HSYNC_FB
VGA_VSYNC_FB
VGA_DDC_CLK_FB
U33
CM2009
VGA_I2C_DAT
VGA_I2C_CLK
VGA_HSYNC
VGA_VSYNC
VGA_BYP
VCC_SYNC
VCC_VIDEO
VCC_DDC
VGA_DDC_DAT_FC
VGA_DDC_CLK_FC
VGA_HSYNC_FC
VGA_VSYNC_FC
Interface Masters, Inc.
RJ45 & VGA
IM13042A
Thursday, July 11, 2013

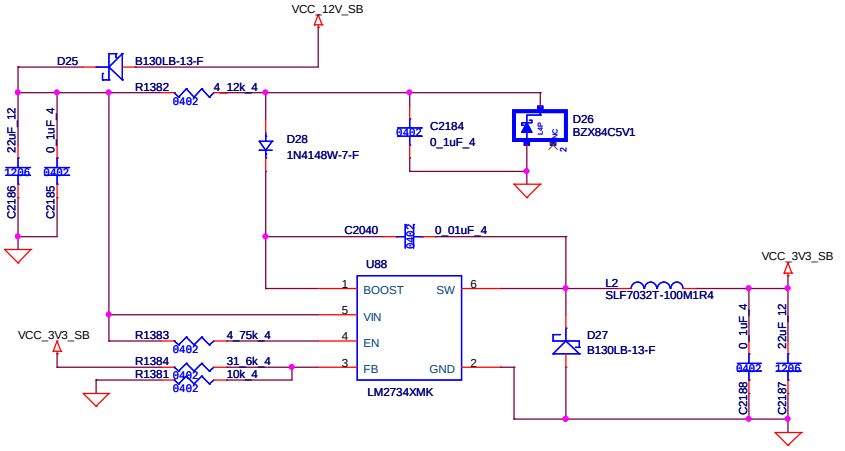

1.8V Bank
U89A
U89B
U89C
U89D
U89E
EPM2210F256C5N
CPLD_TDO
CPLD_TDI
CPLD_TMS
CPLD_TCK
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_CS
SPI_SLN
SPI_FS
SPI_SCK
SPI_MOSI
SPI_MISO
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SPI_SLN
SPI_FS
SPI_CL

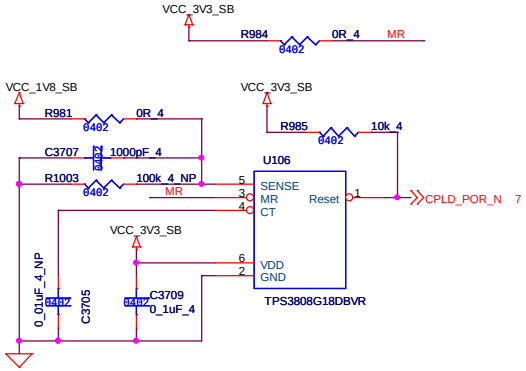


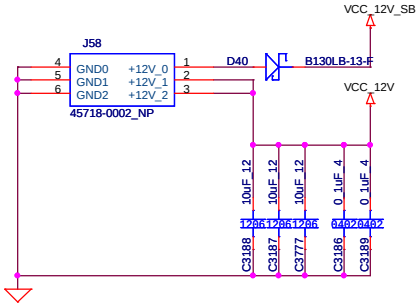












Title: Power Regulation		
Size: Custom	Document Number: IM13042A	Rev: 13
Date: Thursday, July 11, 2013	Sheet 8 of 10	

	Voltage Rails					
	VCC_12V	VCC_5V_SB	VCC_3V3_SB	VCC_5V	VCC_3V3	VCC_1V8
CPU Module	x	x				
Winbond SIO			x		x	
CPLD + Misc (A)					0.3	0.1
SATA	x			x		
Total Current (A)						
Power (W)						

Total typical Power:

Max Power (80% efficiency):

Interface Masters, Inc.		
Title: Power Sequence & Consumption		
Size: Custom	Document Number: IM13042A	Rev: 13
Date: Thursday, July 11, 2013	Sheet 9 of 10	

REVISIONS

REV	PCB Rev	DESCRIPTIONS	ENGINEER	DATE
01	A	Genesis	Ran Z	6/13/2013
04	A	Added fan control, changed regular SATA connector to Mini SATA	Ran Z	6/24/2013
05	A	Added EUSB connector	Ran Z	6/24/2013
06	A	Added CPLD_POR_N signal to cpld	Ran Z	6/26/2013
07	A	Compined the 2 split Com express connectors into one symbol	Ran Z	6/26/2013
08	A	Corrected TP6 footprint	Ran Z	6/27/2013
09	A	Modified Com Express Connector symbol Connect COM Express to CPLD through LPC	Ran Z	7/3/2013
10	A	Added 0ohm resistors to the Winbond LPC bus	Ran Z	7/8/2013
11	A	Power regulation modification	Ran Z	7/9/2013
12	A	removed the break out board	Ran Z	7/11/2013
13	A	Added 2 mini USB connectors	Ran Z	7/11/2013

Interface Masters, Inc.

Title: History

Size: Custom | Document Number: IM13042A | Rev: 13

Date: Thursday, July 11, 2013 | Sheet 10 of 10