IM13037 CPLD

Altera EPM1270F256
Revision 0.1
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1.0 Overview

The Niagara IM13037 board uses an Altera MAX II CPLD to allow the main CPU to control the basic functionality of the board. Some of the features controlled by the CPLD are: Reset, I2C interfaces, Control of Relays and LEDs.

2.0 Internal Registers

The address map of the CPLD internal registers is shown in the table below.
The registers are accessed on a byte basis from the host CPU board.
They are also accessible from a test port thru the SPI protocol.

Table 1. CPLD Registers Address Map

Register Name	Address Offset	Host Access
MAIN_CPLD_SIG_L	0	RO
MAIN_CPLD_SIG_H	1	RO
MAIN_CPLD_REV	2	RO
reserved	3	-
RST_CTL_0	4	R/W
RST_CTL_1	5	R/W
reserved	6 - 8	-
QSFP_PRES	9	RO
INT_STAT_0	10 (0x0A)	RO
INT_EN_0	11 (0x0B)	R/W
INT_STAT_1	12 (0x0C)	RO
INT_EN_1	13 (0x0D)	R/W
reserved	14 - 16	-
LED_CFG	17 (0x11)	R/W
LED_INDX_0	18 (0x12)	R/W
LED_CTL_0	19 (0x13)	R/W
LED_INDX_1	20 (0x14)	R/W
LED_CTL_1	21 (0x15)	R/W
LED_INDX_2	22 (0x16)	R/W
LED_CTL_2	23 (0x17)	R/W
reserved	24 - 26	-
TEST_0	27 (0x1B)	R/W
BA_CTL	28 (0x1C)	R/W
reserved	29	-
MI_BSL	30 (0x1E)	R/W
I2C_BSL	31 (0x1F)	R/W
reserved	32 - 63	-
User Flash Memory (UFM) Interface		
UFM_CTL	64 (0x40)	R/W
UFM_ADDR	65 (0x41)	R/W
UFM_DATAIN_L	66 (0x42)	R/W
UFM_DATAIN_H	67 (0x43)	R/W
UFM_DATAOUT_L	68 (0x44)	RO
UFM_DATAOUT_H	69 (0x45)	RO
reserved	70 - 127	-

MAIN_CPLD_SIG_L – CPLD Signature Low Byte, read only
Returns the value 0x8C.

MAIN_CPLD_SIG_H – CPLD Signature High Byte, read only
Returns the value 0.

MAIN_CPLD_REV – CPLD Revision, read only

7	6 4	3 0
reserved	BRD_REV[2:0]	CPLD_REV[3:0]

bit 7 reserved

bits 6:4 BRD_REV[2:0] – Returns the Board Revision Level

bits 3:0 CPLD_REV[3:0] – Returns the CPLD Revision Level

RST_CTL_0 – Reset Control Register 0

7	6	5	4	3	2	1	0
S_RST	res	res	res	res	PHY[2]	PHY[1]	PHY[0}

bit 7 S_RST – Soft Reset Reset.
When set to 1, all CPLD registers are set to their power up default value.
This bit must be set to 0 for normal operation.

bits 6:3 reserved

bits 2:0 PHY[2:0] – PHY Reset
Writing a 1 into any bit position causes the corresponding BCM84328 device to be reset.
These bits must be set to 0 for normal operation.

RST_CTL_1 – Reset Control Register 1

7	6	5	4	3	2	1	0
res	res	RST_Q5	RST_Q4	RST_Q3	RST_Q2	RST_Q1	RST_Q0

bits 7:6 reserved

bits 5:0 RST_Q[5:0] – QSFP Modules Reset
Writing a 1 into any bit position causes the corresponding QSFP module to be reset.
These bits must be set to 0 for normal operation.

QSFP_PRES - QSFP Presence

7	6	5	4	3	2	1	0
res	res	PRS_Q5	PRS_Q4	PRS_Q3	PRS_Q2	PRS_Q1	PRS_Q0

bits 7:6 reserved

bits 5:0 PRS_Q[5:0] – QSFP Modules Presence
A bit position returns a 1 when the corresponding QSFP module is present.

INT_STAT_0 - Interrupt Status 0, read only

7	6	5	4	3	2	1	0
res	res	res	res	res	PH2_INT	PHY1_INT	PHY0_INT

bits 7:3 reserved

bits 3:0 PHYn_INT - PHY Interrupts
A bit returns a 1 when the interrupt from the corresponding PHY Device is active.

INT_EN_0 - Interrupt Enable 0

7	6	5	4	3	2	1	0
res	res	res	res	res	IE[2]	IE[1]	IE[0]

bits 7:3 reserved

bits 2:0 IE[2:0] – PHY Devices Interrupt Enable
When a bit is set to 1, the interrupt from the corresponding PHY Device is enabled.

INT_STAT_1 - Interrupt Status 1, read only

7	6	5	4	3	2	1	0
res	res	Q5_INT	Q4_INT	Q3_INT	Q2_INT	Q1_INT	Q0_INT

bits 7:6 reserved

bits 5:0 Qn_INT - QSFP Modules Interrupts
A bit returns a 1 when the interrupt from the corresponding module is active.

INT_EN_1 - Interrupt Enable 1

7	6	5	4	3	2	1	0
res	res	IE[5]	IE[4]	IE[3]	IE[2]	IE[1]	IE[0]

bits 7:6 reserved

bits 5:0 IE[5:0] - QSFP Modules Interrupt Enable
When a bit is set to 1, the interrupt from the corresponding module is enabled.

LED_CFG – LED Config Register

7	6	5	4	3	2	1	0
res	res	res	LED_ACT_2	res	LED_ACT_1	res	LED_ACT_0

bits 7:5 reserved

bit 4 LED_ACT_2 -
When set to 0, bits 5:4 and 1:0 of the LED_CTL_2 register are loaded from the LED serial data stream.
When it is 1, those bits must be loaded by the software.
Upon reset, this bit is set to 0.

bit 3 reserved

bit 2 LED_ACT_1 -
When set to 0, bits 5:4 and 1:0 of the LED_CTL_1 register are loaded from the LED serial data stream.
When it is 1, those bits must be loaded by the software.
Upon reset, this bit is set to 0.

bit 1 reserved

bit 0 LED_ACT_0 -
When set to 0, bits 5:4 and 1:0 of the LED_CTL_0 register are loaded from the LED serial data stream.
When it is 1, those bits must be loaded by the software.
Upon reset, this bit is set to 0.

LED_INDX_0 – LED Index Register 0

7	0
SS_INDX[7:0]	

bit 7 reserved

bits 6:0 SS_INDX[6:0] – Serial Stream Index
Points to the LED serial stream 4-bit data field where bits 3:0 of LED_CTL_0 register are loaded from. Bits 7:4 of LED_CTL_0 are loaded from the following LED serial stream data field.

LED_CTL_0 – LED Control Register 0
This register controls the LEDs for ports A0 and A1.

7	6	5	4	3	2	1	0
res	res	ACT_A1[1]	ACT_A1[0]	res	res	ACT_A0[1]	ACT_A0[0]

bits 7:6 reserved

bits 5:4 ACT_A1[1:0] – Channel A1 Activity LED Control
These bits control the activity LED as shown in the table below.

ACT_A0/1[1:0]	**Activity LED State**
00	OFF
01	ON
10	reserved
11	BLINKING

bits 3:2 reserved

bits 1:0 ACT_A0[1:0] – Channel A0 Activity LED Control

These bits control the activity LED as shown in the table above.

LED_INDX_1 – LED Index Register 1
Serial stream index for ports A2 and A3.
The format and functionality is the same as LED_INDX_0.

LED_CTL_1 – LED Control Register 1
This register controls the LEDs for ports A2 – A3.
The format and functionality is the same as LED_CTL_1.

LED_INDX_2 – LED Index Register 2
Serial stream index for ports A4 and A5.
The format and functionality is the same as LED_INDX_0.

LED_CTL_2 – LED Control Register 2
This register controls the LEDs for ports A4 – A5.
The format and functionality is the same as LED_CTL_0.

TEST_0 – Test Register
This register is used for board testing only.

BA_CTL – Bus Allocation Control

7	6	5	4	3	2	1	0
res	B_MD[1]	B_MD[0]	res	res	res	res	res

bit 7 reserved

bits 6:5 B_MD[1:0] – Bus Mode
These bits determine which bus, I2C or MDIO/MDC, is associated with the debug SPI port in bypass mode.

SPI_SLN, SPI_FS	B_MD[1:0]	Access Initiator	Accessed Target
00	xx	Debug SPI Port	CPLD Registers
01	00	Debug SPI Port	none
01	01	Debug SPI Port	none
01	10	Debug SPI Port	I2C Bus
01	11	Debug SPI Port	MDIO/MDC Bus

bits 4:0 reserved

MI_BSL – Management Interface Bus Select

7	6	5	4	3	2	1	0
res	res	res	res	res	res	MI_SL[1]	MI_SL[0]

bits 7:2 reserved

bits 1:0 MI_SL- MI Bus Select
This bit selects the MI Interface as shown in the table below.

MI_SL[1:0]	MDIO/MDC Bus Selected
00	reserved

01	PHY 1
10	PHY 2
11	PHY 3

I2C_BSL – I2C Bus Select

7	6	5	4	3	2	1	0
res	res	res	res	res	I2C_SL[2]	I2C_SL[1]	I2C_SL[0]

bits 7:3 reserved

bits 2:0 I2C_SL[2:0] – I2C Bus select

I2C_SL[2:0]	I2C Bus Selected
000	QSFP 0
001	QSFP 1
010	QSFP 2
011	QSFP 3
100	QSFP 4
101	QSFP 5
110 - 111	reserved

User Flash Memory Interface

The CPLD has an internal User Flash Memory (UFM) that can be used to store any information that needs to be retained after being reset or powered off. The UFM consists of 2 sectors, and each sector has 4096 bits of memory, organized in a 256 x 16 bit fashion. Each data word field can be written a word at a time, but it can only be written to once before any erase operation. The erase functionality of the UFM can only erase the entire sector, not a specific word.

UFM_CTL – User Flash Memory Control

7	6	5	4	3	2	1	0
res	res	OP[1]	OP[0]	SEC_SEL	DATA_VLD	OP_STOP	OP_START

bits 7:6 reserved

bits 5:4 OP[1:0] - Operation Code
This field specifies the operation to be performed.
Encodings are shown in the table below.
The software should not change this field while an operation is in progress (ST = 1).
Upon reset, all bits are set to 0.

OP[1:0]	CPLD Operation
00	UFM Read
01	UFM Write
10	UFM Sector Erase All words in the selected sector will be set to the value of 0xFFFF
11	reserved

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bit 3 SEC_SEL – Sector Select.
This bit selects either sector 0 or sector 1 of the UFM.

bit 2 DATA_VLD – UFM Data Valid, read-only
This bit is set to 1 when the data to be read is valid after a read operation completes.
This bit is provided for testing and can be ignored.

bit 1 OP-STOP
Writing a 1 into this bit position stops any operation in progress.
This bit is provided to reset the UFM access logic in case the operation does not terminate.
It is not used in normal operation.
This bit is self clearing..

bit 0 OP-START
Writing a 1 into this bit position starts an operation as specified by the OP field.
Cleared automatically when the operation is completed.

Note: When an operation is started, the host software must wait until the operation is completed (OP_START bit cleared) before reading any result or before starting another operation.

UFM_ADDR – User Flash Memory Address
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_ADDR[7:0]							

bits 7:0 UFM_ADDR – UFM Address.
This register holds the UFM address of the memory location to be accessed in a read or write operation.

UFM_DATAIN_L – User Flash Memory Data-in, Low-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_DATAIN_L[7:0]							

bits 7:0 UFM_DATAIN_L – UFM Data-in Low-Byte.
This register holds the lower byte of the data word to be written to the UFM in a write operation.

UFM_DATAIN_H – User Flash Memory Data-in, High-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_DATAIN_H[7:0]							

bits 7:0 UFM_DATAIN_H – UFM Data-in, High-Byte.
This register holds the upper byte of the data word to be written to the UFM in a write operation.

UFM_DATAOUT_L – User Flash Memory Data-out, Low-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0

UFM_DATAOUT_L[7:0]

bits 7:0 UFM_DATAOUT_L – UFM Data-out, Low-Byte.
This register holds the lower byte of the data word returned after a read operation.

UFM_DATAOUT_H – User Flash Memory Data-out, High-Byte
Upon reset, all bits are set to 0.

7	6	5	4	3	2	1	0
UFM_DATAOUT_H[7:0]							

bits 7:0 UFM_DATAOUT_H – UFM Data-out, High-Byte.
This register holds the upper byte of the data word returned after a read operation.

3.0 Timing Diagrams

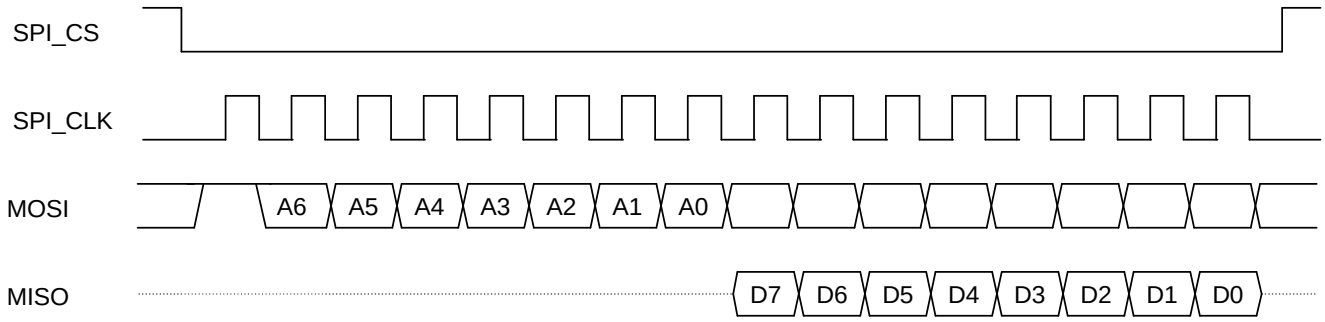


Figure 3-1. Debug SPI Port Read Access, 7-bit Address, 8-bit Data

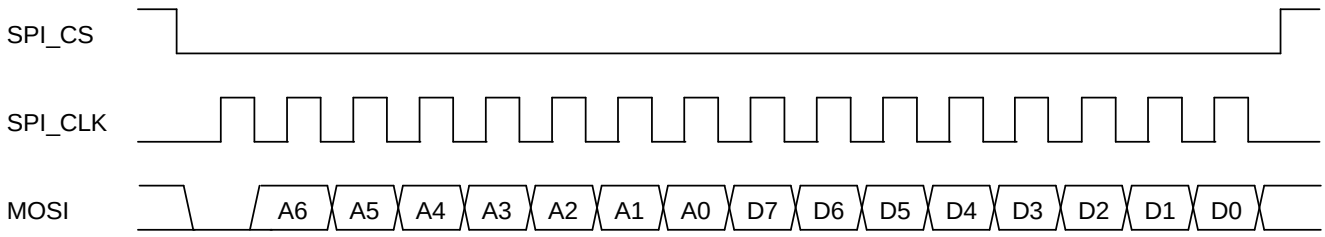


Figure 3-2. Debug SPI Port Write Access, 7-bit Address, 8-bit Data

4.0 History

Document Rev	Changes
0.2	Changed the functionality of the LED_CTL register

0.3	1. added TEST_0 register 2. replaced PBTN_CSR with HP_CSR 3. modified register address map