IM13034B

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Customer Name:

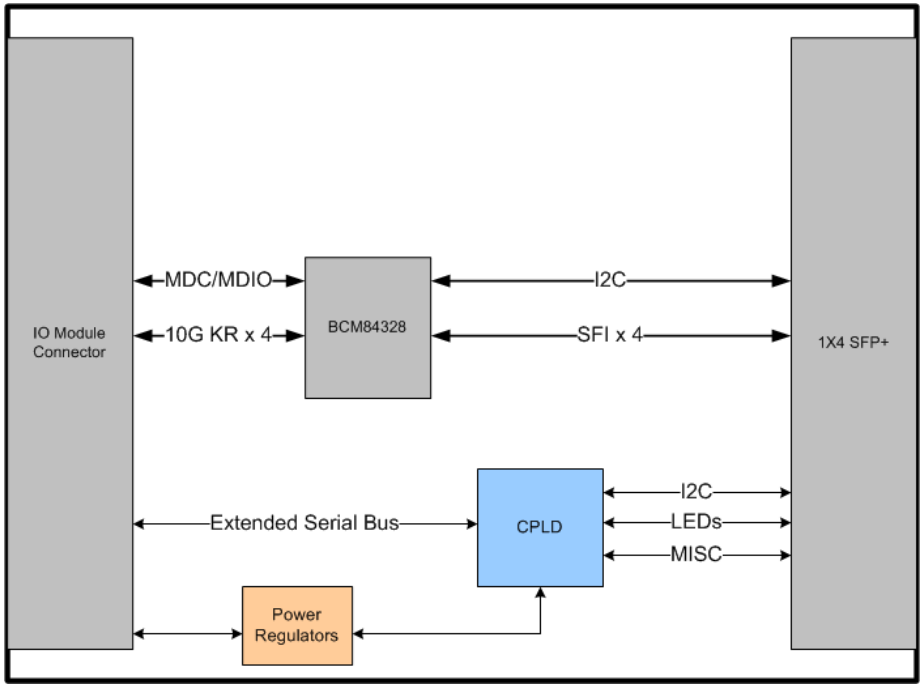
Interface Masters

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www.interfacemasters.com

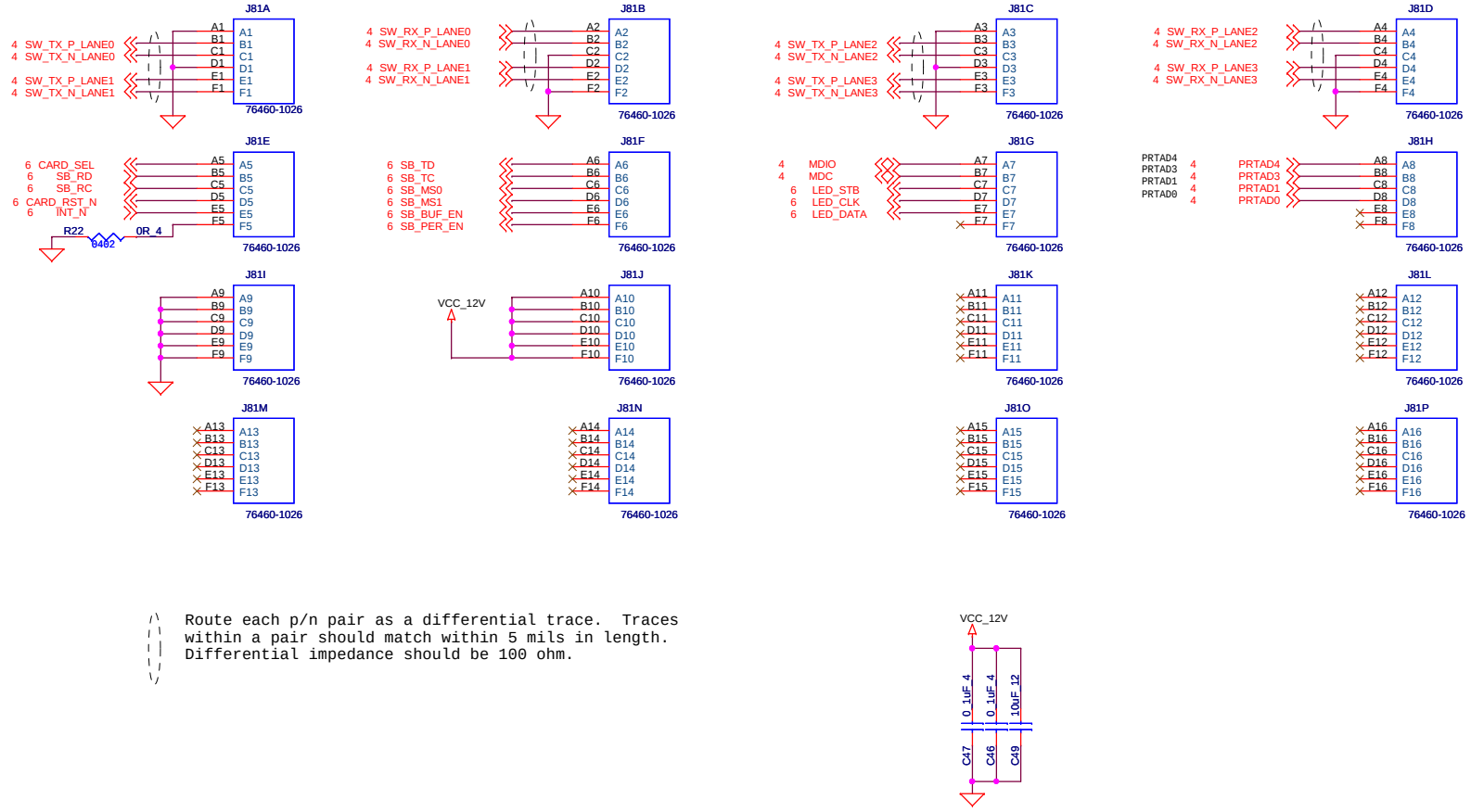
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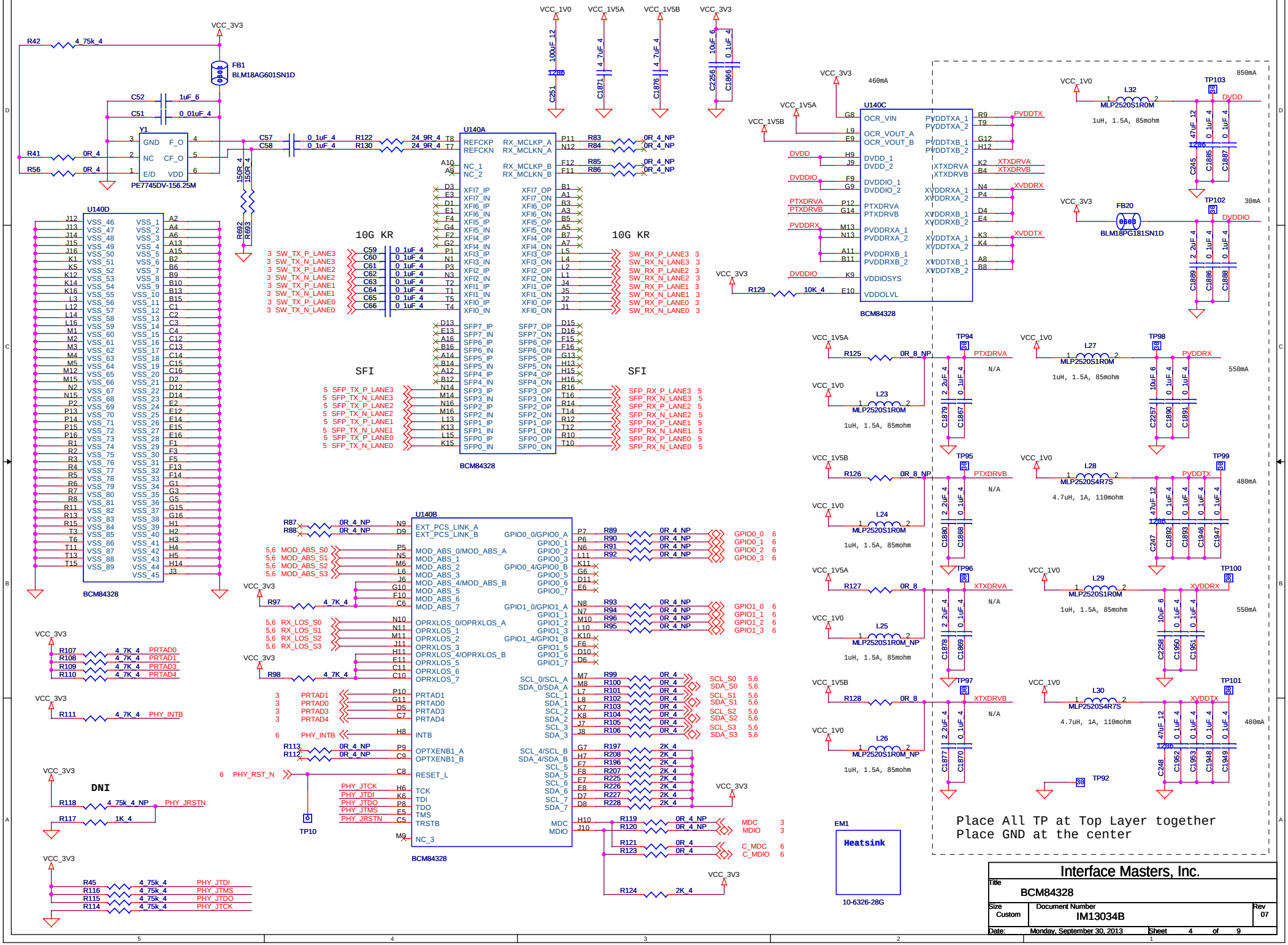
Interface Masters, Inc.		
Title: Block Diagram		
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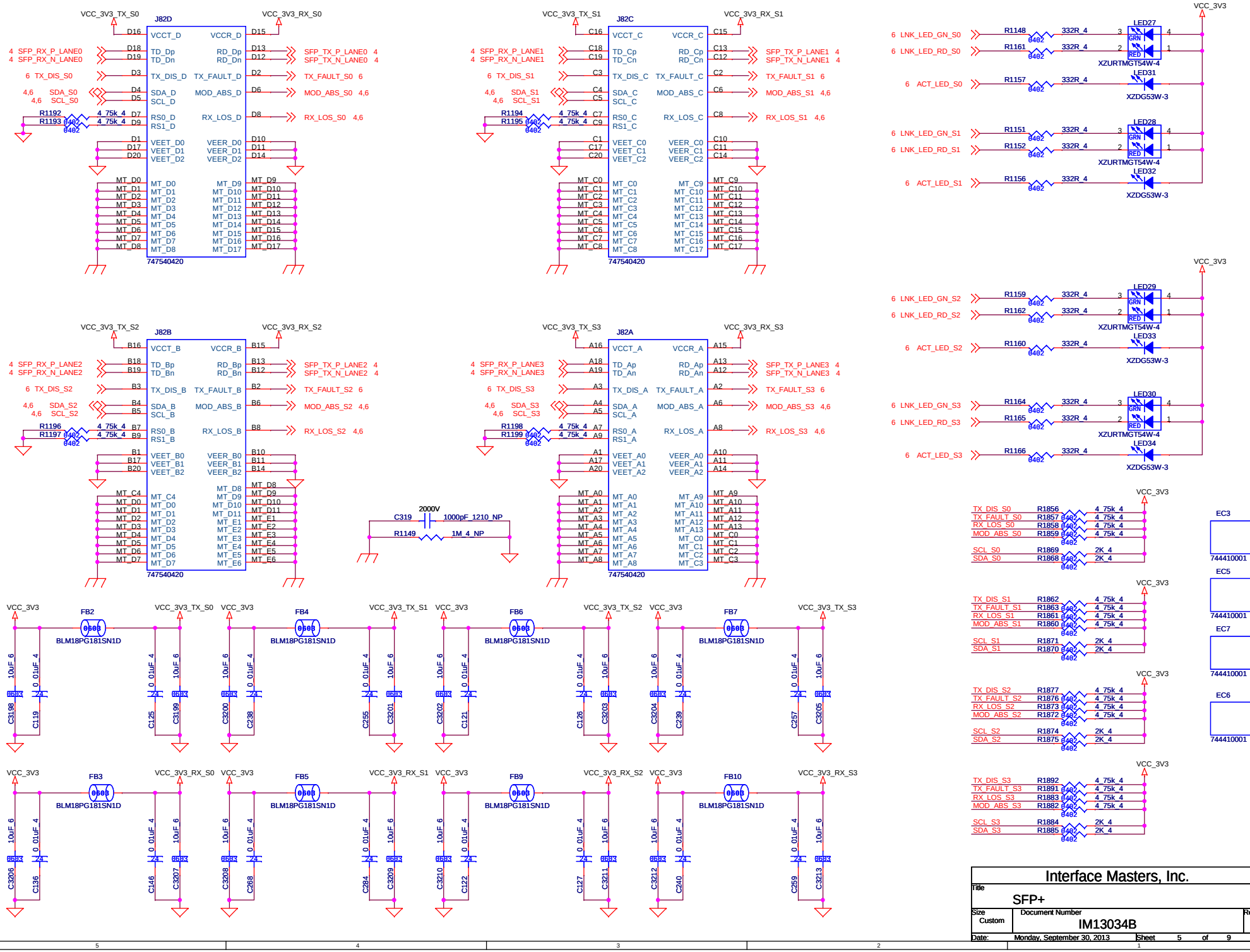


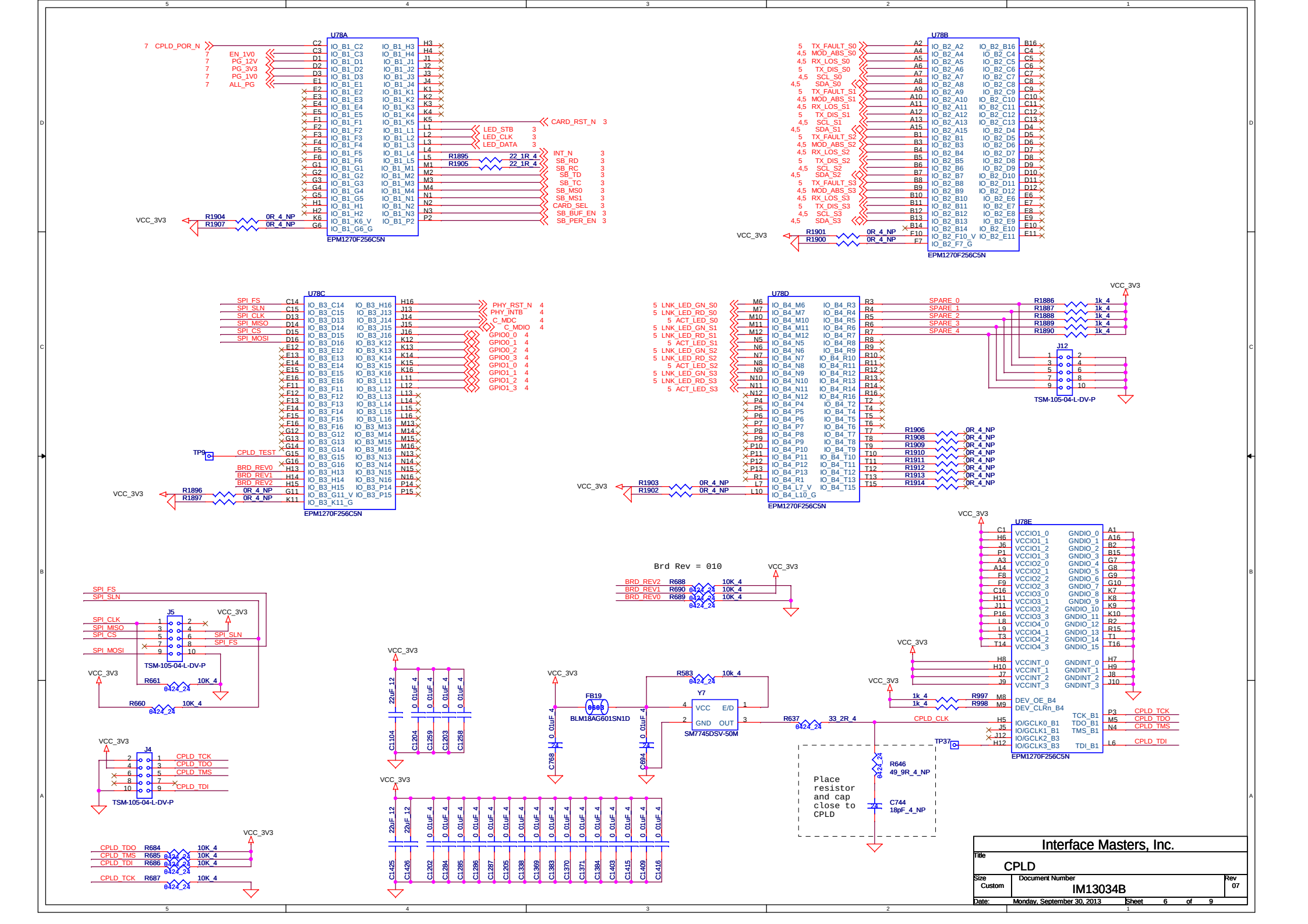
Route each p/n pair as a differential trace. Traces within a pair should match within 5 mils in length. Differential impedance should be 100 ohm.

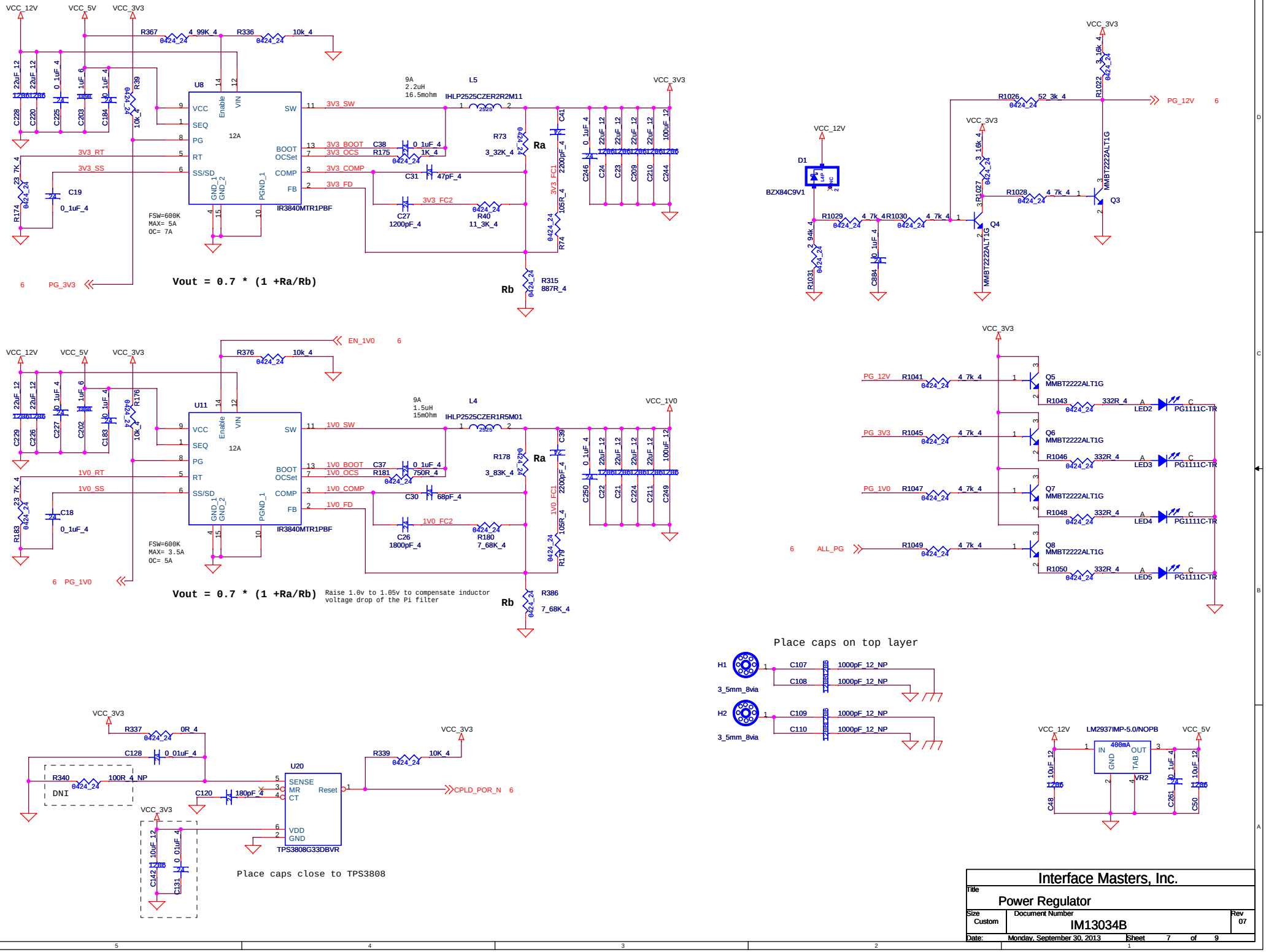
Place cap within 200 mils of the edge connectors.

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VCC_3V3
R42 4_75k_4
FB1
BLM18AG601SN1D
C52 1uF_6
C51 0_01uF_4
Y1
GND F_O
NC CF_O
E/D VDD
PE7745DV-156.25M
R41 0R_4
R56 0R_4
C57 0_1uF_4
C58 0_1uF_4
R122 24_9R_4
R130 24_9R_4
150R_4
150R_4
R692
R693
U140A
REFCKP RX_MCLKP_A
REFCKN RX_MCLKN_A
NC_1 RX_MCLKP_B
NC_2 RX_MCLKN_B
P11 R83 0R_4_NP
N12 R84 0R_4_NP
F12 R85 0R_4_NP
F11 R86 0R_4_NP
10G KR
SFI
XFI7_IP XFI7_OP
XFI7_IN XFI7_ON
XFI6_IP XFI6_OP
XFI6_IN XFI6_ON
XFI5_IP XFI5_OP
XFI5_IN XFI5_ON
XFI4_IP XFI4_OP
XFI4_IN XFI4_ON
XFI3_IP XFI3_OP
XFI3_IN XFI3_ON
XFI2_IP XFI2_OP
XFI2_IN XFI2_ON
XFI1_IP XFI1_OP
XFI1_IN XFI1_ON
XFI0_IP XFI0_OP
XFI0_IN XFI0_ON
3 SW_TX_P_LANE3
3 SW_TX_N_LANE3
3 SW_TX_P_LANE2
3 SW_TX_N_LANE2
3 SW_TX_P_LANE1
3 SW_TX_N_LANE1
3 SW_TX_P_LANE0
3 SW_TX_N_LANE0
C59 0_1uF_4
C60 0_1uF_4
C61 0_1uF_4
C62 0_1uF_4
C63 0_1uF_4
C64 0_1uF_4
C65 0_1uF_4
C66 0_1uF_4
SW_RX_P_LANE3 3
SW_RX_N_LANE3 3
SW_RX_P_LANE2 3
SW_RX_N_LANE2 3
SW_RX_P_LANE1 3
SW_RX_N_LANE1 3
SW_RX_P_LANE0 3
SW_RX_N_LANE0 3
SFP7_IP SFP7_OP
SFP7_IN SFP7_ON
SFP6_IP SFP6_OP
SFP6_IN SFP6_ON
SFP5_IP SFP5_OP
SFP5_IN SFP5_ON
SFP4_IP SFP4_OP
SFP4_IN SFP4_ON
SFP3_IP SFP3_OP
SFP3_IN SFP3_ON
SFP2_IP SFP2_OP
SFP2_IN SFP2_ON
SFP1_IP SFP1_OP
SFP1_IN SFP1_ON
SFP0_IP SFP0_OP
SFP0_IN SFP0_ON
5 SFP_TX_P_LANE3
5 SFP_TX_N_LANE3
5 SFP_TX_P_LANE2
5 SFP_TX_N_LANE2
5 SFP_TX_P_LANE1
5 SFP_TX_N_LANE1
5 SFP_TX_P_LANE0
5 SFP_TX_N_LANE0
SFP_RX_P_LANE3 5
SFP_RX_N_LANE3 5
SFP_RX_P_LANE2 5
SFP_RX_N_LANE2 5
SFP_RX_P_LANE1 5
SFP_RX_N_LANE1 5
SFP_RX_P_LANE0 5
SFP_RX_N_LANE0 5
BCM84328
U140D
VSS_46 VSS_1 A2
VSS_47 VSS_2 A4
VSS_48 VSS_3 A6
VSS_49 VSS_4 A13
VSS_50 VSS_5 A15
VSS_51 VSS_6 B2
VSS_52 VSS_7 B6
VSS_53 VSS_8 B9
VSS_54 VSS_9 B10
VSS_55 VSS_10 B13
VSS_56 VSS_11 B15
VSS_57 VSS_12 C1
VSS_58 VSS_13 C2
VSS_59 VSS_14 C3
VSS_60 VSS_15 C4
VSS_61 VSS_16 C12
VSS_62 VSS_17 C13
VSS_63 VSS_18 C14
VSS_64 VSS_19 C15
VSS_65 VSS_20 C16
VSS_66 VSS_21 D2
VSS_67 VSS_22 D12
VSS_68 VSS_23 D14
VSS_69 VSS_24 E2
VSS_70 VSS_25 E12
VSS_71 VSS_26 E14
VSS_72 VSS_27 E15
VSS_73 VSS_28 E16
VSS_74 VSS_29 F1
VSS_75 VSS_30 F3
VSS_76 VSS_31 F5
VSS_77 VSS_32 F13
VSS_78 VSS_33 F14
VSS_79 VSS_34 G1
VSS_80 VSS_35 G3
VSS_81 VSS_36 G5
VSS_82 VSS_37 G15
VSS_83 VSS_38 G16
VSS_84 VSS_39 H1
VSS_85 VSS_40 H2
VSS_86 VSS_41 H3
VSS_87 VSS_42 H4
VSS_88 VSS_43 H5
VSS_89 VSS_44 H14
VSS_45 J3
BCM84328
U140B
EXT_PCS_LINK_A
EXT_PCS_LINK_B
MOD_ABS_0/MOD_ABS_A
MOD_ABS_1
MOD_ABS_2
MOD_ABS_3
MOD_ABS_4/MOD_ABS_B
MOD_ABS_5
MOD_ABS_6
MOD_ABS_7
OPRXLOS_0/OPRXLOS_A
OPRXLOS_1
OPRXLOS_2
OPRXLOS_3
OPRXLOS_4/OPRXLOS_B
OPRXLOS_5
OPRXLOS_6
OPRXLOS_7
PRTAD1
PRTAD0
PRTAD3
PRTAD4
INTB
OPTXENB1_A
OPTXENB1_B
RESET_L
TCK
TDI
TDO
TMS
TRSTB
NC_3
GPIO0_0/GPIO0_A
GPIO0_1
GPIO0_2
GPIO0_3
GPIO0_4/GPIO0_B
GPIO0_5
GPIO0_6
GPIO0_7
GPIO1_0/GPIO1_A
GPIO1_1
GPIO1_2
GPIO1_3
GPIO1_4/GPIO1_B
GPIO1_5
GPIO1_6
GPIO1_7
SCL_0/SCL_A
SDA_0/SDA_A
SCL_1
SDA_1
SCL_2
SDA_2
SCL_3
SDA_3
SCL_4/SCL_B
SDA_4/SDA_B
SCL_5
SDA_5
SCL_6
SDA_6
SCL_7
SDA_7
MDC
MDIO
BCM84328
R87 0R_4_NP
R88 0R_4_NP
5,6 MOD_ABS_S0
5,6 MOD_ABS_S1
5,6 MOD_ABS_S2
5,6 MOD_ABS_S3
R97 4_7K_4
5,6 RX_LOS_S0
5,6 RX_LOS_S1
5,6 RX_LOS_S2
5,6 RX_LOS_S3
R98 4_7K_4
3 PRTAD1
3 PRTAD0
3 PRTAD3
3 PRTAD4
6 PHY_INTB
R113 0R_4_NP
R112 0R_4_NP
6 PHY_RST_N
TP10
PHY_JTCK
PHY_JTDI
PHY_JTDO
PHY_JTMS
PHY_JRSTN
GPIO0_0 6
GPIO0_1 6
GPIO0_2 6
GPIO0_3 6
GPIO1_0 6
GPIO1_1 6
GPIO1_2 6
GPIO1_3 6
SCL_S0 5,6
SDA_S0 5,6
SCL_S1 5,6
SDA_S1 5,6
SCL_S2 5,6
SDA_S2 5,6
SCL_S3 5,6
SDA_S3 5,6
MDC 3
MDIO 3
C_MDC 6
C_MDIO 6
R124 2K_4
VCC_1V0
VCC_1V5A
VCC_1V5B
VCC_3V3
100uF_12
C251
4_7uF_4
C1871
4_7uF_4
C1876
10uF_6
0_1uF_4
C2256
C1866
U140C
OCR_VIN PVDDTXA_1 PVDDTXA_2
OCR_VOUT_A
OCR_VOUT_B PVDDTXB_1 PVDDTXB_2
DVDD_1 DVDD_2
DVDDIO_1 DVDDIO_2
PTXDRVA
PTXDRVB
PVDDRXA_1 PVDDRXA_2
PVDDRXB_1 PVDDRXB_2
VDDIOSYS
VDDOLVL
XTXDRVA XTXDRVB
XVDDRXA_1 XVDDRXA_2
XVDDRXB_1 XVDDRXB_2
XVDDTXA_1 XVDDTXA_2
XVDDTXB_1 XVDDTXB_2
460mA
DVDD
DVDDIO
PTXDRVA
PTXDRVB
PVDDRX
DVDDIO
R129 10K_4
BCM84328
PVDDTX
XTXDRVA
XTXDRVB
XVDDRX
XVDDTX
L32
MLP2520S1R0M
1uH, 1.5A, 85mohm
TP103
DVDD
850mA
FB20
BLM18PG181SN1D
TP102
DVDDIO
30mA
R125 0R_8_NP
L23
TP94
PTXDRVA
N/A
L27
TP98
PVDDRX
550mA
R126 0R_8_NP
L24
TP95
PTXDRVB
L28
TP99
PVDDTX
480mA
4.7uH, 1A, 110mohm
R127 0R_8
L25
TP96
XTXDRVA
L29
TP100
XVDDRX
R128 0R_8
L26
TP97
XTXDRVB
L30
TP101
XVDDTX
TP92
EM1
Heatsink
10-6326-28G
R107 4_7K_4 PRTAD0
R108 4_7K_4 PRTAD1
R109 4_7K_4 PRTAD3
R110 4_7K_4 PRTAD4
R111 4_7K_4 PHY_INTB
DNI
R118 4_75k_4_NP PHY_JRSTN
R117 1K_4
R45 4_75k_4 PHY_JTDI
R116 4_75k_4 PHY_JTMS
R115 4_75k_4 PHY_JTDO
R114 4_75k_4 PHY_JTCK
Place All TP at Top Layer together
Place GND at the center
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J82D
VCC_3V3_TX_S0
VCC_3V3_RX_S0
SFP_RX_P_LANE0
SFP_RX_N_LANE0
SFP_TX_P_LANE0
SFP_TX_N_LANE0
TX_DIS_S0
TX_FAULT_S0
MOD_ABS_S0
SDA_S0
SCL_S0
RX_LOS_S0
R1192
R1193
4_75k_4
0402
747540420
J82C
VCC_3V3_TX_S1
VCC_3V3_RX_S1
SFP_RX_P_LANE1
SFP_RX_N_LANE1
SFP_TX_P_LANE1
SFP_TX_N_LANE1
TX_DIS_S1
TX_FAULT_S1
MOD_ABS_S1
SDA_S1
SCL_S1
RX_LOS_S1
R1194
R1195
J82B
VCC_3V3_TX_S2
VCC_3V3_RX_S2
SFP_RX_P_LANE2
SFP_RX_N_LANE2
SFP_TX_P_LANE2
SFP_TX_N_LANE2
TX_DIS_S2
TX_FAULT_S2
MOD_ABS_S2
SDA_S2
SCL_S2
RX_LOS_S2
R1196
R1197
J82A
VCC_3V3_TX_S3
VCC_3V3_RX_S3
SFP_RX_P_LANE3
SFP_RX_N_LANE3
SFP_TX_P_LANE3
SFP_TX_N_LANE3
TX_DIS_S3
TX_FAULT_S3
MOD_ABS_S3
SDA_S3
SCL_S3
RX_LOS_S3
R1198
R1199
C319
2000V
1000pF_1210_NP
R1149
1M_4_NP
VCC_3V3
LED27
LED31
LED28
LED32
LED29
LED33
LED30
LED34
XZURTMGT54W-4
XZDG53W-3
LNK_LED_GN_S0
LNK_LED_RD_S0
ACT_LED_S0
LNK_LED_GN_S1
LNK_LED_RD_S1
ACT_LED_S1
LNK_LED_GN_S2
LNK_LED_RD_S2
ACT_LED_S2
LNK_LED_GN_S3
LNK_LED_RD_S3
ACT_LED_S3
R1148
R1161
R1157
R1151
R1152
R1156
R1159
R1162
R1160
R1164
R1165
R1166
332R_4
EC3
EC5
EC7
EC6
744410001
FB2
FB4
FB6
FB7
FB3
FB5
FB9
FB10
BLM18PG181SN1D
VCC_3V3_TX_S0
VCC_3V3_TX_S1
VCC_3V3_TX_S2
VCC_3V3_TX_S3
VCC_3V3_RX_S0
VCC_3V3_RX_S1
VCC_3V3_RX_S2
VCC_3V3_RX_S3
10uF_6
0_01uF_4
C3198
C119
C125
C3199
C3200
C238
C255
C3201
C3202
C121
C126
C3203
C3204
C239
C257
C3205
C3206
C136
C146
C3207
C3208
C268
C284
C3209
C3210
C122
C127
C3211
C3212
C240
C259
C3213
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U78A
EPM1270F256C5N
U78B
EPM1270F256C5N
U78C
EPM1270F256C5N
U78D
EPM1270F256C5N
U78E
EPM1270F256C5N
J12
TSM-105-04-L-DV-P
J5
TSM-105-04-L-DV-P
J4
TSM-105-04-L-DV-P
Brd Rev = 010
Y7
SM7745DSV-50M
FB19
BLM18AG601SN1D
Place resistor and cap close to CPLD
R646 49_9R_4_NP
C744 18pF_4_NP
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CPLD
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Overall Power Sequencing:

VCC_12V
VCC_5V
VCC_3V3 --> VCC_1V0 --> ALL_PWR_GOOD --> RESET

	Voltage Rails	
	1	3.3
SFP+ x 4 (mA)		1140
BCM84328 (mA)	2910	490
CPLD (mA)		200
Total Current (mA)	2910	1830
Power (W)	2.91	6.039
Total Power (W)	8.949	
Total Raw Power (W) Assume 80% Efficiency	11.18625	

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REVISIONS

REV	PCB Rev	DESCRIPTIONS	ENGINEER	DATE
01		Genesis	Kevin Y	3/20/2013
05	B	Minor changes, swap location of LEDs, add test points, chnage some 1206 cap to 0603 cap.	Kevin Y	9/4/2013
06	B	update to enable CPLD MDIO access	Kevin Y	9/13/2013
07	B	update the 10 pin header PN to short pins. update the compensation value for 3.3VSB	Kevin Y	9/30/2013

Interface Masters, Inc.		
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