IM13026 CPLD

Altera EPM3064ATC44-10
Revision 0.1
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1.0 Overview

The IM13026 uses an Altera MAX 3000A CPLD to allow the CPU to control the functions of the board.

2.0 Internal Registers

The address map of the slave CPLD internal registers is shown in the table below. The registers are accessed from the host CPU board thru a Serial Bus interface.

Table 1. CPLD Registers Address Map

Register Name	Address Offset	Access Type
General Registers		
CPLD_SIG_L	0	RO
CPLD_SIG_H	1	RO
CPLD_REV	2	RO
reserved	3	-
FC_SS	4	R/W
FC_STAT	5	RO
reserved	6	-
FAN_PWR_EN	7	R/W
FAN_PWR_ST	8	RO
reserved	9 - 63	-

CPLD_SIG_L – CPLD Signature Low Byte, read only
Returns the value 0x8D.

CPLD_SIG_H – CPLD Signature High Byte, read only
Returns the value 0.

CPLD_REV – CPLD Revision, read only

7	6 4	3 0
reserved	BRD_REV[2:0]	CPLD_REV[3:0]

bit 7 reserved

bits 6:4 BRD_REV[2:0] – Returns the Board Revision Level

bits 3:0 CPLD_REV[3:0] – Returns the CPLD Revision Level

FC_SS – Fan Controllers' Speed Setting

7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	MAX_SPD

bits 7:4 reserved

bit 0 MAX_SPD – Maximum Speed Select
When this bit is set to 1, the MAX_SPEED signals to the FAN controllers are asserted
Upon reset, this bit is set to 1.

FC_STAT – Fan Controllers' Status, read-only

7	6	5	4	3	2	1	0
res	res	res	res	res	res	ALERT_1	ALERT_0

bits 7:2 reserved

bits 1:0 ALERT_[1:0], read-only
Each bit returns a 1 when the ALERT signal from the corresponding fan controller is asserted.

FAN_PWR_EN – FAN Power Enable
Controls the power to the various fan's groups.
Upon power up, all implemented bits are set to 1.

7	6	5	4	3	2	1	0
res	res	res	res	res	res	GR_B_PE	GR_A_PE

bits 7:2 reserved

bit 1 GR_B_PE – Power enable for Group B
When set to 1, the hot swap controller B, which powers fans 1, 2, 5 and 6, is enabled

bit 0 GR_A_PE – Power enable for Group A
When set to 1, the hot swap controller A, which powers fans 0, 3, 4 and 7, is enabled

FAN_PWR_ST – FAN Power Status, read-only

7	6	5	4	3	2	1	0
res	res	GR_B_FLT	GR_A_FLT	res	res	GR_B_PG	GR_A_PG

bits 7:6 reserved

bits 5:4 GR_X_FLT – Power Fault, read-only
Each bit returns a 1 when the FLT# signal from the corresponding hot swap controller is asserted.

bits 3:2 reserved

bits 1:0 GR_X_PG – Power Good, read-only
Each bit returns a 1 when the PG# signal from the corresponding hot swap controller is asserted.

3.0 Timing Diagrams

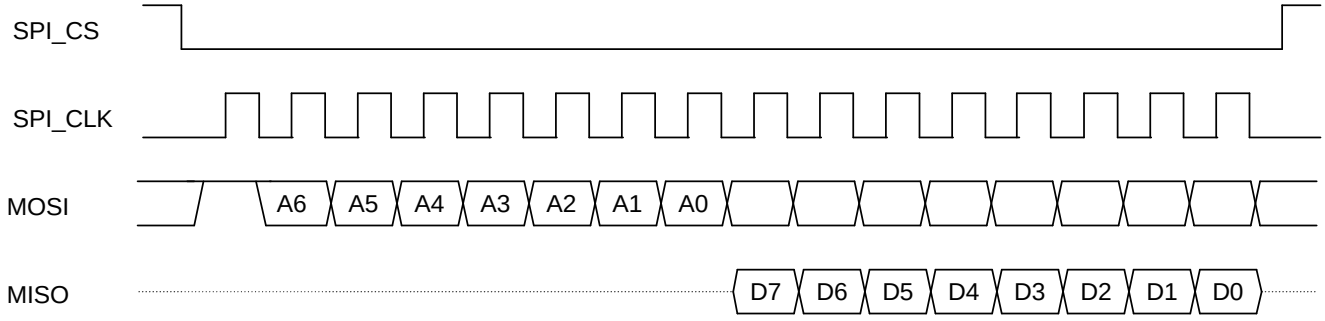


Figure 3-1. Debug SPI Port Read Access, 7-bit Address, 8-bit Data

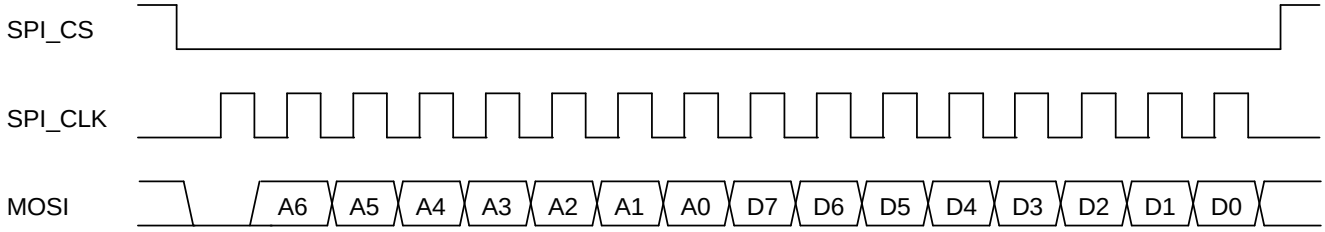


Figure 3-2. Debug SPI Port Write Access, 7-bit Address, 8-bit Data