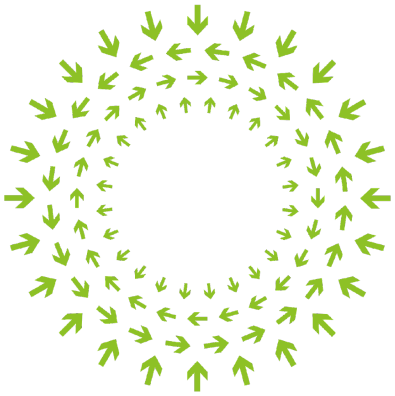

OPEN
Compute Project

Barton Springs 1S Server
Design Specification

Revision 1.0

9/14/2022

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2. OCP TENETS COMPLIANCE

2.1 Openness

The Barton Springs 1 socket server is an open design with clearly defined interfaces compatible with the Grand Canyon Storage platform.

2.2. Efficiency

Barton Springs features a CPU achieving performance/watt gain improvements compared to Bryce Canyon helping to drive a lower power consumption footprint.

2.3. Impact

Barton Springs leverages the latest generation of CPU enabling efficiency gains along with enabling a modular CPU design for future flexibility.

2.4. Scale

Barton Springs is modular, enabling the CPU module to be upgradeable in the future. Barton Springs was designed to accommodate serviceability at scale.

3. REVISION TABLE

Date	Revision	Author	Description
9/14/2022	1.0	Jeff Puglis	Ready for OCP release

4. SCOPE

This specification describes technical specifications for the Barton Springs 1S micro-server based on the 3rd Gen Intel® Scalable Processor “Cooper Lake” used in the Grand Canyon system as part of the Open Compute Project.

5. OVERVIEW

This document describes a single socket server design based on the Intel Xeon Scalable Processor “Cooper Lake” product family, which is referred hereinafter as Barton Springs 1S server. The Barton Springs 1S server uses Intel’s server class processor which incorporates a multi-core CPU, memory controller, and various IO devices. With the higher performance and IO density of the multi-core SoCs, the Barton Springs 1S server is perfect for single or multi node platforms where performance and IO density are key factors. However, platform designers must provide adequate power and cooling to properly handle the SoC’s power and thermal requirements.

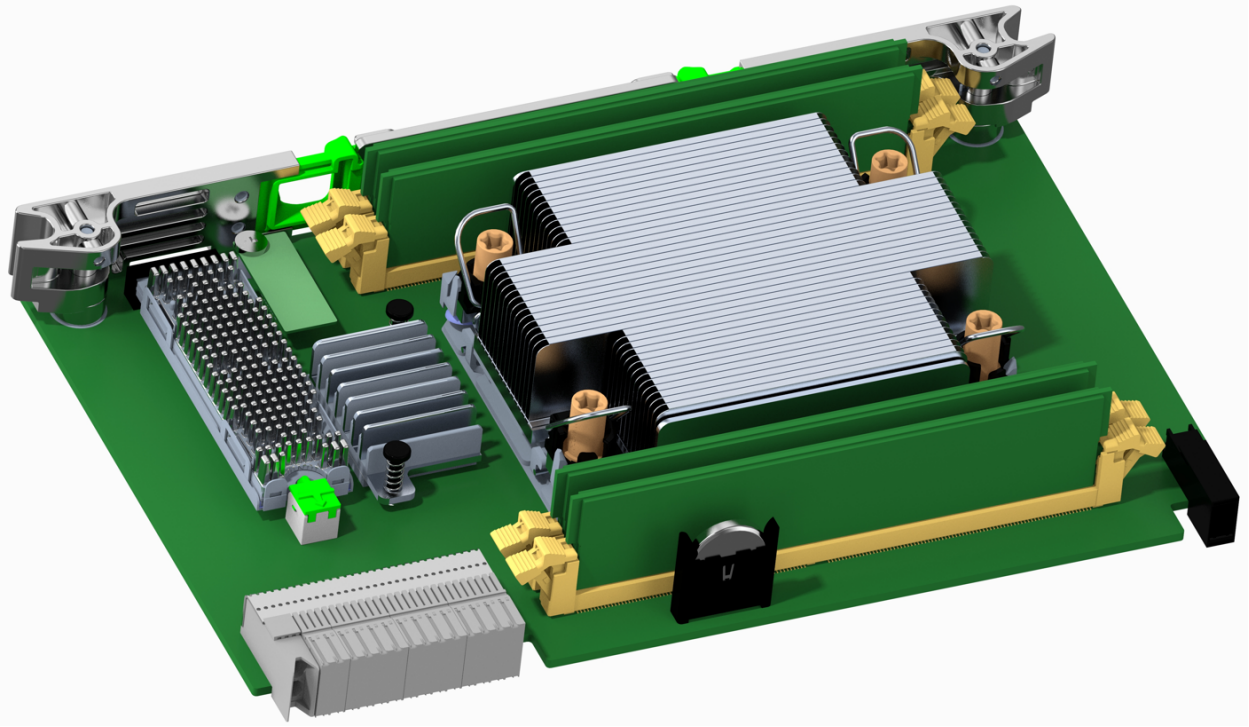

Figure 5.1 Barton Springs Board

6. RACK COMPATIBILITY

NOTE: To achieve interoperability, new specifications and products seeking recognition shall be compatible with an OCP adopted architecture: **ORv2, ORv3, or OpenEDGE** architectures. This is required for storage enclosures and systems, rack frames, and any enclosure which holds a server sled or edge device sled. Compatibility is also desired of server sleds and edge sleds. All other device types not listed are not required to support this.

Barton Springs is intended as a component in the Grand Canyon Storage system. It is not intended to be used directly with a rack.

7. PHYSICAL SPECIFICATIONS AND MAJOR COMPONENTS

7.1. Block Diagram

Below is the overall block diagram for the Barton Springs 1S board.

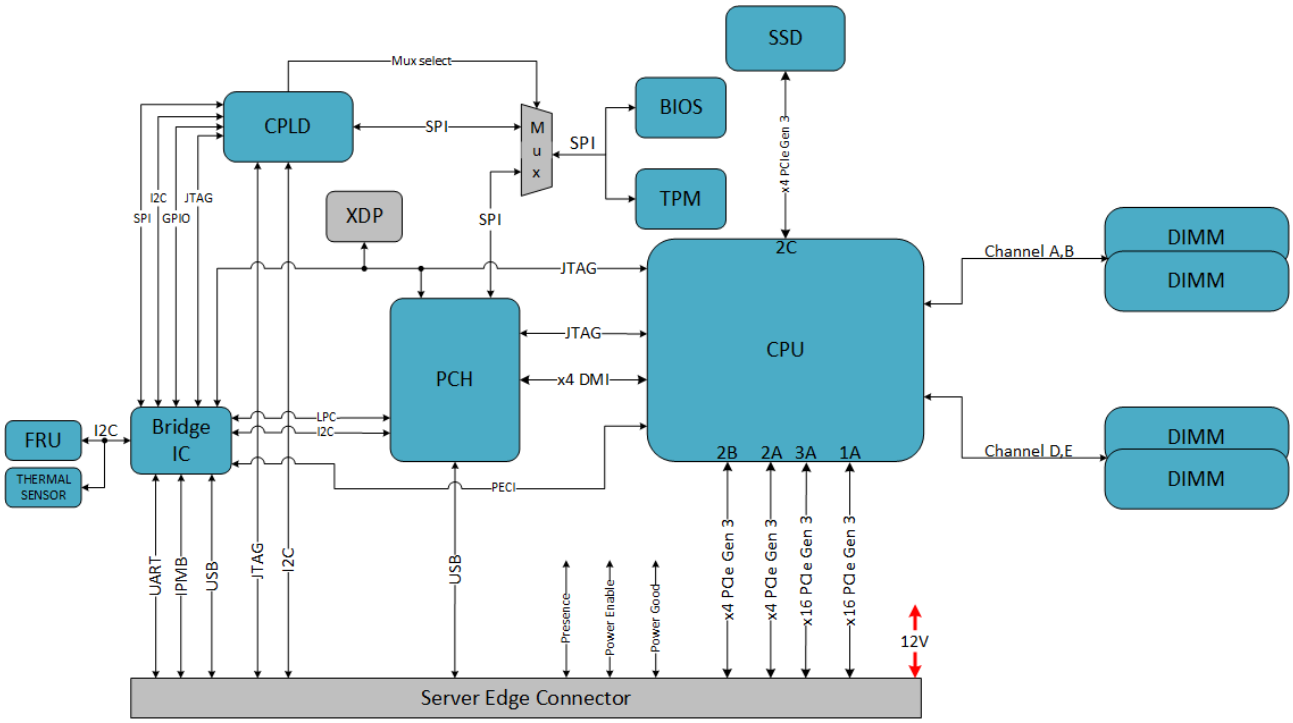

Figure 7.1 Barton Springs Block Diagram

7.2. Major Component Placement and Form Factor

Figure 6.1 below highlights the major components as well as the PCB dimensions.

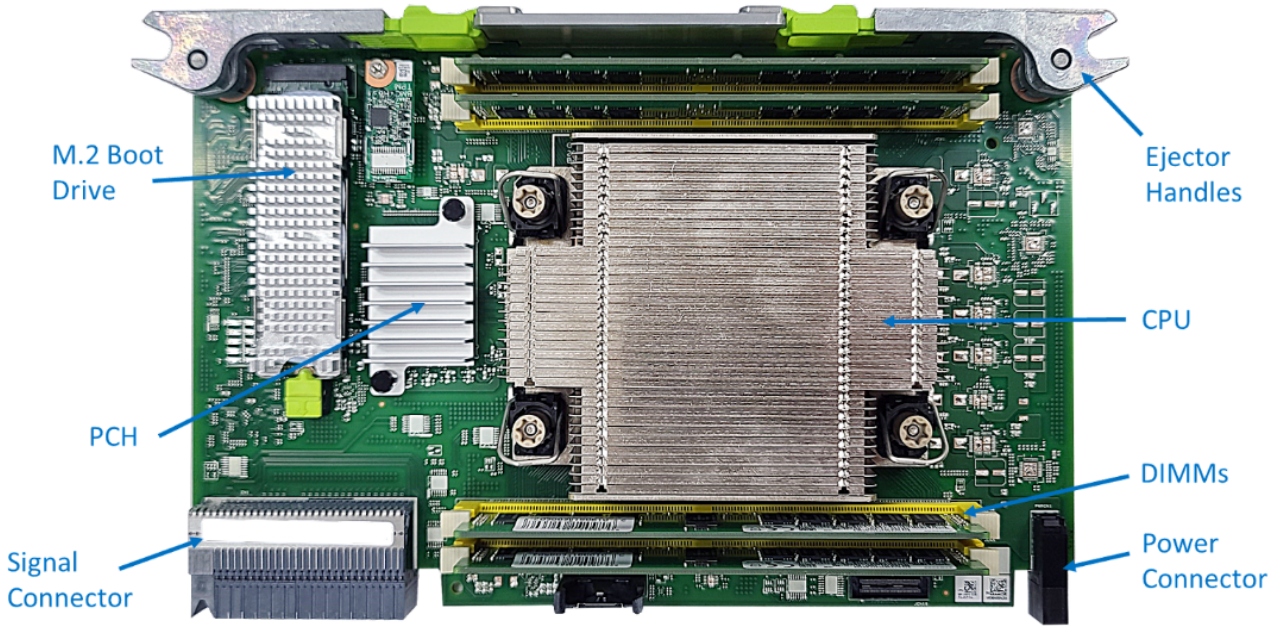

Figure 7.2 Barton Springs Important Components

7.3. CPU and Memory

7.3.1 CPU

The Barton Springs 1S board will use the Intel® Xeon® Scalable Processor Cooper Lake.

7.3.2 Boot Drive

The Barton Springs 1S will utilize 1 M.2 solid-state drive in a 2280 form factor. The drive will be connected to the CPU via the aforementioned PCIe link. A minimum 512GB M.2 NVMe SSD is required as a boot device and for logging.

7.3.3 DIMMs

The Barton Springs 1S supports 1 DDR4 DIMM per channel on 4 channels, with a design target to hit a maximum speed of 3200MT/s but expected to run at 2667MT/s.

7.3.4 FRU EEPROM

The Barton Springs 1S will include a 128Kb Electronically Erasable Programmable Read-Only Memory (EEPROM). This EEPROM will be accessible by I2C from the platform through the Bridge IC.

The EEPROM contains the Field Replaceable Unit Identification (FRU ID) information and any additional configuration information that may be required. The FRU ID is formatted in accordance with the IPMI Platform Management FRU Information Storage Definition document.

The EEPROM must contain the following entries:

- Board Manufacturer
- Board Name
- Board Serial Number
- Board Part Number
- Product Manufacturer
- Product Name
- Product Part Number
- Product Serial Number
- Product Asset Tag
- Product Build: e.g. EVT, DVT, PVT, MP
- Product Version: e.g. C1
- Manufacturing Date and Time
- Manufacturing Lot Code: (preferred, but optional)
- Manufacturing Work Order: (preferred, but optional)
- PCB Revision
- SoC Model Name/Number
- SoC Revision
- SoC TjMAX (Maximum Junction Temperature)

7.4. Platform Controller Hub (PCH)

The Barton Springs 1S uses the Intel® PCH chipset, which supports the following features:

- ACPI power management Logic Support
- Integrated Serial ATA host controller
- xHCI USB controller with SuperSpeed USB 3.0 ports
- Direct Media Interface
- SPI and eSPI interface

- Flexible I/O
- GPIO
- LPC and SMBus

Refer to respective EDS from Intel® with regards to the PCH for the full feature list.

7.5. TPM (Trusted Platform Module) 2.0

The Barton Springs 1S card utilizes the same TPM connector and module that is used on the User Interface Card in the Grand Canyon system. This TPM module enables security features needed for secure boot. The Barton Springs 1S compute card will utilize the Infineon TPM 2.0 SLB9670 series parts.

7.6 Switches and LEDs

Each Barton Springs 1S card has a green heartbeat LED that is controlled by the Bridge IC and blinked if everything is healthy.

There is a blue and amber LED on the Barton Springs 1S card that is controlled by the BMC. These LEDs are used to indicate status of the Barton Springs 1S card according to the LED specifications below in figure 7.1

Permitted States	Separate LEDs (preferred)		Combined Blue/Amber LED (limited space)
	STS (Blue)	FAULT/LOC (Amber)	STS
Module Off/Service Action Allowed			
Module On/Status OK			
Module Off + Fault			
Module Off + Locate			
Module On + Locate			
Firmware Update in Progress	N/A	N/A	

OFF
ON (Steady on)
BLINK (1 Hz rate – 0.5s On, 0.5s Off)

Figure 7.3 LED Behavior

7.7 Debug Header

The Barton Springs 1S server shall support traditional ITP/XDP debug headers.

7.8 PCB Stackup

Version 01 Confidential level <機密等級> : Internal/Classified <密>

Board Number:	20W002-1M
Project Name:	Grand Canyon
Model Name:	GRAND CANYON MB (BS) PVT3
Layer Count:	12
Date:	2022/1/7
Low Loss Material:	EM-526 +RTF2 / TU-863 plus +VLP (Tg>170, Td>365)
Gold Finger (Y/N):	No
Customer:	N/A
Thickness (mm):	2.36
EE / SI Engineer:	Wallace Liu / Min Che
Back Drill Via / Panel Rotation 10° :	No / No

Layer		Cu Weight	Thickness		Glass/Copper Type		Er (1GHz)		DF @16GHz 80C		85 ohm Delay (ps/inch)	
		Wiwynn/Vendor	Wiwynn	Vendor	Wiwynn	Vendor	Wiwynn	Vendor	Wiwynn	Vendor (1GHz 25C)	Wiwynn	Vendor (85 ohm)
	Mask		0.50				3.8		0.036736			
Top	Signal	0.5 oz + plating	1.90		HTE						128.7487	
	Prepreg		2.70				3.3		0.008817			
L2	Ground	1.0 oz	1.30		RTF2							
	Core		4.00				3.3		0.00975			
L3	Signal	1.0 oz	1.30		RTF2						153.8046	
	Prepreg		4.00				3.3		0.00975			
L4	Ground	1.0 oz	1.30		RTF2							
	Core		3.00				3.3		0.00975			
L5	Signal	1.0 oz	1.30		RTF2						153.8046	
	Prepreg		18.00				3.3		0.00975			
L6	Power	2.0 oz	2.60		RTF							
	Core		10.00				3.3		0.00975			
L7	Power	2.0 oz	2.60	0.00	RTF	0						
	Prepreg		18.00	0.00	0	0	3.3	0	0.00975	0		
L8	Signal	1.0 oz	1.30	0.00	RTF2	0					153.8046	0
	Core		3.00	0.00	0	0	3.3	0	0.00975	0		
L9	Ground	1.0 oz	1.30	0.00	RTF2	0						
	Prepreg		4.00	0.00	0	0	3.3	0	0.00975	0		
L10	Signal	1.0 oz	1.30	0.00	RTF2	0					153.8046	0
	Core		4.00	0.00	0	0	3.3	0	0.00975	0		
L11	Ground	1.0 oz	1.30	0.00	RTF2	0						
	Prepreg		2.70	0.00	0	0	3.3	0	0.008817	0		
Bottom	Signal	0.5 oz + plating	1.90	0.00	HTE	0					128.7487	0
	Mask		0.50	0.00	0	0	3.8	0	0.036736	0		
Thickness requirement : 2.36 ± 10% (mm)		mil (with solder mask)	93.80	0.00								
		mm (with solder mask)	2.38	0.00								

Figure 7.4 Barton Spring Stackup

8. THERMAL DESIGN REQUIREMENTS

To meet thermal reliability requirements, the thermal and cooling solution should dissipate heat from the components when the system is operating at its maximum TDP (Thermal Design Power). The thermal solution should be found by setting a high-power target for initial design in order to avoid redesign of the cooling solution. However, the final thermal solution of the system should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. The thermal solution should not allow any overheating issue for any components in the system. The CPU or memory should not throttle due to any thermal issue under the following environment:

- Inlet temperature lower than or equal to 35°C, and 0-inch H_2O datacenter pressure with all FANs in each thermal zone running properly.
- Inlet temperature lower than or equal to 35°C, and 0.005-inch H_2O datacenter pressure with one FAN (or one rotor) in each thermal zone failed.

8.1. Data Center Environmental Conditions

This section outlines Meta data center operational conditions.

8.1.1 Location of Data Center/Altitude

The maximum altitude is 6,000 ft above sea level. Any variation of air properties or environmental difference due to the high altitude needs to be deliberated into the thermal design.

8.1.2 Cold-Aisle Temperature

Data centers generally maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with 3°C standard deviation. The cold aisle temperature in a data center may fluctuate minutely depending on the outside air temperature. Every component must be cooled and must maintain a temperature below its maximum specification temperature in the cold aisle.

8.1.3 Cold-Aisle Pressurization

Data centers generally maintain cold aisle pressure between 0 inches H_2O and 0.01 inches H_2O. The thermal solution of the system should consider the worst operational pressurization possible, which generally is 0 inches H_2O and 0.001 inches H_2O with a single fan (or rotor) failure.

8.1.4 Relative Humidity

Data centers usually maintain a relative humidity between 20% and 90%. The thermal solution must sustain uninterrupted operation of the system across the aforementioned RH range.

8.2. Server Operational Condition

8.2.1 System Volumetric Flow

The unit of airflow (or volumetric flow) used for this spec is cubic feet per minute (CFM). The CFM can be used to determine the thermal expenditure or to calculate the approximate Delta T of the system. The thermal expenditure is quantified by the metric CFM/W, which is calculated by the formula shown on the following page.

$$\text{Thermal Expenditure} = \frac{\text{System airflow}}{\text{Total system power consumption, including fans}} \ [\text{CFM/W}]$$

The required airflow is 0.115 CFM per watt in the system level at sea level. The desired airflow per watt is 0.1 or lower in the system up to 35°C (95°F) ambient temperature at sea level for both 1U and 2U blade form factors. The cooling solution shall take the pre-heating effect from the expansion card into consideration if there is any.

8.2.2 Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The server blade design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 7% thermal margin for every component on the card.

8.2.3 Upper Critical Threshold

The upper critical threshold (UCT) setting should allow the detection of abnormal thermal behaviors in the system. The UCT values for the sensors that are not used in Fan Speed Control (FSC) should use a 15% thermal margin from the worst experiment data. The UCT values for the sensors used in FSC, except for CPU, inlet, and outlet sensors, should use a 20% thermal margin from the worst experiment data.

8.2.4 Thermal Testing

Thermal testing must be performed at a low inlet temperature 15°C (59°F) and up to 35°C (95°F) inlet temperature to guarantee the design is free of thermal defect and has high temperature reliability. Rack-level airflow testing is recommended to evaluate rack level containment and ensure the thermal design will meet rack-level deltaT requirement.

8.3. CPU Cooling Solution

8.3.1 Passive Cooling Solution

The heat sink must be a thermally optimized design at the lowest cost. Passive cooling is desired. Heat sink installation must be uncomplicated. The heat sink fins should be aligned with the airflow direction. Heat sinks must not block debug headers or connectors and may require cutouts in order to avoid tall electrical components on the server card.

8.4. Reliability Requirements

The operating life of the server card is a minimum of 3 years with a target life of 5 years. All pertinent reliability data for CPU cooling solution and PCBA must be provided to meet the MTBF of 1.5 million hours.

8.5 M.2 Cooling Solution

The Barton Springs 1S will support one M.2 NVME device. [MR1]

The cooling solution for M.2 cooling must be a thermally optimized design at the lowest cost. Passive cooling is required with TIM and heat sink solution being desired. Integrated heatsink is desired to enable easy serviceability. The solution must maintain all M.2 component temperatures within their operational limits during all stress conditions. 6.7mm M.2 connectors must be used to allow spacing between the integrated heat sink base and server board PCB.

8.6 Temperature and Power Sensors

Each card must provide following sensors:

- Temperature sensors for PCH, CPU, DIMM, voltage regulators and other critical chips
- Power sensors for the PCH, CPU, DIMM and the whole card
- Voltage sensors for all voltage rails
- Power/current sensors for rails providing more than 10W
- One inlet ambient temperature sensor and one outlet ambient temperature sensor

The BMC on the platform must be able to read all these sensors via the Bridge IC. Additionally, over-temperature thresholds must be configurable, and an alert mechanism must be provided to enable thermal shutdown and/or an increase in airflow. The sensors are accurate to +/-2°C and desired to be within 2% tolerance across the whole operation temperature range. The goal sensor accuracy is +/-1°C.

8.7 Server Card Air Baffle

The card level air baffle must be designed to help maintain temperatures of all major components on the server card by reducing bypass air and increasing airflow through key components. The air baffle must be easy to service with the goal of requiring no tooling to remove. The air baffle must not have a large adverse effect on system level pressure drop.

9. I/O SYSTEM AND MANAGEMENT

This section will define all the different interfaces utilized on the Barton Springs 1S server card.

The primary server management functions will be provided using a BMC on the platform. The BMC on the platform will use an I_2C bus as the management interface. This section also identifies the required information that must be accessible from the BMC.

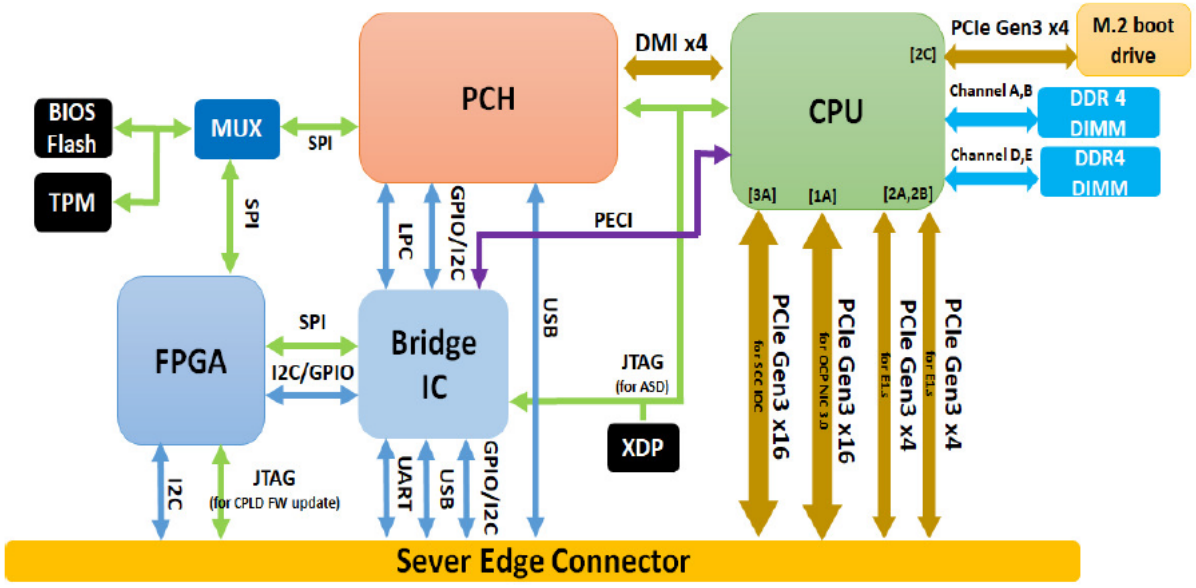

Figure 9.1 Barton Springs Block Diagram

9.1. Platform Agnostic Throttle Management Architecture (PATMA)

The Barton Springs 1S will support PATMA, a protection mechanism that will allow the server to throttle itself before tripping hardware faults. This implementation will utilize a CPLD to enable hardware abstraction through the platform BMC where utilities will have the ability to monitor throttle sources, toggle throttling sources, reprogram pre-defined thresholds, log throttle events.

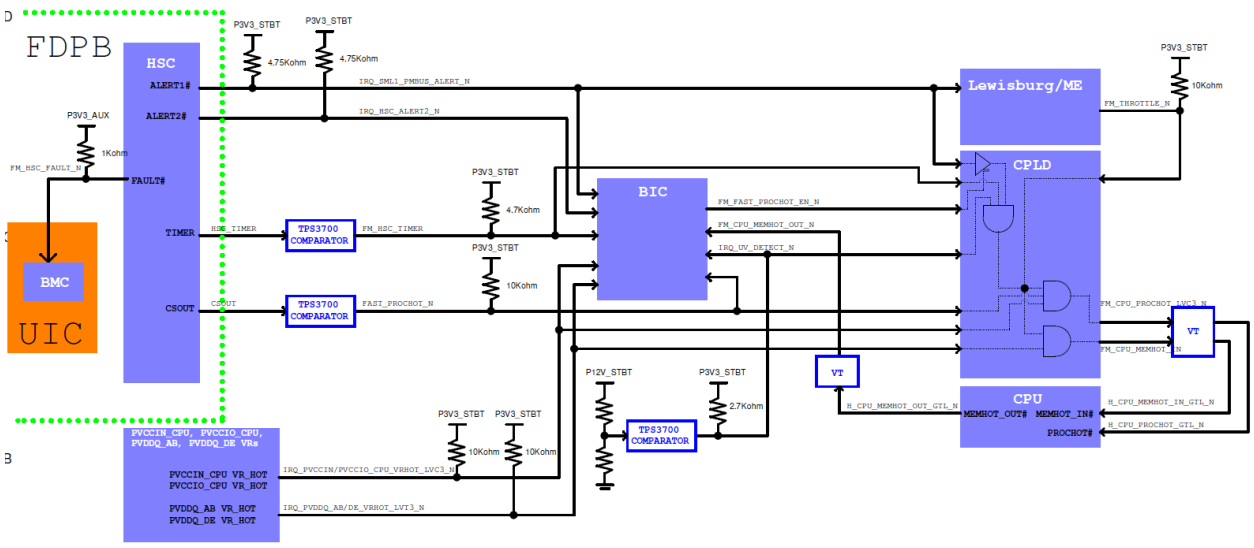

Figure 9.2 Barton Springs PATMA block diagram

9.2. Bridge IC (BIC)

The Barton Springs 1S will use a Bridge IC which is defined as a bridging device between the CPU and the platform's BMC. The Bridge IC will be powered by stand-by voltage rails so that it can be accessed by the BMC when the card is off.

The Bridge IC has a dedicated I2C bus to the CPU's Intel® Manageability Engine that supports IPMB. The Bridge IC behaves as a transparent bridge to forward IPMI messages between the BMC and CPU's Intel® Manageability Engine. With this transparent bridge, the BMC can directly work with the Intel® Manageability Engine to perform most server management functions. The Bridge IC will also implement a system interface LPC to enable in-band server manageability. A KCS interface is implemented and it supports both standard SMM and SMS interfaces.

The Bridge IC will have a FRU EEPROM in addition to thermal sensors on a local I2C bus. The BMC can communicate with the Bridge IC to acquire the FRU and thermal data through the Intelligent Platform Management Bus. The thermal sensors are primarily used to measure the inlet and outlet temperatures of the server for the platform thermal management's algorithm.

It is recommended to use a versatile microcontroller as the Bridge IC. The microcontroller should have two Serial Peripheral Interfaces (SPI). The first SPI bus is used for its own boot ROM if it does not have an integrated boot ROM. The second SPI shall be used to reprogram the CPU's boot ROM when it is corrupted with a multiplexer and BMC's support.

9.3. IPMB Interface

The Bride IC provides an IPMB interface for the BMC to access various IPMI resources on the Barton Springs 1S. To meet this requirement, the Bridge IC shall implement various standard IPMI commands. It shall implement FRUID commands to identify the 1S server, System Event Log (SEL) commands to store server specific event logs, and Sensory Data Repository (SDR) commands to identify various sensors on the server.

9.4. Message Transfer

The Bridge IC will utilize KCS interfaces to transfer information between the CPU and platform BMC.

For in-band management, the Bridge IC can forward the CPU's Keyboard Controller Style (KCS) request to the BMC and then send the received response back to the CPU.

When the BMC sends a request on the I2C bus meant for the CPU's Intel® Manageability Engine, the Bridge IC will forward the command on the I2C bus and send the received response back to the BMC.

It is possible to implement an alternative SOL through the Bridge IC. When the alternative SOL features are enabled, the serial data from the CPU's serial port shall be sent to the BMC through the I2C bus. When the BMC sends SOL data, it will be emitted through the serial port.

9.5. Platform Discovery and Configuration

The Bridge IC provides a way for the BMC to discover platform capabilities such as electrical interface assignment. It also provides a way to discover and configure its own capabilities like enabling and disabling the SOL interface and/or POST code interface.

9.6. POST Code Access

During the power-on stage, the CPU will send out status/error information on the POST Code interface. The Bridge IC needs to provide a way for the BMC to access POST Code information. The Bridge IC shall keep the latest POST Code in a 230-byte buffer. Whenever the BMC is available, the Bridge shall send the POST Code as soon as it is received on the POST Code interface. Whenever the BMC is not available (such as the BMC being in a firmware update mode or during boot-up) the Bridge IC shall add the latest POST Code at the top of the 230-byte buffer. The BMC shall be able to retrieve the POSTCode buffer from the Bridge IC with the latest POST Code.

9.7. Interrupts and Errors

Figure 9.3 below shows the various error and interrupt signals on the Barton Springs compute card.

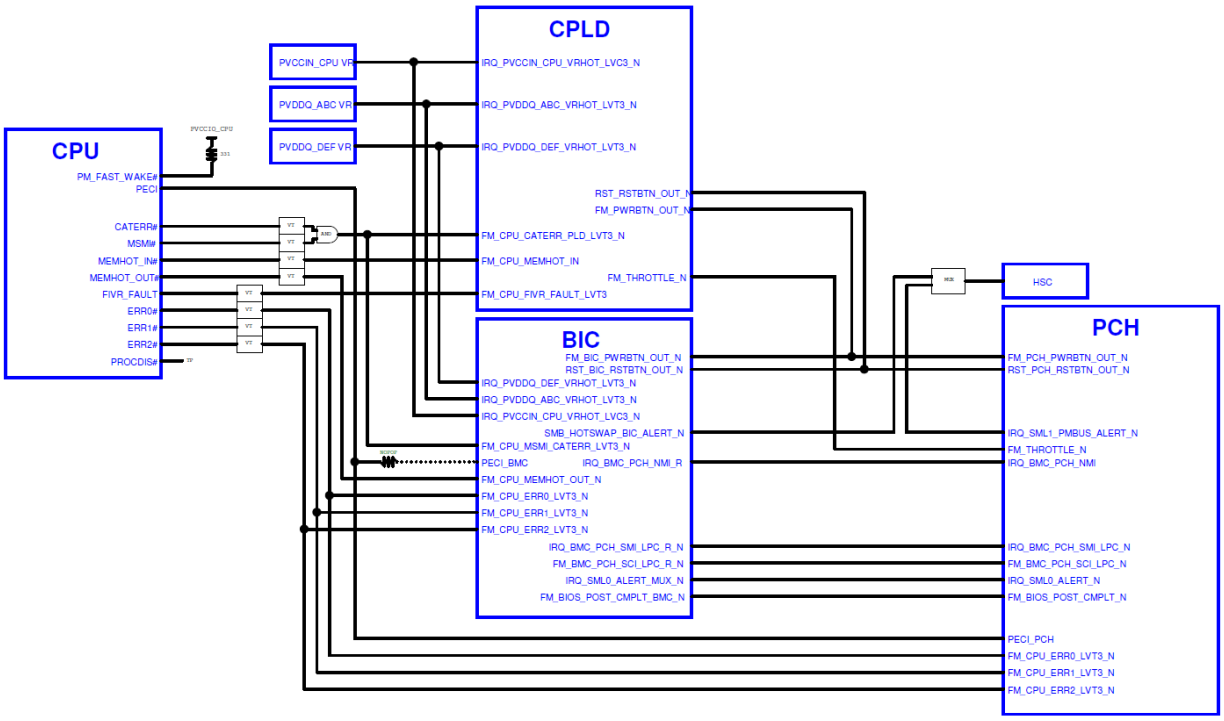

Figure 9.3 Barton Springs Error and Interrupt Signals

9.8. JTAG

The diagram below shows the JTAG architecture on the Barton Springs compute card.

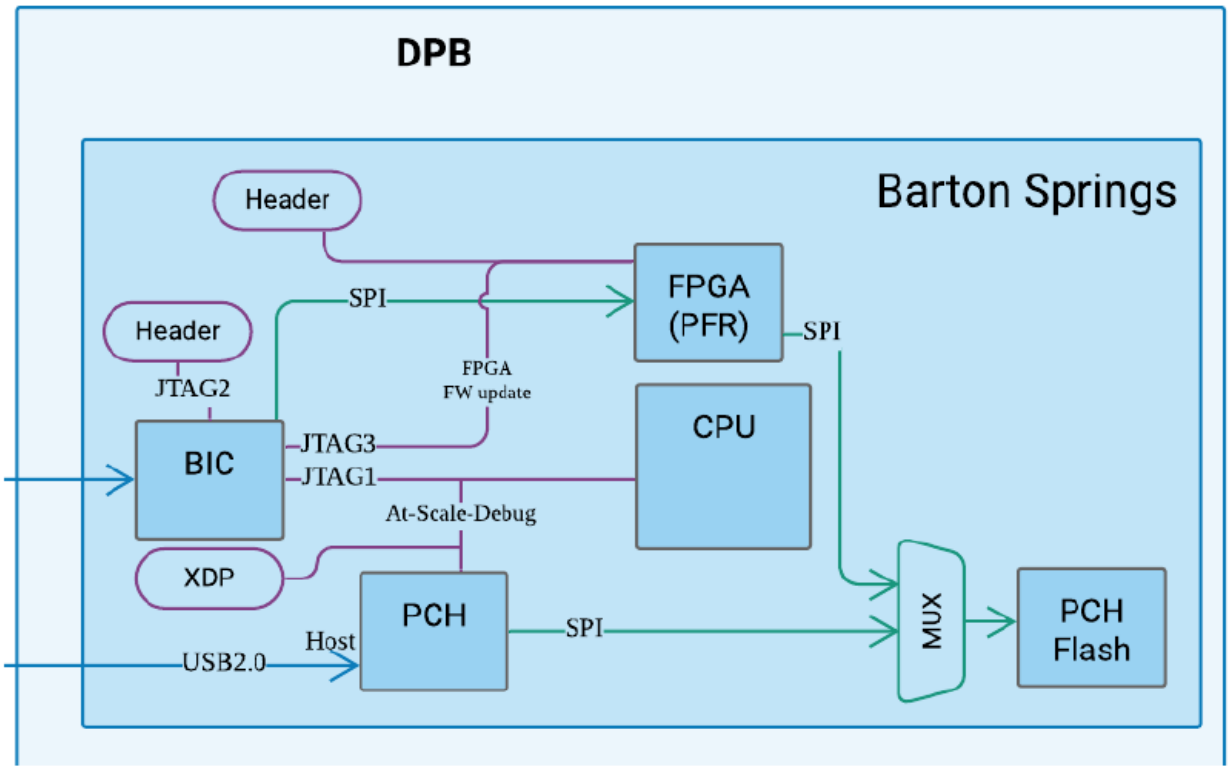

Figure 9.4 Barton Springs JTAG Configuration

9.9. USB

The Barton Springs 1S supports a single USB 2.0 connection. This interface connects to both the front USB connector on the UIC card as well as to the BMC through a USB hub located on the UIC board.

9.10. Serial Port

The Barton Springs 1S supports 1 UART connection with the intent for it to be routed to its platform's BMC so that the CPU can be accessed locally or remotely via Serial Over Lan (SOL). This serial port can be used for debugging purposes.

9.11. PCIe

Up to 40 external PCIe Gen 3 lanes are supported while on board The Barton Springs 1S will utilize 4 PCIe Gen 3 lanes to communicate with its NVMe M.2 boot drive.

9.12 SPI

SPI is the BIOS interface for the PCH. Barton Springs will use Quad SPI to load BIOS quickly. PFR uses the CPLD to act as the Platform Root of Trust for ensuring security and preventing intrusion and corruption of SPI Flash. The CPLD can talk to the SPI Flash via the SPI mux which it controls. The CPLD also has a direct path to the SPI Flash to monitor traffic and enforce SPI filtering.

The platform BMC can program the SPI Flash Out of Band (OOB), through the Bridge IC. To enable this action, the CPLD will implement a mux in its logic to allow the Bridge IC to use the PFR SPI path.

9.13 I2C

A single I_2C communication bus is used to connect the BMC on the platform to the Bridge IC on the server side. This is used as the primary server management interface. It will support a minimum speed of 400kHz with up to 1Mhz being preferred. The I_2C alert signal is required and is used as an interrupt for both the Bridge IC and the BMC.

The Barton Springs 1S will also have a local I2C bus to communicate with a FRU EEPROM and thermal sensors. The diagram below shows a high level of the I2C configuration on the Barton Springs board.

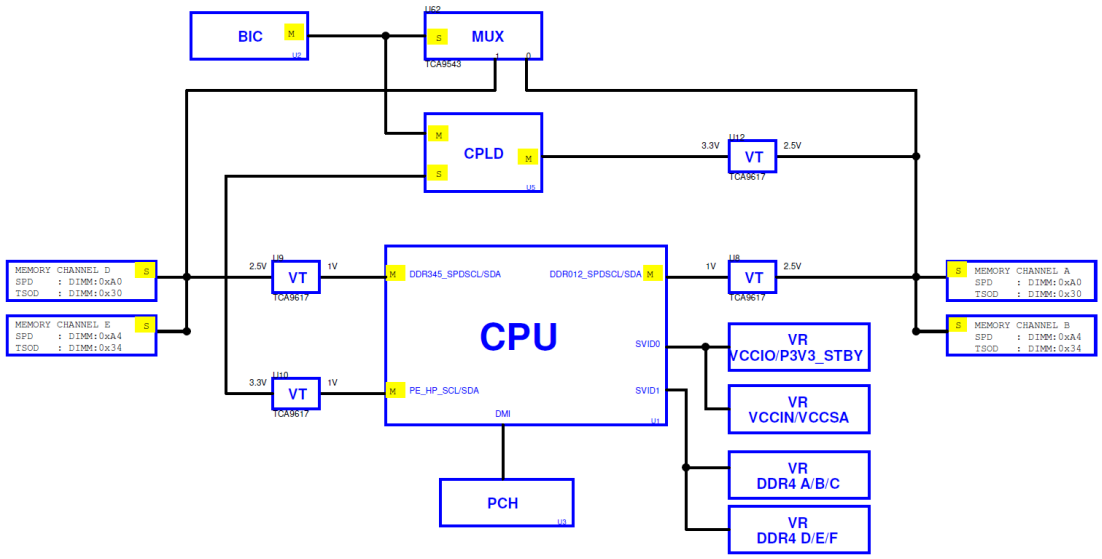

Figure 9.5 Barton Springs I2C Configuration

9.13.1 I2C Detailed Diagrams

Figure 9.7 and Figure 9.8 show the more detailed implementation of the I2C architecture on the Barton Springs Compute board.

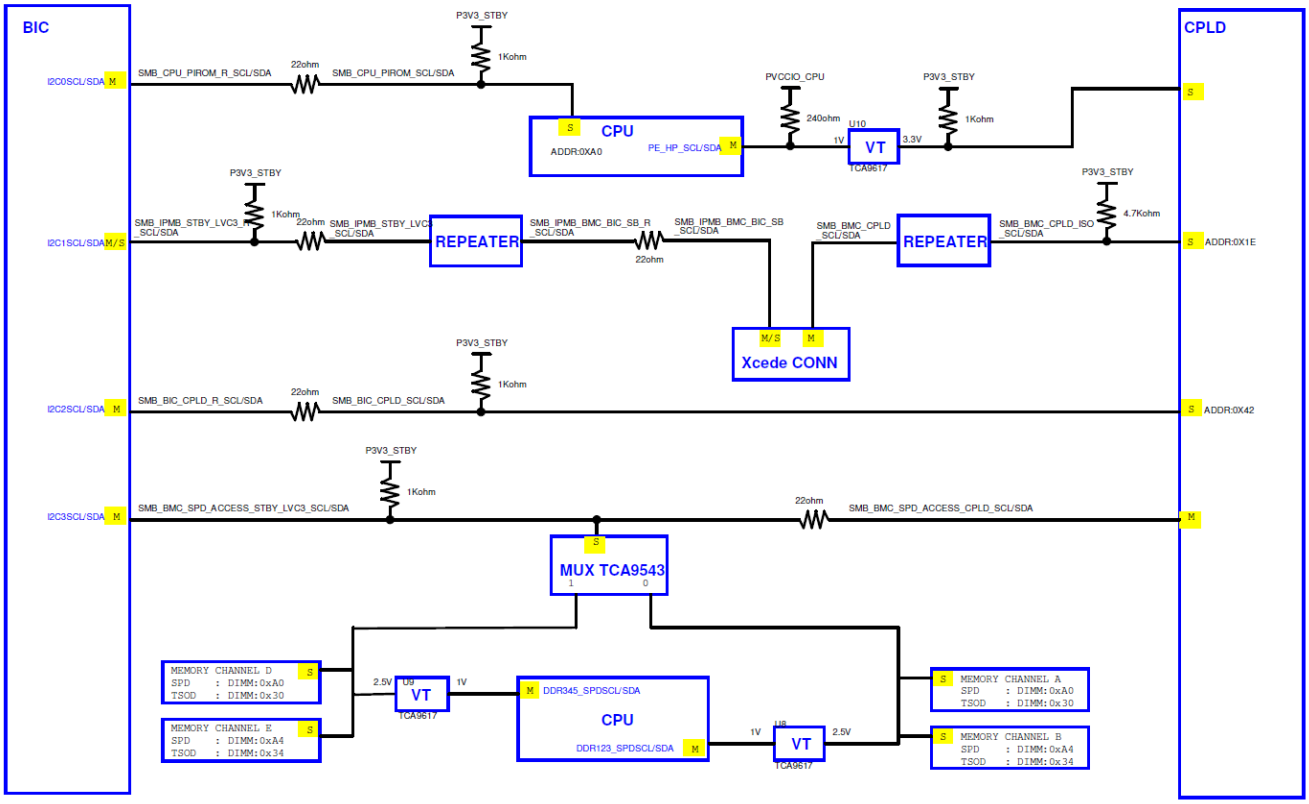

Figure 9.6 Barton Springs I2C Architecture - Detailed

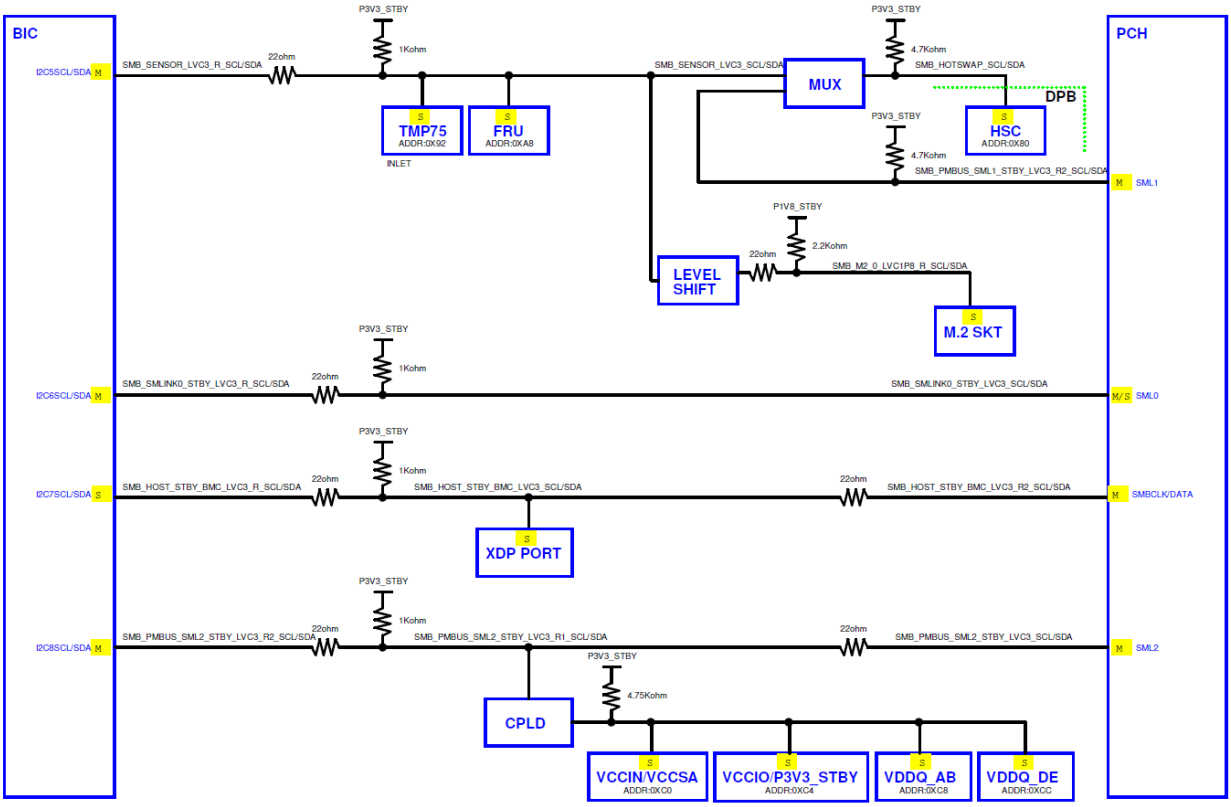

Figure 9.7 Barton Springs I2C Architecture - Detailed

9.13.2 I2C Addressing

The I2C bus address for the Bridge IC is configured as 0x40. The BMC on the platform shall be configured as 0x20.

I2C addresses can be found in the detailed I2C block diagrams in the previous section.

9.14 MIPI/Debug Block Diagram

Figure 9.9 below shows the MIPI/debug interfaces available on the Barton Springs compute card.

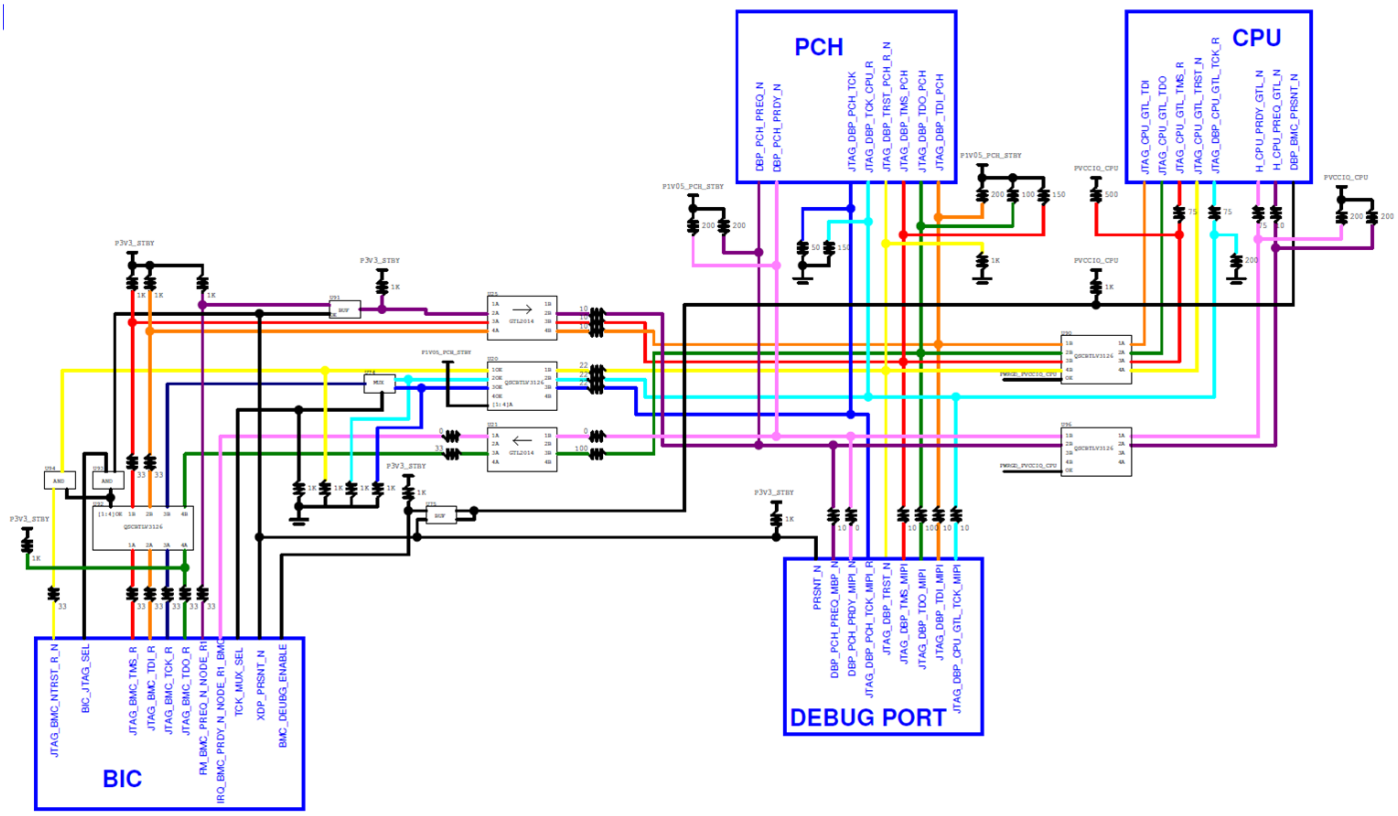

Figure 9.8 Barton Springs MIPI/Debug Interfaces

9.15. Clocking Architecture

Figure 9.10 below highlights the clocking architecture utilized on the Barton Springs compute card.

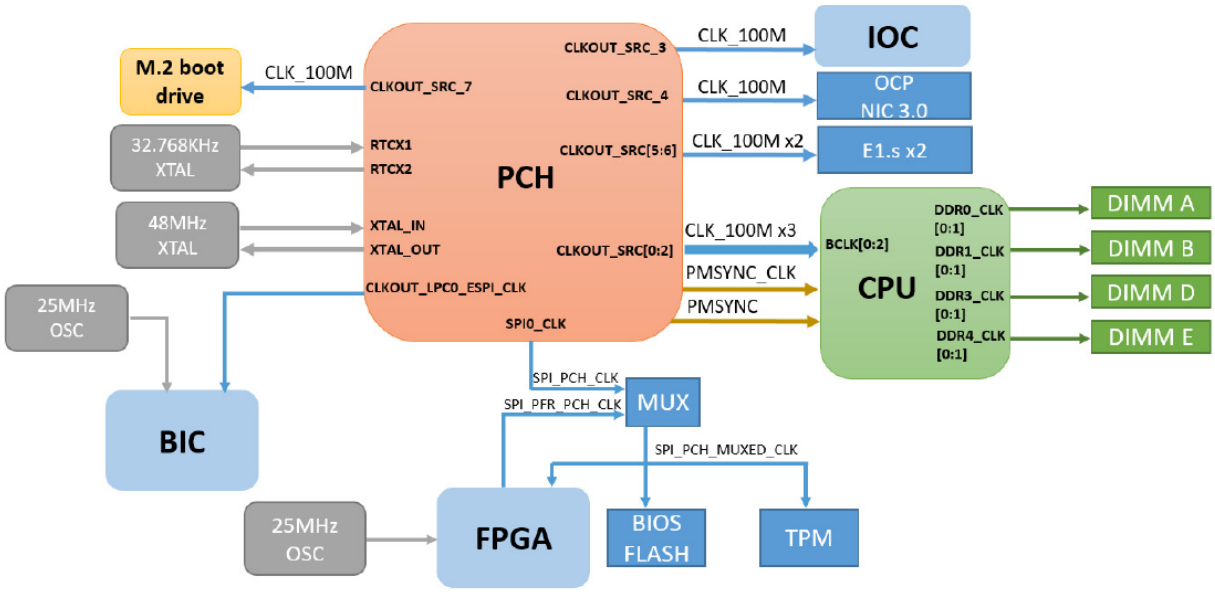

Figure 9.9 Barton Springs Clocking Architecture

10. RACK IMPLEMENTATION

Barton Springs will be implemented as part of the Grand Canyon system and not directly interact with a rack.

11. MECHANICAL

11.1. Barton Springs Dimensions

The overall dimensions of the card are 242.5mm x 153mm as seen in figure xxx below.

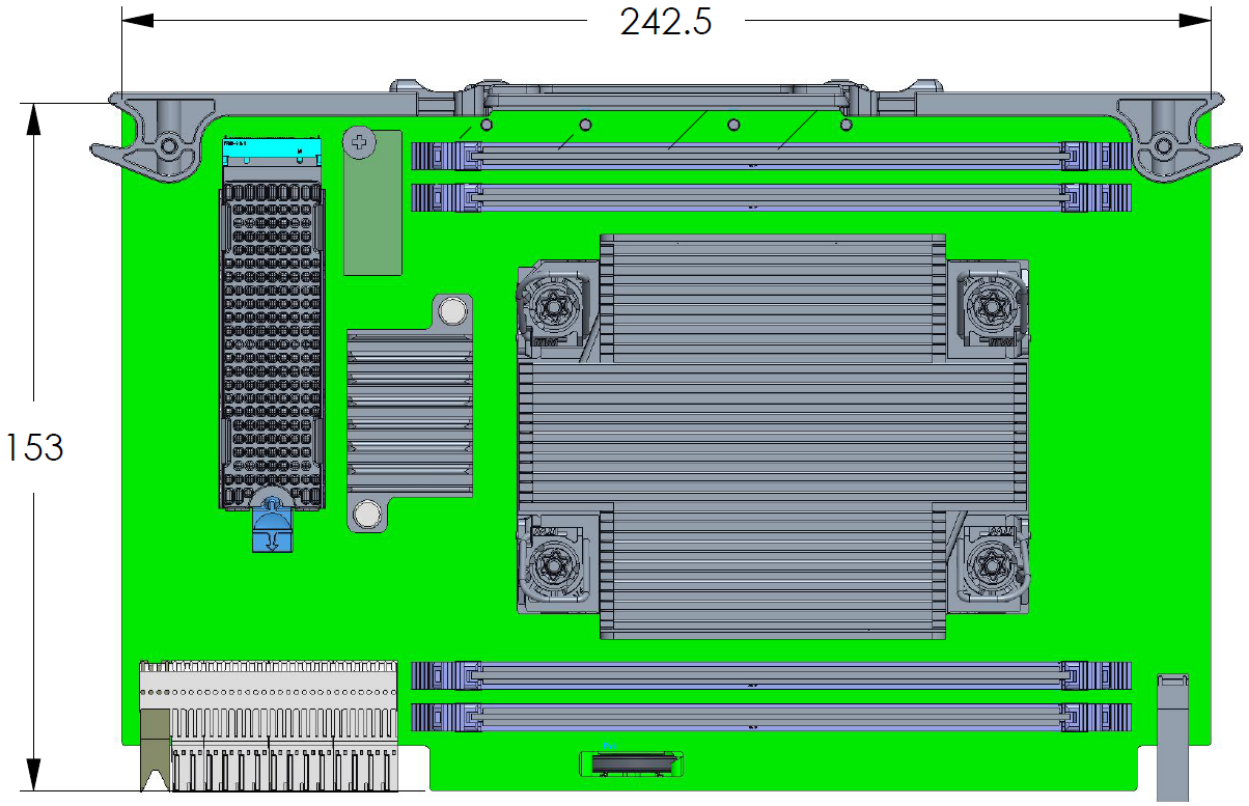

Figure 11.1 Barton Springs Dimensions (Top View)

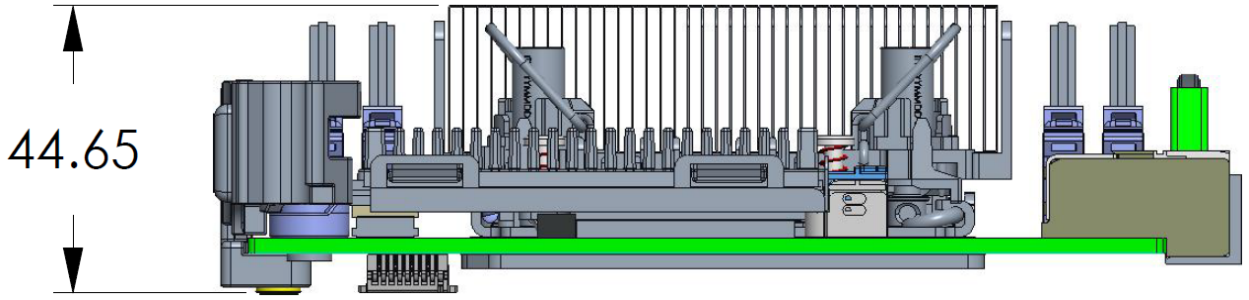

Figure 11.2 Barton Springs Dimensions (Side View)

11.2. PCB Thickness

The thickness of the PCB shall be 2.36mm ± 2.4mm.

Components with significant height will be placed on the top side with a maximum height limit of 36.1mm. Low profile components of a height less than 6.1mm can be placed on the bottom side.

11.3. Heat Sink & PHM

The heat sink must be a thermally optimized design at the lowest cost. Heat sinks must not block debug headers or connectors. The heat sink fins should be aligned with the airflow direction. The maximum heat sink height from the top of the PCB is 36.1mm.

The heat sink is part of a PHM (Processor Heatsink Module), which consists of the heatsink, CPU, and processor carrier. This is to be installed onto the PCB-mounted bolster plate and socket. All components that are part of this stack are to be designed and assembled per Intel specifications for the LGA4189 socket Cooper Lake CPU.

11.4. Connectors

11.4.1 Backplane Connector

Barton Springs uses an Amphenol XCede HD backplane connector assembly, PN JX410-51433. This assembly consists of three 4-pair 8-position 85 ohm impedance HSD modules, one 4-pair 4-position 85 ohm impedance LC module, and one guide module.

11.4.2 Power Connector

For power, Barton Springs uses an Amphenol XCede HD 3 pair power module, PN 928-3000-D7H.

11.5. Latches

Barton Springs features two spring-based latch ejectors to securely install it into the Bryce Canyon system. The latches shall each have a spring-based touchpoint that is Pantone 375C colored.

12. POWER SYSTEM

Below is the power architecture for the Barton Springs 1S server design

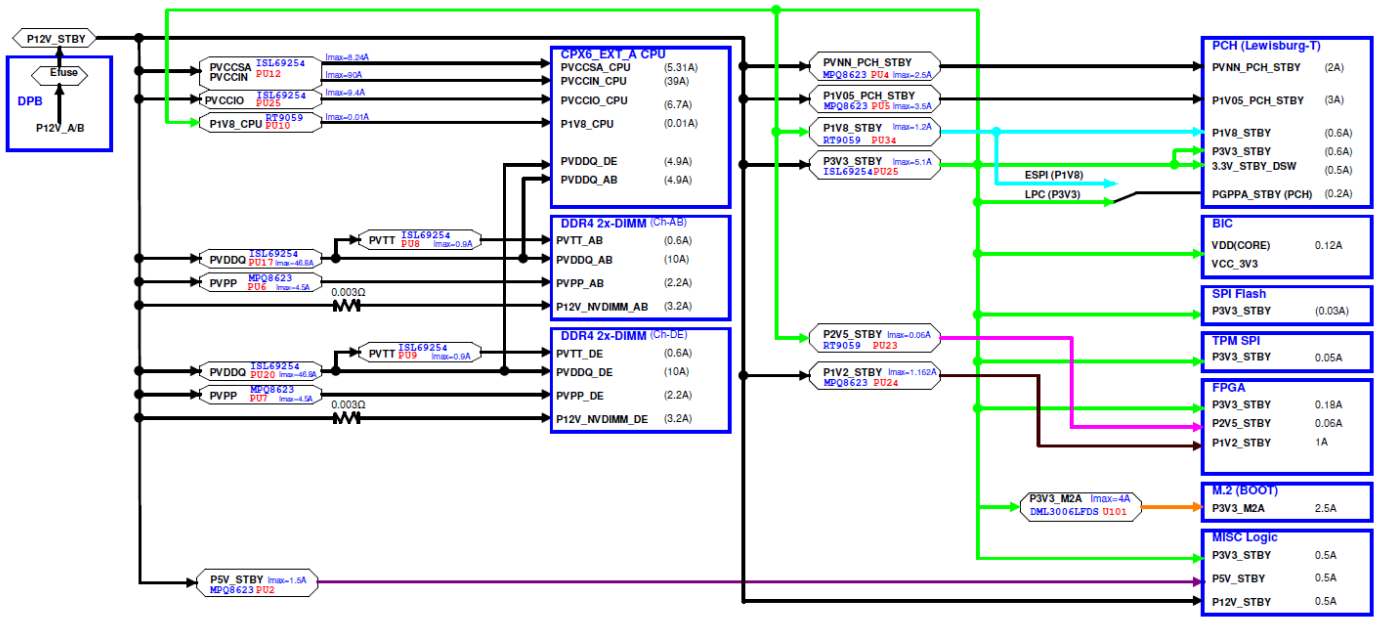

Figure 12.1 Barton Springs Power Architecture

12.1. Input Voltage

The input voltage to the Barton Springs 1S server card will be +12.5V +/-7%.

12.2. Power Sequencing

Below is a diagram of the power sequencing circuitry for the Barton Springs 1S board.

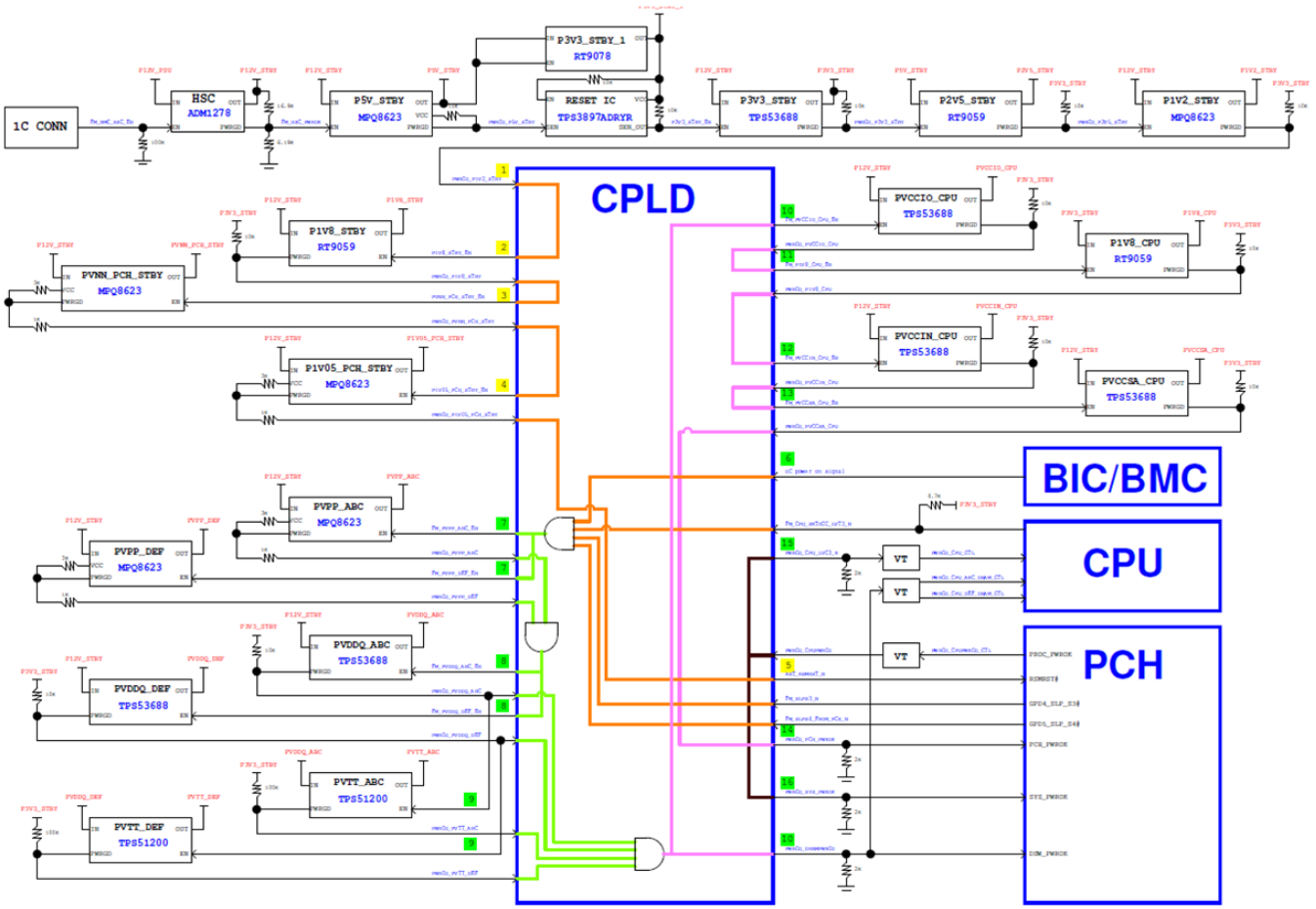

Figure 12.2 Barton Springs Power Sequencing Design

12.3. Power Good and Reset Diagram

The diagram below shows the power good and reset architecture for the Barton Springs compute card.

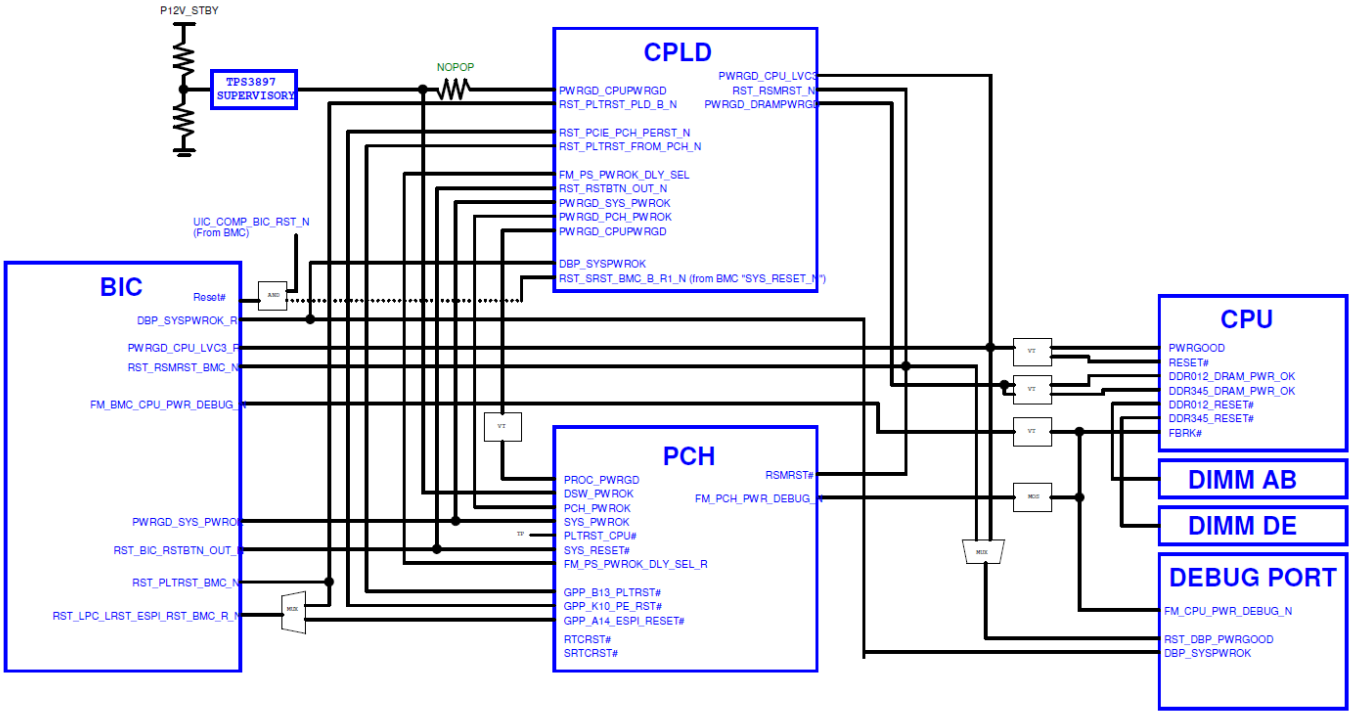

Figure 12.3 Barton Springs Power Good and Reset Diagram

12.4. Power and Reset Timing

Figure 12.4 below shows the power and reset timing for the Barton Springs compute card.

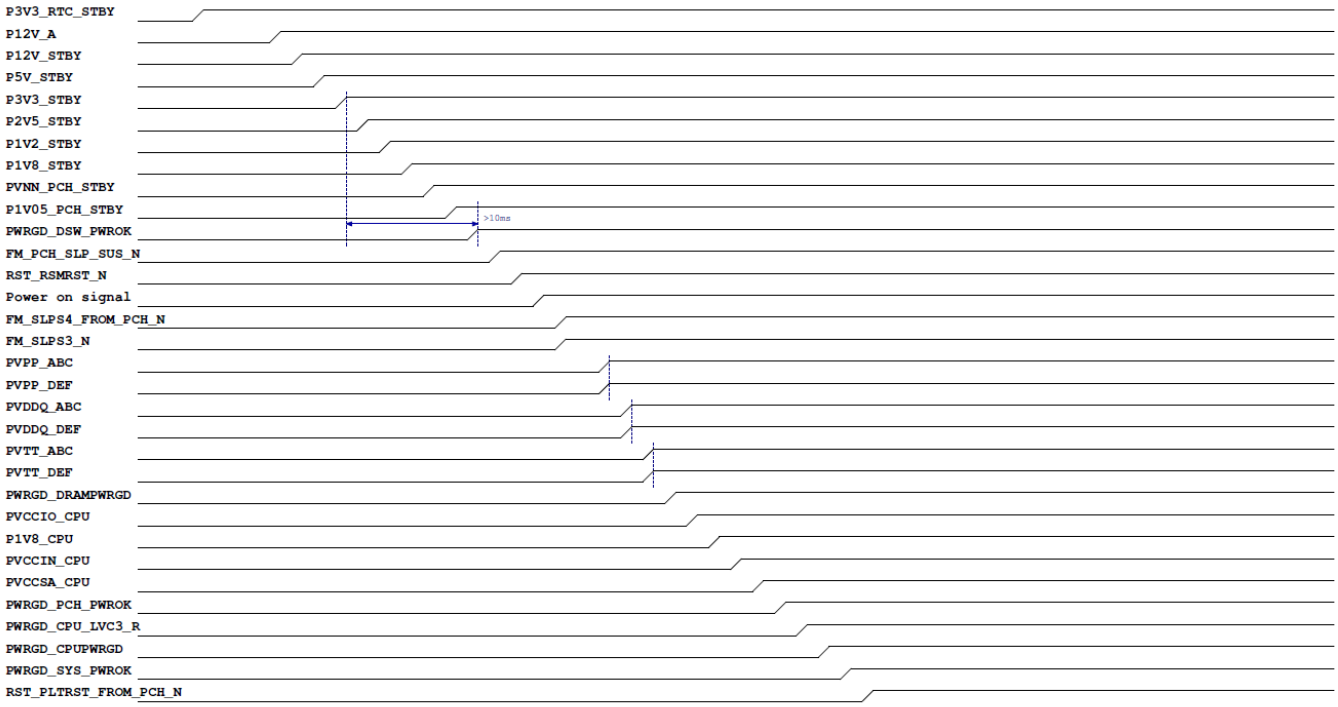

Figure 12.4 Barton Springs Power and Reset Timing

13. ENVIRONMENTAL AND REGULATIONS

Responsible for successful completion and demonstration of compliance to the FCC Authorization Program Requirements, EU Directive requirements, and NRTL Product Safety requirements specified below for L10 product.

13.1 Regulatory Compliance

- FCC Compliance: The product shall comply with FCC subpart 15 b class A. Characterization documentation and test data shall be provided.
- CE Compliance: The Product shall comply with the EU Directives noted below. Meta shall be provided with a CE Declaration of Conformity and complete technical reports and other documentation files for the following:

A. The Low Voltage Directive; 2014/35/EU
B. The EMC Directive; 2014/30/EU
C. RoHS 2 Directive; 2011/65/EU, unless there are legal exemptions allowed
D. REACH Regulation; 1907/2006

13.2 Product Safety Compliance

Barton Springs shall be tested in a host system (Grand Canyon). The host L10 system shall be Listed by a Nationally Recognized Testing Laboratory (“NRTL”) acceptable to Customer. Each L10 unit shipped shall bear the Listing Mark in accordance with the listing requirements of the NRTL. Testing and evaluation shall be conducted to the following latest standards deemed appropriate by the NRTL per equipment classification requirements.

- UL 62368-1, IEC 62368-1 and EN 62368-1; hazard-based performance standard for Audio video, IT & Communication Technology Equipment.

NRTL Certificate and complete technical report(s) per EN 60950-1, UL 60950-1, CAN/CSA-C22.2 No. 60950-1; Safety of Information Technology Equipment, General Requirements per Edition 2 and Amendment 2.

14. Environmental Requirements

Barton Springs (as a component of the Grand Canyon system) must meet the following environmental requirements:

- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: 0°C to +35°C
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C (long-term storage)
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-rating to 1000m (6000 feet)

14.1. Vibration & Shock

Barton Springs (as a component of the Grand Canyon system) must meet shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) and IEC721-3-(*) Standard and Levels. The testing requirements are summarized in 14.1 on the following page.

Table 14.1: Vibrations and Shock Testing Requirements

	Operating	Non-Operating
Vibration	0.4g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave / minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 5 to 500 Hz, 10 sweeps at 1 octave / minute per each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks per each of the three axes	12g, half-sine 11mS, 6 shocks per each of the three axes

14.2. EMC Compliance

Barton Springs shall be tested in a host system (Grand Canyon). The host L10 system including Barton Springs shall meet all relevant EMC requirements included in the latest version of the following standards.

- FCC CFR47 Part 15, Subpart B, Class A criteria
- EU EMC Directive (2004/108/EC); common broad objectives for EMC regulations, so that electrical equipment approved by any EU member country will be acceptable for use in all other EU countries.
- Meta compliance requirements: FBPN 18-00020

14.3. Labels and Markings

The motherboard shall include the following labels on the component side of the motherboard. The labels shall not be placed in a way which may cause them to disrupt the functionality or the airflow path of the motherboard.

Description	Type	Barcode Required?
Safety Markings	Silk Screen	No
Vendor P/N, S/N, REV (Revision would increment for any approved changes)	Adhesive label	Yes
Vendor Logo, Name & Country of Origin	Silk Screen	No
PCB Vendor Logo, Name	Silk Screen	No
Date Code (Industry Standard: WEEK / YEAR)	Adhesive label	Yes
RoHS compliance	Silk Screen	No
WEEE Symbol. The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the Manufacturer at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silk Screen	No
CE Marking	Silkscreen	No
UL Marking	Silkscreen	No

14.4 Mean Time Between Failures (MTBF)

14.4.1 MTBF Prediction

The board design shall have a minimum calculated MTBF of 300K hours at a 95% confidence level at a typical usage condition of 25°C ambient temperature.

- Recommended software is Relex
- For non-critical parts, use standard / default number in Relex
- For high failure rate parts, get actual data from each vendor

14.4.2 MTBF Demonstration

The board design shall also demonstrate the MTBF requirement above by running test as below:

- At full load for 50% of time, and performing AC cycling test 50% of time
- At 45°C ambient temperature for acceleration
- Total test duration needs to be calculated, discussed with and approved by Meta

14.5 Environmental Compliance

Barton Springs shall meet the following environmental compliance requirements. The vendor may provide technical documentations including Declaration of Conformity for the host system including Barton Springs.

- RoHS Directives (2015/863/EU); aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture.
- REACH Regulation (EC) No 1907/2006; registration with the European Chemicals Agency (ECHA), evaluation, authorization and restriction of chemicals.
- WEEE Directive (2012/19/EU); aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture.
- All other environmental requirements described in FBPN: 18-000142.

15. Prescribed Materials

15.1. Disallowed Components

The following components are not to be used in the design of the system:

- Components disallowed by the European Union's Restriction of Hazardous Substances directive (RoHS 6)
- Trimmers and/or potentiometers
- Dip switches

15.2. Capacitors & Inductors

The following limitations apply to the use of capacitors:

- Only aluminum organic polymer capacitors made by high quality manufacturers are used; they must be rated 105°C.

- All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under the worst conditions.
- Tantalum capacitors using manganese dioxide cathodes are forbidden.
- SMT ceramic capacitors with case size >1206 are forbidden (size 1206 are still allowed when installed far from the PCB edge and with a correct orientation thatminimizes risk of cracks).
- Ceramic material for SMT capacitors must be X7R or better material (COG or NP0 type are used in critical portions of the design).
- Conditional usage of X5R ceramic material must be based on evaluation of worst-case thermal conditions and upon approval from Meta.
- Only SMT inductors may be used. The use of through hole inductors is disallowed.

15.3. Component Derating

Please refer to Facebook_Consolidated_Derating_Guidelines_Rev1.0 document. In addition, here are some callouts to ensure best derating practices are followed throughout the design and validation process:

- Use vendor guidelines and datasheet callouts only for that vendor's components
- Thermal derating needs to be accounted for (simulation and measurement correlation is expected to drive CFM targets)
- Special attention to capacitors and estimated lifetime of a capacitor with voltage and temperature derating in place

15.4 Sustainable Materials

Materials and finishes that reduce the life cycle impact of servers should be used where cost and performance are not compromised. This includes the use of non-hexavalent metal finishes, recycled and recyclable base materials and materials made from renewable resources, with associated material certifications.

Meta identified plastic alternatives including polypropylene plus natural fiber (PP+NF) compounds that meet functionality requirements while reducing cradle-to-gate environmental impact when compared to PC/ABS. GreenGranF023T is one acceptable alternate material. JPSECO also offers a PP+NF material that is acceptable; the model number will be available at a later date. It is strongly preferred that such alternatives are identified and used. If a vendor is unable to use this, or a similar alternate material, the vendor will provide a list of materials that were considered and why they were not successfully incorporated.

The supplier shall use Halogen Free (IEC 61249-2-21), arsenic-free (less than 1000 ppm, or 0.1% by weight) and phthalate-free (less than 1000 ppm, or 0.1% by weight) material by default and discuss with Meta and get written approval if there is difficulty with sourcing in L10.

16. System Firmware and Error Handling

All Server products must have a completed OSF Tab in the 2021 Supplier Requirements. At this time, this is not required for any other product types. Please check with the OSF leadership for updates.

Vendors shall be responsible for supplying and customizing the BIOS for the Barton Springs 1S. The specific requirements are outlined in this section. Vendors must make changes to the BIOS at any point in the Barton Springs 1S life cycle (development, production, and sustaining) upon request.

16.1 Specification Compliance

The system BIOS needs to comply with the following specification:

- UEFI Specification version 2.6
- ACPI Specification version 6.2
- SMBIOS Specification version 3.11

16.2 Configuration and Features

The BIOS is tuned to minimize card power consumption. It has the following features:

- Disables unused devices, including PCIe lanes, USB ports, SATA/SAS ports, etc.
- A BIOS setup menu
- The SOC settings can be turned to achieve the optimal combination of performance and power consumption.

16.3 BIOS Settings Tools

The card supplier shall provide a tool to make BIOS setting changes without requiring a BIOS reflash. The BIOS settings update tool must also support success and failure codes so that updates can be easily scripted. This tool has to be compatible in a Linux OS environment.

16.4 PXE Boot

The BIOS supports PXE boot and provides the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first available Ethernet device.

The default boot device priority is:

1. Network (search all configured network interfaces)
2. HDD, SDD, or flash device (local or remote)
3. CD-ROM
4. Removable Device

This process loops indefinitely and requires no user intervention.

16.5 iSCSI Boot

The BIOS shall be capable of iSCSI boot.

16.6 Other Boot Options

The BIOS also supports booting from SATA/SAS and USB interfaces. The BIOS provides the capability to select different boot options.

16.7 BIOS Updates

The BIOS can be updated from the OS under the following scenarios:

- Scenario 1: Sample/Audit BIOS settings
  - Return current BIOS settings, or
  - Save/export BIOS settings in a human-readable form that can be restored/imported (as in Scenario 2)
- Scenario 2: Update BIOS with pre-configured set of BIOS settings
  - Update/change multiple BIOS settings
  - Reboot
- Scenario 3: BIOS/firmware update with a new revision
  - Load new BIOS/firmware on a machine and update, retain current BIOS settings
  - Reboot

Additionally, the update tools have the following capabilities:

- Update from the operating system
- Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots).
- No user interaction (such as prompts)
- BIOS updates and option changes do not take longer than five minutes to complete.

16.8 Remote BIOS Update

The BIOS can be updated remotely under these scenarios:

- Scenario 1: Sample/Audit BIOS settings
  - Return current BIOS settings, or
  - Save/export BIOS settings in a human-readable form that can be restored/imported (as in Scenario 2).
- Scenario 2: Update BIOS with a pre-configured set of BIOS settings
  - Update/change multiple BIOS settings
  - Reboot
- Scenario 3: BIOS/firmware update with a new revision
  - Load new BIOS/firmware on machine and update, retain the current BIOS settings.
  - Reboot

Additionally, the update tools have the following capabilities:

- Update from the remote host over the LAN connections to BMC
- Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots).
- No user interaction (like prompts)
- BIOS updates and option changes do not take longer than 20 minutes to complete.
- Can be scripted and propagated to multiple machines

16.9 SMBIOS Event Log

Per the SMBIOS specification Version 2.6, the BIOS implements SMBIOS Type 15 for an event log and the assigned area is large enough to hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB) and follows the SMBIOS event log organization format for the event log.

A system access interface and application software must be provided to retrieve and clear the event log from the BIOS, including, at minimum, a Linux application for the CentOS operating system.

system and driver as needed. The event log must be retrieved and stored as a readable text file that is easy to handle by a scripting language under Linux. Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID.

16.10 Logged Errors

The following list of errors are logged by the BIOS or Bridge IC. These errors must include the date, time, and location information so that the failing components can be easily identified.

- CPU/Memory errors: Both correctable ECC and uncorrectable ECC errors are logged into the event log. Error categories include DRAM, Link, and others.
- PCIe errors: Any errors that have status registers are logged into the event log, including root complex, endpoint device, and any switch upstream/downstream ports if available. Link disable on errors is also to be logged. Fatal, non-fatal, or correctable error classification follows the chipset vendor's recommendation.
- POST errors: All POST errors detected by the BIOS during POST are logged into the event log.
- SATA or SAS errors: All correctable and uncorrectable errors are logged.
- System reboot events
- Sensor reboot events
- Sensor values exceeding warning or critical thresholds
- Power-startup sequencing failure events

The System Event Log (SEL) format and decoding scheme need to comply with the Meta Unified SEL Format.

16.11 Error Thresholds

An error threshold setting must be enabled for both correctable and uncorrectable errors. Once the programmed threshold is reached, an event is triggered and logged.

- Memory Correctable ECC: The threshold default value is 1,000. When the threshold is reached, the BIOS logs the event and includes the physical DIMM location.

16.12 POST Codes

The BIOS outputs a set of Power-On Self Test (POST) codes identifying the current initialization step and any errors encountered along the initialization. The output is provided on the serial console and errors are logged. Errors in POST need to be sent to the BMC in the form of a SEL.

During the boot sequence, the BIOS shall initialize and test each DIMM module. If a module fails initialization or does not pass the BIOS test, the following POSTCodes should indicate which DIMM has failed:

- The first hex character indicates which CPU interfaces the DIMM module.

- The second hex character indicates the number of the DIMM module.
- The POST Code will also display both the error major code and minor code from the memory reference code.
- The display sequence will be “00”, DIMM location, Major code and Minor code with a one second delay for every code displayed.
- The BIOS shall repeat the display sequence indefinitely to allow time for a technician to service the system.

16.13 HOTPLUG Support For PCIe Devices

The BIOS needs to be configured to allow PCIe hot-plug support. This is to ensure that any failure of the PCIe devices connected to the CPU will not bring down the system and allow continued operation in a reduced capacity manner. Logging of such events needs to be done. The HOTPLUG will be categorized in the two following scenarios:

- Software managed HOTPLUG - Removal and addition of M.2 devices on a powered system with OS running. The software shall be staged to get ready for device removal and addition in this scenario. After the process is complete, the serviced device is supposed to come back online.
- Surprise hot removal - M.2 device is not behaving as expected due to errors either on the PCIe link or on the device itself alone. The expectation in this case is only on containing the error and ensuring system availability.

16.14 Latency for SMI Error Handling

It is expected that the error handling of SMI should have latency no more than 20mS. It is expected that this implementation is done using unified SEL for Error/Fault report.

16.15 Support of AC Cycling of PCIe Devices

In the event of device error for PCIe devices in the expansion systems (like accelerators for example), there exists be a mechanism to power cycle these PCIe devices connected using the register in the PCIe config space. This mechanism would need to be made working with devices connecting directly to the Root Complex (CPU) or the PCIe switch. The procedure would generally involve control of GPIOs upon toggling the register. This GPIO could be on the PCIe switch or a CPLD connecting to the reset, power and clock control to the device. It should be noted that for the case where a PCIe switch is not involved, this may involve the following:

- CPU to issue a I2C command through its Hot Plug SMBUS controller to server board CPLD.
- Server CPLD to relay this event to the server BIC either through interrupt, or BIC polling.

- Server BIC to transfer this information to the expansion board BIC.
- Expansion board BIC to sequence the control of power/reset to the relevant device with the expansion board CPLD as a logic gate.

The completed checklist shall be uploaded and available at:

https://github.com/opencomputeproject/OpenSystemFirmware/[vendor_name]/[product_name]/

17. HARDWARE MANAGEMENT

17.1 Redfish Compliance

All Products shall have a completed Hardware Management Tab in the 2021 Supplier Requirements.

17.2 Source Availability

All Products shall have a completed BMC Tab in the 2021 Supplier Requirements if applicable.

Barton Spring is the compute sub-system of GrandCanyon, it shares the same BMC h/w OOB management system with GrandCanyon. Please refer to the GrandCanyon OCP spec to get the source code.

18. SECURITY

All products shall have a completed Security Tab in the 2021 Supplier Requirements.

19. REFERENCES (OPTIONAL)

[1] “Title”, publication year, publication journal/conference/standard, volume, pages, link to publication if available

[2] OCP Profiles - https://github.com/opencomputeproject/OCP-Profiles

[3] Redfish Interop Validator - https://github.com/DMTF/Redfish-Interop-Validator

[4] Redfish Service Validator - https://github.com/DMTF/Redfish-Service-Validator

[5] Redfish Service Conformance Check - https://github.com/DMTF/Redfish-Service-Conformance-Check

APPENDIX A - REQUIREMENTS FOR IC APPROVAL

List all the requirements in one summary table with links from the sections.

Requirements	**Details**	**Link to which Section in Spec**
Contribution License Agreement	OCP CLA	Barton Springs Design S…
Tenets	Openness Efficiency Impact Scale	Barton Springs Design S…
Will they apply for OCP product recognition?		