

Assembly Design Kits (ADK)

Version 1.0

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About Open Compute Foundation

The Open Compute Project (OCP) is a collaborative Community of hyperscale data center operators, telecom, colocation providers and enterprise IT users, working with the product and solution vendor ecosystem to develop open innovations deployable from the cloud to the edge. The OCP Foundation is responsible for fostering and serving the OCP Community to meet the market and shape the future, taking hyperscale-led innovations to everyone. Meeting the market is accomplished by addressing challenging market obstacles with open specifications, designs, and emerging market programs that showcase OCP-recognized IT equipment and data center facility best practices. Shaping the future includes investing in strategic initiatives and programs that prepare the IT ecosystem for major technology changes, such as AI & ML, optics, advanced cooling techniques, composable memory and silicon. OCP Community-developed open innovations strive to benefit all, optimized through the lens of impact, efficiency, scale and sustainability. Learn more at www.opencompute.org

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Compliance with Open Compute Project Tenets

Openness

In this white paper, experts in their fields have contributed their knowledge of chiplet workflows and rules used during the assembly process of heterogeneous chiplet systems.

Efficiency

This white paper strives to improve the efficiency of architects, engineers and manufacturers involved in the integration of heterogenous chiplet systems by providing file format to enable the exchange of design rules for the assembly process.

Impact

This white paper is the first to describe a format for exchanging design rules as they relate to the assembly of heterogeneous chiplet systems.

Sustainability

The contributors hope that this white paper, the first of its kind, will benefit anyone interested in growing the Open Chiplet Economy.

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Executive Summary

The **Assembly Design Kits (ADK)** provide a standardized and open framework designed to address the growing complexities of modern semiconductor assembly and integration. Developed as part of the Open Compute Project (OCP), the ADK facilitates the seamless exchange of design data and ensures compatibility across a wide range of stakeholders, including chip designers, manufacturers, and system integrators.

ADKs enable efficient integration of heterogeneous chiplet systems by defining standardized rules, formats, and tolerances for key design elements such as geometries, layers, interconnects, and assembly processes. These kits promote openness, streamline design workflows, and reduce manual interventions, thereby significantly improving design efficiency, scalability, and innovation.

Key benefits include:

1. **Openness**: Encourages collaboration through shared design formats and specifications.
2. **Efficiency**: Enhances design productivity by reducing redundancy and automating key aspects of integration.
3. **Impact**: Supports the adoption of cutting-edge technologies like AI, advanced cooling, and composable memory, driving innovation in data center hardware.
4. **Sustainability**: Optimizes resources, reduces waste, and aligns with environmentally conscious design practices.

The ADK is poised to play a critical role in advancing the chiplet economy by simplifying the integration of advanced silicon solutions and fostering an ecosystem of interoperable, high-performance semiconductor designs. This white paper outlines the structure, components, and applications of the ADK to support its adoption and implementation across the industry.

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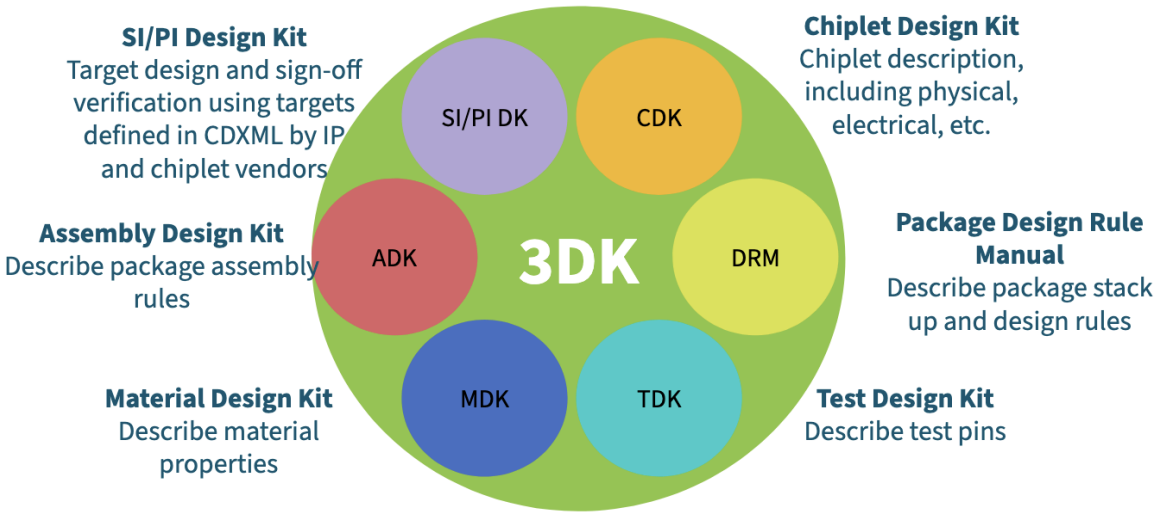
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Introduction

The **Assembly Design Kits (ADK)** aim to establish a standardized framework for the design, integration, and validation of complex chiplet and substrate systems. The increasing complexity of modern semiconductor technologies, coupled with the demand for heterogeneous integration, necessitates a collaborative and open approach to design. ADKs address this need by providing specifications, tools, and guidelines that streamline the development process across various stakeholders, including designers, manufacturers, and integrators.

By standardizing file formats, design rules, and tolerances, ADKs enable efficient data exchange and interoperability across platforms, promoting innovation and reducing development cycles. The kit also supports the integration of advanced design techniques like AI and machine learning into the assembly process, ensuring scalability and adaptability for future technologies.



3D-IC Design Kits (3DK)

Architecture	Chiplet selection	CDK for choosing chiplets ADK for chiplet compatibility DRM for package technology
	Package planing	DRM for choosing a technology MDK for material properties
	System planning	ADK for physical floorplan CDK for netlist creation
	Performance analysis	SI/PI Design Kit MDK for thermal

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Design	DFT	TDK for test connectivity
	Package routing	DRM for design rules
Sign-off	SI/PI analysis	SI/PI Design Kit for sign-off targets MDK for material properties
	Thermal and mechanical analysis	MDK for material properties

Structure

Header

Header object includes information about SI technology, device family, revision/version, giving general information about the file device.

Attribute Name	Definition	Data Type	Required	Example Value
Process	SI process Name	String		xxxx.x
Revision		Integer	Yes	1
version		Integer	Yes	0
DeviceName	Device Name	String		
Date		String		1/1/2025
CellName	Device root Cell Name	String		
Products		String Array		XXX,XXX
Description	Die Function	String		XXX
Units	Definition Units	String	Yes	UM

Includes

Header object includes rule files for top and bottom die files, the current die rules operate upon.

Attribute Name	Definition	Data Type	Required	Example Value
RulesFile	Full path of Top/Botton Die rules file	String	Yes	./xxxx.x.rules
Alias	Alias to refer the file	String	Yes	xxxx.x

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GlobalTolerances

Global Tolerance object linear/angular and Area tolerance values with checking for rules in the absence of rule specific tolerance.

Attribute Name	Definition	Data Type	Required	Example Value
Linear	Linear tolerance for distance checks	float	Yes	xx.xx
Angular	Angular tolerance in Degrees for angle checks	float	Yes	xx.xx
Area	Area tolerance for area/density checks	float	Yes	xx.xx

VersionMap

Version Map object documents the rule version that is currently being used. Used for documentation and parsing additional parameters when applying rule checks.

Attribute Name	Definition	Data Type	Required	Example Value
RuleName	Rule/Check name	string	Yes	BladeAndOffsetCut
Version	Rule Version	integer	Yes	1

Layers

Layers object documents list of layers of the die where various artifacts exist, metal, via, fiducials, outlines, in datatype/layer number format. Used in case of gds/stream die file inputs.

Attribute Name	Definition	Data Type	Required	Example Value
Name	User Defined layer Name	string	Yes	BladeAndOffsetCut
LayerNumber	Layer Number	int	No	xxxx
DataType	Data type of the layer	int		xx

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Geometries

Geometries object documents list of geometries supported by the die file specifically for bump shapes. Used in case of gds/stream die file inputs.

Attribute Name	Definition	Data Type	Required	Example Value
Name	Rectangle	string	Yes	Rectangle

Pads

Pads object documents types of pads present on the die, used to reference the pad as shortcut in the rules. Dimensions can be exact or ranges. Only Name is needed for yDie, all parameters needed in case of gds/stream die file inputs.

Attribute Name	Definition	Data Type	Required	Example Value
Name	User Defined pad name	string	Yes	C4Pads
Geometry	Pad Geometry type	string	Yes	Square
BoxWidth	Bounding Box Width	float	No	xx
BoxHeight	Bounding Box Height	float	No	xx
BoxMinWidth	Bounding Box Minimum Width	float	No	x
BoxMinHeight	Bounding Box Minimum Height	float	No	x
BoxMaxWidth	Bounding Box Maximum Width	float	No	xx
BoxMaxHeight	Bounding Box Maximum Height	float	No	xx
LayerName	Layer name to find the Pads	String	No	BumpsLayer
Properties	Custom Pads Properties	String	no	Probe=True

Fiducials

Fiducials object documents types of Fiducials present on the die, used to reference the pad as shortcut in the rules. Dimensions can be exact or ranges. Only Name is needed for yDie, all parameters needed in case of gds/stream die file inputs.

Attribute Name	Definition	Data Type	Required	Example Value

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Name	User Defined Fiducials name	string	Yes	YFiducialGeometry
Geometry	Pad Geometry type	string	No	Square
BoxWidth	Bounding Box Width	float	Yes	xx.x
BoxHeight	Bounding Box Height	float	Yes	xx.x
BoxMinWidth	Bounding Box Minimum Width	float	No	
BoxMinHeight	Bounding Box Minimum Height	float	No	
BoxMaxWidth	Bounding Box Maximum Width	float	No	
BoxMaxHeight	Bounding Box Maximum Height	float	No	
CellName	Cell name of the fiducial	string	Yes	Y
LayerName	Layer name to find the Fiducial	String	Yes	PRSFidutialLayer

Outlines

Outlines object documents various die outlines i.e., active die edge, physical die edge etc. Only Name is needed for yDie, all parameters needed in case of GDSstream die file inputs.

Attribute Name	**Definition**	**Data Type**	**Required**	**Example Value**
Name	User Defined Outline Name	string	Yes	ActiveEdge
Geometry	Pad Geometry type	string	No	Square
BoxWidth	Bounding Box Width	float	No	xx.x
BoxHeight	Bounding Box Height	float	No	xx.x
LayerName	Layer name to find the Fiducial	String	Yes	ActiveEdgeLayer
CellName	Cell name of the fiducial	string	No	

Section

Section object documents logical separation of checks based on functional areas.

Attribute Name	**Definition**	**Data Type**	**Required**	**Example Value**
Name	User Friendly section Name	string	Yes	Die Size Rules

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Number	Section Number	string	Yes	x.x
SubSections	List Sub sections	array	No	
Rules	List Rules	array	No	

SubSection

Sub Section object documents logical separation of checks based on functional areas.

Attribute Name	**Definition**	**Data Type**	**Required**	**Example Value**
Name	User Friendly Sub Section Name	string	Yes	Die Size
Number	Section Number	string	Yes	x.x
SubSections	List Sub sections	array	No	
Rules	List Rules	array	No	

Rules

Rule object documents the definition, check time i.e., dimension, distance, angle, density values to check and their types. Not all rule parameters are defined in the tables. The relationship between the rule parameters is documented in the rule documentation.

Dimension Rule

Attribute Name	**Definition**	**Data Type**	**Required**	**Example Value**
DisplayName	User Friendly Rule Name	string	Yes	Die Active Size
Description	Rule Description	string	Yes	
Url	Rule Documentation	string	No	
Tolerance	Local/Global Tolerance	string	Yes	
Object	Object on which the rule applies	string	Yes	Outlines.ActiveEdge
MeasureType	Rule type	string	Yes	Dimension
RuleParameters	List of rule parameters to check	Array	Yes	
Name	User friendly rule Parameter Name	String	Yes	Minimum Width of Active Edge

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RuleName	Machine readable rule Parameter Name	String	Yes	ActiveEdgeWidth
Value	Rule Value	String/float/ i nt	Yes	xxxx
Notes	Rule value specific notes	String	Yes	
Check	Expression type Min/max/equals/greater/less etc	String	Yes	Minimum

Ratio Rule

Attribute Name	**Definition**	**Data Type**	**Required**	**Example Value**
DisplayName	User Friendly Rule Name	string	Yes	Die Active Size Aspect Ratio
Description	Rule Description	string	Yes	
Url	Rule Documentation	string	No	
fo	Local/Global Tolerance	string	Yes	
Object	Object on which the rule applies	string	Yes	Outlines.ActiveEdge
MeasureType	Rule type	string	Yes	Ratio
RuleParameters	List of rule parameters to check	Array	Yes	
Name	User friendly rule Parameter Name	String	Yes	Maximum Aspect Ratio for Active Edge (Length/Width)
RuleName	Machine readable rule Parameter Name	String	Yes	EnvelopAspectRatio
Value	Rule Value	String/float/ i nt	Yes	xxxx
Notes	Rule value specific notes	String	Yes	
Check	Expression type Min/max/equals/greater/less etc	String	Yes	Maximum

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Pitch Rule

Attribute Name	Definition	Data Type	Required	Example Value
DisplayName	User Friendly Rule Name	string	Yes	C4 Pad to C4 Pad Minimum and maximum pitch
Description	Rule Description	string	Yes	
Url	Rule Documentation	string	No	
Tolerance	Local/Global Tolerance	string	Yes	
Object	Object on which the rule applies	string	Yes	Pads.C4Pads
MeasureType	Rule type	string	Yes	Pitch
RuleParameters	List of rule parameters to check	Array	Yes	
Name	User friendly rule Parameter Name	String	Yes	Minimum Bump Pitch
RuleName	Machine readable rule Parameter Name	String	Yes	MinPitch
Value	Rule Value	String/float/ i nt	Yes	xxx.xx
Notes	Rule value specific notes	String	Yes	
Check	Expression type Min/max/equals/greater/less etc	String	Yes	Maximum

Distance Rule

Attribute Name	Definition	Data Type	Required	Example Value
DisplayName	User Friendly Rule Name	string	Yes	C4 Pad Center to Active Edge Minimum/Maximum Distance
Description	Rule Description	string	Yes	
Url	Rule Documentation	string	No	
Tolerance	Local/Global Tolerance	string	Yes	
FromObject	Object on which the rule applies	string	Yes	Pads.C4Pads

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ToObject	Object on which the rule applies			Outlines.ActiveEdge
MeasureType	Rule type	string	Yes	Distance
RuleParameters	List of rule parameters to check	Array	Yes	
Name	User friendly rule Parameter Name	String	Yes	Minimum Bump to Active Edge Distance
RuleName	Machine readable rule Parameter Name	String	Yes	BumpCenterToEdgeDistance
Value	Rule Value	String/float/int	Yes	xxxx.x
Notes	Rule value specific notes	String	Yes	
Check	Expression type Min/max/equals/greater/less etc	String	Yes	Minimum

Area Rule

Attribute Name	**Definition**	**Data Type**	**Required**	**Example Value**
DisplayName	User Friendly Rule Name	string	Yes	C4 Pad Pattern to Micro pad pattern airgap Area, size
Description	Rule Description	string	Yes	
Url	Rule Documentation	string	No	
Tolerance	Local/Global Tolerance	string	Yes	
Object	Object on which the rule applies	string	Yes	Pads.C4Pads
MeasureType	Rule type	string	Yes	Area
RuleParameters	List of rule parameters to check	Array	Yes	
Name	User friendly rule Parameter Name	String	Yes	Maximum air gap area between C4bump patter
RuleName	Machine readable rule Parameter Name	String	Yes	AirgapArea

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Value	Rule Value	String/float/ i nt	Yes	xx.xx
Notes	Rule value specific notes	String	Yes	
Check	Expression type Min/max/equals/greater/less etc	String	Yes	Maximum

Density Rule

Attribute Name	**Definition**	**Data Type**	**Required**	**Example Value**
DisplayName	User Friendly Rule Name	string	Yes	Large C4 Pad local density
Description	Rule Description	string	Yes	
Url	Rule Documentation	string	No	
Tolerance	Local/Global Tolerance	string	Yes	
Object	Object on which the rule applies	string	Yes	Pads.C4Pads
ObjectContainer	The Container object for density	string		Outlines.ActiveEdge
MeasureType	Rule type	string	Yes	Density
RuleParameters	List of rule parameters to check	Array	Yes	
Name	User friendly rule Parameter Name	String	Yes	Minimum Local Density
RuleName	Machine readable rule Parameter Name	String	Yes	LocalDensity
Value	Rule Value	String/float/ i nt	Yes	x.xx
Notes	Rule value specific notes	String	Yes	
Check	Expression type Min/max/equals/greater/less etc	String	Yes	Minimum

Count Rule

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Attribute Name	Definition	Data Type	Required	Example Value
DisplayName	User Friendly Rule Name	string	Yes	I fiducial count
Description	Rule Description	string	Yes	
Url	Rule Documentation	string	No	
Tolerance	Local/Global Tolerance	string	Yes	
Object	Object on which the rule applies	string	Yes	Fidutials.IFiducial Outline
MeasureType	Rule type	string	Yes	Count
RuleParameters	List of rule parameters to check	Array	Yes	
Name	User friendly rule Parameter Name	String	Yes	Number of I Fiducials
RuleName	Machine readable rule Parameter Name	String	Yes	fidCount
Value	Rule Value	String/float/int	Yes	1
Notes	Rule value specific notes	String	Yes	
Check	Expression type Min/max/equals/greater/less etc	String	Yes	Equal

Si Interposer Rules

Category	Description	Parameters/Rules	Rule Type	Comment
Dimension constraints	Interposer's dimensions align precisely with the intended specifications to fit within the semiconductor package.	Minimum via diameter Minimum pad/bump size clearance/annular ring	Distance/Dimension	Needs for the rules such the objectives, problem, etc.
		min space		
		min line		
Chip alignment	Accurate alignment of the interposer with other components such as the die, substrate, or package	Placement accuracy Alignment marks/targets Differential expansion rules	Distance/Dimension	

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Layer alignment	Ensuring proper alignment between the different layers of the interposer such as metal layers	TSV to TSV alignment Via to RDL (Redistribution Layer) alignment Via to active area alignment	Distance/Dimension	Define common terminology such as RDL/conductor?
Interconnect	Specifications for the design and layout of interconnects such as traces, vias, microbumps.	bump pitch (min, max / tolerence) TSV pitch TSV size/aspect ratio bump pitch	Distance/Dimension	max ball size, min pitch (with exemption such as corner sand edge of si interposer)
3D stacking		Layer to layer alignment	Distance/Dimension	
General / User Defined Guidelines / Recommendation				
Thermal management	thermal dissipation and management			
Si Integrity	minimal loss, crosstalk, or interference			
Mechanical stress	mechanical stress, package dimension			

XML Schema

adk.xsd

OCP Demo Example

	Glass
# Metal Layer	3
Metal thickness	4um
Dielectric thickness	15um
Dielectric constant	3.3
Minimum Wire W/S	2um/2um
Via size	22um
Bump size	16um

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Die-to-Die spacing	100um
Micro-bump pitch	35um
C4 bump pitch	650um

Die Rules Example

yDie_Example_TOP2_BSB_v1.3.ydie

```
<DieDesignRuleSpec>
 <Header>
  <Process>Glass</Process>
  <Revision>1</Revision>
  <Version>1</Version>
  <Units>um</Units>
 </Header>

 <Sections>
  <Section>
   <Name>Metal Layer</Name>
   <Number>3</Number>
  </Section>
  <Section>
   <Name>Metal thickness</Name>
   <Number>4</Number>
   <Attributes>
    <Attribute>
     <Name>Thickness</Name>
     <Value>4</Value>
     <Units>um</Units>
    </Attribute>
   </Attributes>
  </Section>
  <Section>
   <Name>Dielectric thickness</Name>
   <Number>15</Number>
   <Attributes>
    <Attribute>
     <Name>Thickness</Name>
     <Value>15</Value>
     <Units>um</Units>
    </Attribute>
   </Attributes>
  </Section>
  <Section>
```

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```
  <Name>Dielectric constant</Name>
  <Number>3.3</Number>
  <Attributes>
   <Attribute>
    <Name>Constant</Name>
    <Value>3.3</Value>
   </Attribute>
  </Attributes>
 </Section>
 <Section>
  <Name>Minimum Wire W/S</Name>
  <Number>2</Number>
  <Attributes>
   <Attribute>
    <Name>Width/Spacing</Name>
    <Value>2um/2um</Value>
   </Attribute>
  </Attributes>
 </Section>
 <Section>
  <Name>Via size</Name>
  <Number>22</Number>
  <Attributes>
   <Attribute>
    <Name>Size</Name>
    <Value>22</Value>
    <Units>um</Units>
   </Attribute>
  </Attributes>
 </Section>
 <Section>
  <Name>Bump size</Name>
  <Number>16</Number>
  <Attributes>
   <Attribute>
    <Name>Size</Name>
    <Value>16</Value>
    <Units>um</Units>
   </Attribute>
  </Attributes>
 </Section>
 <Section>
  <Name>Die-to-Die spacing</Name>
  <Number>100</Number>
  <Attributes>
   <Attribute>
    <Name>Spacing</Name>
    <Value>100</Value>
    <Units>um</Units>
```

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```
    </Attribute>
   </Attributes>
  </Section>
  <Section>
   <Name>Micro-bump pitch</Name>
   <Number>35</Number>
   <Attributes>
    <Attribute>
     <Name>Pitch</Name>
     <Value>35</Value>
     <Units>um</Units>
    </Attribute>
   </Attributes>
  </Section>
  <Section>
   <Name>C4 bump pitch</Name>
   <Number>650</Number>
   <Attributes>
    <Attribute>
     <Name>Pitch</Name>
     <Value>650</Value>
     <Units>um</Units>
    </Attribute>
   </Attributes>
  </Section>
 </Sections>
</DieDesignRuleSpec>
```

yDie XML Example

Based on the Intel yDie example data, yDie_Example_TOP2_BSB_v1.3.ydie

```
<?xml version="1.0" encoding="UTF-8"?>
<die_definition>
  <format_version>0.1</format_version>
  <date>Fri Sep 22 08:37:15 2023</date>
  <name>YDIE_TOP2_A0</name>
  <mask_version>A0</mask_version>
  <pkg_type>FC-xGA</pkg_type>
  <process>P1278.2</process>
  <die_owner>
    <name>cjankenb</name>
    <email>christopher.j.ankenbauer@intel.com</email>
  </die_owner>
  <units>um</units>
  <si_design_grid>0.0005</si_design_grid>
```

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```
  <thickness>~</thickness>
  <description>~</description>

  <die_edges>
    <active_edge_geometry>
      <polygon>-2500 -1250 2500 -1250 2500 1250 -2500 1250</polygon>
      <seal_ring>16.2 17.28 16.2 17.28</seal_ring>
      <seal_ring_to_frame_scribe_line>75 65 75 65</seal_ring_to_frame_scribe_line>
      <remnant_scribe>55 45 55 45</remnant_scribe>
      <calculated_active_size>5000 2500</calculated_active_size>
      <calculated_stepping_size>5182.4 2664.56</calculated_stepping_size>
      <calculated_physical_size>5142.4 2624.56</calculated_physical_size>
    </active_edge_geometry>
    <stepping_edge_geometry>
      <rectangle>5182.4 2664.56 0 0</rectangle>
    </stepping_edge_geometry>
  </die_edges>

  <coordinate_space_reference>
    <reference_view>wafer_frontside_up</reference_view>
    <origin_reference>active_edge_center</origin_reference>
    <geo_transform_to_si_design>1 R0 2500 1250</geo_transform_to_si_design>
    <thermal_compensation_factor_applied>false</thermal_compensation_factor_applied>
    <thermal_compensation_factor>1.0</thermal_compensation_factor>
    <rotation_to_wafer_notch_down>R0</rotation_to_wafer_notch_down>
  </coordinate_space_reference>

  <bump_regions>
    <bump_region uid="BSB">
      <wafer_side>back</wafer_side>
      <bump_geometries>
        <bump_geometry uid="bumpR1_15x15um">
          <wafer_side>back</wafer_side>
          <reference_polygons>
            <bump>
              <rectangle>15 15</rectangle>
            </bump>
          </reference_polygons>
        </bump_geometry>
      </bump_geometries>
    </bump_region>
  </bump_regions>

  <backside_bumps_total_count>8010</backside_bumps_total_count>
  <backside_bumps>
    <backside_bump index="0" x="-2216.775" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4963" mechanical="false" probe="true"/>
    <backside_bump index="1" x="-2109.295" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4955" mechanical="false" probe="true"/>
```

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```
    <backside_bump index="2" x="-1518.155" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4976" mechanical="false" probe="true"/>
    <backside_bump index="3" x="-1625.635" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4953" mechanical="false" probe="true"/>
    <backside_bump index="4" x="-2377.995" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4973" mechanical="false" probe="true"/>
    <backside_bump index="5" x="-2270.515" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4952" mechanical="false" probe="true"/>
    <backside_bump index="6" x="-927.015" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4959" mechanical="false" probe="true"/>
    <backside_bump index="7" x="-819.535" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4939" mechanical="false" probe="true"/>
    <backside_bump index="8" x="-1464.415" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4972" mechanical="false" probe="true"/>
    <backside_bump index="9" x="-67.175" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4948" mechanical="false" probe="true"/>
    <backside_bump index="10" x="-1195.715" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4960" mechanical="false" probe="true"/>
    <backside_bump index="11" x="-13.435" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4950" mechanical="false" probe="true"/>
    <backside_bump index="12" x="-2324.255" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4974" mechanical="false" probe="true"/>
    <backside_bump index="13" x="255.265" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4947" mechanical="false" probe="true"/>
    <backside_bump index="14" x="523.965" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4966" mechanical="false" probe="true"/>
    <backside_bump index="15" x="-1679.375" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4951" mechanical="false" probe="true"/>
    <backside_bump index="16" x="-282.135" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4967" mechanical="false" probe="true"/>
    <backside_bump index="17" x="40.305" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4940" mechanical="false" probe="true"/>
    <backside_bump index="18" x="577.705" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4961" mechanical="false" probe="true"/>
    <backside_bump index="19" x="-658.315" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4969" mechanical="false" probe="true"/>
    <backside_bump index="20" x="631.445" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4944" mechanical="false" probe="true"/>
    <backside_bump index="21" x="-1034.495" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4956" mechanical="false" probe="true"/>
    <backside_bump index="22" x="-389.615" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4954" mechanical="false" probe="true"/>
    <backside_bump index="23" x="738.925" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4941" mechanical="false" probe="true"/>
    <backside_bump index="24" x="846.405" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4957" mechanical="false" probe="true"/>
    <backside_bump index="25" x="-497.095" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4949" mechanical="false" probe="true"/>
    <backside_bump index="26" x="-1141.975" y="-1189.695" bump_geometry="bumpR1_15x15um"
```

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```
bump_region="BSB" pad_function="TOPNET_4962" mechanical="false" probe="true"/>
    <backside_bump index="27" x="-980.755" y="-1189.695" bump_geometry="bumpR1_15x15um"
bump_region="BSB" pad_function="TOPNET_4958" mechanical="false" probe="true"/>
    <!-- More bumps go here, up to index 8010 -->
  </backside_bumps>

</die_definition>
```

HRL Example

Layer	Description
Antenna Patch	Glass thickness range, TSV size, spacing and density
Interface 12	micro-bump size, density, stacking allowed?
III-V	Substrate thickness, bump size supported?, bond-pad layer sizes and spacing
Interface 23	micro-bump size, density, stacking allowed
Si RDL	Thickness, via and bump size and density
Interface 34	micro-bump to chiplet, stacking rules?, size, density
Interface 35	interface to PCB, stacking rules, size, density
Chiplet	Thickness, bond-pad and micro-bump size and density, (micro-bump stacking rules may need to take into account chiplet local metal density?)

XML file:

```
<?xml version="1.0" encoding="UTF-8"?>
<die_definition>
  <format_version>0.1</format_version>
  <date>Fri Sep 22 08:37:15 2023</date>
  <name>YDIE_TOP2_A0</name>
  <layers>
    <layer>
      <name>Antenna Patch</name>
      <description>Glass thickness range, TSV size, spacing and density</description>
    </layer>

    <layer>
      <name>Interface 12</name>
      <description>micro-bump size, density, stacking allowed?</description>
      <properties>
        <micro_bump_size>15um</micro_bump_size>
        <density>400 bumps/cm²</density>
        <stacking_allowed>true</stacking_allowed>
      </properties>
    </layer>
```

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```
    <layer>
      <name>III-V</name>
      <description>Substrate thickness, bump size supported, bond-pad layer sizes and
spacing</description>
      <properties>
        <substrate_thickness>200um</substrate_thickness>
        <bump_size>50um</bump_size>
        <bond_pad_layer_size>20um</bond_pad_layer_size>
        <bond_pad_spacing>30um</bond_pad_spacing>
      </properties>
    </layer>

    <layer>
      <name>Interface 23</name>
      <description>micro-bump size, density, stacking allowed?</description>
      <properties>
        <micro_bump_size>10um</micro_bump_size>
        <density>500 bumps/cm²</density>
        <stacking_allowed>false</stacking_allowed>
      </properties>
    </layer>

    <layer>
      <name>Si RDL</name>
      <description>Thickness, via and bump size and density</description>
      <properties>
        <thickness>5um</thickness>
        <via_size>0.5um</via_size>
        <bump_size>8um</bump_size>
        <density>1000 bumps/cm²</density>
      </properties>
    </layer>

    <layer>
      <name>Interface 34</name>
      <description>micro-bump to chiplet, stacking rules, size, density</description>
      <properties>
        <micro_bump_size>12um</micro_bump_size>
        <density>700 bumps/cm²</density>
        <stacking_rules>stacking allowed between chiplet and interface 34</stacking_rules>
      </properties>
    </layer>

    <layer>
      <name>Interface 35</name>
      <description>interface to PCB, stacking rules, size, density</description>
      <properties>
        <micro_bump_size>20um</micro_bump_size>
        <density>600 bumps/cm²</density>
```

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```
        <stacking_rules>stacking allowed between PCB and interface 35</stacking_rules>
      </properties>
    </layer>

    <layer>
      <name>Chiplet</name>
      <description>Thickness, bond-pad and micro-bump size and density, stacking rules</description>
      <properties>
        <thickness>10um</thickness>
        <bond_pad_size>25um</bond_pad_size>
        <micro_bump_size>8um</micro_bump_size>
        <density>1200 bumps/cm²</density>
        <stacking_rules>micro-bump stacking rules dependent on chiplet local metal
density</stacking_rules>
      </properties>
    </layer>
  </layers>
</die_definition>
```

References

1. Github: https://github.com/opencomputeproject/OCP-SVR-ODSA-3DK-PADK

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