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OPEN Compute Project

AMD DC-SCM 1.0 Adapter Reference Designs

Revision 1.0

Hawaii – V Reference Design

Hawaii – H Reference Design

Lanai Root of Trust (RoT) Reference Design

Version 1.0

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2. Compliance with OCP Tenets

AMD is contributing all design collateral related to the Hawaii and Lanai cards, AMD's implementation of DC-SCM 1.0 specification, to the OCP community to enable faster design cycles for the adopters. Reference design collaterals are provided for both the vertical and horizontal form factor implementations of the DC-SCM 1.0 specification. The design files include Schematics, Layout, Bill-of-Materials, 3-D Mechanical files, FPGA source code for Hawaii along with detailed descriptions of our implementation.

2.1. Openness

AMD's reference designs are implemented using industry standard tools. Implementers of DC-SCM1.0 designs can build the boards as is or add customizations of their own to support their motherboard implementations. Availability of full design material enables implementers to adopt the DC-SCM1.0 spec with minimal to no effort. Further, the firmware used for system management functions is based on OpenBMC. OpenBMC is a community developed project and is open for anyone to utilize and contribute.

2.2. Efficiency

Availability of full design collateral and Gerber files enables implementers to add customizations to match their specific motherboard implementations as needed and build the designs with little to no effort significantly improving design turnaround time. Additional modularity is enabled in Hawaii design by implementing Platform RoT subsystem on a mezzanine card (Lanai card) that plugs in to Hawaii. Implementers can design their own security sub-system based on vendor of their choice or come up with specific implementations based on individual needs.

2.3. Impact

Through the donation of a complete DC-SCM 1.0 reference design AMD shows commitment to advancing the idea of DC-SCM and supporting the continued build out of modular systems moving forward.

2.4. Scale

AMD has provided to the OCP community all design data related to Hawaii, with which any entity possessing a reasonable skill set can put together their own version of Hawaii and Lanai. AMD works with OEMs and Datacenters across the globe, helping them to build platforms based on this architecture. AMD, however, does not have the retail sales infrastructure to build and sell direct these adapters and is not in a position to do so.

3. Version Table

Date	Version #	Author	Description
5/26/2022	1.0	Ravi Bingi Greg Sellman Mahesh Prabhu	Initial Release

4. Scope

This document defines the technical details for:

- A DC-SCM 1.0 compliant, vertical form factor (VFF) adapter, **Hawaii-V**
- A DC-SCM 1.0 compliant, horizontal for factor (HFF) adapter, **Hawaii-H**
- A Platform Root of Trust (RoT) module, **Lanai**

5. Overview

Outlined within these reference designs are implementation details for both vertical and horizontal DC-SCM adapters, compliant to the DC-SCM 1.0 Specification (SPEC, DC-SCM, Google, Microsoft).

Also included within these reference designs and donation are details related to a Platform Root of Trust (RoT) Module.

The useful purpose of the adapter(s) is/are to move common server management, security, and control features from a typical processor motherboard architecture onto a smaller common form factor module. These modules contain all the FW states previously housed on a typical processor motherboard. This provides benefits to both the user and developer.
From a Data Center perspective, this enables common management and security to be deployed across a higher percentage of platforms. It also enables deployment of management and security upgrades on platforms within a generation without redesign of more complex components.

A typical DC-SCM design enables the design and deployment of Host Processing Module (HPM) complexes to become a simpler exercise with increased efficiency for time to market deployment. With a standardized DC-SCI pinout and definition, it can be used as a vehicle to drive common boot, monitoring, control, and remote debug for diverse platforms.

6. Rack Compatibility

As these are DC-SCM adapter reference design with use cases only within a larger system or platform, Rack Compatibility is N/A.

7. Physical Specifications

Described within this section are the physical attributes of the DC-SCM adapter.

- Block Diagram(s)
- Form Factor(s)
- Connector, Switch and LED Details
- Dimensions
- PCB Stackup

7.1 Block Diagrams

Shown below are high level block diagrams for both the DC-SCM and Platform RoT Module

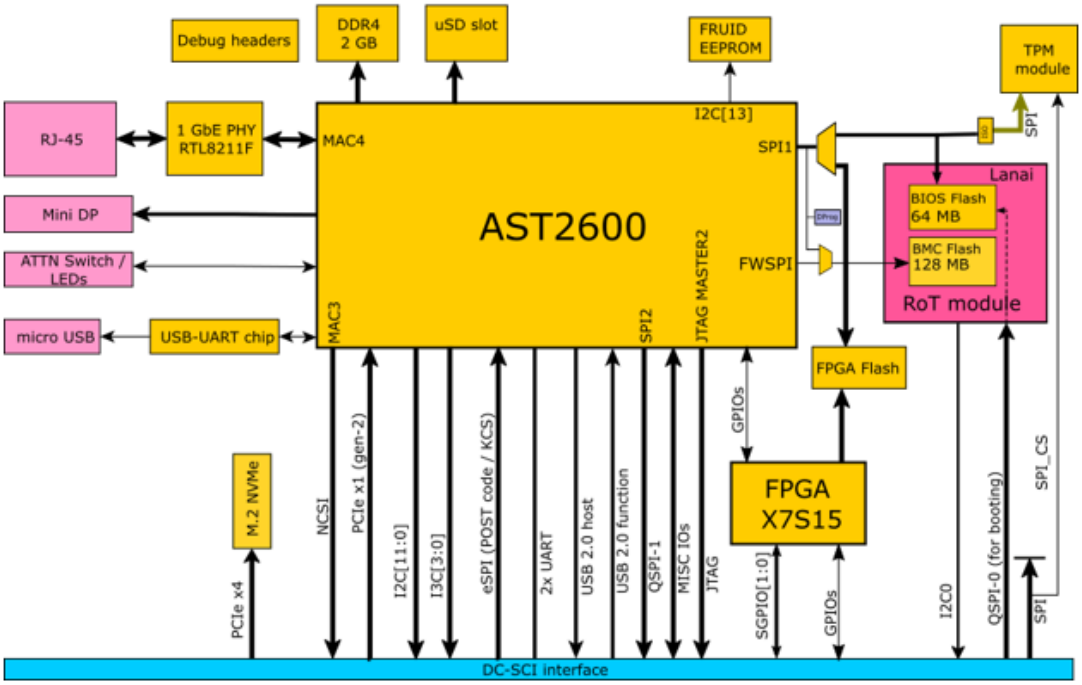


Figure 1: Hawaii DC-SCM 1.0, Block Diagram

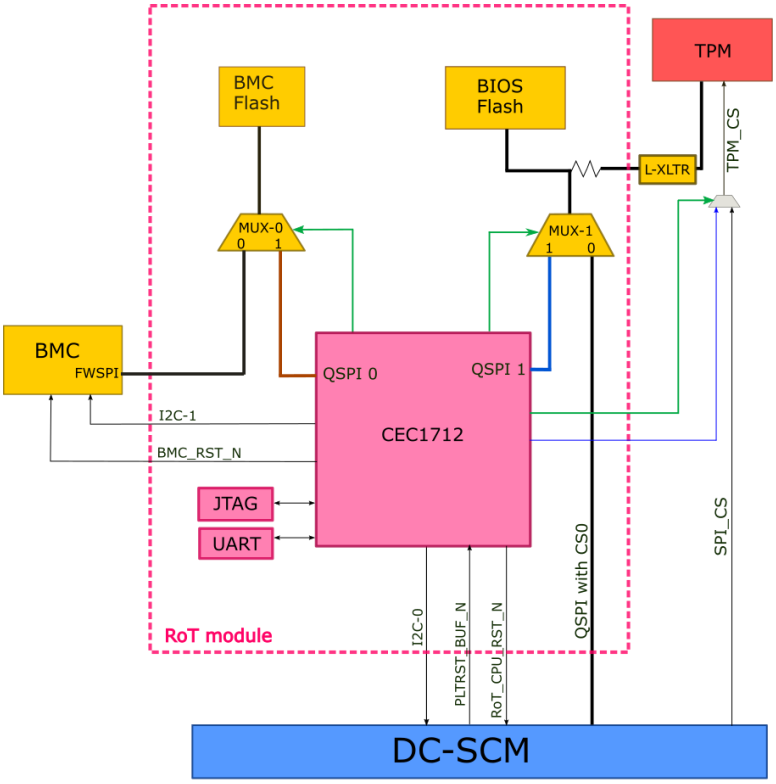


Figure 2: Lanai Platform RoT Module, Block Diagram

7.2 Form Factors

This DC-SCM 1.0 contribution includes both Vertical (VFF Option 1) and Horizontal form factors as follows.

The Hawaii-V and Hawaii-H have almost identical schematics barring the differences listed in table below.

Feature	**Hawaii-V**	**Hawaii-H**
Optional M.2 connector	Yes	No
VGA header	No	Yes
Debug / test signals	Quantity and access via headers and resistors is different between two form-factors.	

Hawaii-V, vertical form factor DC-SCM 1.0.

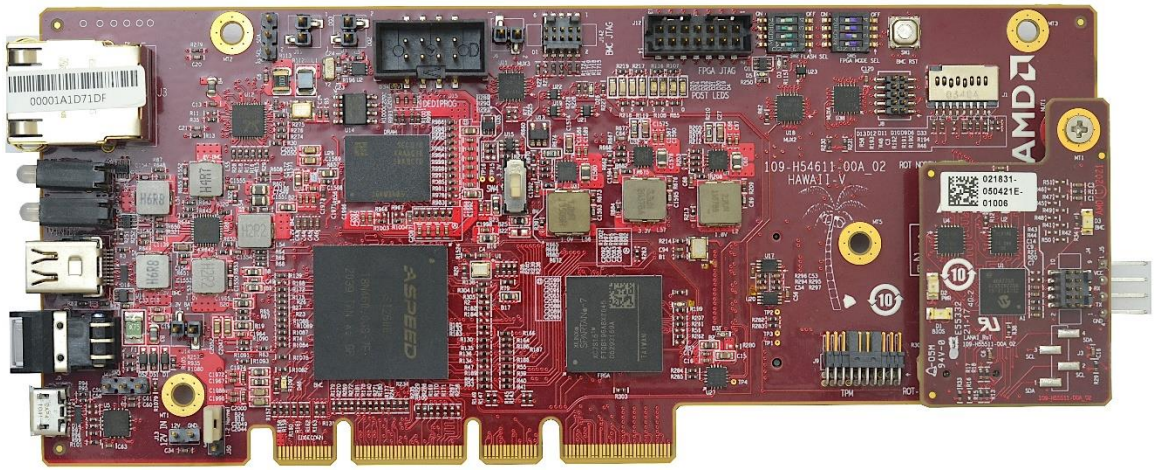


Figure 3: Hawaii-V, Vertical DC-SCM 1.0

Hawaii-H, horizontal form factor DC-SCM 1.0.

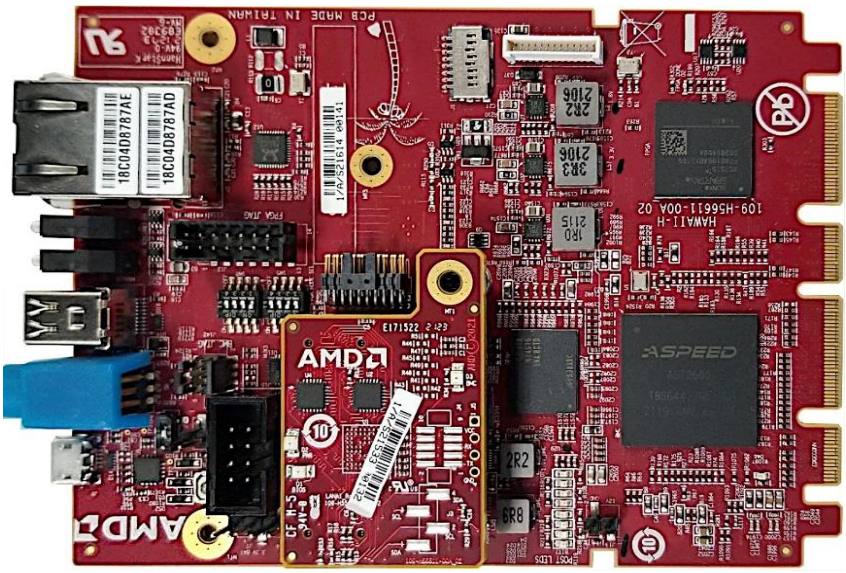


Figure 4: Hawaii-H, Horizontal DC-SCM 1.0

The Lanai Platform Root of Trust (RoT) module is shown below in Figure 5.

Figure 5: Lanai, Platform Root of Trust (RoT) Module

7.3 Connector, Switch and LED Details

Shown below are the location and description of key connectors, switches and LEDs on the DC-SCM(s).

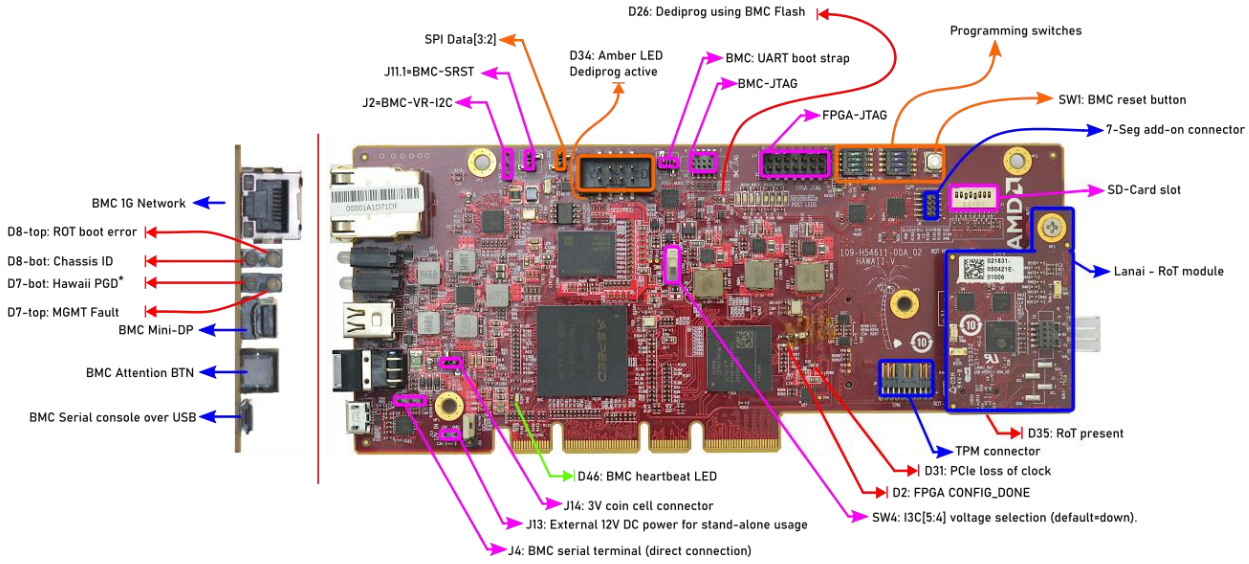


Figure 6: Hawaii-V, Connector, Switch & LED Detail

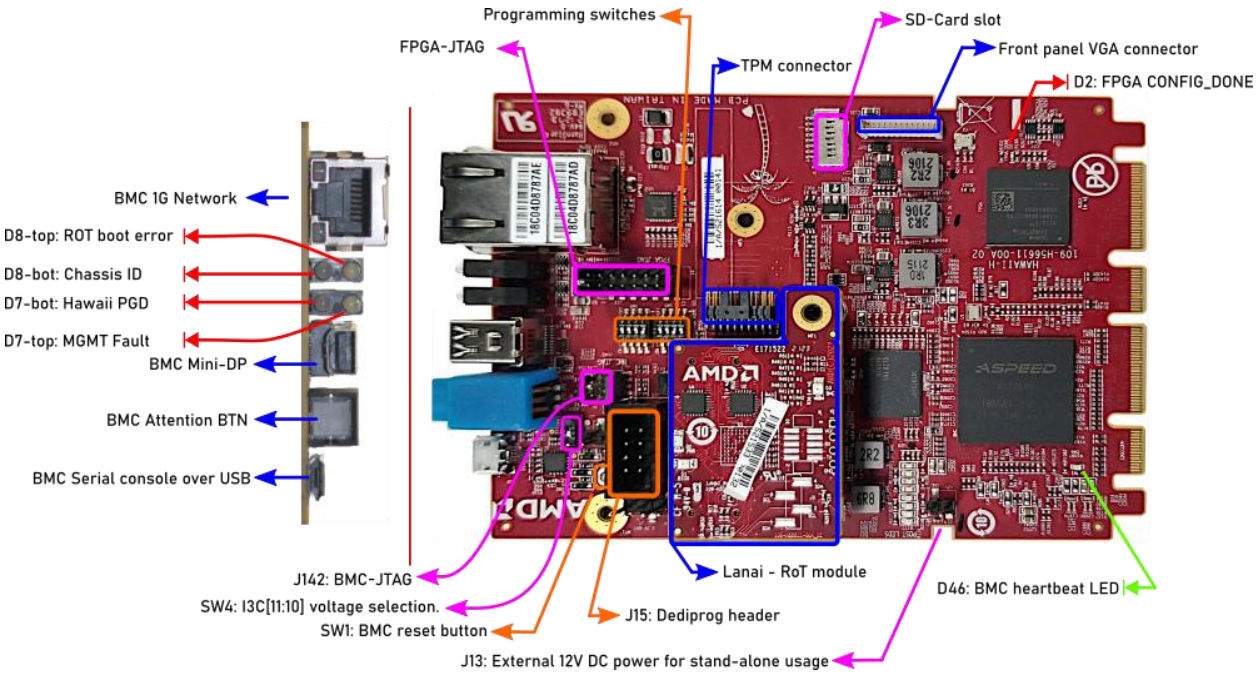


Figure 7: Hawaii-H, Connector, Switch & LED Detail

7.4 Dimensions

Both the horizontal and vertical DC-SCM implementations are aligned with the DC-SCM 1.0 specification with two notable exceptions.

1. The optional M.2 module on the Hawaii-V vertical form factor (VFF) adapter exceeds the allowable bottom side z-height.
2. Optional debug headers may also exceed allowable z-heights and are recommended to be removed/NoPOP prior to production.

See DC-SCM 1.0 Specification, Section 2, for additional information related to adapter dimensions.

7.5 PCB Stack-ups

7.5.1 Hawaii DC-SCM Stackup

Figure 8 below shows the 14-layer stackup, line widths and spacings used in the development of the Hawaii DC-SCM.

Vias	Layer	Type	Material	Thickness mm [mils] (1)	10Ghz Dk (2)	Ref Plane
		DIELECTRIC	SOLDERMASK	0.0127 [0.50]	4.00	
	L1	CONDUCTOR	1/2 OZ COPPER + PLATE	0.0460 [1.81]		L2
		DIELECTRIC	PREPREG IT-170GRA1 1067	0.0685 [2.70]	3.03	
	L2	PLANE	1 OZ COPPER	0.0305 [1.20]		
		DIELECTRIC	IT-170GRA1 CORE 1086	0.0762 [3.00]	3.36	
	L3	CONDUCTOR	1/2 OZ COPPER	0.0152 [0.60]		L2 & L4
		DIELECTRIC	PREPREG IT-170GRA1	0.1450 [5.71]	3.29	
	L4	PLANE	1 OZ COPPER	0.0305 [1.20]		
		DIELECTRIC	IT-170GRA1 CORE 1086	0.0762 [3.00]	3.36	
	L5	CONDUCTOR	1/2 OZ COPPER	0.0152 [0.60]		L4 & L6
		DIELECTRIC	PREPREG IT-170GRA1	0.1450 [5.71]	3.29	
	L6	PLANE	1/2 OZ COPPER	0.0152 [0.60]		
		DIELECTRIC	IT-170GRA1 CORE 106	0.0508 [2.00]	3.12	
	L7	PLANE	1 OZ COPPER	0.0305 [1.20]		
		DIELECTRIC	PREPREG IT-170GRA1 1078	0.0762 [3.00]	3.16	
	L8	PLANE	1 OZ COPPER	0.0305 [1.20]		
		DIELECTRIC	IT-170GRA1 CORE 106	0.0508 [2.00]	3.12	
	L9	PLANE	1/2 OZ COPPER	0.0152 [0.60]		
		DIELECTRIC	PREPREG IT-170GRA1	0.1450 [5.71]	3.29	
	L10	CONDUCTOR	1/2 OZ COPPER	0.0152 [0.60]		L9 & L11
		DIELECTRIC	IT-170GRA1 CORE 1086	0.0762 [3.00]	3.36	
	L11	PLANE	1 OZ COPPER	0.0305 [1.20]		
		DIELECTRIC	PREPREG IT-170GRA1	0.1450 [5.71]	3.29	
	L12	CONDUCTOR	1/2 OZ COPPER	0.0152 [0.60]		L11 & L13
		DIELECTRIC	IT-170GRA1 CORE 1086	0.0762 [3.00]	3.36	
	L13	PLANE	1 OZ COPPER	0.0305 [1.20]		
		DIELECTRIC	PREPREG IT-170GRA1 1067	0.0685 [2.70]	3.03	
	L14	CONDUCTOR	1/2 OZ COPPER + PLATE	0.0460 [1.81]		L13
		DIELECTRIC	SOLDERMASK	0.0127 [0.50]	4.00	
			Thickness Over Copper (4)	1.5658 [61.65]		
			Thickness Over Soldermask (4)	1.5912 [62.65]		

Figure 8: Hawaii DC-SCM 14-layer Stackup

7.5.2 Lanai Platform RoT Stackup

Figure 9 below shows the 6-layer stackup, line widths and spacings used in the development of the Lanai Platform RoT module.

Vias	Layer	Type	Material	Thickness mm [mils] (1)
		DIELECTRIC	SOLDERMASK	0.0127 [0.50]
	L1	CONDUCTOR	1/2 OZ COPPER + PLATE	0.0460 [1.81]
		DIELECTRIC	1080 PREPREG	0.0686 [2.70]
	L2	PLANE	1 OZ COPPER	0.0305 [1.20]
		DIELECTRIC	CORE 1080	0.0762 [3.00]
	L3	CONDUCTOR	1/2 OZ COPPER	0.0152 [0.60]
		DIELECTRIC	PREPREG	1.1016 [43.37]
	L4	CONDUCTOR	1/2 OZ COPPER	0.0152 [0.60]
		DIELECTRIC	CORE 1080	0.0762 [3.00]
	L5	PLANE	1 OZ COPPER	0.0305 [1.20]
		DIELECTRIC	1080 PREPREG	0.0686 [2.70]
	L6	CONDUCTOR	1/2 OZ COPPER + PLATE	0.0460 [1.81]
		DIELECTRIC	SOLDERMASK	0.0127 [0.50]
			Thickness Over Copper (4)	1.5746 [61.99]
			Thickness Over Soldermask (4)	1.6000 [62.99]

Figure 9: Lanai Platform RoT Module 6-layer Stackup

8. Thermal Design Requirements

Thermal design requirements are as follows.

8.1 Operating Environment

- Ambient Temperature: 5℃ to 35℃ (45℉ to 95℉)
- Relative Humidity: 20% to 80% (non-condensing)

8.2 Cooling Considerations

- Passively cooled adapter with no expectation of a need for a dedicated heatsink or fan for the adapter(s)
- Airflow circulation within a standard rack chassis is expected to be sufficient for keeping the card within operating temperature.

9. I/O System

The following subsections detail the I/O interfaces available on both the Hawaii-V and Hawaii-H DC-SCM adapters.

9.1 DC-SCI Interface

As DC-SCM 1.0 conforming adapters, both the Hawaii-V and Hawaii-H follow the DC-SCI interface specification as outlined in the OCP DC-SCM 1.0 specification. The only notable deviation is that the Hawaii-H adapter does not support or make provision for the PCIe x4 connection between the main planar and DC-SCM. DC-SCI interface pinouts for both adapters are shown below.

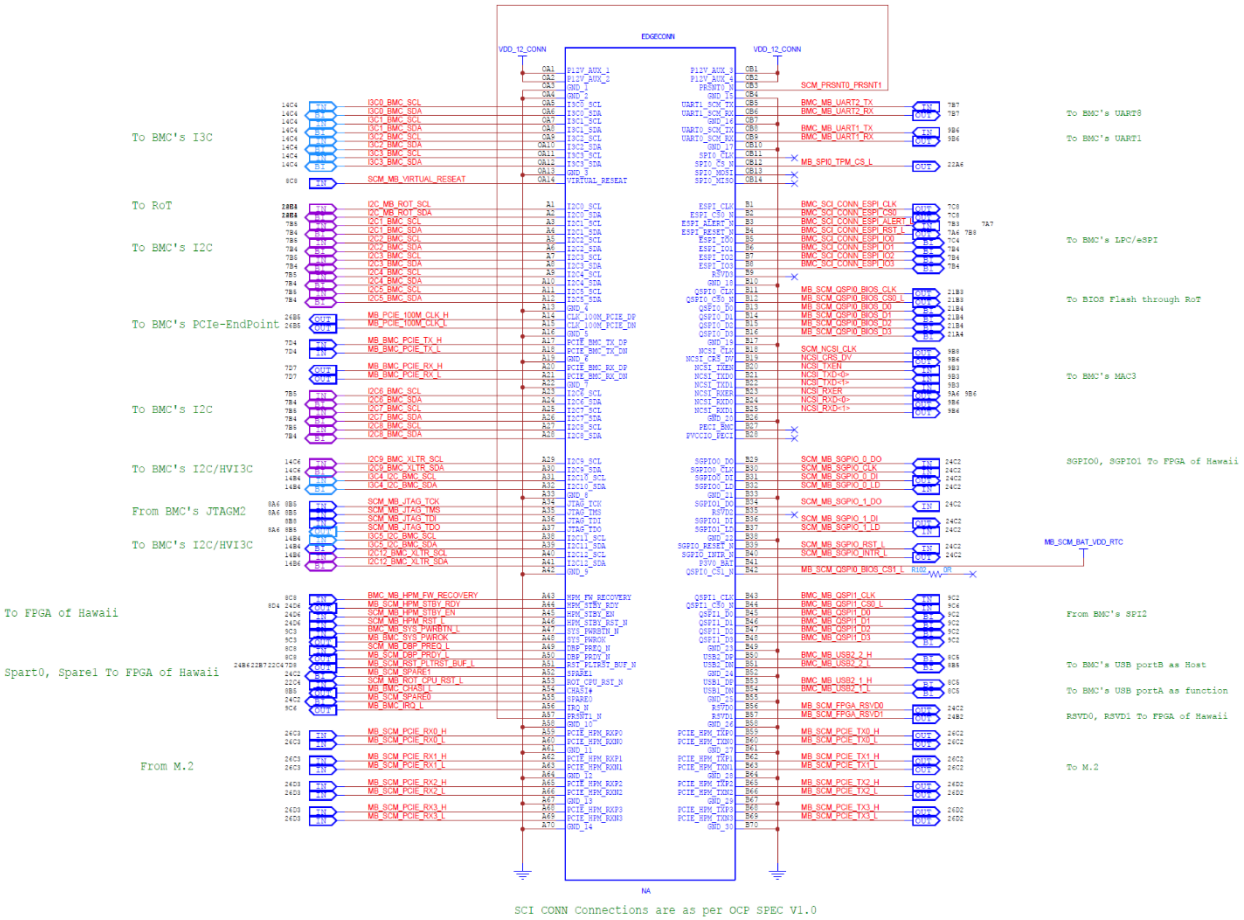


Figure 10: Hawaii-V, DC-SCI Interface Connector

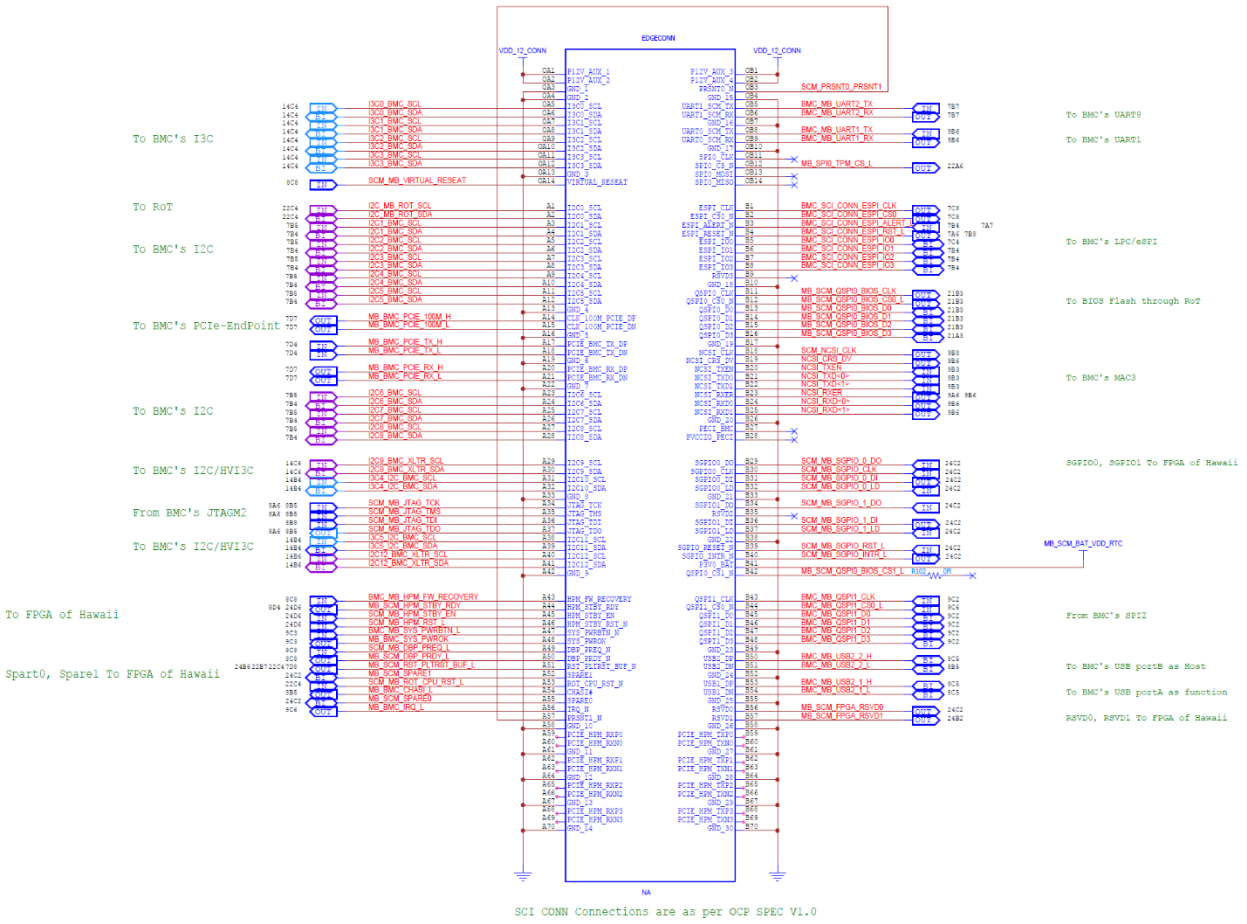


Figure 11: Hawaii-H, DC-SCI Interface Connector (No x4 PCIe)

9.2 I/O Faceplate

From an I/O faceplate perspective, both the Hawaii-V and Hawaii-H are identical. As shown below in Figure 12, both adapters provide the following I/O as part of the faceplate.

- 1x BMC 1GbT network interface to the ASpeed AST-2600 BMC
  - Realtek RTL8211F PHY
- 1x Mini DisplayPort (DP) for direct access to platform video
- 1x micro-USB connector for serial console access to the BMC
- 1x BMC Attention button / LED
- 4x LEDs for:
  - Root of Trust Boot Error (Red)
  - Chassis Identification (Green)

- Hawaii Power Good (Green)
- Management Fault (Red)

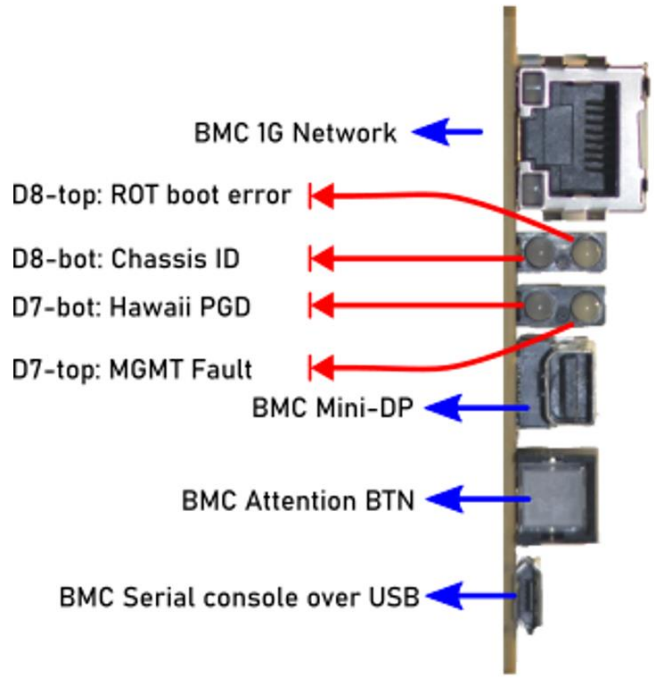


Figure 12: Hawaii DC-SCM I/O Faceplate

9.3 Additional I/O Definition

Beyond the base DC-SCI connections and I/O provided on the faceplate, both the Hawaii-V and Hawaii-H adapters include several additional I/O, be it headers/connectors, switches or LEDs. Each adapters additional I/O is detailed below.

9.3.1 Hawaii-V Additional I/O

ARM debug header

The debug header J142 provides a means to debug the firmware running on AST2600 if needed.

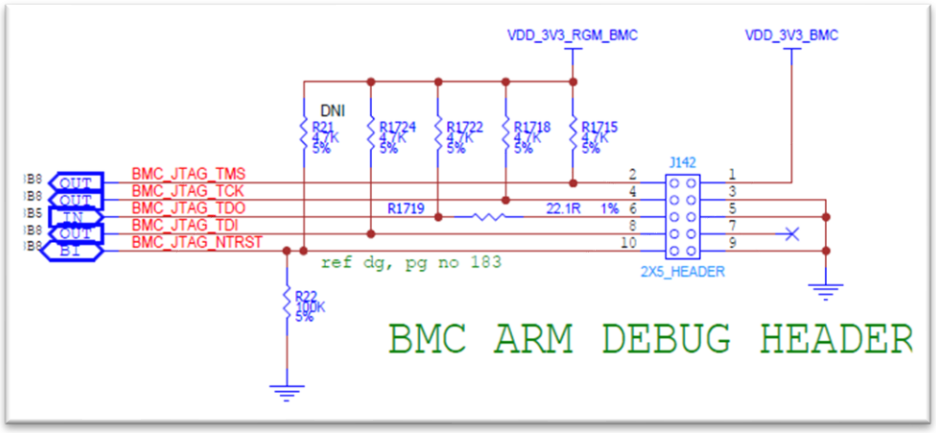


Figure 13: Hawaii-V; BMC ARM Debug Header, J142

RTC battery header

The RTC voltage rail of BMC chip can be configured to take supply from either the DC-SCI interface or from a coin-cell that can be connected to J14.

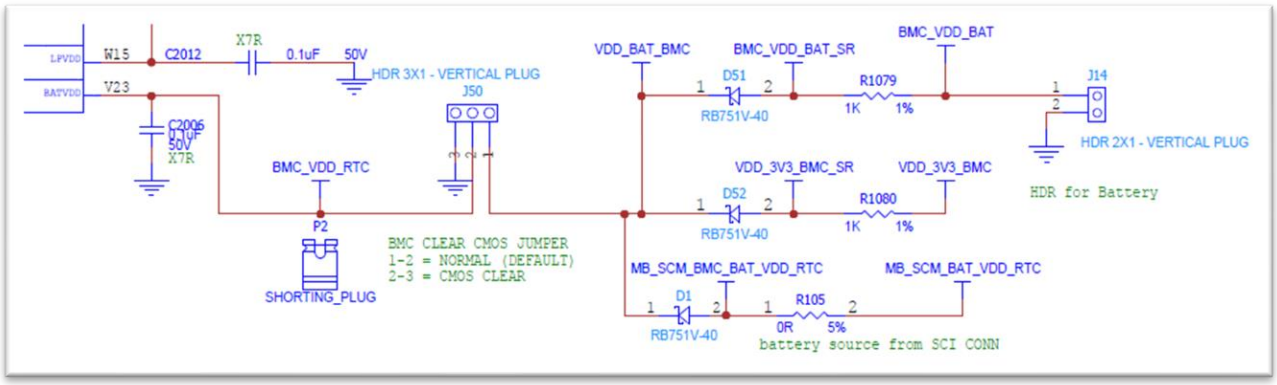


Figure 14: Hawaii-V; RTC battery connector, J14

Voltage set switch for I2C[11:10]

The four DC-SCI I2C ports I2C[12:9] operate at 3.3V as per spec by default.

Hawaii has a provision to configure I2C11 and I2C10 as I3C. Further, in I3C mode, users can set the operating voltage level of the ports I2C[11:10] to 1.8 using the SW4.

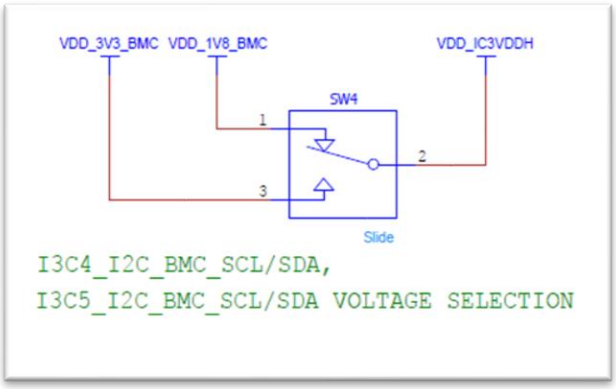


Figure 15: Hawaii-V; Voltage set switch for I2C[11:10], SW4

DediProg programming header J15

A single DediProg header J15 can be used to program the three flash devices on Hawaii (FPGA flash located on Hawaii, BIOS and BMC flash located on Lanai).

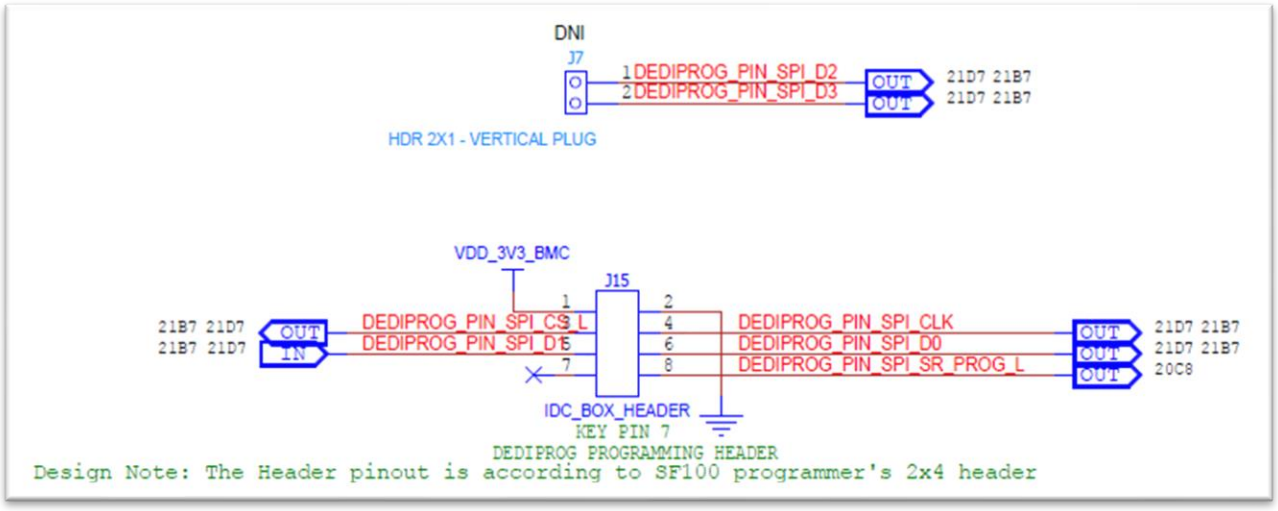


Figure 16: Hawaii-V; Dediprog Programming Header, J15

The switches on SW2 allow routing of signals on the single DediProg header to any of the three flash devices as per the settings in picture Figure 17 below.

```
BMC Flash
Program using Dediprog : SW2.1 = OFF, SW2.3 = ON
Read from BMC (Default): SW2.1 = OFF, SW2.3 = OFF

BIOS Flash
Program using Dediprog : SW2.1 = ON, SW2.2=ON, SW2.3 = OFF
Program using BMC      : SW2.1 = ON, SW2.2=ON, SW2.3 = OFF
Read from Motherboard  : SW2.1 = OFF, SW2.2=OFF, SW2.3 = OFF

FPGA Flash
Program using Dediprog : SW2.1 = ON, SW2.2=OFF, SW2.3 = OFF
Program using BMC      : SW2.1 = ON, SW2.2=OFF, SW2.3 = OFF
Read from FPGA         : SW2.1 = OFF, SW2.2=OFF , SW2.3 = X
```

Figure 17: Hawaii-V; Switch settings for DediProg based programming

Furthermore, all the flash devices could be programmed using BMC. When using BMC to program the devices, SW2 settings do not apply. The DediProg programming header, if inserted in J15 and active, will have precedence over BMC.

Pluggable TPM header

The TPM header J9 allows capability to support various dTPM module vendors.

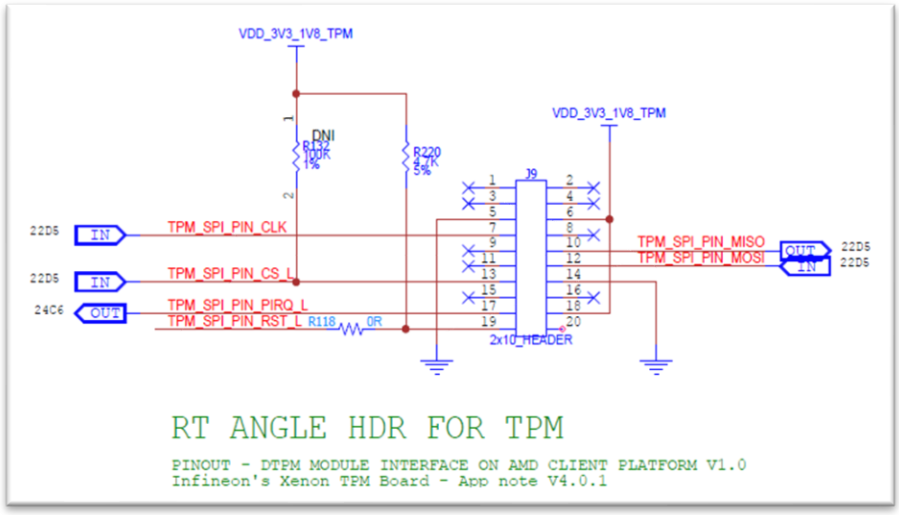


Figure 18: Hawaii-V; Pluggable TPM Header, J9

Platform Root-of-Trust headers

The PRoT module Lanai connects to Hawaii over two connectors J10 & J16. The PRoT houses the BMC and BIOS flash chips along with a controller that can be programmed for enabling platform security functions. Since the BIOS and BMC flash chips are present on Lanai card, it is mandatory to have the Lanai card installed on Hawaii.

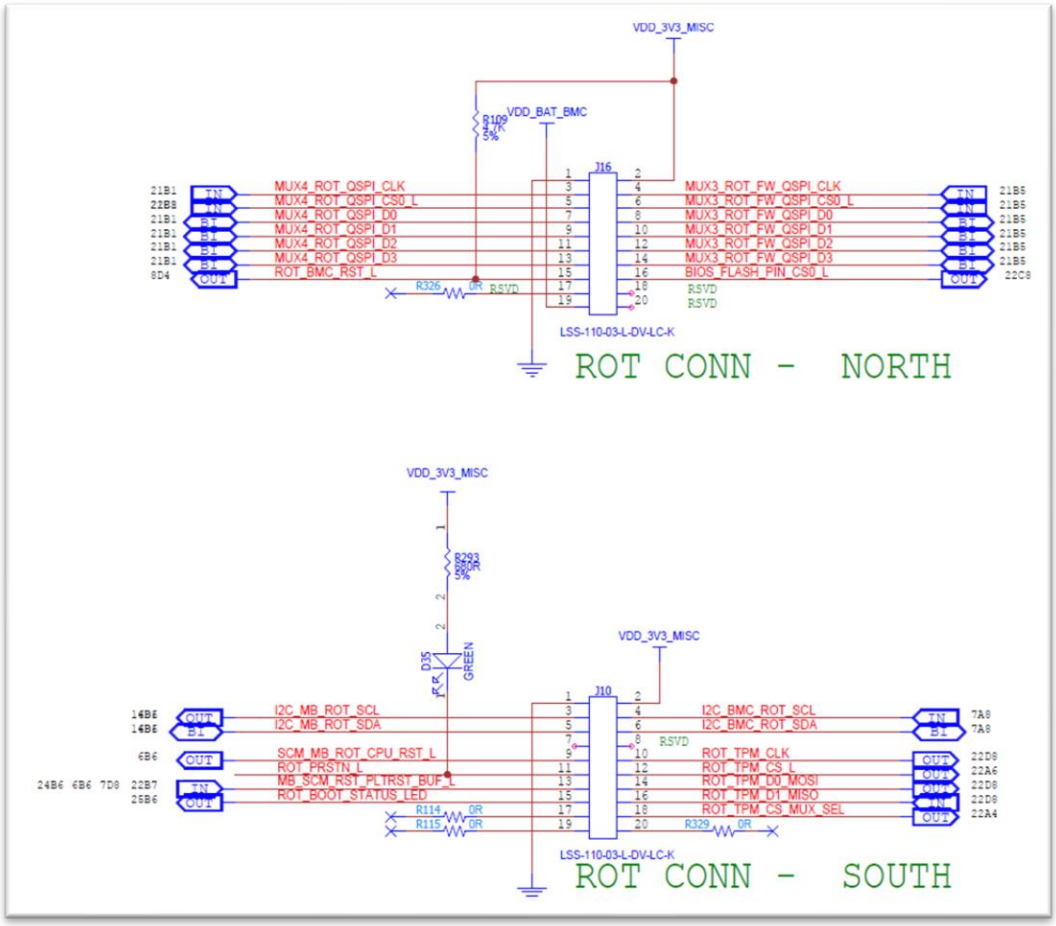


Figure 19: Hawaii-V; Platform Root of Trust Headers (Lanai Platform RoT), J10, J16

FPGA debug header

The J12 is the FPGA JTAG header and accepts a Xilinx Platform Cable for development and debug of FPGA firmware.

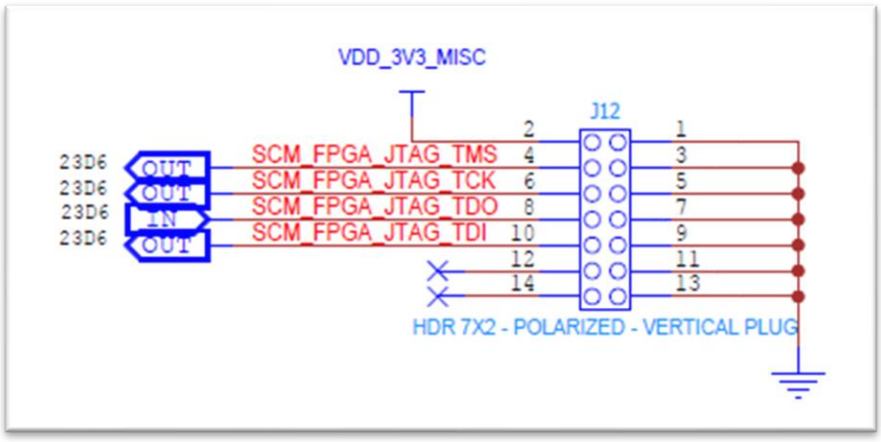


Figure 20: Hawaii-V; FPGA Debug Header, J12

M.2 connector header

The optional M.2 connector is present only on Hawaii-V and is located on bottom side of the PCB. This connector supports 2242 form-factor M.2 drive and can be No-Populated by default. When this optional connector is installed, the Hawaii card will exceed the back-side height keep-out requirement.

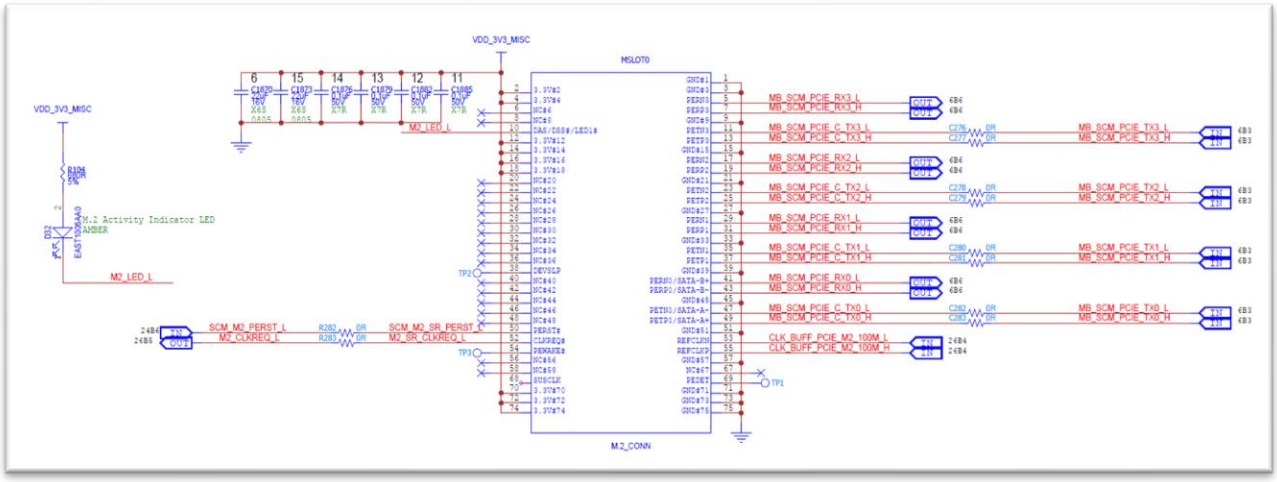


Figure 21: Hawaii-V; M.2 Connector, MSlot0

9.3.2 Hawaii-H Additional I/O

ARM debug header

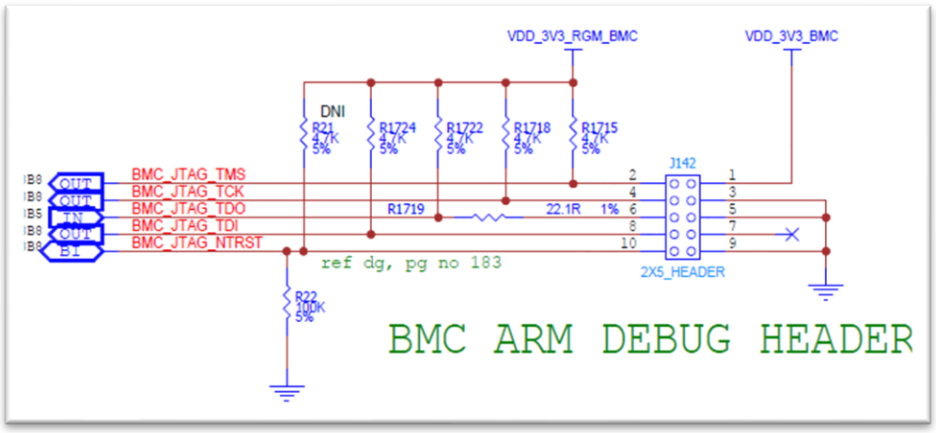


Figure 22: Hawaii-H; BMC ARM Debug Header, J142

RTC battery header

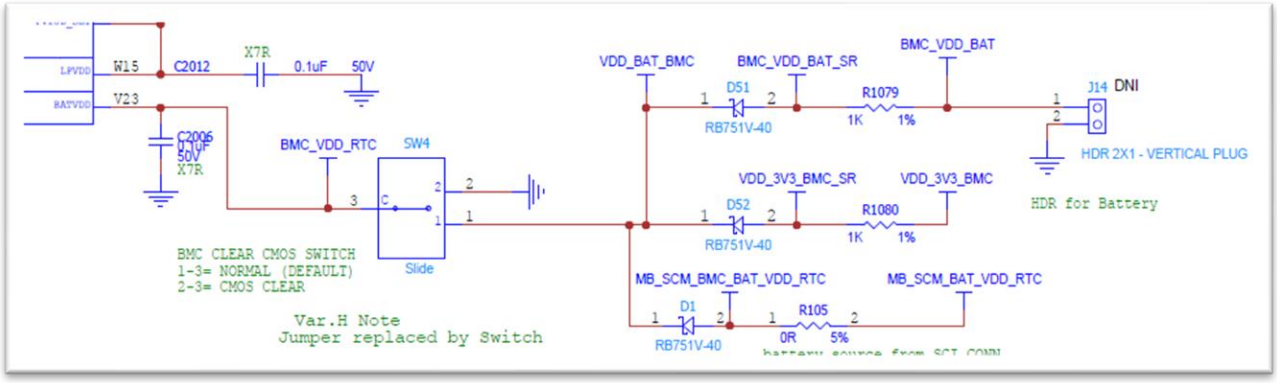


Figure 23: Hawaii-H; BMC Clear CMOS Switch, SW4

VGA header

The VGA header on Hawaii-H is provisioned to connect to a front panel VGA connector on rack form-factor platforms in which the DC-SCM card is located on the rear IO panel

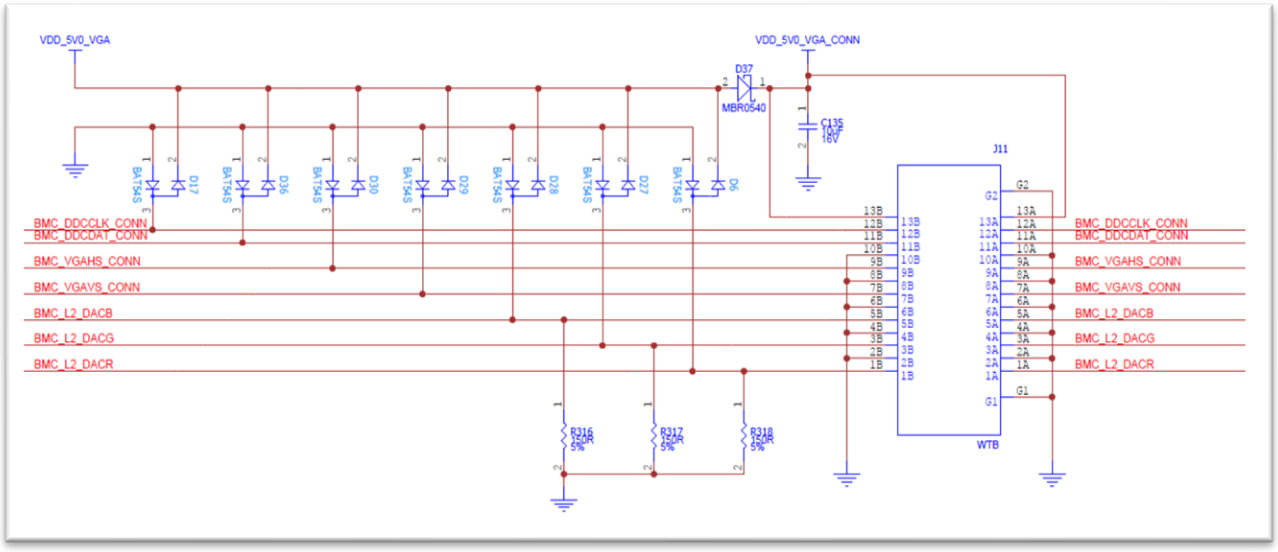


Figure 24: Hawaii-H; VGA Header, J11

DediProg programming header J15

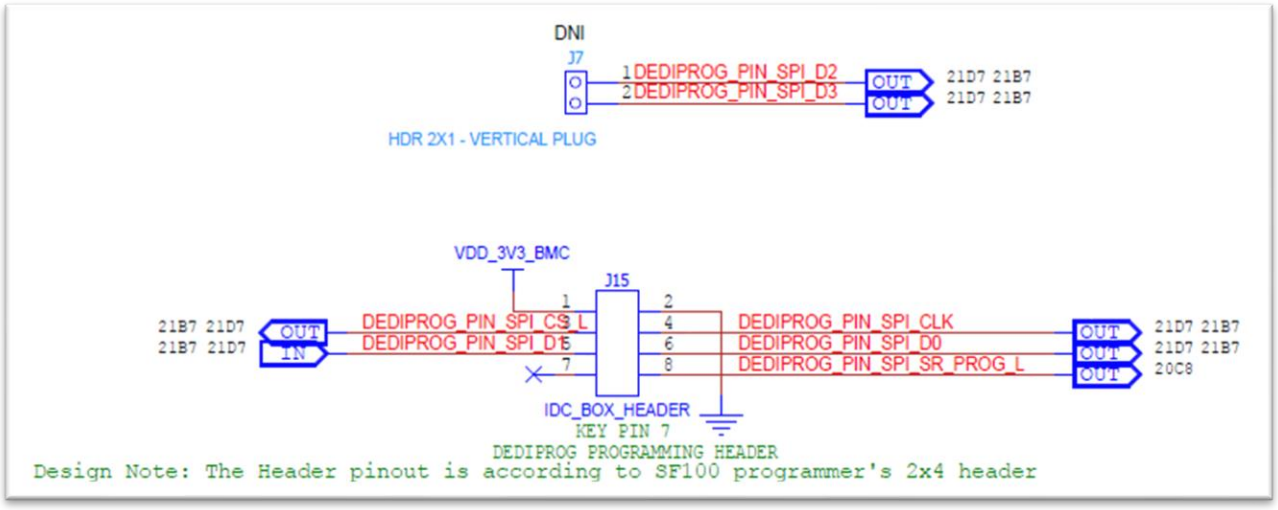


Figure 25: Hawaii-H; Dediprog Programming Header, J15

Platform Root-of-Trust headers

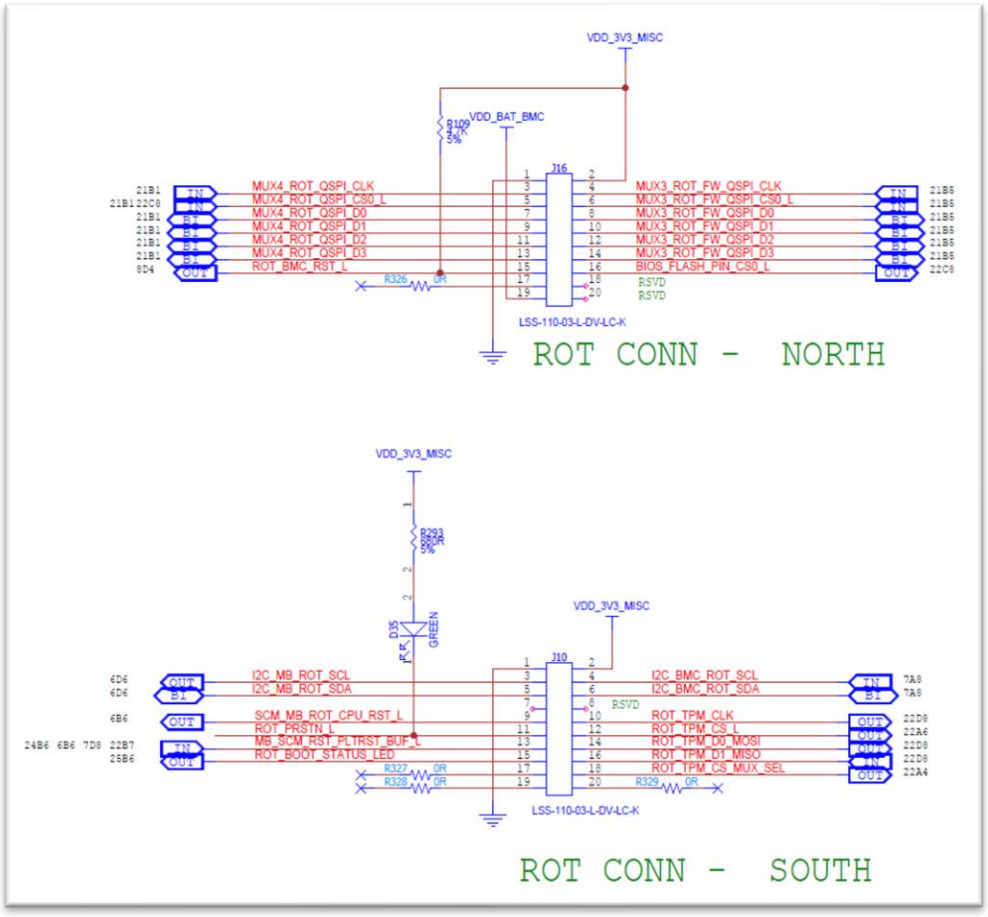


Figure 26: Hawaii-H; Platform Root of Trust Headers (Lanai Platform RoT), J10, J16

Pluggable TPM header

The TPM header J9 allows capability to support various dTPM module vendors.

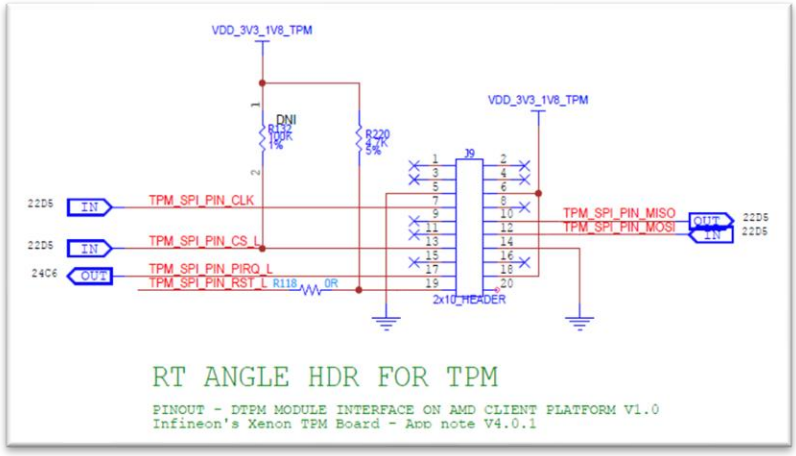


Figure 27: Hawaii-H; Pluggable TPM Header, J9

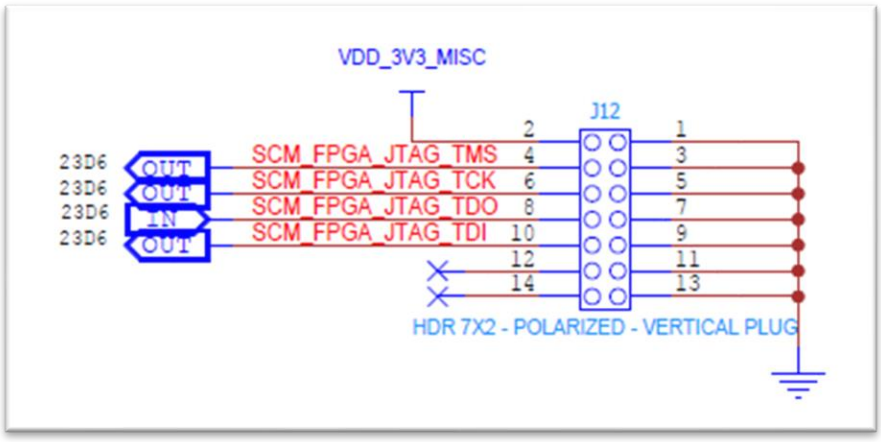


Figure 28: Hawaii-H; FPGA Debug Header, J12

10. Rear Side Power, I/O, Expansion Board and Midplane Subsystems

N/A for these adapter contributions. Adapter power details are further described in Section 12.

11. Mechanical

Key mechanical features of both the Hawaii-V and Hawaii-H DC-SCM 1.0 adapters include:

- 14-layer stackups built initially with IT170 PCB material, Hawaii-V & Hawaii-H
- 6-layer stackup, Lanai Platform RoT
- Vertical, VFF (Hawaii-V) and Horizontal, HFF (Hawaii-H) form factors
- Board outlines and PCB thickness aligned with the DC-SCM 1.0 specification
- Card edge fingers plug compliant with an SFF-TA-1002 4C+ card edge connector.

Refer to DC-SCM 1.0 specification for additional details regarding physical form factor requirements.

12. Onboard Power System

In accordance with the base DC-SCM 1.0 specification both the horizontal and vertical form factor DC-SCM adapters accept 4x pins of 12V_Aux (P12V_AUX) as their input voltage along with 1x pin for 3V battery (P3V0_BAT).

Table 1: Hawaii DC-SCM Input Voltage

	Minimum	Nominal	Maximum
Input Voltage	10V DC	12.3V DC	14V DC
Input Power	N/A	N/A	28W
Inrush Rise Time	5ms	N/A	200ms
*Input Current	N/A	N/A	2.8A

*Input current is based on 1A per pin rating, derated at 70%. Total of 4x power pins on the DC-SCI.

Table 2: Hawaii DC-SCM Battery Voltage

Signal Name	I/O	Voltage (V)	Description
P3V0_BAT	I	3.0	- 3.0V from coin cell battery located on the HPM. - DC-SCM ensures that drain on this rail is less than 1uA.

From there all other adapter voltages are derived and sequenced as shown below in Figures 41 & 42.

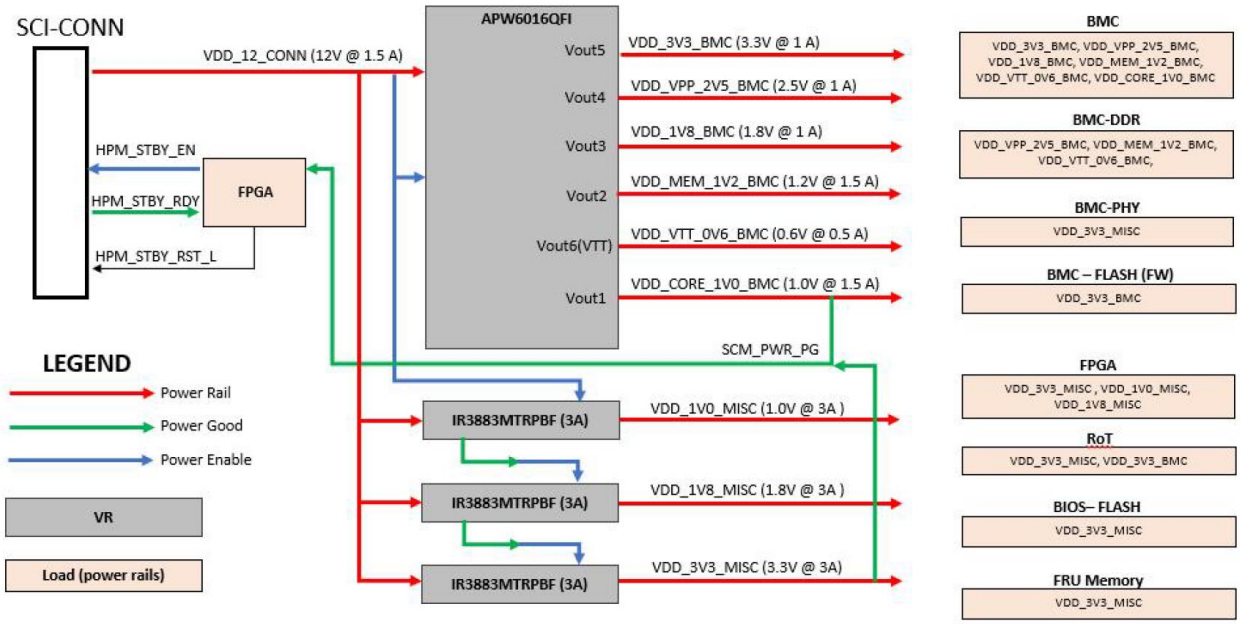
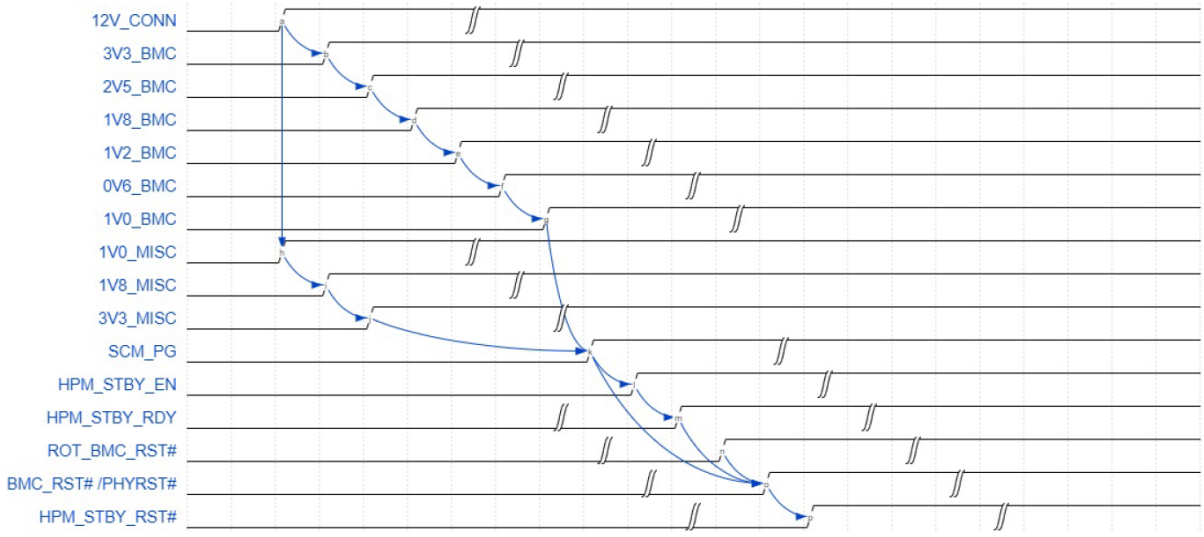


Figure 29: Hawaii DC-SCM Adapter Voltage Regulators



Note: not-to-scale

Figure 30: Hawaii DC-SCM Adapter Power Sequence

13. Environmental Regulations/Environmental Requirements

As this is a DC-SCM adapter with use cases only within a larger system or platform, Environmental Regulations and Requirements are N/A and assumed to be completed as part of a larger, overall platform qualification.

That said, circuitry has been provided on external facing ports, switches and LEDs in support of EMC/EMI compliance and ESD resistance.

14. Prescribed Materials

N/A

15. Software Support (recommended)

N/A

16. System Firmware

BMC firmware:

The BMC chip AST2600 runs OpenBMC, a version of Linux.

A link to OpenBMC is provided here: https://github.com/openbmc/openbmc

FPGA firmware:

The Spartan-7 FPGA implements the SGPIO master and provides SGPIO serialization-deserialization function.

The FPGA binaries are generated using Xilinx Vivado build tool (version 2020 was used for this project).

Firmware upgrade is done either using Dediprog DP-100 programming tool or through BMC interface.

SGPIO interface functions:

The SGPIO interface on Hawaii provides 32x general purpose outputs and 32x general purpose inputs.

The 32 outputs are placed across two 16-bit registers with address 0x10 and 0x18.

The 32 inputs are placed across two 16-bit registers with address 0x20 and 0x28.

The table below provides additional detail for each of the signals.

Table 3: FPGA GPIO Definition

Sl No	FPGA Pin	BMC Pin	Signal name	Direction (W.R.T to BMC)	SGPIO Register Address	Register Bit offset
1	H4	A18	HPM_BMC_GPIOH0	OUT	0x10	0
2	L5	A17	HPM_BMC_GPIOH3	OUT	0x10	1
3	M11	C15	HPM_BMC_GPIOL4	OUT	0x10	2
4	M12	F15	HPM_BMC_GPIOL5	OUT	0x10	3
5	G1	M26	HPM_BMC_GPION7	OUT	0x10	4
6	P13	AC15	HPM_BMC_GPIOV3	OUT	0x10	5
7	H11	AE14	HPM_BMC_GPIOV5	OUT	0x10	6
8	J12	AD15	HPM_BMC_GPIOV6	OUT	0x10	7
9	J13	AF15	HPM_BMC_GPIOV7	OUT	0x10	8
10	G4	K26	HPM_BMC_GPIOA4	OUT	0x10	9
11	F4	L24	HPM_BMC_GPIOA5	OUT	0x10	10
12	D12	AA12	HPM_BMC_GPIOY3	OUT	0x10	11
13			UNUSED_OUT1_1	OUT	0x10	12
14			UNUSED_OUT1_2	OUT	0x10	13
15			DEBUG1_1	OUT	0x10	14
16			DEBUG1_2	OUT	0x10	15
17	M4	B18	HPM_BMC_GPIOH1	OUT	0x18	0
18	P5	C18	HPM_BMC_GPIOH2	OUT	0x18	1
19	L12	D14	HPM_BMC_GPIOM0	OUT	0x18	2
20	H12	B13	HPM_BMC_GPIOM1	OUT	0x18	3
21	H14	A12	HPM_BMC_GPIOM2	OUT	0x18	4
22	A4	AD26	HPM_BMC_GPIOO0	OUT	0x18	5
23	A3	AD22	HPM_BMC_GPIOO1	OUT	0x18	6
24	B3	AD23	HPM_BMC_GPIOO2	OUT	0x18	7
25	A2	AD24	HPM_BMC_GPIOO3	OUT	0x18	8
26	C3	AD25	HPM_BMC_GPIOO4	OUT	0x18	9
27	B5	AC22	HPM_BMC_GPIOO5	OUT	0x18	10
28	G14	W24	HPM_BMC_GPIOP1	OUT	0x18	11

Sl No	FPGA Pin	BMC Pin	Signal name	Direction (W.R.T to BMC)	SGPIO Register Address	Register Bit offset
29	F13	AA24	HPM_BMC_GPIOP3	OUT	0x18	12
30	D14	AB23	HPM_BMC_GPIOP5	OUT	0x18	13
31	D4	D21	HPM_BMC_GPIOG6	OUT	0x18	14
32			UNUSED_OUT0_1	OUT	0x18	15
33	M13	E14	HPM_BMC_GPIOM3	IN	0x20	0
34	H13	B12	HPM_BMC_GPIOM4	IN	0x20	1
35	F14	C12	HPM_BMC_GPIOM5	IN	0x20	2
36	E2	AB26	HPM_BMC_GPIOQ3	IN	0x20	3
37	J1	Y26	HPM_BMC_GPIOQ4	IN	0x20	4
38	D1	R26	HPM_BMC_GPIOS4	IN	0x20	5
39	K3	P24	HPM_BMC_GPIOS5	IN	0x20	6
40	J2	P23	HPM_BMC_GPIOS6	IN	0x20	7
41	M14	T24	HPM_BMC_GPIOS7	IN	0x20	8
42	B14	AF11	UNUSED_IN1_1	IN	0x20	9
43	C12	AD12	UNUSED_IN1_2	IN	0x20	10
44	J11	AA17	UNUSED_IN1_3	IN	0x20	11
45	C5	AB17	UNUSED_IN1_4	IN	0x20	12
46	K11	-	ESPI_BOOT_SEL	IN	0x20	13
47	N14	A15	HPM_BMC_GPIOI7	IN	0x20	14
48	K12	AC16	UNUSED_IN1_5	IN	0x20	15
49	F12	J23	HPM_BMC_GPIOB4	IN	0x28	0
50	E12	G26	HPM_BMC_GPIOB5	IN	0x28	1
51	P12	J24	HPM_BMC_GPIOB7	IN	0x28	2
52	N10	B16	HPM_BMC_GPIOI6	IN	0x28	3
53	F1	P25	HPM_BMC_GPION0	IN	0x28	4
54	E4	N23	HPM_BMC_GPION1	IN	0x28	5
55	D2	N25	HPM_BMC_GPION2	IN	0x28	6
56	D3	N24	HPM_BMC_GPION3	IN	0x28	7
57	C1	P26	HPM_BMC_GPION4	IN	0x28	8

Sl No	FPGA Pin	BMC Pin	Signal name	Direction (W.R.T to BMC)	SGPIO Register Address	Register Bit offset
58	B1	M23	HPM_BMC_GPION5	IN	0x28	9
59	F2	N26	HPM_BMC_GPION6	IN	0x28	10
60	D13	AB22	HPM_BMC_GPIOP0	IN	0x28	11
61	F3	AA23	HPM_BMC_GPIOP2	IN	0x28	12
62	E13	W23	HPM_BMC_GPIOP4	IN	0x28	13
63	C14	AB24	HPM_BMC_GPIOP6	IN	0x28	14
64	C4	B21	HPM_BMC_GPIOG7	IN	0x28	15

17. Hardware Management

Hawaii/Lani being a DC-SCM 1.0 contribution and DC-SCM itself being effectively defined as a hardware management module; it is our belief that a majority of the suggested information for this section has been covered above in greater detail.

- The Hawaii card architecture contains a dedicated 1Gb/s capable RJ-45 port for OOB manageability.
- Hawaii uses an embedded NIC PHY and does not use any modular OCP management module.
- The adapter is enabled in all power state except G3.
- The BMC chip used is ASPEED AST2600, with a 2 GB DRAM and a 128 MB flash for firmware storage.
- Firmware for BMC and FPGA can be updated programmatically. There is no failover/rollback protection.
- The following LEDs are available for diagnostic and debug usage
    - BMC heartbeat LED (D46)
    - FPGA Config done LED (D2)
    - Dediprog active LED (D36)
    - “Flash-in-Programming-Mode” indicators (BMC flash: D26, BIOS flash: D3, FPGA flash: D5)
- The card supports telemetry of 12V input and major BMC voltage rails (1.0V, 1.8V, 3.3V and RTC battery voltage)

18. Security (only for Platform Boards and Systems)

N/A

19. References (recommended)

N/A

Appendix A - Checklist for IC approval of this Specification

Item	Status or Details	Link to detailed explanation
Is this contribution entered into the OCP Contribution Portal?	Yes	
Was it approved in the OCP Contribution Portal?	Yes	
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	No	This is a reference design contribution only. AMD is NOT making available units for retail consumption.
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	No	See above.

Appendix B - OCP Supplier Information and Hardware Product Recognition Checklist

N/A, reference design contribution only.