

Edgecore AS7315-27X

Main PCB FPGA Specification

Revision 1.0



OPEN
Compute Project

Revision History

Revision	Date	Author	Description
1.0	9/25/2019	Jeff Catlin	Initial OCP Release

Contents

Revision History	2
Licenses	5
FPGA register	7
Offset 0x00 PCB Version (Read Only).....	8
Offset 0x01 FPGA version (Read Only).....	8
Offset 0x02 Power module status (Read&Write)	8
Offset 0x03 Power Enable (Read&Write)	9
Offset 0x04 DC/DC Margin control-1 (Read&Write).....	9
Offset 0x05 DC/DC Margin control-2 (Read&Write).....	10
Offset 0x16 UART select (Read & Write)	10
Offset 0x17 USB_Present (Read & Write).....	10
Offset 0x18 QSFP28_Present_Port01 ~ 03 (Read Only).....	11
Offset 0x19 QSFP28_LPMODE_Port01~03 (Read& Write)	11
Offset 0x20 Interrupt-1 (Read Only)	12
Offset 0x21 Interrupt-1 Mask (Read & Write).....	12
Offset 0x22 Interrupt-2 (Read Only)	12
Offset 0x23 Interrupt-2 Mask(Read & Write)	13
Offset 0x24 Interrupt-3 (Read & Write)	13
Offset 0x25 Interrupt-3 Mask (Read & Write).....	14
Offset 0x30 Reset-1 (Read& Write)	14
Offset 0x31 Reset-2 (Read& Write)	14
Offset 0x32 Reset-3 (Read Only).....	15
Offset 0x40 System LED-1 (Read& Write).....	15
Offset 0x41 System LED-2 (Read& Write).....	16
Offset 0x42 BITS LLP (Read& Write)	17
Offset 0x50 Heater state (Read& Write).....	17
Offset 0x60 Misc. control and state signals (Read& Write).....	17
Offset 0x70 I2C_WDPLL Mux Control	18

Offset 0x71 10MHz Mux Control	18
Offset 0x72 4K Hz Mux Control.....	19
Offset 0x73 1pps Mux Control	19
Offset 0x80 I2C LM75 CPLD Mux Control	20
Offset 0x81 LM75_1 Temp Stored	20
Offset 0x82 LM75_2 Temp Stored	20
Offset 0x83 LM75_3 Temp Stored	21
Offset 0x84 LM75_CPU Temp Stored	21
Offset 0x85 LM75_BMC Temp Stored	21
Offset 0x86 Cyclone4 FPGA I2C to UART & SPI Ctrl	21
Offset 0x87 Reset-4 (Read& Write)	22
Cyclone4 FPGA I2C to UART & SPI Address mapping.....	22
I2C to Uart Command Example.....	23

Licenses

All semiconductor devices that may be referred to in this specification, or required to manufacture products described in this specification, will be considered referenced only, and no intellectual property rights embodied in or covering such semiconductor devices shall be licensed as a result of this specification or such references. Notwithstanding anything to the contrary in the CLA, the licenses set forth therein do not apply to the intellectual property rights included in or related to the semi-conductor devices identifies in the specification. These references include without limitation the reference to devices listed below. For clarity, no patent claim that reads on such semiconductor devices will be considered a “Granted Claim” under the applicable Contributor License Agreement for this specification

Feature	AS7315-27X
CPU sub-system	CPU: Intel ® Atom™ Processor C3508,1.6GHZ DDR SDRAM: 8GB x 2 2400MHz with ECC (SO-DIMM) DDR4 SPI Flash (Boot): 16MB x 2 M.2 SSD: 32GB MLC TPM: SLB 9665XT2.0 FW5.63 INFINEON
Management	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45), Alarm port on fantray (RJ45).
Timing	GNSS GPS Receiver(SMB), Stack Sync (RJ45), 1GE Stack (RJ45), BITS (RJ45), TOD PPS (RJ45)
MAC	BroadcomBCM88470, 300Gbsfull duplex switching
Ethernet Ports	3x100GE QSFP28 (two support stacking), 4x1/10/25G SFP28 and 20x1/10G SFP+
CPLD	Altera 5M2210ZF324I5N (FBGA324) and 5M1270ZF256I5 (FBGA256)
FPGA	Altera EP4CGX30CF23I7N
PCB	20-Layers, EM891Kfor Mainboard 14-Layers,CPU module 8-Layers,TG 150 Power Connection Board 4-Layers, TG 150 FAN Board 4-Layers, TG 150Backplane Board
Power Supply	Max 300W PSU, DC to DC, 1+1 redundant load-sharing, hot-swappable Notes: The airflow is left to right (PSU side is inlet) from chassis system view.
Cooling	5 fan-tray modules with 5 pcs of 40mm x40mm x 28mm 12V fans, hot-swappable
Dimension	L(Depth):299.8±0.5mm(11.8031±0.0196inch) x W(Width):438.4±0.5mm(17.259808 ± 0.0196 inch) x H(Height):43.25±0.5 mm(1.7027±0.0196inch)

As of September 25, 2019, this specification is contributed under the OCP Contributor Licensing Agreement (OCP-CLA) by the following entities:
Acton Technology Corporation, through its subsidiary Edgecore Networks Corporation

Limitations of the OCP CLA license are noted below:
No Limitations

You can review the signed copies of the OCP-CLA for this specification on the OCP website. <http://www.opencompute.org/products/specsanddesign>
Usage of this specification is governed by the OCPHL permissive. You can review this license at <http://www.opencompute.org/participate/legal-documents/>

Your use of this Specification may be subject to other third-party rights. THIS SPECIFICATION IS PROVIDED "AS IS." The contributors expressly disclaim any warranties (express, implied, or otherwise), including implied warranties of merchantability, non-infringement, fitness for a particular purpose, or title, related to the Specification. The entire risk as to implementing or otherwise using the Specification is assumed by the Specification implementer and user. IN NO EVENT WILL ANY PARTY BE LIABLE TO ANY OTHER PARTY FOR LOST PROFITS OR ANY FORM OF INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION OR ITS GOVERNING AGREEMENT, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

FPGA register

Address	Register	R/W	Default value
0x00	PCB Version	Read Only	0x01
0x01	FPGA Version	Read Only	0x01
0x02	Power module status	Read Only	0x3C
0x03	Power Enable	Read&Write	0x01
0x04	DC/DC Margin control-1	Read&Write	0x00
0x05	DC/DC Margin control-2	Read&Write	0x00
0x16	UART Select	Read&Write	0x00
0x17	USB Present	Read&Write	0x04
0x18	QSFP28_Present_Port01 ~ 03	Read Only	0x07
0x19	QSFP28_LPMODE_Port01 ~ 03	Read&Write	0x07
0x20	Interrupt-1	Read Only	0xFF
0x21	Interrupt-1 Mask	Read&Write	0x00
0x22	Interrupt-2	Read Only	0xFF
0x23	Interrupt-2 Mask	Read&Write	0x00
0x24	Interrupt-3	Read Only	0xFF
0x25	Interrupt-3 Mask	Read&Write	0x00
0x30	Reset-1	Read&Write	0xFF
0x31	Reset-2	Read&Write	0xFF
0x32	Reset-3	Read Only	0xFF
0x40	System LED-1	Read&Write	0xFF
0x41	System LED-2	Read&Write	0xFF
0x50	Heater state	Read&Write	0x0F
0x60	Misc. control and state signals	Read&Write	0x25
0x70	I2C WDPLL Mux Control	Read&Write	0x00
0x71	10M Hz Mux Control	Read&Write	0x00
0x72	4K Hz Mux Control	Read&Write	0x00
0x73	1PPS Mux Control	Read&Write	0x00
0x80	I2C LM75 CPLD Mux Control	Read&Write	0x10
0x81	LM75_1 Temp Stored	Read&Write	0x00
0x82	LM75_2 Temp Stored	Read&Write	0x00
0x83	LM75_3 Temp Stored	Read&Write	0x00
0x84	LM75_CPU Temp Stored	Read&Write	0x00
0x85	LM75_BMC Temp Stored	Read&Write	0x00

Address	Register	R/W	Default value
0x86	Cyclone4 FPGA I2C to UART & SPI Ctrl	Read&Write	0x03
0x87	Reset-4	Read&Write	0xFF

Table 1 FPGA I/O Register Table

Note: 0x04, 0x05 just only for margin testing.

Offset 0x00 PCB Version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)			
2:0	PCB_version[2:0]	R		001: R0A 010: R0B Others: Reserved

Offset 0x01 FPGA version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FPGA_ver[7:0]	R	001	[2:0]: FPGA version

Offset 0x02 Power module status (Read&Write)

Bit	Name	R/W	Reset Value	Description
7	PS2_ON	R/W	0	0:PSU2 12V output 1: PSU2 12V no output
6	PS1_ON	R/W	0	0:PSU1 12V output 1: PSU1 12V no output
5	PS2_AC_ALERT	R	1	0: PSU2 POWER Fail 1: PSU2 POWER Good
4	PS1_AC_ALERT	R	1	0: PSU1 POWER Fail 1: PSU1 POWER Good
3	PS2_12V_PG	R	1	0: PSU2 12V Power Fail

				1: PSU2 12V Power Good
2	PS1_12V_PG	R	1	0: PSU1 12V Power Fail 1: PSU1 12V Power Good
1	PS2_PRESENT	R	0	0: PSU2 Present 1: PSU2 not Present
0	PS1_PRESENT	R	0	0: PSU1 Present 1: PSU1 not Present

Offset 0x03 Power Enable (Read&Write)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	USB_PWRON_N	R/W	1	0: USB HUB power converter disable 1: USB HUB power converter enable

Offset 0x04 DC/DC Margin control-1 (Read&Write)

Bit	Name	R/W	Reset Value	Description
7	VDD1P8_MARGIN_HIGH	R/W	0	0: VDD1P8_MARGIN high switch turn off 1: VDD1P8_MARGIN high switch turn on
6	VDD1P8_MARGIN_LOW	R/W	0	0: VDD1P8_MARGIN low switch turn off 1: VDD1P8_MARGIN low switch turn on
5	VDD1P2_DDR_MARGIN_HIGH	R/W	0	0: VDD1P2_MARGIN high switch turn off 1: VDD1P2_MARGIN high switch turn on
4	VDD1P2_DDR_MARGIN_LOW	R/W	0	0: VDD1P2_MARGIN low switch turn off 1: VDD1P2_MARGIN low switch turn on
3	VDD1P25_MARGIN_HIGH	R/W	0	0: VDD1P25_MARGIN high switch turn off 1: VDD1P25_MARGIN high switch turn on
2	VDD1P25_MARGIN_LOW	R/W	0	0: VDD1P25_MARGIN low switch turn off 1: VDD1P25_MARGIN low switch turn on
1	VDD1P0_MARGIN HIGH	R/W	0	0: VDD1P0_MARGIN high switch turn off 1: VDD1P0_MARGIN high switch turn on
0	VDD1P0_MARGIN LOW	R/W	0	0: VDD1P0_MARGIN low switch turn off 1: VDD1P0_MARGIN low switch turn on

Offset 0x05 DC/DC Margin control-2 (Read&Write)

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3	XFP_3V3_MARGIN_HIGH	R/W	0	0: XFP_3V3_MARGIN high switch turn off 1: XFP_3V3_MARGIN high switch turn on
2	XFP_3V3_MARGIN_LOW	R/W	0	0: XFP_3V3_MARGIN low switch turn off 1: XFP_3V3_MARGIN low switch turn on
1	VPP_DDR2P5_MARGIN_HIGH	R/W	0	0: VPP_DDR2P5_MARGIN high switch turn off 1: VPP_DDR2P5_MARGIN high switch turn on
0	VPP_DDR2P5_MARGIN_LOW	R/W	0	0: VPP_DDR2P5_MARGIN low switch turn off 1: VPP_DDR2P5_MARGIN low switch turn on

Offset 0x16 UART select (Read & Write)

Bit	Name	R/W	Reset Value	Description
7				
6	GPS_RX or CPU_TX(FPGA1588_TOD_OUT_R) to FPGA1588_UART1_TOD_OUT	R/W	0	0: Switch FPGA1588_TOD_OUT_R to output. 1: Switch GPS_UART_RX_R to output.
5	FPGA_SN65C_2DE	R/W	0	0: Switch TOD_RJ45 as input. 1: Switch TOD_RJ45 as output.
4	FPGA_SN65C_1DE	R/W	0	0: Switch 1pps to input. (not define) 1: Switch 1pps to output. (not define)
3:2	GPS_UART_RX_R (ToD_GPS) GPS_UART_RJ_RX (ToD_RJ45)	R/W	00	[3:2] 00: select GPS as UART input to the CPU. 01: select ToD_RJ45 as UART input to the CPU.
1:0	CPLD_RJ_UART_RX_R (RJ45) CPLD_USB_UART_RX_R (USB)	R/W	01	[1:0] 00: select RJ45 as UART input to the CPU. 01: select USB as UART input to the CPU.

Offset 0x17 USB_Present (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	USB_Enable	R/W	1	1: USB ENABLED and USB cable is installed, USB Rx connects to CPU, If the USB cable is NOT installed, the RJ Rx signal connects to the CPU. 0: USB DISABLED, the RJ Console port will

				become the primary Rx.
1	USB_SUSP_L	R	0	1: indicates that the host USB port and USB console port is active. 0: indicates that the host USB port is in sleep mode or the USB cable is not connected.
0	USB_VBUS_DET	R	0	1: indicates that the Micro USB console is inserted. 0: No USB cable module be installed

Offset 0x18 QSFP28_Present_Port01 ~ 03 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	(Reserved)	R/W	0	
2	QSFP_PRSNT_P03	R	1	0: Show QSFP28 module has been installed 1: No QSFP28 module be installed
1	QSFP_PRSNT_P02	R	1	0: Show QSFP28 module has been installed 1: No QSFP28 module be installed
0	QSFP_PRSNT_P01	R	1	0: Show QSFP28 module has been installed 1: No QSFP28 module be installed

Offset 0x19 QSFP28_LPMODE_Port01~03 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:2	(Reserved)	R/W	0	
1	QSFP_MODE_P03	R/W	1	0: Module work in High Power. 1: Module work in Lowe Power.
1	QSFP_MODE_P02	R/W	1	0: Module work in High Power. 1: Module work in Lowe Power.
0	QSFP_MODE_P01	R/W	1	0: Module work in High Power. 1: Module work in Lowe Power.

Note1: Depend on transceiver supplier support this function or not.

Note2: Need to consider “Power_over-ride” and “Power_set” software control bits.

Offset 0x20 Interrupt-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	CPLD2_INT	R	1	0: Interrupt assert 1: Interrupt deassert
6	CPU_THERMALTRIP	R	1	0: Interrupt assert 1: Interrupt deassert
5	CPU_PROCHOT	R	1	0: Interrupt assert 1: Interrupt deassert
4	LM75BD3_INT	R	1	0: Interrupt assert 1: Interrupt deassert
3	LM75BD2_INT	R	1	0: Interrupt assert 1: Interrupt deassert
2	LM75BD1_INT	R	1	0: Interrupt assert 1: Interrupt deassert
1	LM75BD_HEATER_INT_1	R	1	0: Interrupt assert 1: Interrupt deassert
0	LM75BD_HEATER_INT_0	R	1	0: Interrupt assert 1: Interrupt deassert

Offset 0x21 Interrupt-1 Mask (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD2_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
6	CPU_THERMALTRIP_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
5	CPU_PROCHOT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
4	LM75BD3_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
3	LM75BD2_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
2	LM75BD1_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
1	LM75BD_HEATER_INT_1_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
0	LM75BD_HEATER_INT_0_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable

Offset 0x22 Interrupt-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	UCD90160_INT	R	1	0: Interrupt assert 1: Interrupt deassert
6	INT_MGMT_PHY_N	R	1	0: Interrupt assert

				1: Interrup deassert
5	MAC_CPLD_INT_L	R	1	0: Interrup assert 1: Interrup deassert
4	THERMAL_INT_L	R	1	0: Interrup assert 1: Interrup deassert
3	USB_PWRFLT_N	R	1	0: Interrup assert 1: Interrup deassert
2	ZL30773_INT_REQ	R	1	0: Interrup assert 1: Interrup deassert
1	QSFP_INT_P02	R	1	0: Interrup assert 1: Interrup deassert
0	QSFP_INT_P01	R	1	0: Interrup assert 1: Interrup deassert

Offset 0x23 Interrup-2 Mask(Read & Write)

Bit	Name	R/W	Reset Value	Description
7	UCD90160_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
6	INT_MGMT_PHY_N_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
5	MAC_CPLD_INT_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
4	THERMAL_INT_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
3	USB_PWRFLT_N_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
2	ZL30773_INT_REQ_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
1	QSFP_INT_P02_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
0	QSFP_INT_P01_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable

Offset 0x24 Interrup-3 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	QSFP_INT_P03	R	1	0: Interrup assert 1: Interrup deassert
5	FAN_INT_L	R	1	0: Interrup assert 1: Interrup deassert
4	INT_DS26503_L(BITS)	R	1	0: Interrup assert 1: Interrup deassert
3	CPLD23_INT_CPU	R/W	1	0: Interrup assert 1: Interrup deassert
2	MAC_INT_L	R/W	1	0: Interrup assert 1: Interrup deassert,这个中断的作用?
1	USB1_PWRFAULT	R/W	1	0: Interrup assert 1: Interrup deassert

0	SYS_CPLD_INT_CPU	R/W	1	0: Interrup assert 1: Interrup deassert
---	------------------	-----	---	--

Offset 0x25 Interrupt-3 Mask (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	QSFP_INT_P03_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
5	FAN_INT_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
4	INT_DS26503_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
3	CPLD23_INT_CPU_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
2	MAC_INT_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
1	USB1_PWRFAULT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
0	SYS_CPLD_INT_CPU_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable

Offset 0x30 Reset-1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	I2C_CPU1_RESET_N ---RESET PCA9548(0x72)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
6	I2C_CPU0_RESET_N --- RESET PCA9548(0x76)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
5	QSP01_P02_RESET_N --- RESET PCA9548(0x74)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
2	SP17_P24_RESET_N --- RESET PCA9548(0x73)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
1	SP09_P16_RESET_N --- RESET PCA9548(0x71)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	SP01_P08_RESET_N --- RESET PCA9548(0x70)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

Offset 0x31 Reset-2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
-----	------	-----	-------------	-------------

7	RST_BITS_DS26503_R	R/W	0	1: The Device is in normal operating state 0: The Device is in reset state
6	CPLD_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
5	QSFP_RST_P02_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
4	QSFP_RST_P01_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
3	MAC_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
2	MGMT_PHY_RST_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
1	30773_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	USB_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

Offset 0x32 Reset-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:5	(Reserved)	R/W	0	
4	Reset_button_RST	R	1	0: Button reset to CPLD. Indicates Reset Button had pushed.
3	CPU_JTAG_RST_R	R	1	TBD
2	SYS_SW_RST_N	R	1	0: Indicate FPGA reset the system all of device, system is in a reset state
1	UCD90160_RST_L	R/W	1	TBD, no use
0	POWER_RST	R	1	TBD

Offset 0x40 System LED-1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	LOC_A	R/W	1	0: Flashing by remote management command. Assists the technician in finding the right device for service in the rack. (show Amber blink) 1: Not a particular switch that technician need to find. (LED off)
5	FAN_G FAN_A	R/W	11 Now no	00: indicator light is off. 10: System FAN operating normally.

4			function Control by fan int and LM75B temp	01: System FAN tray present but is fault. 11:Green blinking->System FAN tray is power on but not running due to low temperature (which means FAN is function OK)
3	PSU2_G	R/W	0	0: indicator light is on when power good enable. 1: indicator light is off.
2	PSU2_A	R/W	1	0: indicator light is on when power good disable. 1: indicator light is off.
1	PSU1_G	R/W	0	0: indicator light is on when power good enable. 1: indicator light is off.
0	PSU1_A	R/W	1	0: indicator light is on when power good disable. 1: indicator light is off.

Offset 0x41 System LED-2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	ALARM_G ALARM_A	R/W	00	
5:4	DIAG_G DIAG_A	R/W	11	[5:4] 00: System self-diagnostic test is in progress.(show Green Blink) 01: System self-diagnostic test successfully completed. (show Green) 10: System self-diagnostic test has detected a fault. (show Amber) 11: Diagnostic doesn't active.(LEDs are all off)
3	ToD_G	R/W	1	0: indicator light is on. (when ToD port enable) 1: indicator light is off.
2	ToD_A	R/W	0	
1	BITS_G	R/W	1	0: indicator light is on. (when LLP enable) 1: indicator light is off.
0	BITS_A	R/W	0	

Offset 0x42 BITS LLP (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	RLOS_FPGA	R	1	0: indicates that the LLP cable is inserted.

Offset 0x50 Heater state (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	I2C_CTRL_HEATER/ PWR_EN	R/W	0	1: HEATER/ PWR_EN Control by i2c 0: HEATER/ PWR_EN Control by fpga
5	MB2_PWR_EN	R/W	0	1: Turn on DC12V switch 0: Turn off DC12V switch
4	MB1_PWR_EN	R/W	0	1: Turn on DC12V switch 0: Turn off DC12V switch
3	Fan_idle	R	1	1: Fan normal operating 0: Fan stop operating
2	HEATER_ENABLE_3	R/W	1	1: Heater disable. 0: Heater enable.
1	HEATER_ENABLE_2	R/W	1	1: Heater disable. 0: Heater enable.
0	HEATER_ENABLE_1	R/W	1	1: Heater disable. 0: Heater enable.

Offset 0x60 Misc. control and state signals (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	RESET_MAC88470	R	0	1: The Device is in normal operating state 0: The Device is in reset state
6	SW1_Select	R/W	0	0: CPU JTAG signals pass through to FPGA 1: CPU JTAG signals pass through to FAN_CPLD
5	SYS_PWR_READY_R	R	1	1: Power sequence is ready. 0: Power sequence is not ready.
4	1588_EEPROM_SEL	R/W	1	0: The WAN-PLL's EEPROM control signal comes from CPU 1: The WAN-PLL's EEPROM control signal comes from WAN-PLL

3	ID_Button	R/W	0	TBD
2	EE_WP	R/W	1	0:EEPROM write protect disable 1:EEPROM write protect enable
1	1588_FPGA_UART1_ToD_SEL	R/W	1	1:TOD signal output to TOD_RJ CON 0:TOD signal output to GPS CON
0	UCD9090_ALERT_L	R/W	1	TBD

Offset 0x70 I2C_WDPLL Mux Control

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2	I2C_MUX2_EN	R/W	0	0: internal cyclone4 i2c master to WAN_PLL_30773_SCL/SDA_FP 1: enable I2C1: WAN_PLL_82P30773_SCL/SDA to WAN_PLL that CPU can access WDPLL.
1:0	(Reserved)	R/W	0	

Offset 0x71 10MHz Mux Control

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	10M_SYNCE_FPGA_R (default) 10MHZ_WDPLL_1588_OUT_R_FPGA	R/W	1	0: Select sync-E as input to the SMB Conn out and MAC. 1: Select 1588 as input to the SMB Conn out and MAC.

Offset 0x72 4K Hz Mux Control

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	4K_SYNCE_FPGA_R(default) 4K_1588_FPGA_R	R/W	R/W	0: Select sync-E as input to MAC. 1: Select 1588 as input to MAC.

Offset 0x73 1pps Mux Control

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3:2	FAP_NSE_SYNC_IN1(default) MAC_1PPS_IN_2 MAC_1PPS_IN_1	R/W	00	00: Select MAC_NSE_SYNC_IN 1 as input to WDPLL and 1PPS_MAC_OUT_MUX 01: Select MAC_NSE_SYNC_OUT as input to WDPLL and 1PPS_MAC_OUT_MUX 10: Select MAC_GPIO1 as input to WDPLL and 1PPS_MAC_OUT_MUX
1:0	1PPS_SYNC_E_1588_OUT_R_FPGA(default) 1PPS_WDPLL_1588_OUT_R_FPGA 1PPS_MAC_OUT_MUX	R/W	00	00: Select sync-E as input to SMB CONN and MAC 01: Select 1588 as input to SMB CONN and MAC 10: Select MAC as input to SMB CONN and MAC

Offset 0x80 I2C LM75 CPLD Mux Control

Bit	Name	R/W	Reset Value	Description
7:5	I2C_Channel_Sel	R/W	000	110: LM75B1_HEATER BMC 101: LM75B0_HEATER CPU 100: LM75BD3_SCLK U18 011: LM75BD2_SCLK U29 010: LM75BD1_SCLK U27 001: FAN_SCL_FPGA_R FAN_CPLD 0x66 000: I2C not selected Notice: When bit4 =1 recommend set bit7:5 to 3'b000
4	wl2cMasterEn	R/W	1	LM75B / FPGA to CPLD I2C Master / I2C_MUX2 Enable Control 1 : Enable FPGA to CPLD I2C Master & LM75B Temp IC I2C Master Disable I2C_MUX2 (Automatic control) 0 : Disable FPGA to CPLD I2C Master & LM75B Temp IC I2C Master Enable I2C_MUX2 Notice: When bit4 =1 CPU can't access LM75B & FAN_CPLD (Manual control)
3:0	(Reserved)	R/W	0	

Offset 0x81 LM75_1 Temp Stored

Bit	Name	R/W	Reset Value	Description																																																
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><thead><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr></thead><tbody><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></tbody></table> Notice: Only store Temp Reg MSByte address:0x4C	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

Offset 0x82 LM75_2 Temp Stored

Bit	Name	R/W	Reset Value	Description
-----	------	-----	-------------	-------------

7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table> Notice: Only store Temp Reg MSByte address:0x49	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

Offset 0x83 LM75_3 Temp Stored

Bit	Name	R/W	Reset Value	Description																																																
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table> Notice: Only store Temp Reg MSByte address:0x4A	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

Offset 0x84 LM75_CPU Temp Stored

Bit	Name	R/W	Reset Value	Description																																																
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table> Notice: Only store Temp Reg MSByte address:0x4E	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

Offset 0x85 LM75_BMC Temp Stored

Bit	Name	R/W	Reset Value	Description																																																
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register <table><tr><th colspan="8">MSByte</th><th colspan="8">LSByte</th></tr><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>D10</td><td>D9</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr></table> Notice: Only store Temp Reg MSByte address:0x4F	MSByte								LSByte								7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X
MSByte								LSByte																																												
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																					
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X																																					

Offset 0x86 Cyclone4 FPGA I2C to UART & SPI Ctrl

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	

3	ToD_RX (GPS_UART_RJ_RX) Control	R/W	0	0: FIFO not save ToD_RX in
2	GPS_RX (GPS_UART_RX_R) Control	R/W	0	0: FIFO not save GPS_RX in
1	I2C_to_UART Controller Module Reset control	R/W	1	0: Reset I2C_to_UART Controller module
0	I2C_to_SPI Module Reset control I2C_to_UART Module Reset control	R/W	1	0: Reset iic_to_spi & iic_to_uart module

Offset 0x87 Reset-4 (Read& Write)

Bit	Name	R/W	Reset Value	Description
4		R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
2	TPM_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
1	FT2232H_RESET_N(U 转 JTAG)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	QSFP_RST_P03_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

Cyclone4 FPGA I2C to UART & SPI Address mapping

I2C Address: 0x62 (7 bit) Offset address mode: 1 byte

SPI_BITS: SCLK: 1250000, CPOL=1, CPHA=1

UART_GPS : Core Speed: 38400 hz / Data Bit: 8bit / Parity: None / Stop Bit: 1bit /Not include CTS/RTS

UART_ToD : Core Speed: 38400 hz / Data Bit: 8bit / Parity: None / Stop Bit: 1bit /Not include CTS/RTS

FIFO_GPS: Depth:256

FIFO_ToD: Depth:256

Table 1.1. System Address mapping control by I2C slave to Avalon Master

	i2cslave_to_avlmm_bridge_0_avalon_master
mm_bridge_0.s0	
spi_0_spi_control_port	0x0000_0000 - 0x0000_001f
uart_gps.sl	0x0000_0020 - 0x0000_003f
uart_gps_read_fifo.in	0x0000_00a0 - 0x0000_00a3
uart_gps_read_fifo.out	0x0000_00a4 - 0x0000_00a7
uart_gps_read_fifo.in_csr	0x0000_0060 - 0x0000_007f
uart_tod.sl	0x0000_0040 - 0x0000_005f
uart_tod_read_fifo.in	0x0000_00b0 - 0x0000_00b3
uart_tod_read_fifo.out	0x0000_00b4 - 0x0000_00b7
uart_tod_read_fifo.in_csr	0x0000_0080 - 0x0000_009f

Table 1.2. SPI Master Core Address mapping control by I2C slave to Avalon Master

Internal Address	Register Name	Type [R/W]	32-11	10	9	8	7	6	5	4	3	2-0
0	rxdata ⁽⁸⁾	R	RXDATA (n-1..0)									
1	txdata ⁽⁸⁾	W	TXDATA (n-1..0)									
2	status ⁽⁶⁾	R/W			EOP	E	RRDY	TRDY	TMT	TOE	ROE	
3	control	R/W		SSO ⁽⁷⁾	IEOP	IE	IRRDY	ITRDY		ITOE	IROE	
4	Reserved	—										
5	slaveselct ⁽⁷⁾	R/W	Slave Select Mask									
6	eop_value ⁽⁸⁾	R/W	End of Packet Value (n-1..0)									

Table 1.3 Uart Master Core Address mapping control by I2C slave to Avalon Master

Offset	Register Name	R/W	Description/Register Bits													
			15:13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	rxdata	RO	Reserved					(2)	(2)	Receive Data						
1	txdata	WO	Reserved					(2)	(2)	Transmit Data						
2	status ⁽¹⁾	RW	Reserved	eop	cts	dcts		e	rrdy	trdy	tmt	toe	roe	brk	fe	pe
3	control	RW	Reserved	ieop	rts	idcts	trbk	ie	irrdy	itrdy	itmt	itoe	iroe	ibrk	ife	ipe
4	divisor ⁽³⁾	RW	Baud Rate Divisor													
5	endof-packet ⁽³⁾	RW	Reserved					(2)	(2)	End-of-Packet Value						

Table 1.4 FIFO CSR register Address mapping control by I2C slave to Avalon Master

offset	31				24	23				16	15					8	7	6	5	4	3	2	1	0
base	fill_level																							
base + 1																			i_status					
base + 2																			event					
base + 3																			interrupt enable					
base + 4	almostfull																							
base + 5	almostempty																							

I2C to Uart Command Example

1. I2C write data to UART GPS TX flow

i2c read addr:0x62 offset :0x28(status) → Check offset 0x28 bit 5(TOE) , 6(ROE) is equal to 1 or not

i2c write addr:0x62 offset :0x24(txdata) Data:0xFF → UART TX Send 0xFF to GPS RX

2. i2c read data from UART GPS RX flow

i2c read addr:0x62 offset :0x64(status) bit 1 → Check offset 0x64 bit0 is equal to 1 or not

i2c read addr:0x62 offset :0xA4(fifo.out) → Read data from fifo output data is gps tx data\

3. i2c read data from UART ToD RX flow

i2c read addr:0x62 offset :0x84(status) bit 1 → Check offset 0x84 bit0 is equal to 1 or not

i2c read addr:0x62 offset :0xB4(fifo.out) → Read data from fifo output data is ToD tx data