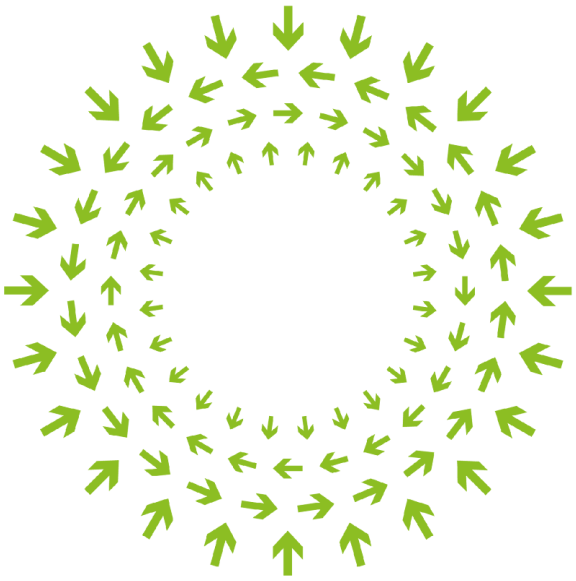


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Compute Project

48V Onboard Power Solution Qualification Checklist

Version 1.0.0

Effective 11/15/24

Contributors: Google, Microsoft, Meta, STMicroelectronics, Texas Instruments, Delta, Cyntec Corp, Intel Corporation

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2. Acknowledgements

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List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

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[Shingo Kunii and Shohei Masuda **Murata**]
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3. Compliance with OCP Tenets

1.1. Openness

By providing a standardized 48V 1st Stage Power Qualification Requirements overview for OCP, it provides other Hyperscaler and suppliers with the guidelines and inputs to anticipate the quality and reliability requirements for future designs.

1.2. Efficiency

Contributes to the reduction of design, development cost as well as efficiency in supply chain management by providing 48V 1st Stage Qualification Requirements through OCP. The common qualification requirements allow for suppliers to be able to create and reuse a common set of operation procedures for different Hyperscalers. Hyperscalers can also anticipate and re-use design efforts for next generation products.

1.3. Impact

By providing this contribution we are empowering Hyperscaler or suppliers to achieve faster time-to-market development by investing early and determining their roadmap of requirements. Suppliers can invest early and get higher return on investment as they scale their tools, resources and processes across multiple target customers.

1.4. Scale

With the continued increase in the Data Center Power requirements, anticipating and achieving power efficiency is paramount. The creation and sharing of the 48V Ist Stage Power Qualification Requirements can empower not just other Hyperscalers and suppliers that provide direct solutions, but also to subtier suppliers who support those solution level suppliers.

1.5. Sustainability

Providing this 48V 1st Stage Power common footprint solution for Data centers enables efficient and responsible power consumption. The common footprint allows for efficiencies and responsible supply chain development and management that help suppliers only invest and develop in solutions that will likely meet customer needs. Suppliers may save resources in testing and personnel for reliability and quality metrics.

4. Objective

This document details the general design verification and qualification requirements of 48V power solutions for high-performance and high-density 48V rack applications. The detailed information on 48V power solutions provided in this qualification specification is based on the alignment of the 48V Qualification Requirements OCP Work stream participants.
The partnership aims to drive common solutions in 48V power, specifically by establishing more common footprint blocks, improving supply chain efficiency, increasing design flexibility, reducing qualification processes during product development, and standardizing industry guidelines related to reliability and testing.

5. Background

Google, in partnership with Microsoft, presented Onboard Power Delivery Specs and Qualifications at OCP 2023. The presentation included an overview of onboard power evolution shown in figure-1 and an example illustrates the power related failures under a complex data center environment shown in figure-2.

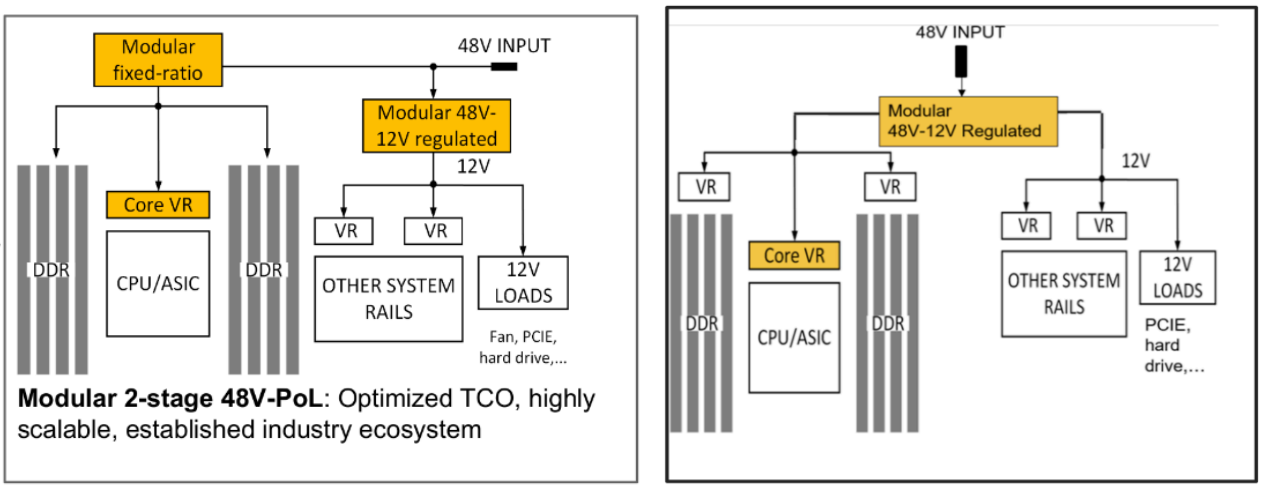


Figure-1 Google and Microsoft onboard power evolution

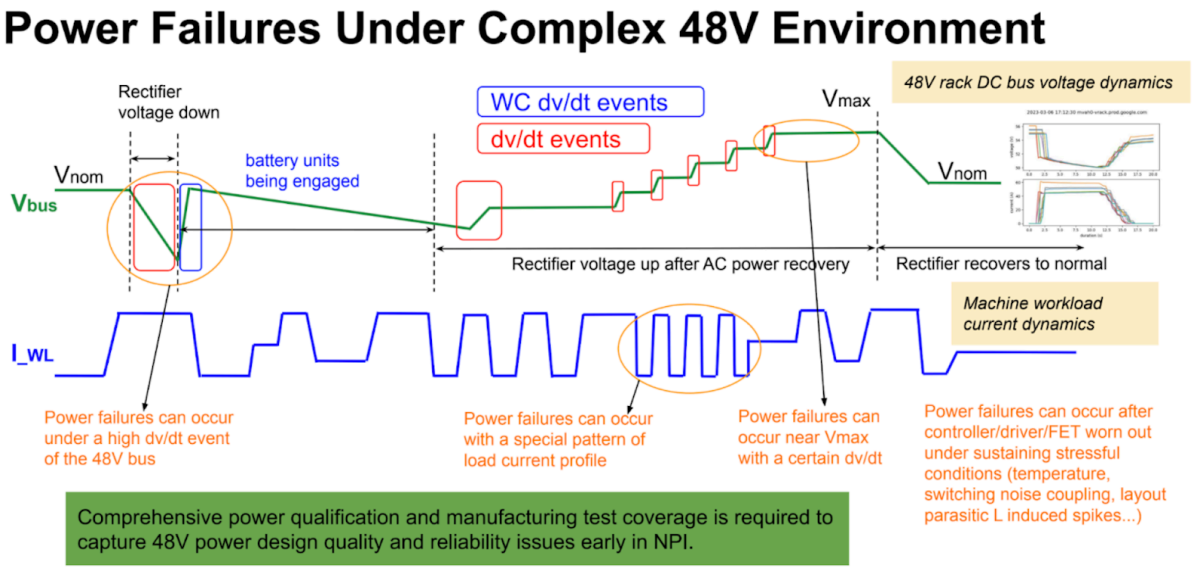


Figure-2 Power related failures under a complex data center environment

Considering the differences and complexities of workloads, system applications, data center environments, and rack resonance with parasitic inductance, a more comprehensive design verification checklist has been developed. This checklist, detailed in this specification as shown in Figure 3, covers bench-level qualification, chamber qualification, manufacturing testing, and reliability testing.

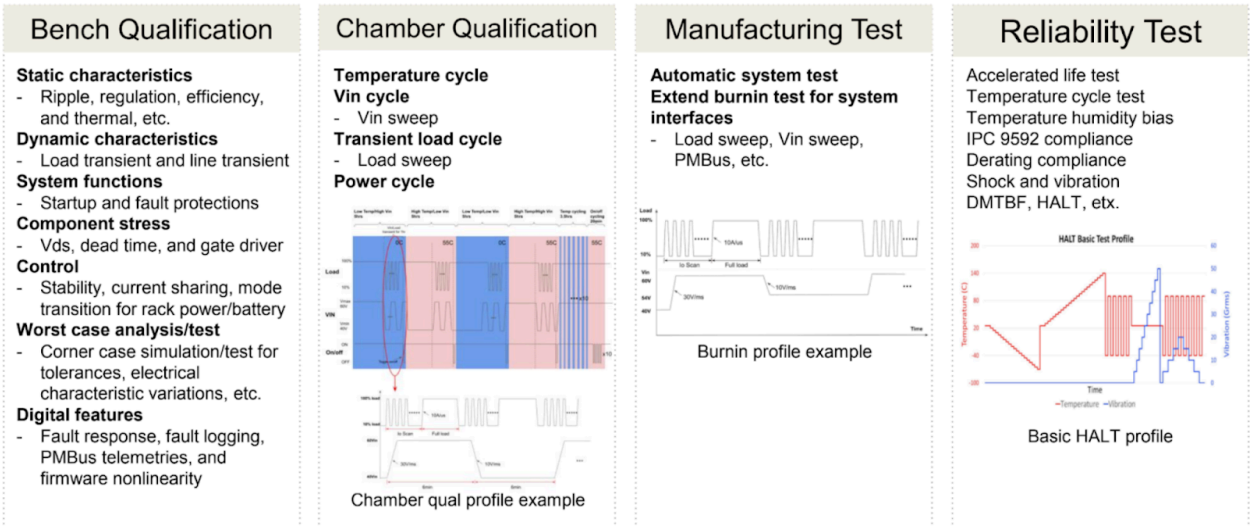


Figure-3 Comprehensive power design qualification checklist

6. Bench test requirements

Static characteristics

Items	*Description*
Static voltage	Measure the output voltage at typical, minimum and maximum input voltages. Sweep the load current from 0% to 100%, in 20% increments.
Ripple and noise	Measure the input and output voltage ripple at typical, minimum and maximum input voltages, with the load current at 0%, 50%, and 100%.
Cin characterization	Make sure the input MLCC and electrolytic capacitors are properly selected and ripple is within acceptable range.
Cout characterization	Make sure the output MLCC and electrolytic capacitors are properly selected and ripple is within acceptable range.
Efficiency	1. Measure the efficiency curve at typical, minimum and maximum input voltages. 2. Perform loss analysis and breakdown. 3. Correlate efficiency measurement data with simulation models and provide guidelines. 4. Identify key performance gaps and root causes. 5. Provide efficiency optimization guidelines in terms of efficiency v.s. size v.s. transient performance tradeoffs.
Thermal	1. Characterize key powertrain components temperature rise under nominal/worst load conditions and line voltage conditions. 2. 2R model for thermal simulation. 3. Thermal verification report with correlation and measurement.

Dynamic characteristics

Items	*Description*
Load transient	3D load transient test (frequency up to switching freq, duty cycle) under max line, nominal line and min line voltages.
Input swing	Test output regulation with fast dv/dt line transient (30V/ms upslope and 10V/ms downslope). Vin from 40V to 60V.

Input swing + load transient	A mix of the above two tests.
Input filter damping	Sweep the load frequency close to input filter resonance.

System functions

Items	***Description***
Start up	Test the startup under different enable, bias, Vin sequence or generate a sequencing spec and validate the system startup to the spec.
Pre-biased start-up	Test the startup behavior under different Vout bias situations.
Shut down	Test shut down sequencing, timing, and the discharge time of Vout and intermediate voltage nodes such as flying capacitor voltage.
Power cycle	1. This test will be performed cycling Vin (converter input voltage) between 0V and 60V with 16sec period and 50% duty cycle. 2. There could be 1 W passive load at the output. 3. This test will be performed by cycling EN pin of the controller IC with 16sec period and 50% duty cycle.
Fault protection	1. Validate each fault protection function and behavior, e.g., UVP, OVP, OCP, OTP. 2. Characterize the sensing accuracy of voltage, current, and temperature.

Control loop

Items	***Description***
Loop gain	Bode plot analysis at different input voltages, loadings and output caps. Test Loop gain using Min and Max recommended output capacitance based on module Technical Spec.
SW node characterization	Characterize and understand factors that affect SW node jitter and Vout low frequency / random frequency ripples under different loading.
CCM-DCM transition	Verify the system response if the converter has different operating modes at light-load and heavy-load.

Mode transition	Any non-linear functionalities that lead to different operating modes and transitions (i.e., converter circuit operating mode change at 50% duty cycle).
Current sharing	Make sure both static and dynamic current sharing are acceptable (e.g., within 10%) and no large current imbalance that may trigger OCP or reduce OCP margins.

Critical voltage node and timing

Items	***Description***
Power FET Vds	Characterize MOSFET Vds worst case overshoot stress / avalanche across operating conditions. (Line voltage, switching frequency, duty cycle, temperature, load current)
Power FET Vgs	Characterize the switch gate voltage during ON/OFF transition.
Deadtime	Make sure the deadtimes are sufficient and symmetrical across all switches, especially when multiple types of switches and gate drivers are used.
Flying capacitor	1. Make sure the capacitor ripple (especially at full load) is within the acceptable range. 2. The RMS current of each flying capacitor shall not cause over 20C temp rise for reliability consideration. 3. Make sure the capacitor dc voltage is at the designed voltage. 4. If there are multiple flying capacitors, make sure their voltages are balanced to the desired level.
Pin specification	1. Bootstrap. Make sure no ringing will overstress the BOOT pin. 2. SW node and other pins that could go negative. Make sure no overstress could potentially cause reliability issues. 3. All pins are within the datasheet spec. 4. Gate driver output capability. 5. PWM pins. Characterize PWM behaviors, noise sensitivity and jitter over line voltage and load current. 6. Voltage ripple on VCC pin.

Worst case analysis / test

Items	*Description*
For any of the above tests, identify any potential corner or worst cases that will stress the VR most	Create the worst case scenario to stress and validate the IBC behavior.
DFMEA	Characterize the potential failure modes.

Digital features

Items	*Description*
Fault logging, fault threshold & response	Generate the faults from the controller (e.g., OC, OV, UVLO.) to verify the fault registers.
PMBus telemetries	1. Validate current sense voltage accuracies through telemetry. 2. Validate PMBus registers read/ write operations.
Black box logging test	Validate the black box function when power cycle, enable toggled, loose power supply (bias power is alive), and faults occur.
Communication bus	Verify communication functionality during the test.
Status and alerts	Read out corresponding registers for status and alert during the test.
Standard	PMBus version 1.3.1 and later, SMBus version 3.2 and later.

7. Chamber qualification

Objective

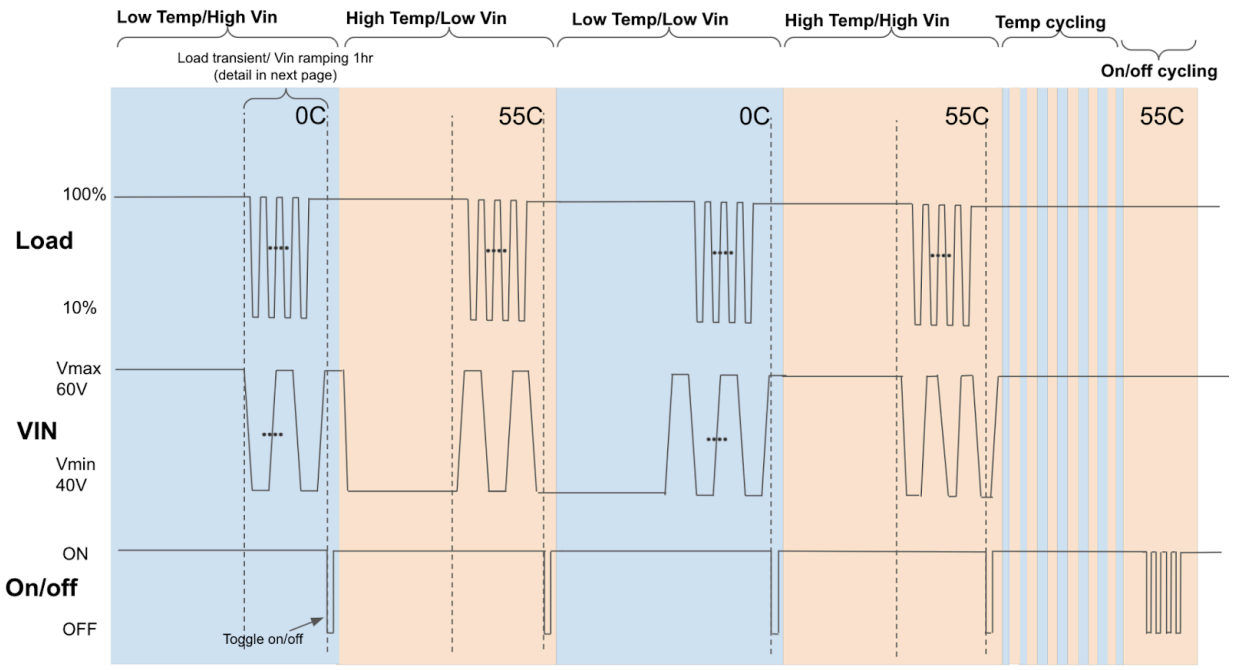
Test a certain number of test boards in the chamber, with a variety of stresses including input voltage swings, load swings, temperature cycling, and power cycling.

Quantity

3 boards as minimum. If there are 2nd sources for the major power components (e.g., FETs, magnetics, flying capacitors, PCB, or others), separate boards into different configs.

Test Steps

Profile (24 hour based)	***Description***
Duration: 0 - 5 hr Low Temp (0C), High Vin (60V)	● For the first 4 hours, running at full load condition. ● For the last hour, run Vin cycling and load sweep as shown in Figure-4. Power cycle the system at the end.
Duration: 5 - 10 hr High Temp (55C), Low Vin (40V)	● For the first 4 hours , running at full load condition. ● For the last hour, run Vin cycling and load sweep as shown in Figure-4. Power cycle the system at the end.
Duration: 10 - 15 hr Low Temp (0C), Low Vin (40V)	● For the first 4 hours , running at full load condition. ● For the last hour, run Vin cycling and load sweep as shown in Figure-4. Power cycle the system at the end.
Duration: 15 - 20 hr High Temp (55C), High Vin (60V)	● For the first 4 hours , running at full load condition. ● For the last hour, run Vin cycling and load sweep as shown in Figure-4. Power cycle the system at the end.
Duration: 20 - 23 hr Temperature cycling High Vin (60V), Full load	● Ramp up temperature from 0C to 55C at 10 C/min. ● Stay at 55 C for 10 mins. ● Then ramp down from 55 C to 0C at 10 C/min. ● Stay at 0C for 10 mins.
Duration: 23 - 24 hr ON/OFF cycling High Temperature (55C), High Vin (60V), Full load	● Repetitive ON/OFF the system with remote EN signal.



Voltage Cycling & Load Transient Profile

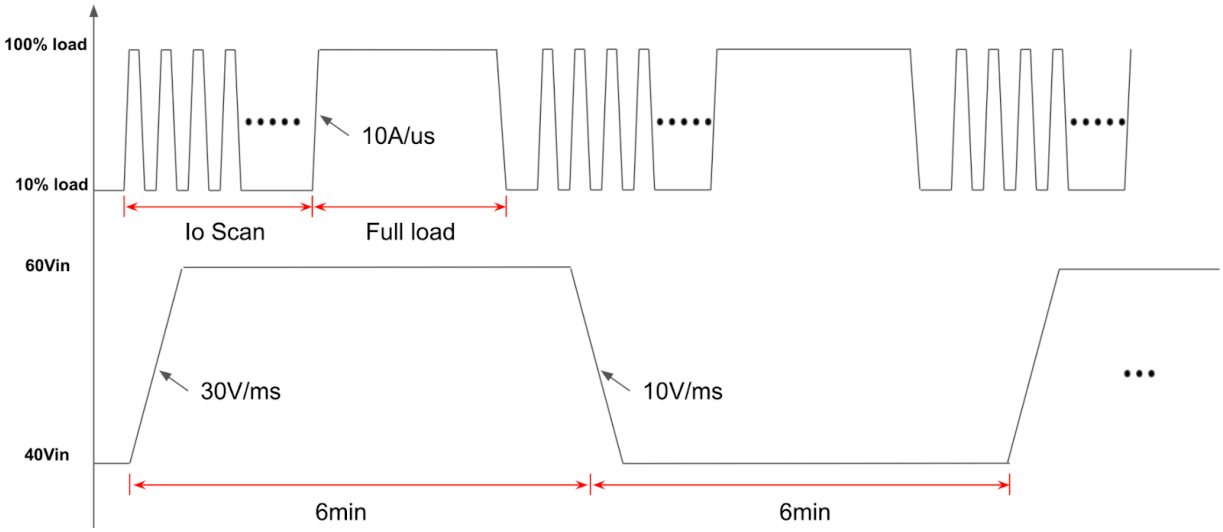


Figure-4 Chamber qualification profile

Pass/Fail Criteria

No functionality failures, parameter drift (e.g. Vout).
No efficiency degradation and no telemetry reporting drift

8. Manufacturing burn-in test

A 100% burn-in must be conducted for products where 100% HASS is not done, thereby screening out infant mortality parts which are susceptible to early life cycle failure.
In the burn-in MFG test, the power system Vout OV/UV are temporarily set with a narrower band. Any defective part that may cause unusual voltage excursions will trigger UV/OV warning or protection. By doing so, defective parts would be screened out.
Another method is to establish the Maverick lot methodology without need to change the values.
The burn-in process typically starts with a duration of 24 hours, with a decision process to reduce the burn-in time when no failures occur after a set number of hours.
Standard IPC-9592B or later version gives plans for reduction of burn-in times given observed failure rates over a set number of unit-hours. Product specific requirements may exceed the IPC-9592B (Appendix E Option 1) or later requirements as illustrated in the following example.

Burn-in load condition: Adjustable on-time duration to avoid contact pins damage or trigger OTP. Load should be enough to maintain the maximum rated temperature based on the given airflow in the burn-in chamber.

Interval	Duration (Hours)	Temperature (°C)	Load (A)	Vin (Voltage)	Minimum Quantity
Initial	24	55	95%	Nominal	2,500
1	12	55	95%	Nominal	5,000
2	6	55	95%	Nominal	7,500
3	4	55	95%	Nominal	10,000
Exit Criterion: <1000 DPPM yield rate, failure root cause has been identified and fixed					

Note: Review the number of units to make sure in each time the total Unit-Hours is the same

For products with reliability above 1 million Hrs MTBF is recommended to determine the number of units and minimum test time no less than 4 hours. Use CHISQR distribution and the expected MTBF data to determine the number of units.

Enhanced burn-in profile (Optional)
Vin 30V/ms ramp up and 10V/ms ramp down.
Vin sweep with load shmoo.

9. Reliability test

Item	Test Name	Conditions	Standard	Sample size per Lot	No. of Assembly Lot	Pass/fail criteria
Accelerated Life Test						
1	High Temp Operating Bias	V_stress = highest rated V and lowest rated V, Full Load, Maximum junction temperature. OTP is not triggered during the test. Read point = 250 hrs, 500 hrs, 750 hrs and 1000 hrs	IPC 9592 5.2.5	30	1	No failure at ATE test
2	ELFR	V_stress = highest rated V Maximum junction temperature. Enable cycling (1 sec off) 100 cycles (under 1mF o/p cap) Read point = 48 hrs	JESD-22-A 108	Minimum quantity is 77, or more to support MTBF requirement	3	To demonstrate ELF < 0.3% for the first 6 months of operation
3	ELFR ORT	For ORT, sample and time to be defined by the expected reliability (MTBF) and use CHiSQR distribution for the calculations Read point = 2 weeks to 4 weeks	JESD-22-A 108	Depending on expected Reliability and calculations with CHISQR distribution	1	To demonstrate ELF < 0.1% for the first 6 months of operation at the 8th month and forward
Compliance						
4	Latch up	Tj at 25°C and Tj.max	JESD78	3	1	No failure at ATE test
5	ESD Human Body Model HBM	Class 2, >2kV	JS-001-2012 or Latest version	3	1	No failure at ATE test
6	ESD Charged Device Model	Class 2, >250V	JESD22-C 101-E or	3	1	No failure at ATE test

	CDM		Latest version			
Accelerated Environmental Stress Test						
7	MSL Preconditioning	Moisture Sensitivity Level based on product specification and in compliance with the IPC 9592 standards for reflow, storage, and baking requirements.	IPC 9592 5.2.2.1	144	1	No failure at ATE test
8	Highly Accelerated Life Test (HALT) (STRIFE)	Low Temp Step Test x 3pcs High Temp Step Test x 3pcs Rapid Thermal Cycling x 3pcs 6 DOF Random Vib.Test x 3pcs Input Voltage Test x 3pcs Output Load Test x 3pcs Combined Stresses Test x 3pcs	IPC 9592 5.2.3	21	1	Test to Fail
9	Temperature Cycling Test (TCT)	700 Cycles chamber temperature range of -40°C to 125°C. ATE test at 150c, 300c, 450c, 600c, 700c and 30 min dwell time, Note: dwell time starts when the assembly reaches thermal equilibrium, not chamber set point. Thermo-couple characterization for equilibrium time for loaded chamber. 15C/min. ramps	IPC 9592 5.2.6	30	1	No failure at ATE test
10	Temperature Humidity Bias (THB)	85°C, 85%RH. Vstress = highest rated V Output load = min load Test Duration = 1000 hrs, ATE tested every 250 hrs	IPC 9592 5.2.4	30	1	No failure at ATE test
11	High Temperature Storage (HTS)	125°C module, 1000hrs	JESD22-A 103D Condition A	3	1	No failure at ATE test
12	Power & Temperature Cycles	Vstress = highest rated V Output load = 50% of full load Total 3000 power cycles	IPC 9592 5.2.7	3	1	No failure at ATE test

Multi-Chip Module Specific Test						
13	Random Vibration (Operating & Non operating)	JESD22B103: Condition 1 (Peak acceleration 20G)	IPC 9592 5.2.9/10	3	1	Pre/Post test should have no failure at ATE
14	Mechanical Shock	JESD22B104: Condition A (Peak acceleration 50G)	IPC 9592 5.2.11 JEDEC JESD22-B 110	3	1	Pre/Post full functional
15	Board Level Reliability (Board level TC) (ATC)	0 to 100C, 1500 cycles, 10 min dwell time and total cycle time of 60 min	IPC 9592 5.2.14.3.			Pre/Post full functional
MTBF Demonstration						
16	DMTBF (goal > 0.05 %/year at min. 60 % CL)	Tjmax=125C and Tcase= 115C		Sample size defined by MTBF and time		Zero unresolved failures
Other						
17	Solderability Test	IPC-9592B, IPC/ECA J-STD-002 Test A (dip and look).		5	1	No failure at ATE test
18	Ongoing Reliability Test (ORT)	Fast dv/dt sweep - 30V/ms ramp up and 10V/ms ramp down Thermal cycling				Constant monitoring

Note: The standards quoted in the reliability test are compatible with the latest version and subject to later update version.

Appendix A - Acronyms

For the purposes of the OCP 48V workgroup specification, the following acronyms apply:

Acronym / Abbreviation	***Definition***
ATE	Automatic Test Equipment
CCM-DCM	Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM)
CHISQR	Chi-square statistical test for observed vs. expected data
DFMEA	Design Failure Mode and Effects Analysis
DMTBF	Demonstrated Mean Time Between Failures
ESD	Electrostatic Discharge
FET	Field-effect Transistor
IPC	Institute of Printed Circuits: Requirements for Power Conversion Devices for the Computer and Telecommunications Industries
JEDEC	Joint Electron Device Engineering Council: An industry group that develops open standards for Microelectronics. e.g. JESD78
MLCC	Multi-Layer Ceramic Capacitor
MTBF	Mean Time Between Failures
OC	Over Current
OCP	Overcurrent Protection
OV	Over Voltage
OVP	Over Voltage Protection
UVLO	Under Voltage Lock Out
UVP	Under Voltage Protection