

MOXLIE RISER

<5 SLOT>

VERSION: 3.0
STAGE: PVT2
DATE: 2018.07.26

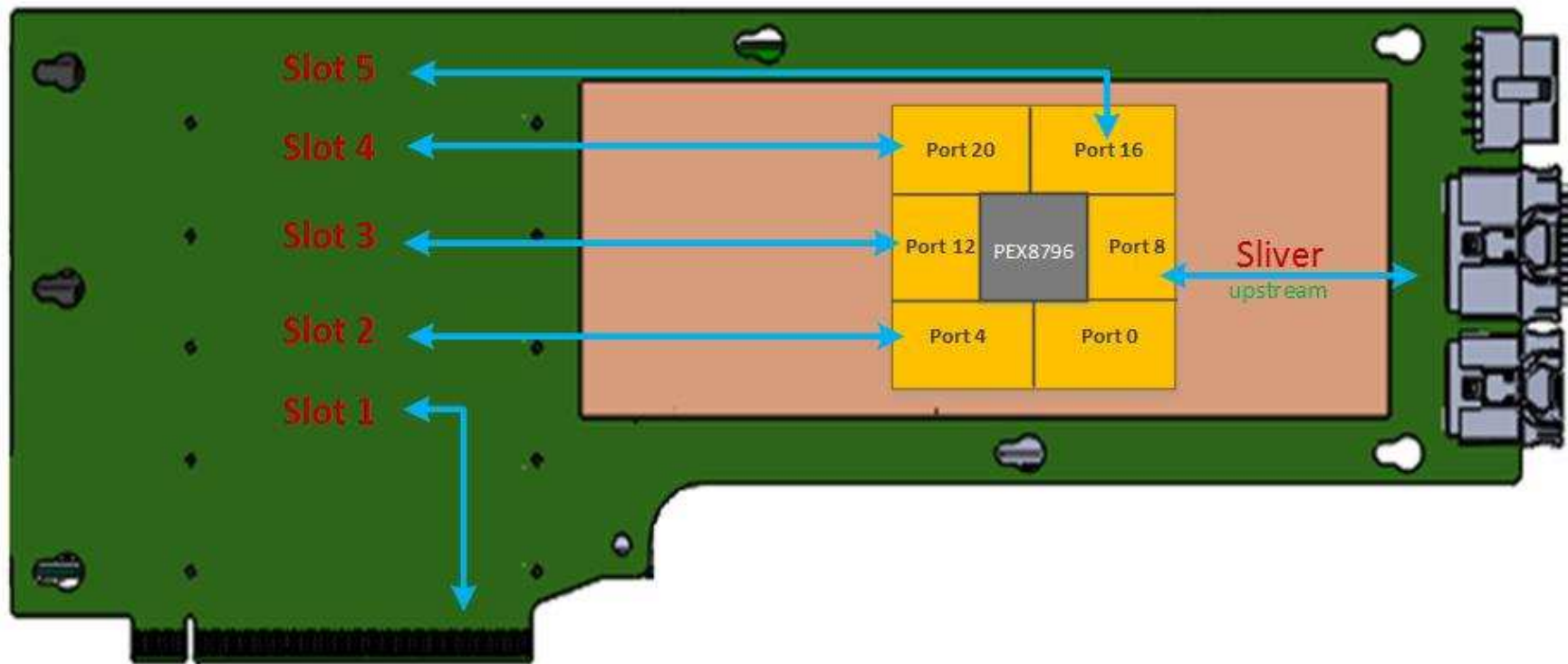


DEPARTMENT	DESIGNER	NAME	PROJECT		DOCUMENT NUMBER		REV
	REVIEWER	NAME	<ZT_PROJ>		<ZT_NUMBER>		<ZT_REV>
			SIZE	C	DATE	Thu Jul 26 13:46:44 2018	SHEET 1 OF 44

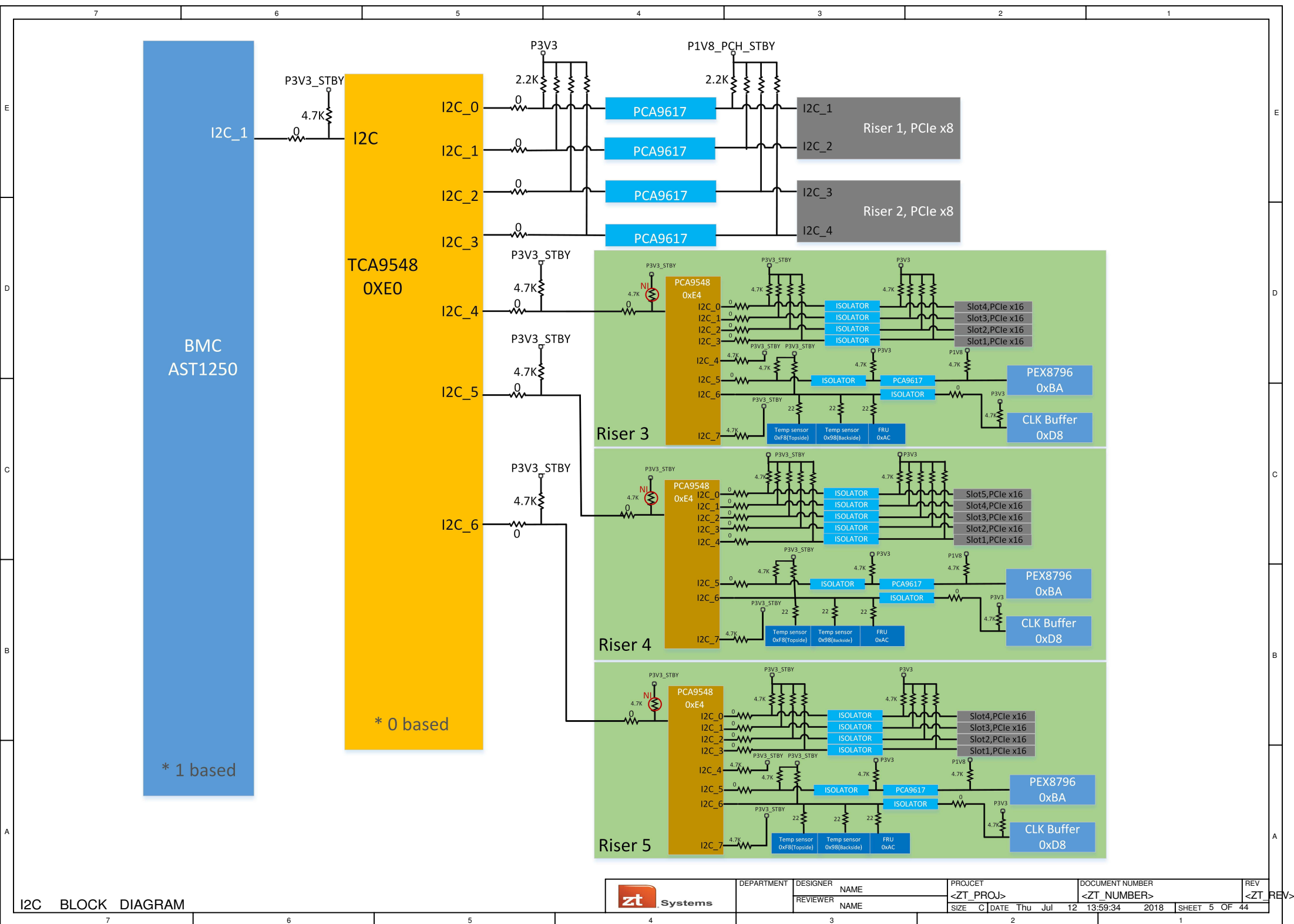
Dielectric and Copper Properties									
Layer			Copper		Dielectric Material			Layer	
Name	Description	Type	Weight	Type	Type	Er	Df	Design Thickness (mil)	Actual Thickness (mil)
Top_SM	Top Soldermask	Soldermask			Soldermask	3.5	0.030	0.50	
L1top	Signal_L1top	Signal	0.5 oz. plated	STD				1.90	
PP_L1top_L2	Prepreg	PP			Material 1	3.6	0.009	2.70	
L2	GND_L2	GND	1.0 oz.	RTF				0.65	
Core_L2_L3	Core	Core			Material 2	3.6	0.009	3.00	
L3	Signal_L3	Signal	1.0 oz.	RTF				0.65	
PP_L3_L4	Prepreg	PP			Material x	3.6	0.009	5.50	
L4	GND_L4	GND	1.0 oz.	RTF				0.65	
Core_L4_L5	Core	Core			Material y	3.6	0.009	3.00	
L5	Signal_L5	Signal	1.0 oz.	RTF				0.65	
PP_L5_L6	Prepreg	PP			Material y	3.6	0.009	9.50	
L6	PWR_L6	PWR	1.0 oz.	RTF				1.30	
Core_L6_L7	Core	Core			Material 2	3.8	0.009	4.00	
L7	PWR_L7	PWR	1.0 oz.	RTF				1.30	
PP_L7_L8	Prepreg	PP			Material y	3.6	0.009	9.50	
L8	Signal_L8	Signal	1.0 oz.	RTF				0.65	
Core_L8_L9	Core	Core			Material y	3.6	0.009	3.00	
L9	GND_L9	GND	1.0 oz.	RTF				0.65	
PP_L9_L10	Prepreg	PP			Material x	3.6	0.009	5.50	
L10	Signal_L10	Signal	1.0 oz.	RTF				0.65	
Core_L10_L11	Core	Core			Material 2	3.6	0.009	3.00	
L11	GND_L11	GND	1.0 oz.	RTF				0.65	
PP_L11_L12bot	Prepreg	PP			Material 1	3.6	0.009	2.70	
L12bot	Signal_L12bot	Signal	0.5 oz. plated	STD				1.90	
Bot_SM	Bot Soldermask	Soldermask			Soldermask	3.5	0.030	0.50	

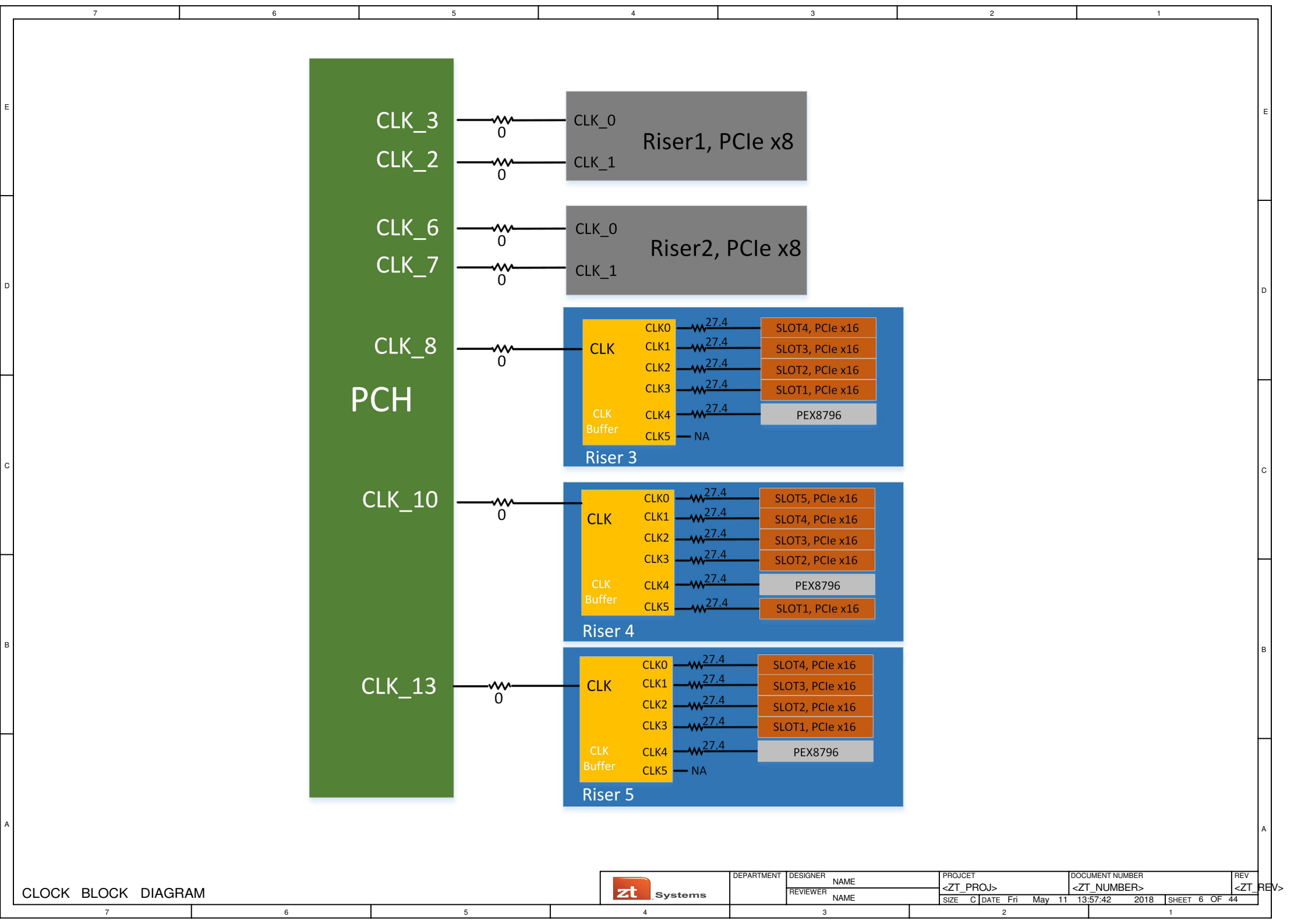
with soldermask, total thickness: 64.0 0.0
without soldermask, total thickness: 63.0 0.0

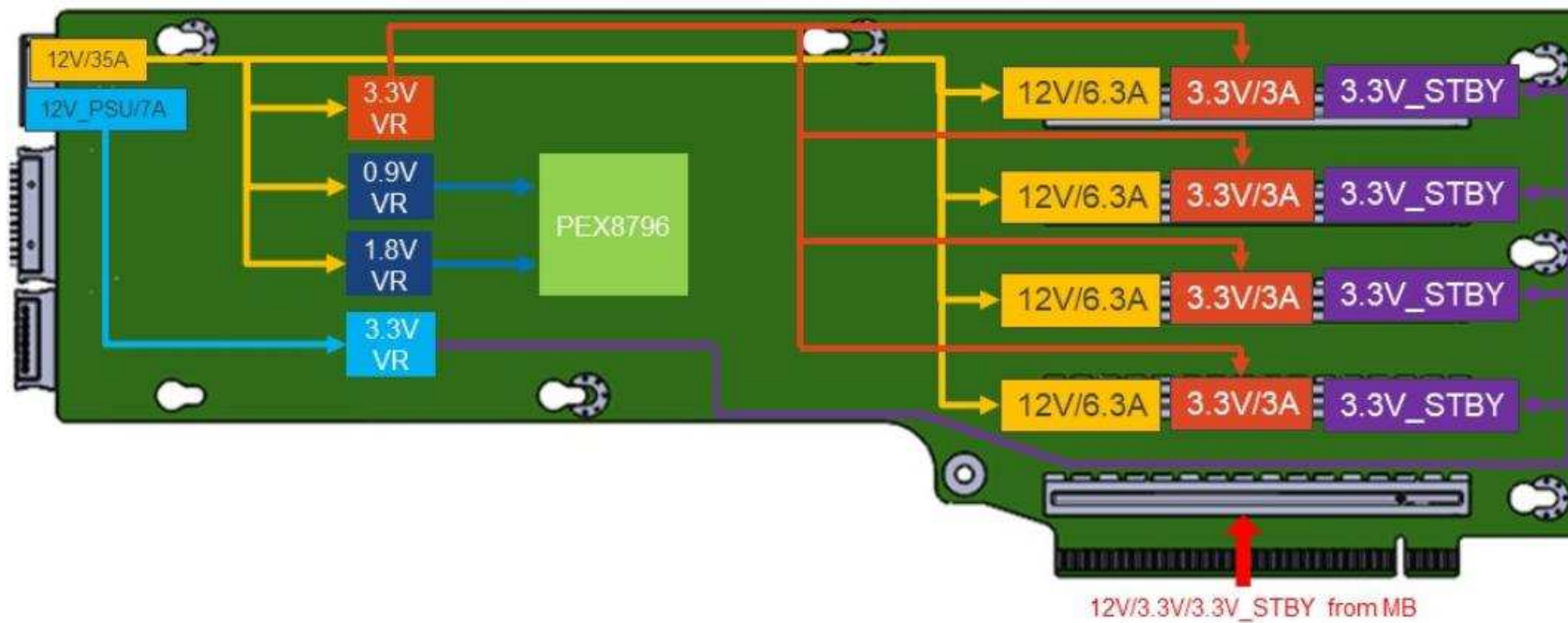


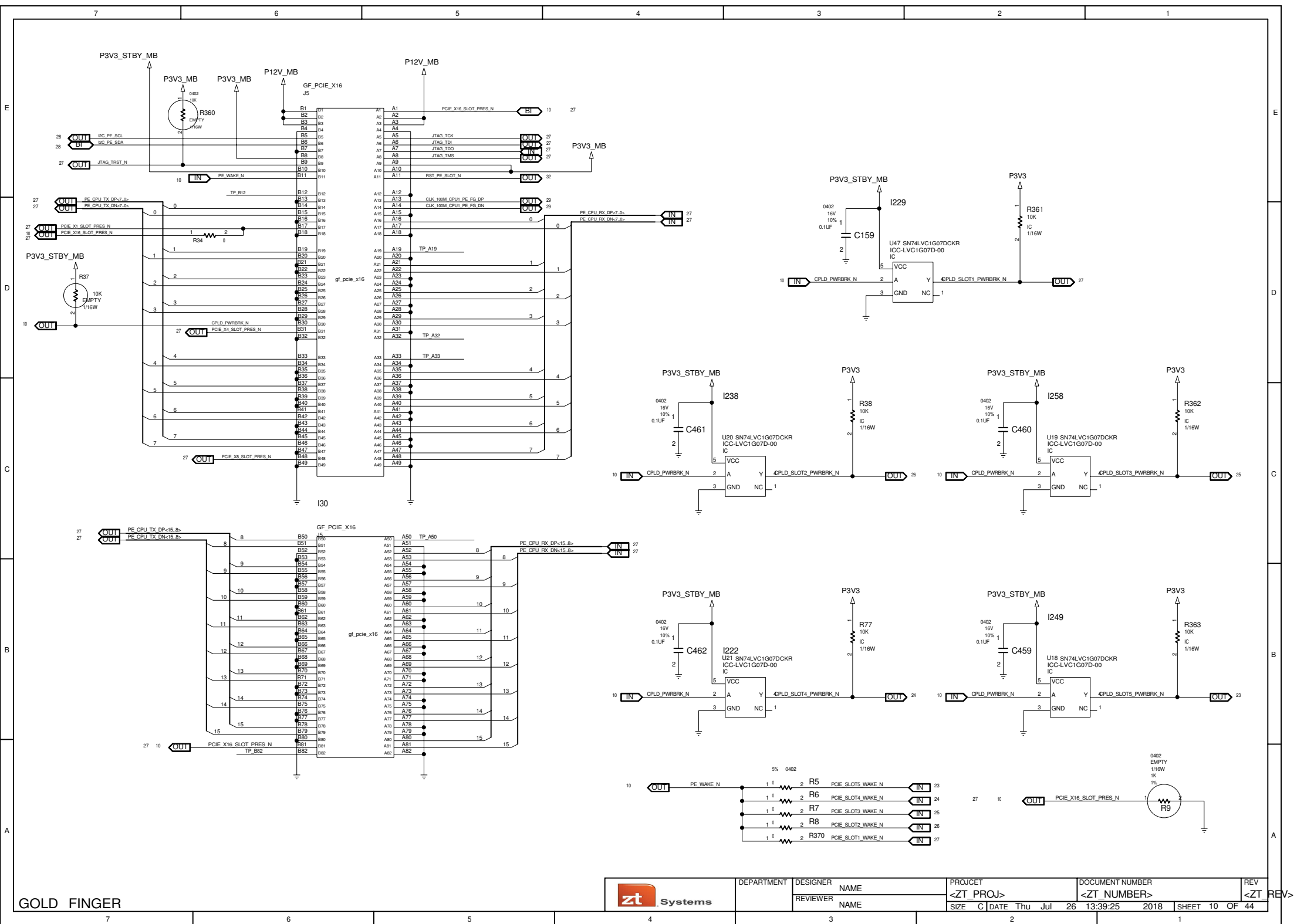


PEX8796	PORTS	SLOTS	NUMBER
PORT	0		
PORT	4	SLOT	2
PORT	8	UPSTREAM(FROM	SLIVER CONN)
PORT	12	SLOT	3
PORT	16	SLOT	5
PORT	20	SLOT	4



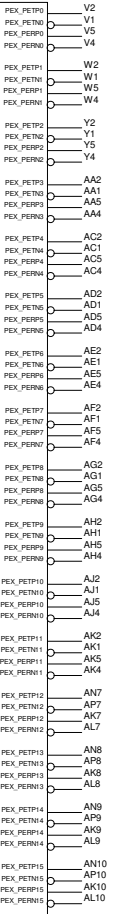
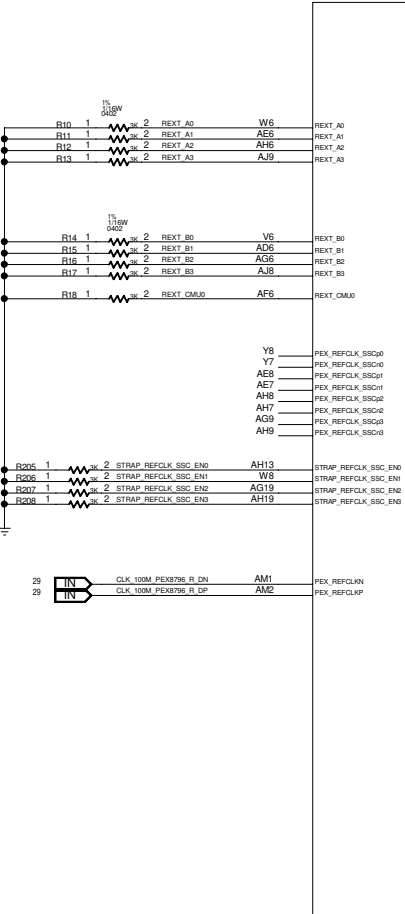






PEX8796 PORT 0(0~15)

I1
PEX8796-AB80BIG
U1
ICC-PEX8796A-00
IC



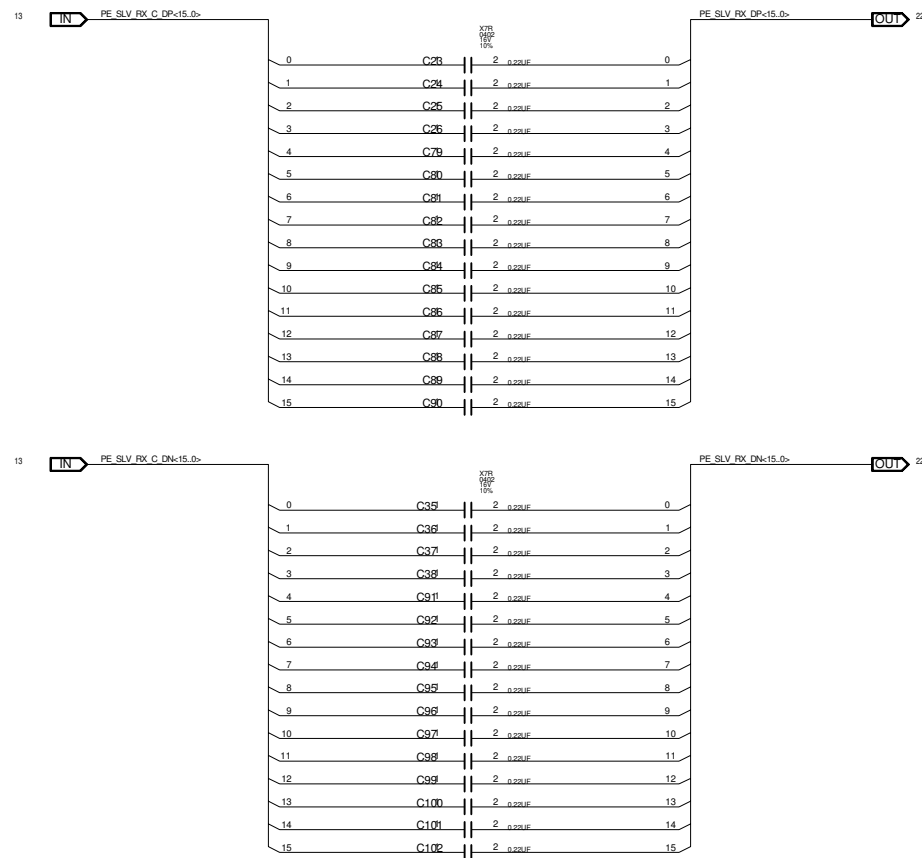
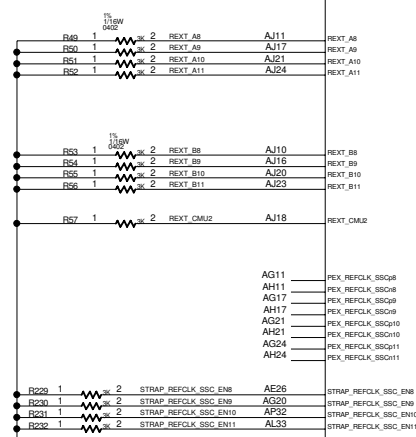


PEX8796 PORT 8(32~47)

U1
PEX8796-AB80BIG
ICC-PEX8796A-00
IC

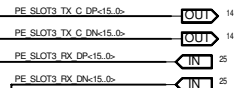
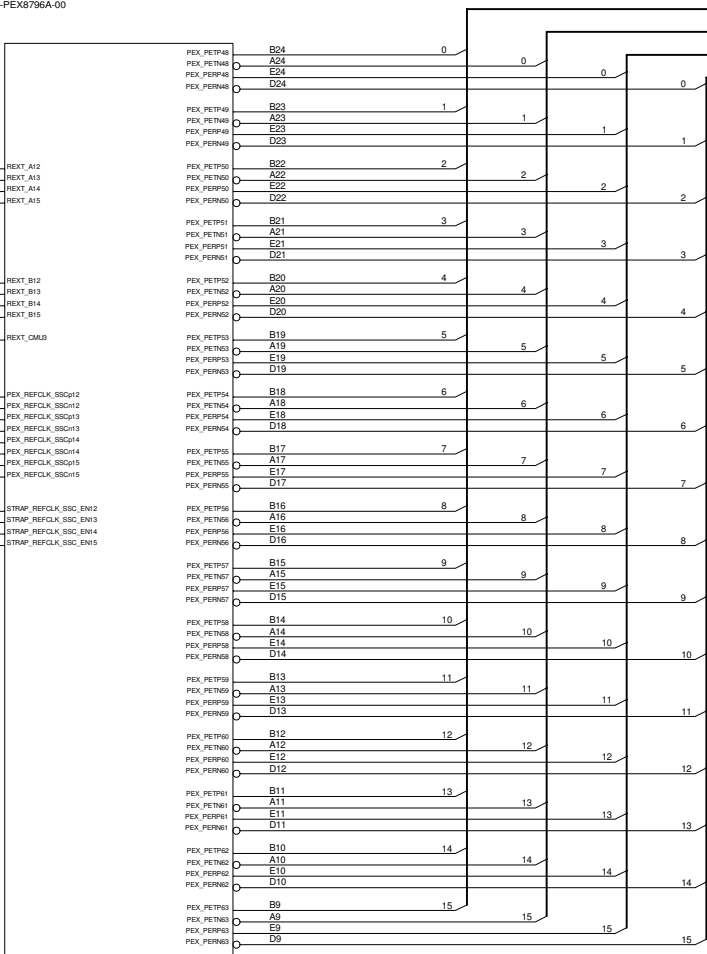
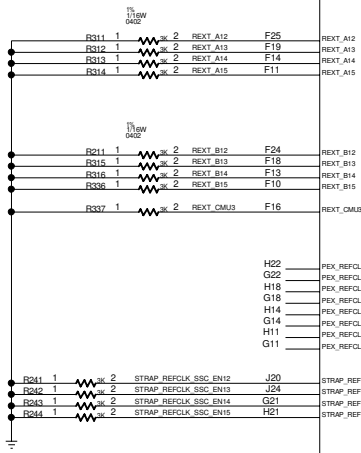
PE SLV RX C DP<15.0> 13
PE SLV RX C DN<15.0> 13
PE SLV TX DP<15.0> 22
PE SLV TX DN<15.0> 22

UPSTREAM
FROM SLIVER CONN

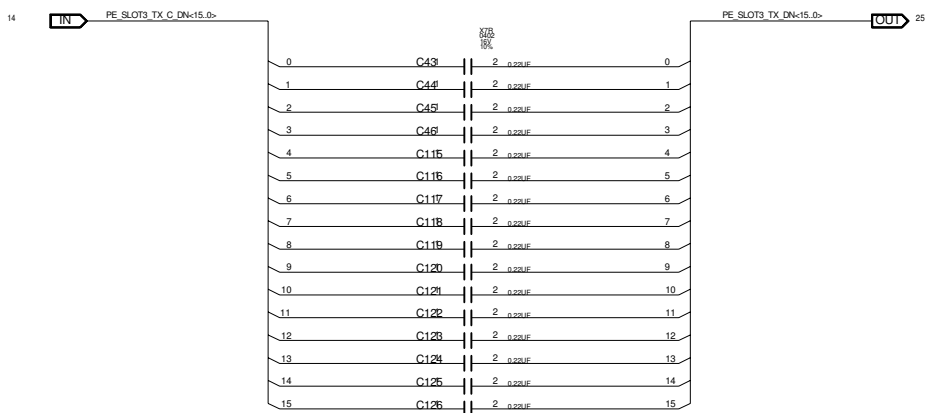
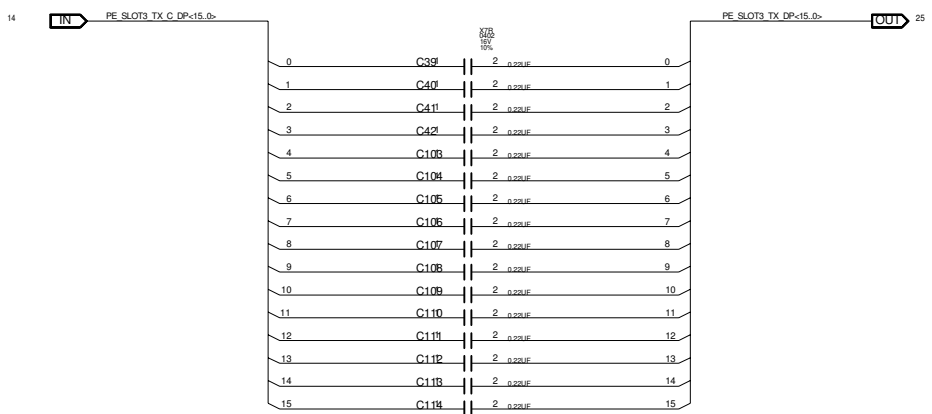


PEX8796 PORT 12(48~63)

U1
PEX8796-AB80BIG
ICC-PEX8796A-00
IC

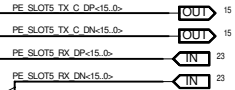
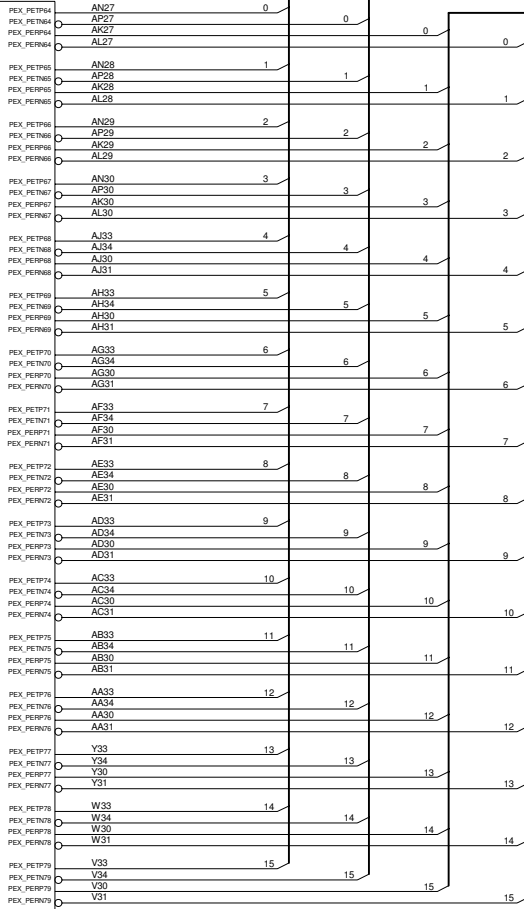
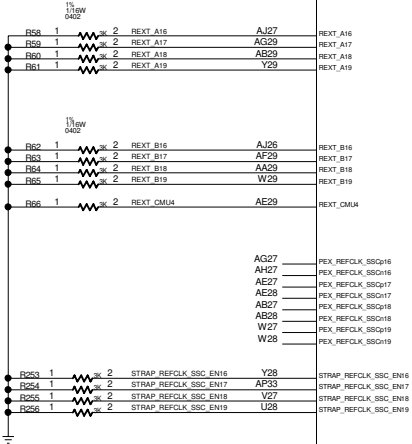


PCIE SLOT3(J3)

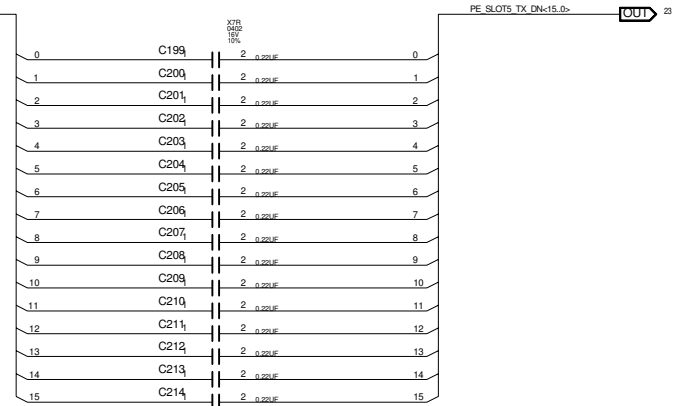
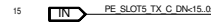
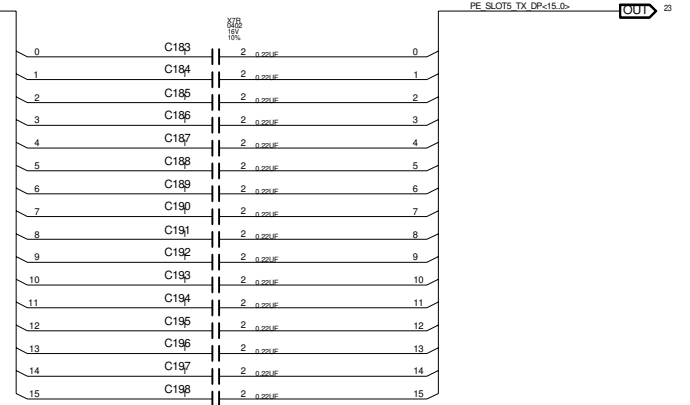


PEX8796 PORT 16(64~79)

U1
PEX8796-AB80BIG
ICC-PEX8796A-00
IC

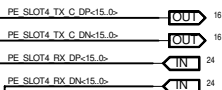
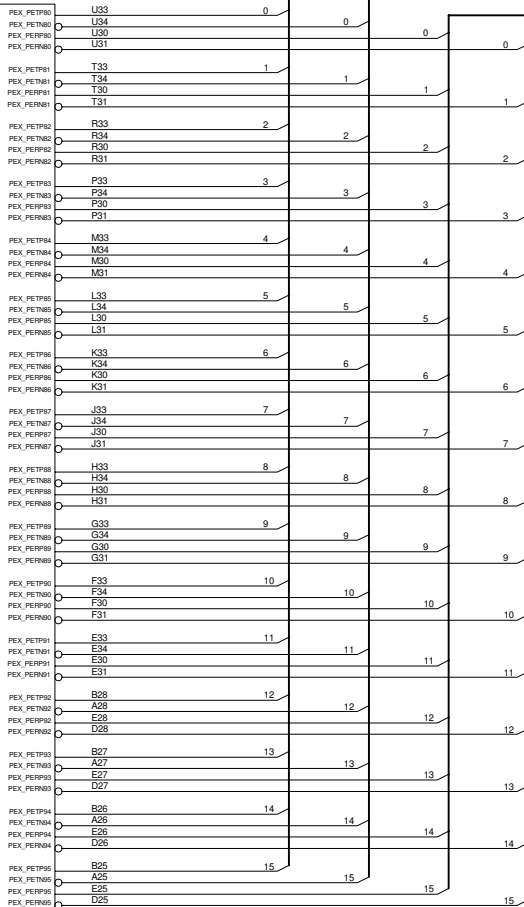
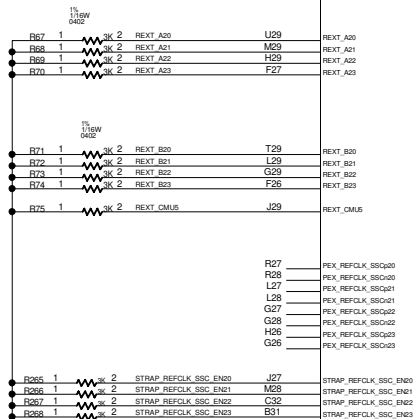


PCIE SLOT 5(J9)

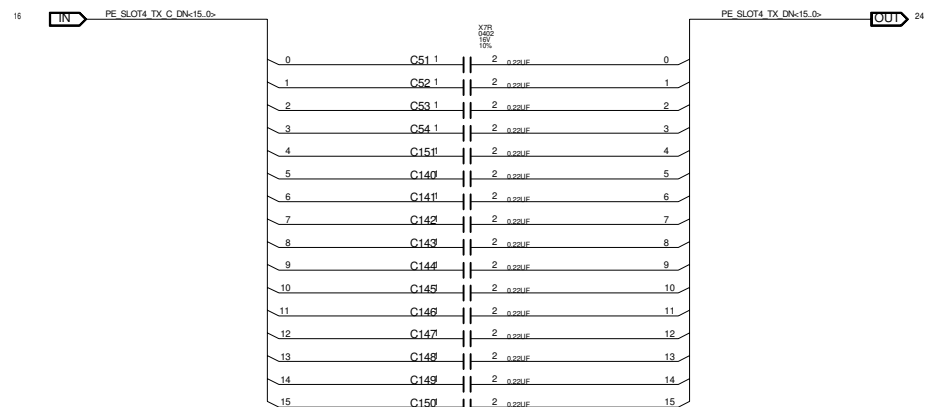
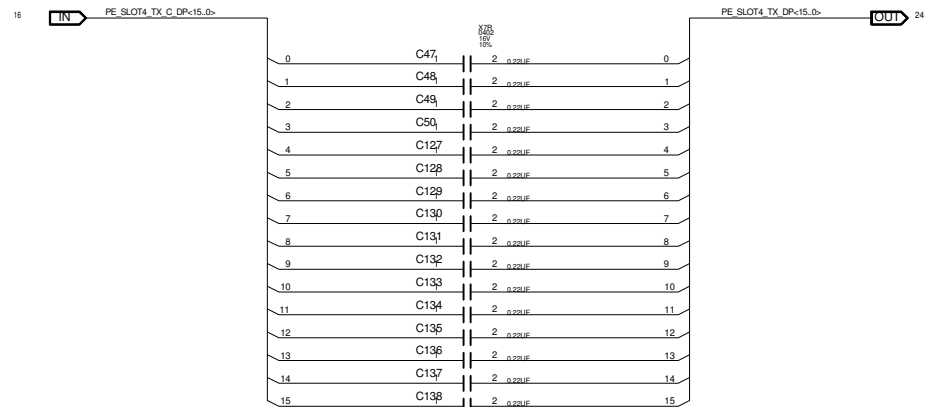


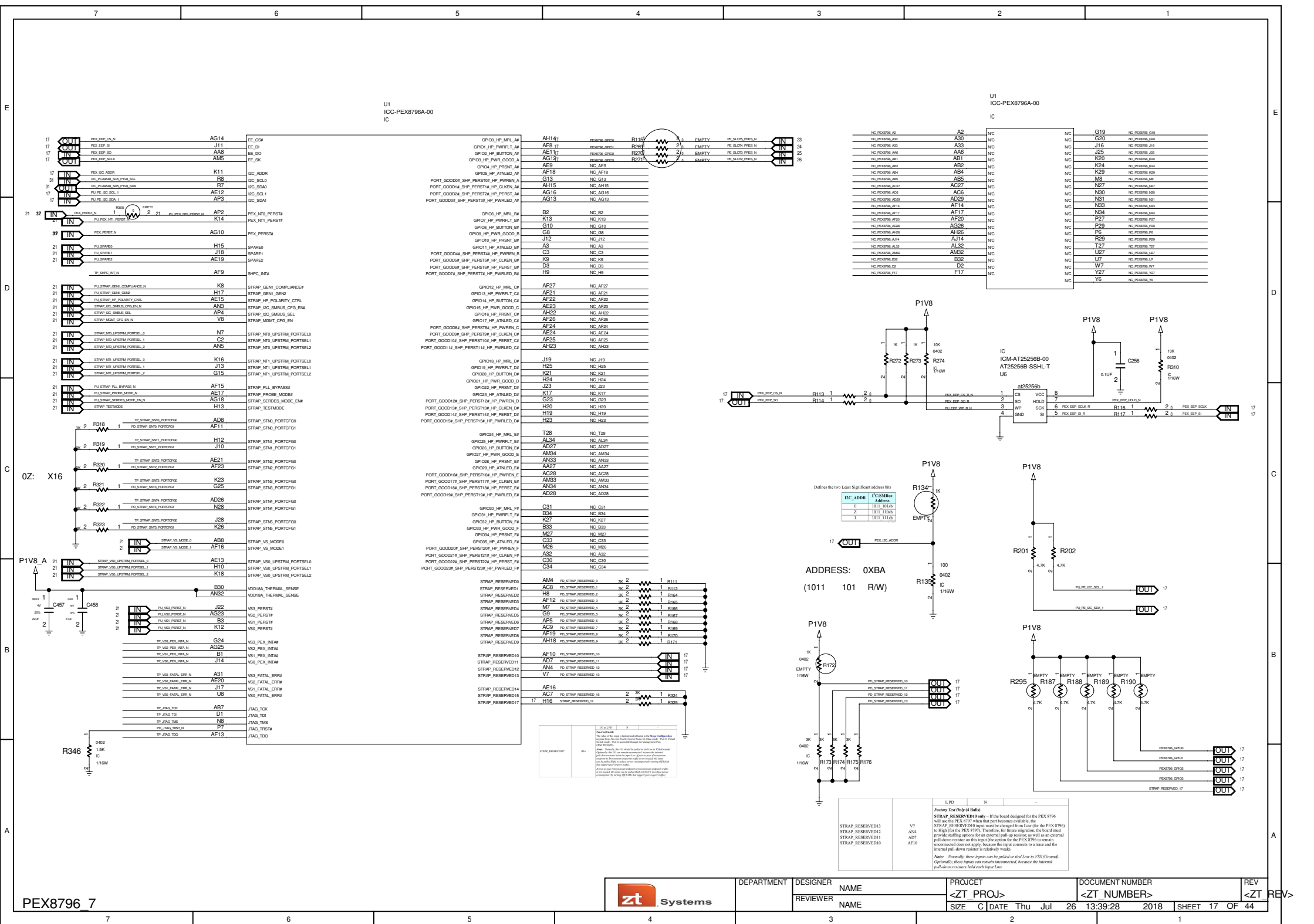
PEX8796 PORT 20(80~95)

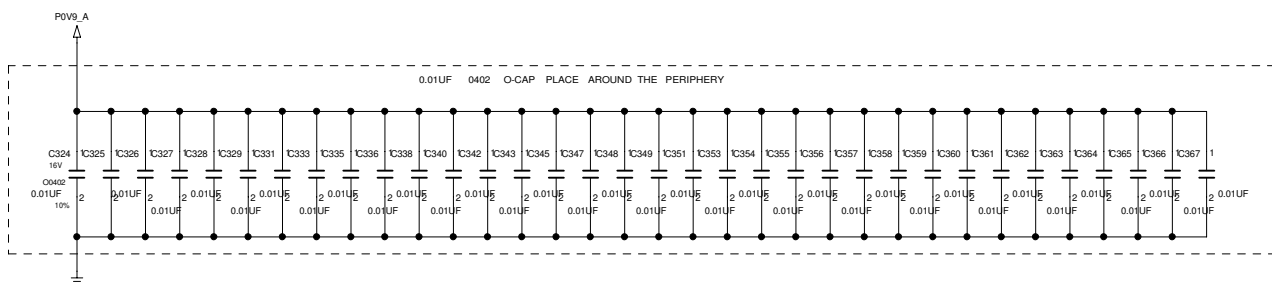
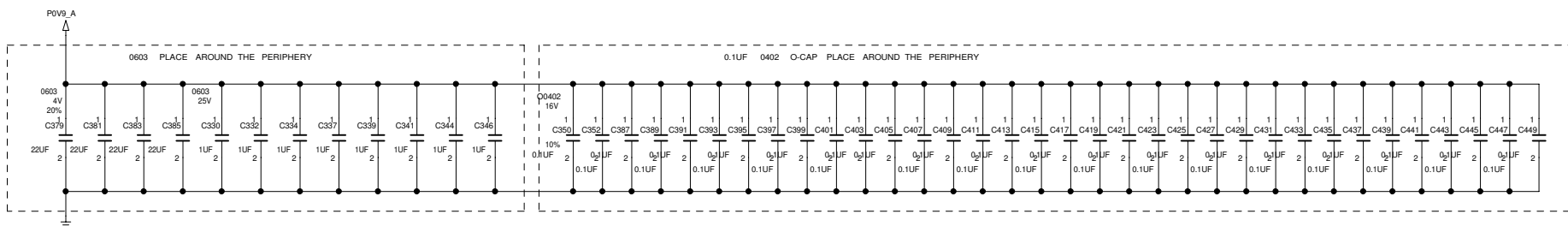
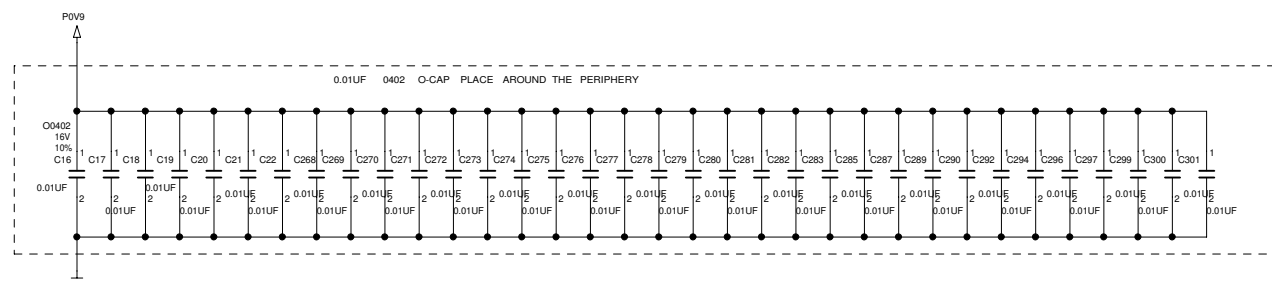
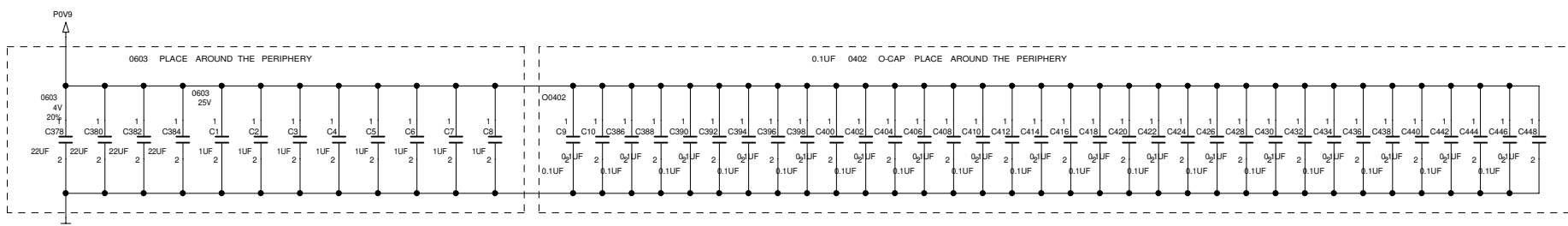
U1
ICC-PEX8796A-00
IC

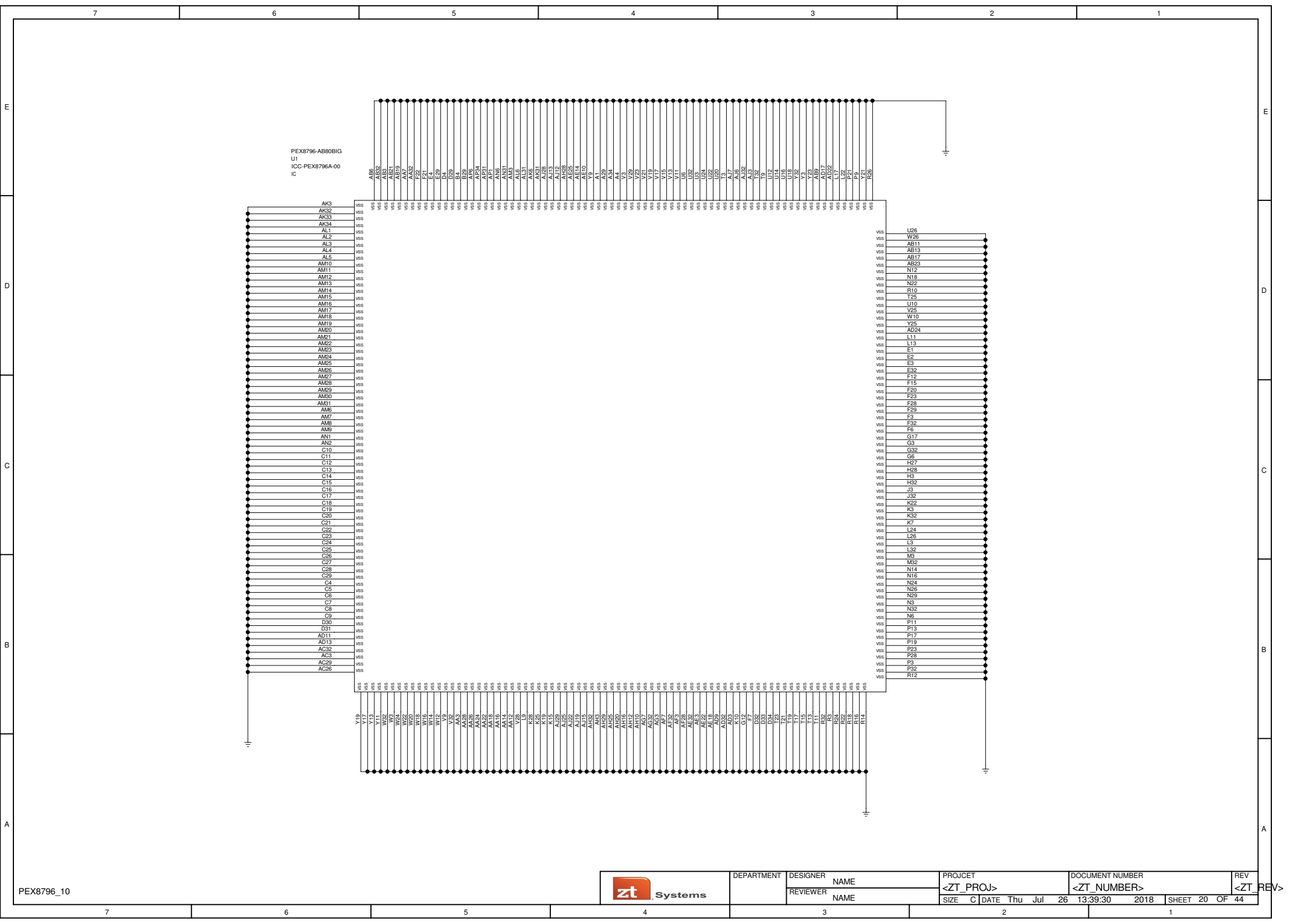


PCIE SLOT4(J4)

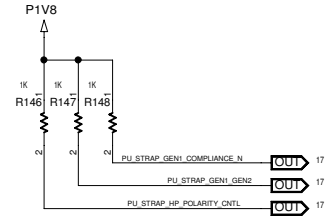
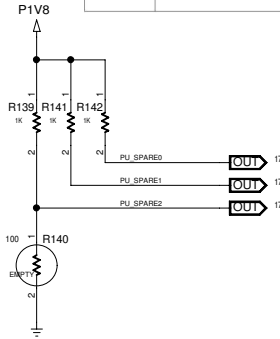
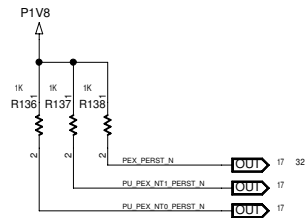
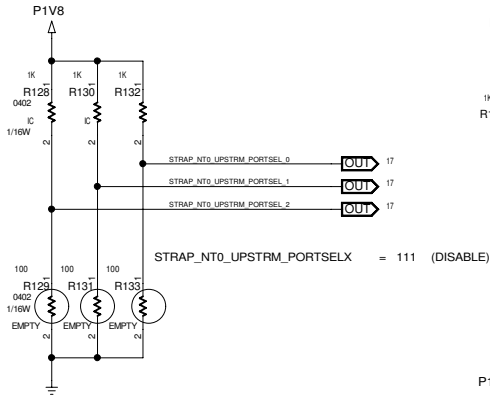




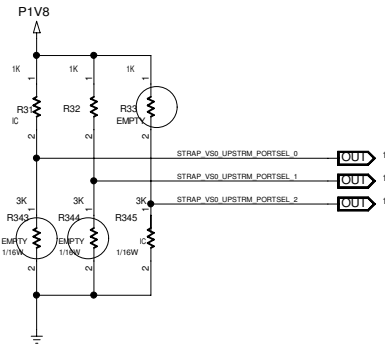
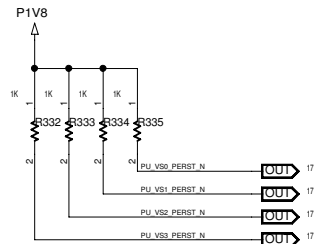




PEX_NT_PERST_N:
0= WRITING 0 CLEARS THE RESET CONDITION
1= CAUSES RESET

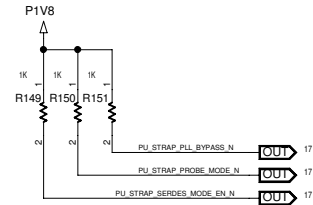


STRAP_VS0_UPSTRM_PORTSEL[2:0]=011(PORT8)



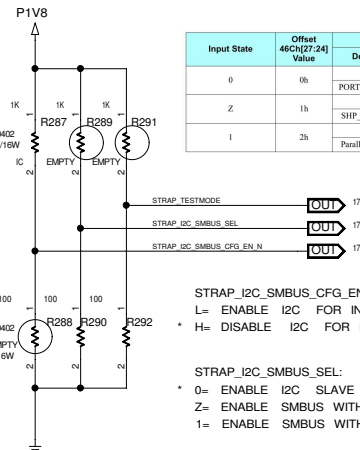
STRAP_I2C_SMBUS_SEL	Offsets 2Ch[9, 8]	Offsets 4Ch[6, 7]
0	0, 1	1, -
Z	1, 0	0, 0
1	1, 1	0, 1

0 = Enables I²C Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus
Z = Enables SMBus with Address Resolution Protocol (ARP), on the I2C_SCL0 and I2C_SDA0 2-wire bus
1 = Enables SMBus without ARP, on the I2C_SCL0 and I2C_SDA0 2-wire bus



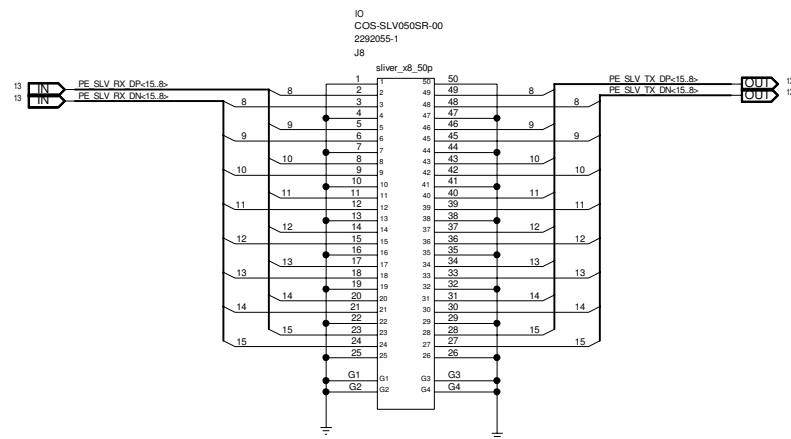
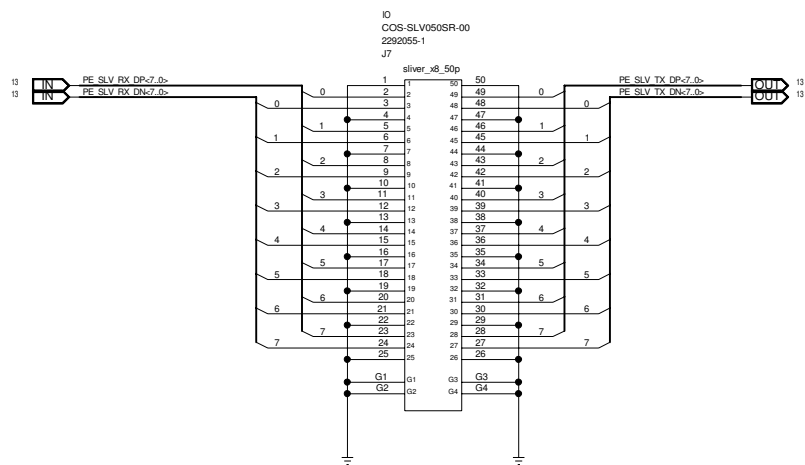
STRAP_PLL_BYPASS#	AF15	L, PU	No	-
STRAP_PROBE_MODE#	AE17	L, PU	No	-
STRAP_SERDES_MODE_IN#	AG18	L, PU	No	-

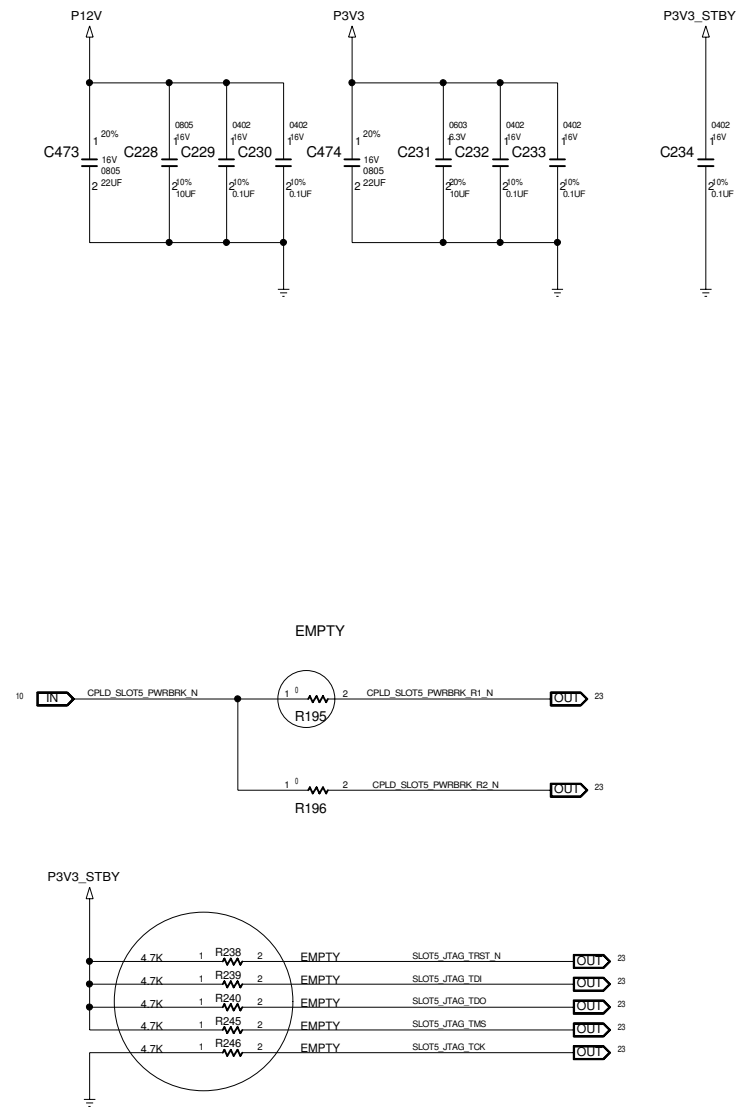
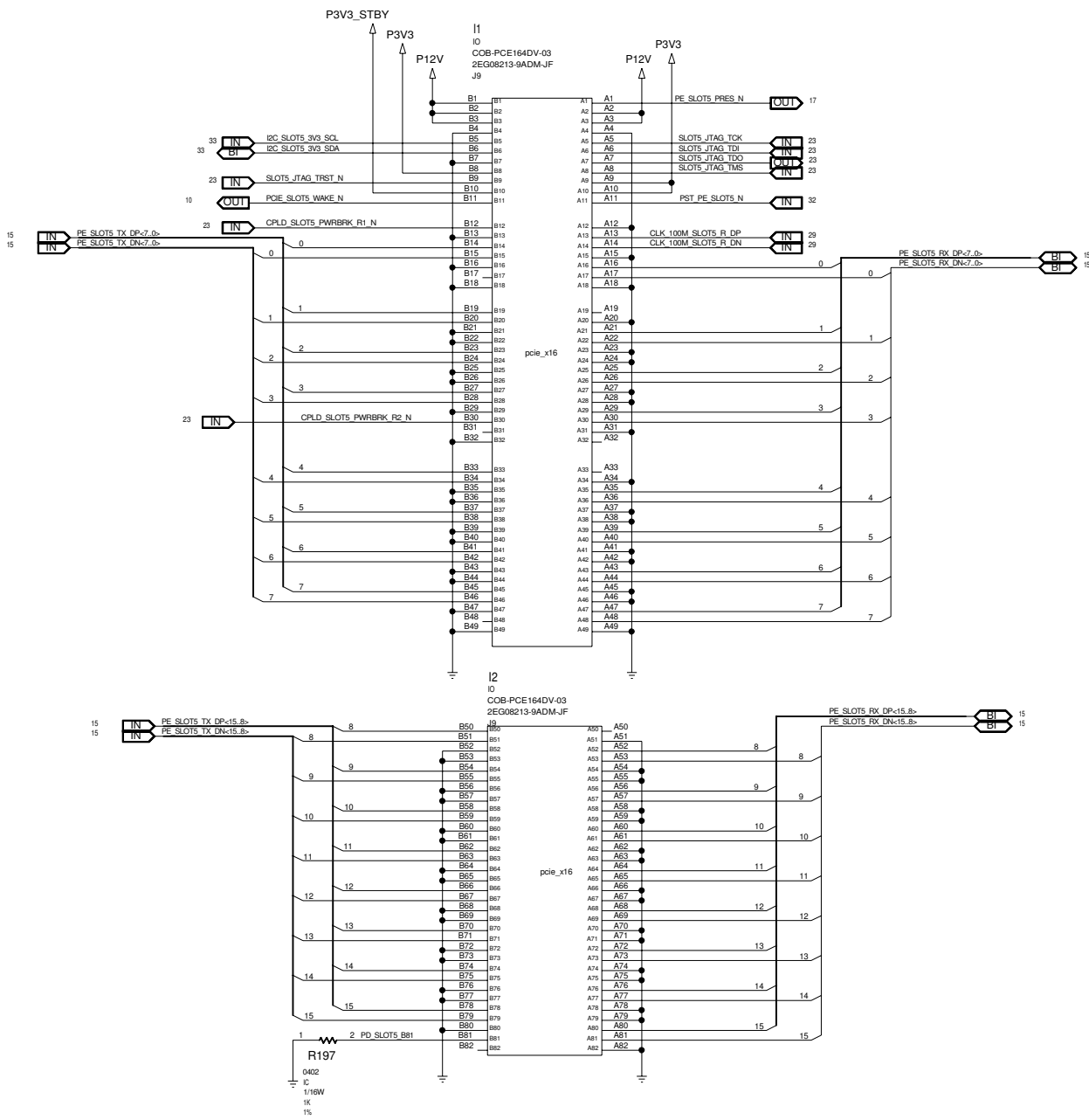
Input State	Offset 46Ch[27:24] Value	TESTMODE Default Functionality
0	0b	0 PORT_GOOD# = GPIOx input
Z	1b	1 SHF_PERST# = GPIOx input
1	2b	2 Parallel Hot Plug I/O (default)?

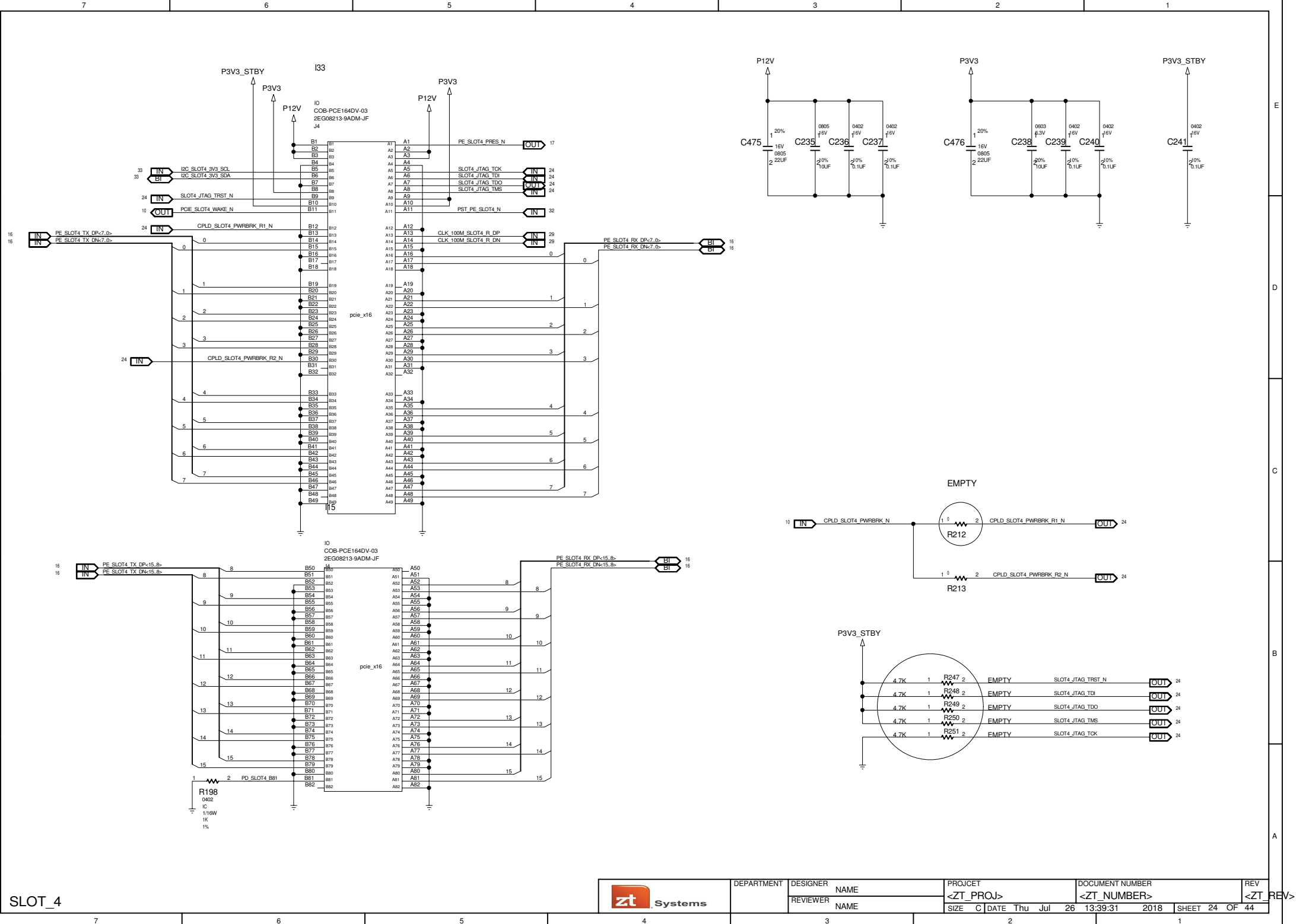


STRAP_I2C_SMBUS_CFG_EN#:
L= ENABLE I2C FOR INITIAL DEVICE CONFIGURATION
H= DISABLE I2C FOR INITIAL DEVICE CONFIGURATION

STRAP_I2C_SMBUS_SEL:
0= ENABLE I2C SLAVE PROTOCOL ON I2C_SCL0/SDA0
Z= ENABLE SMBUS WITH ADDRESS RESOLUTION PROTOCOL(ARP) ON I2C_SCL0/SDA0
1= ENABLE SMBUS WITHOUT ARP ON I2C_SCL0/SDA0



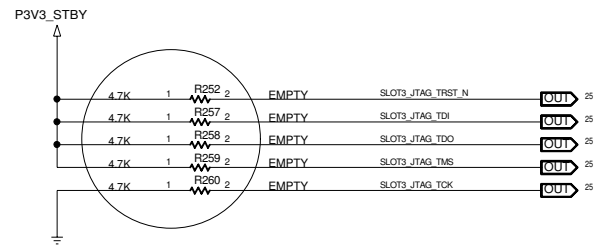
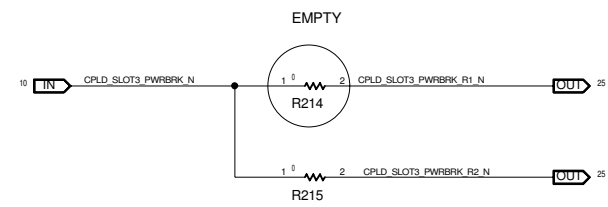
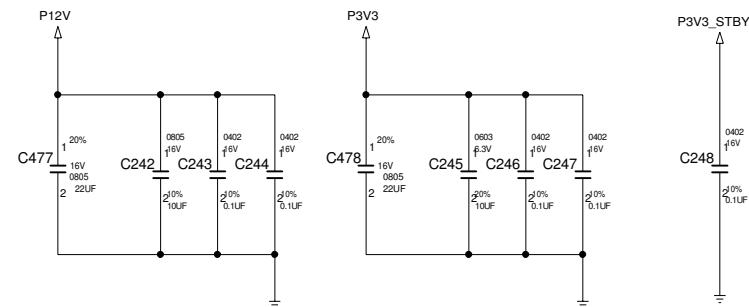
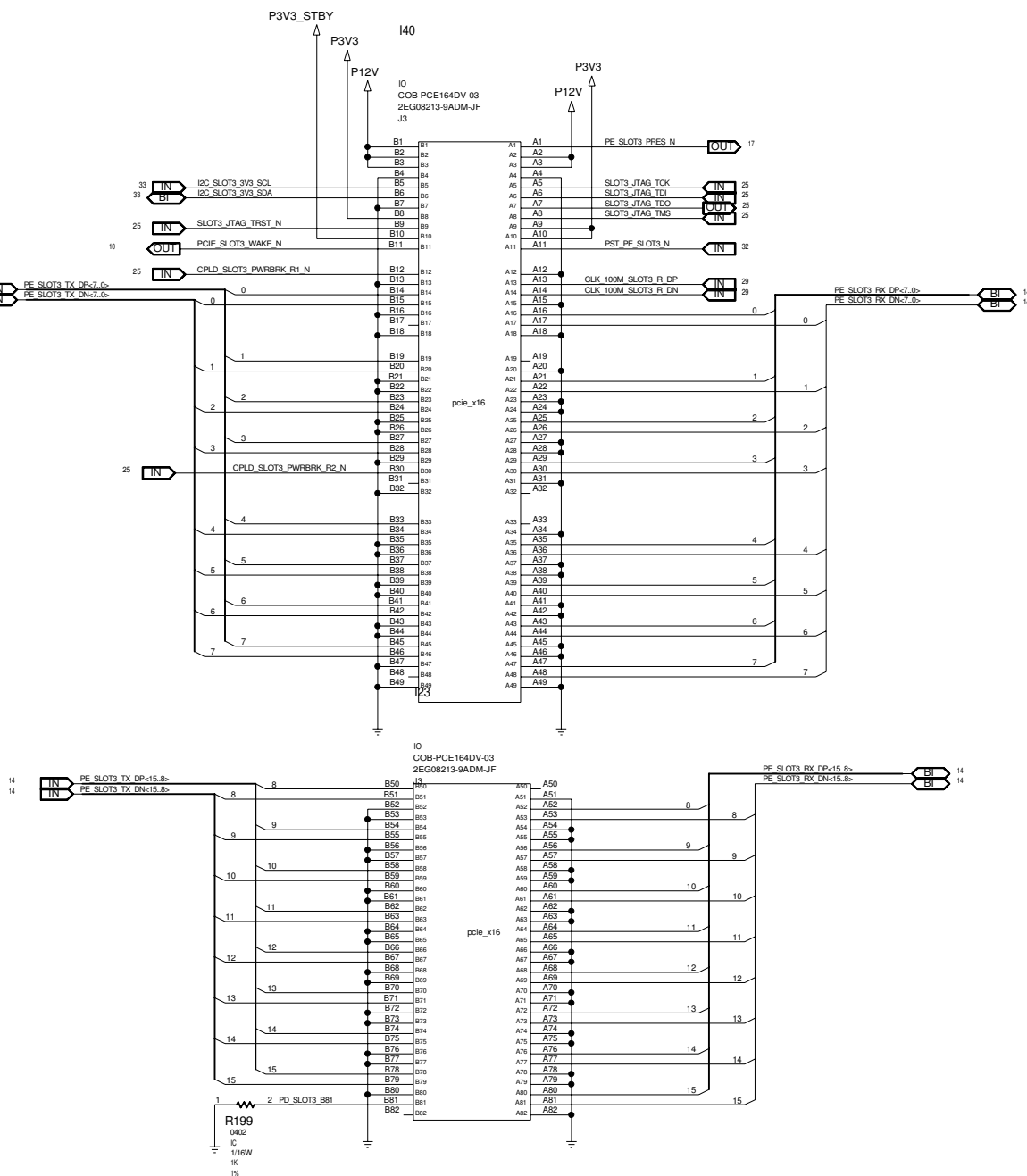


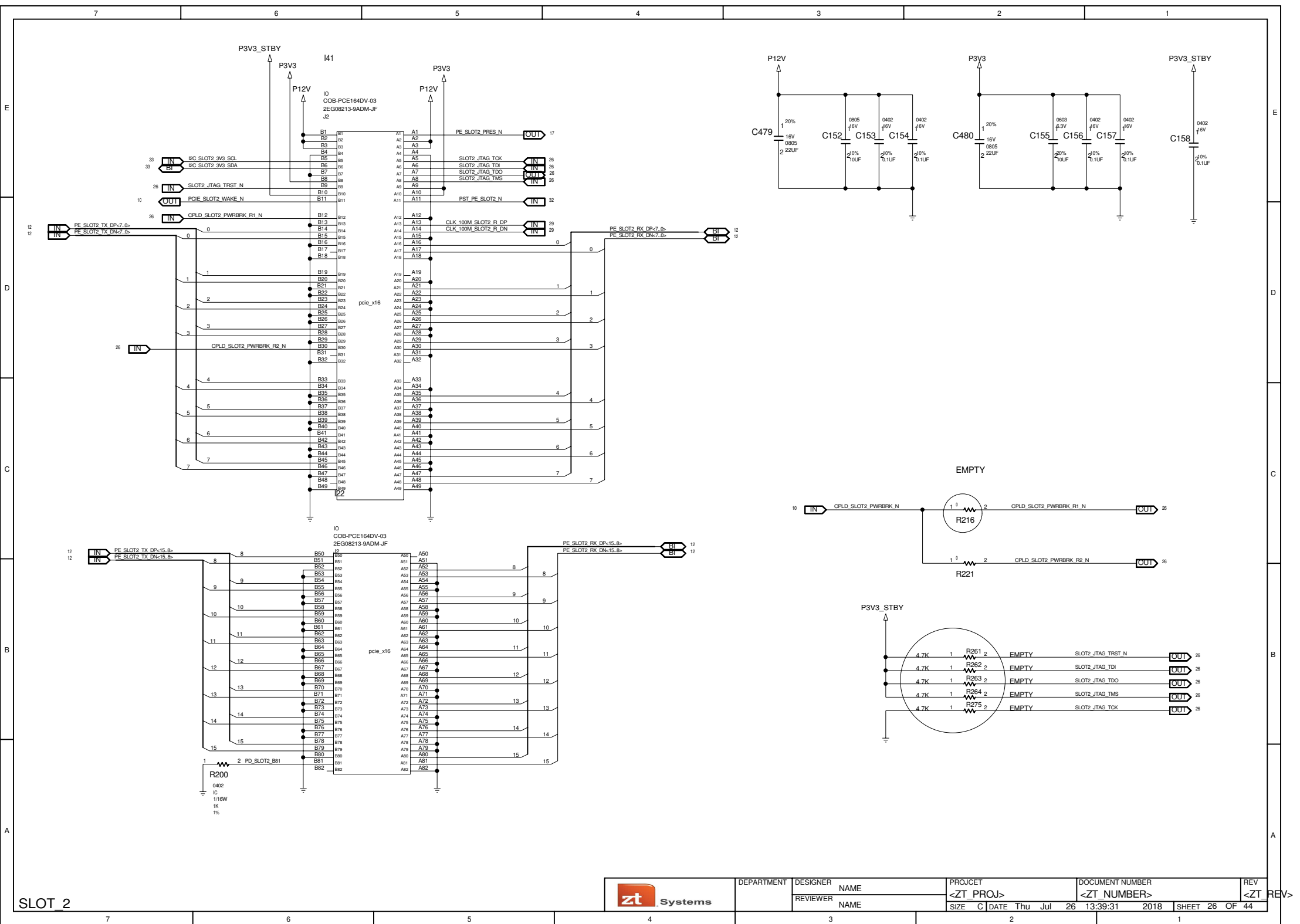


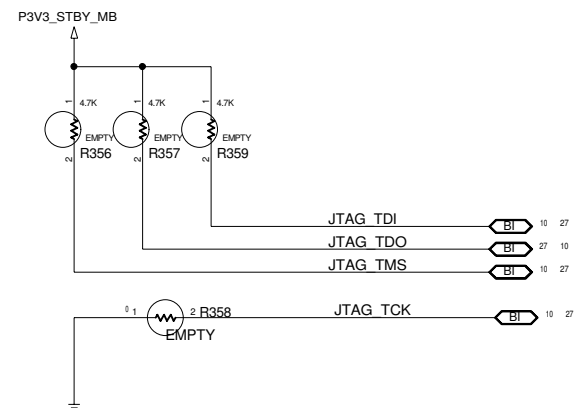
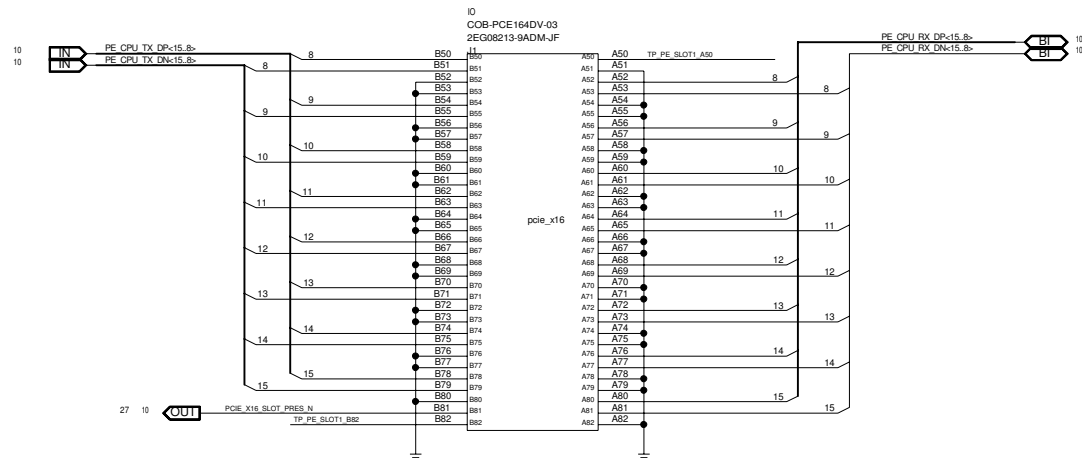
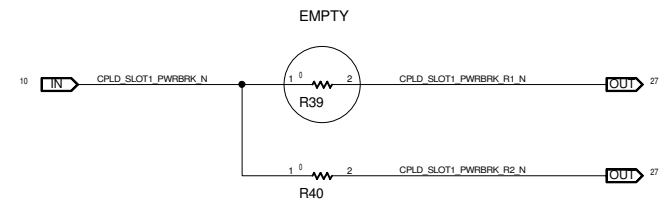
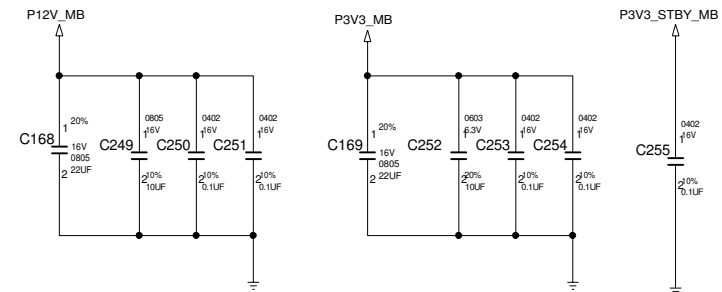
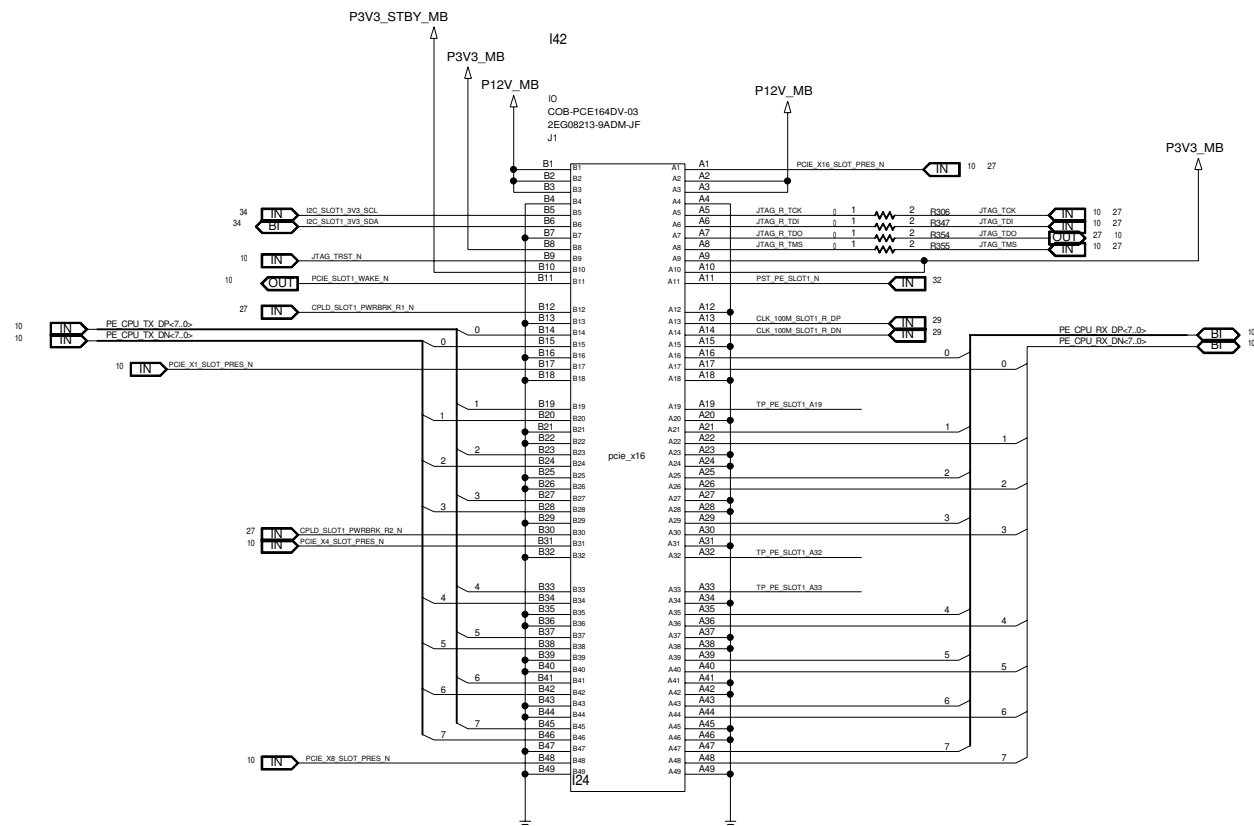
SLOT_4

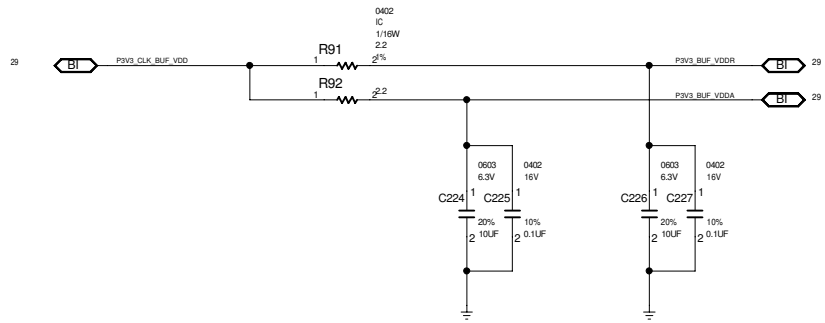


DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
	REVIEWER	NAME	<ZT_PROJ>	<ZT_NUMBER>	<ZT_REV>
SIZE	C	DATE	Thu Jul 26 13:39:31 2018	SHEET 24 OF 44	

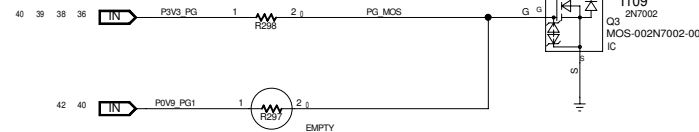


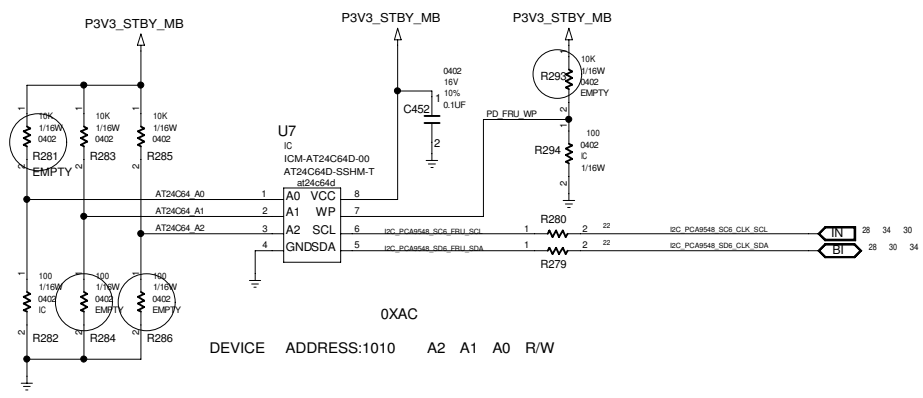
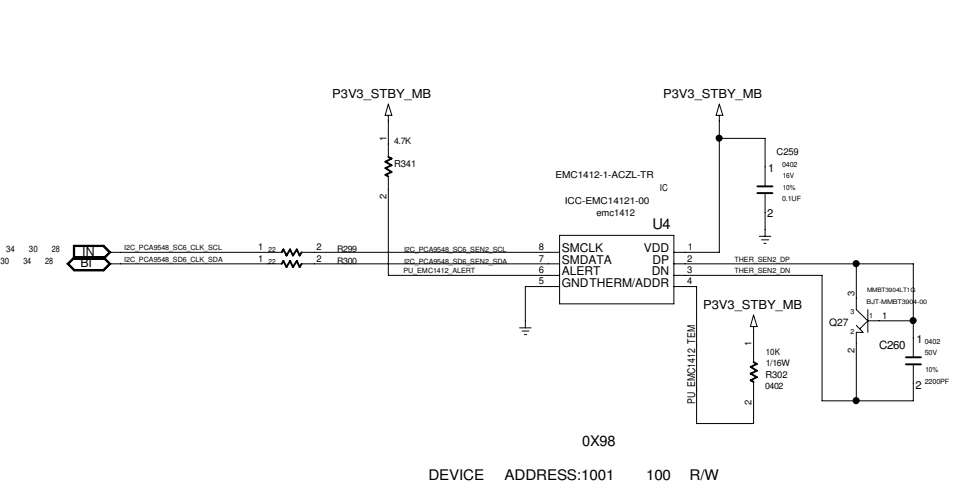
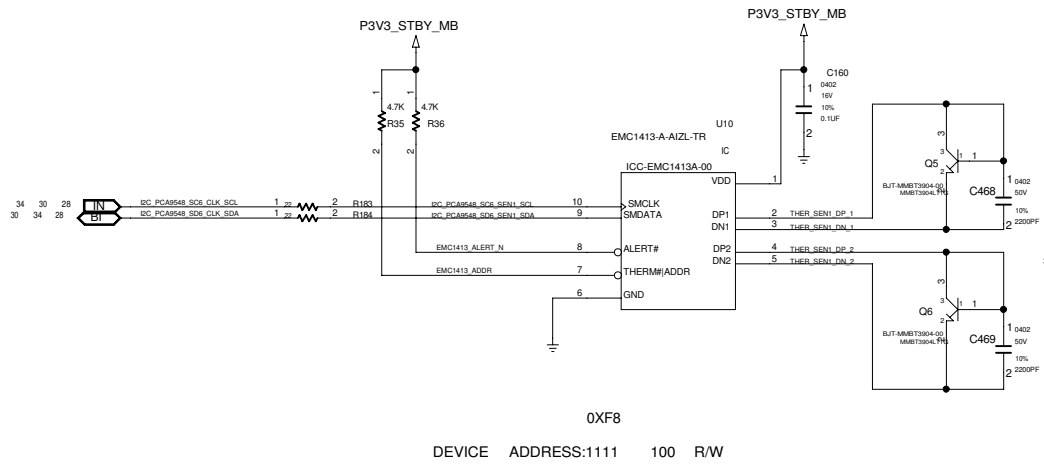


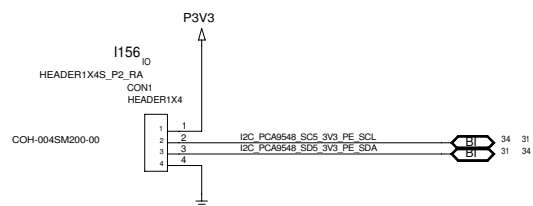
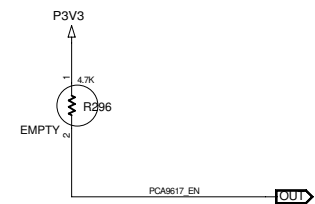
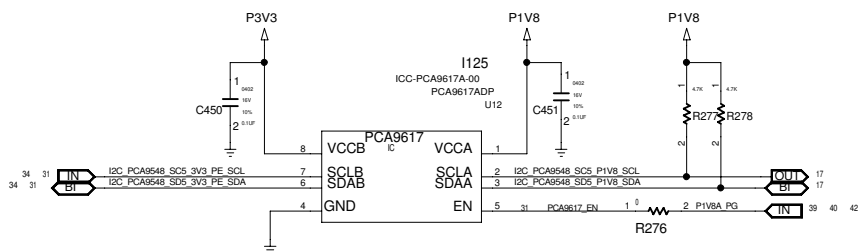


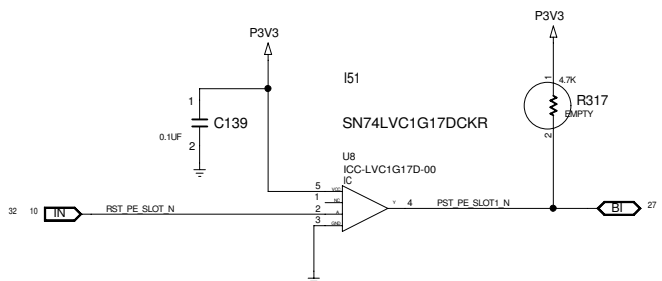
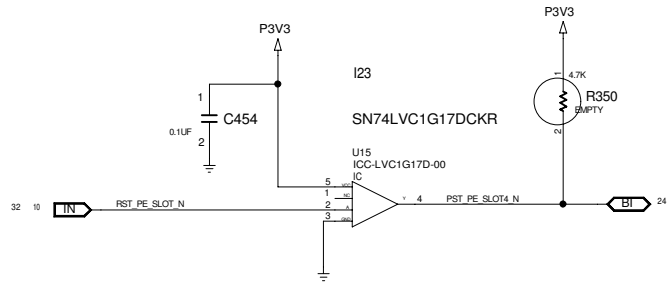
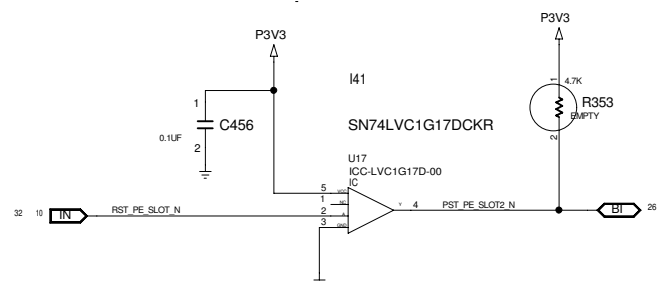
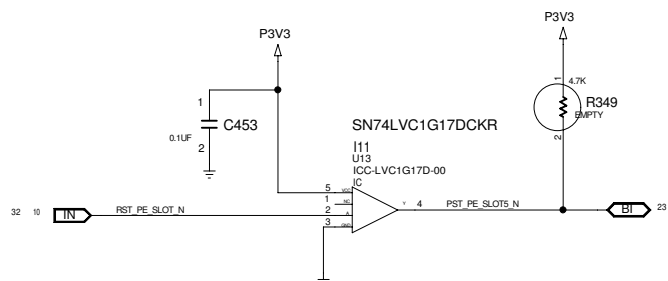
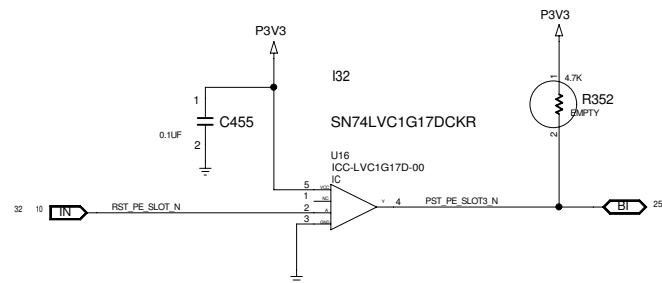
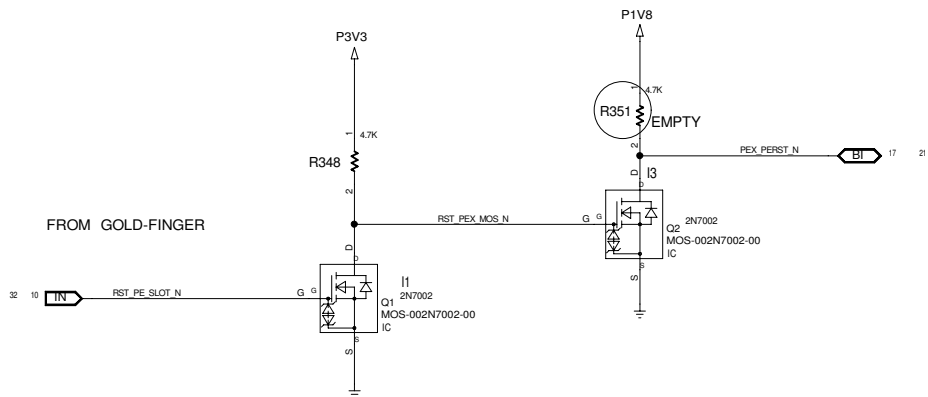


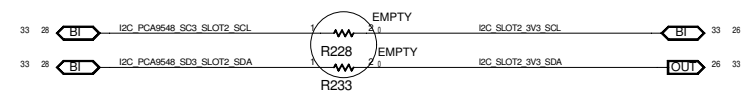
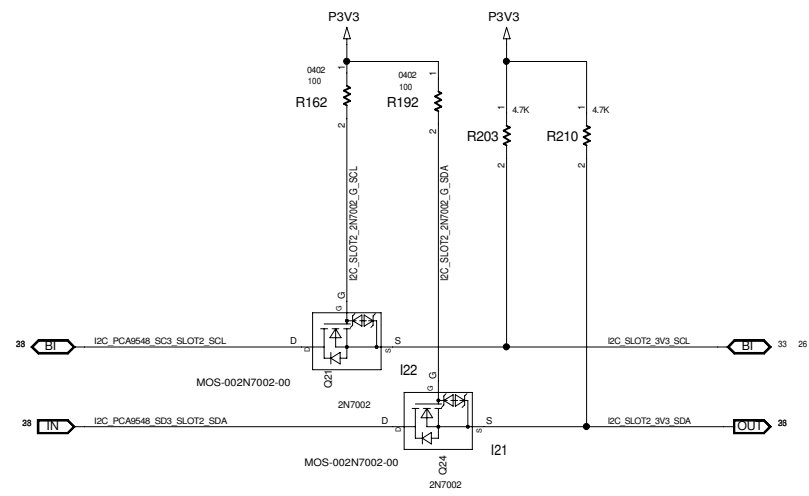
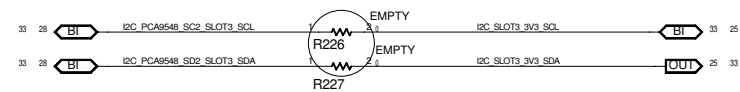
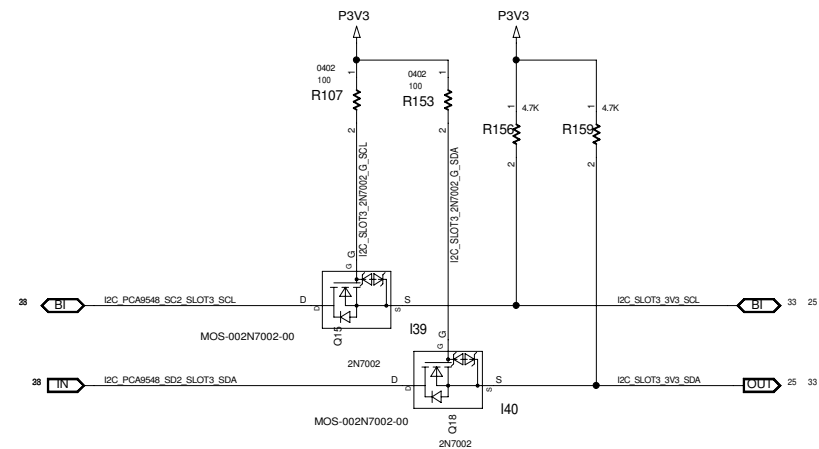
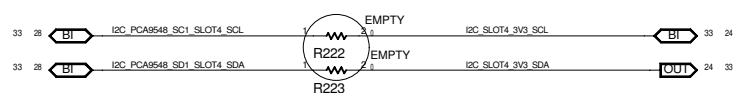
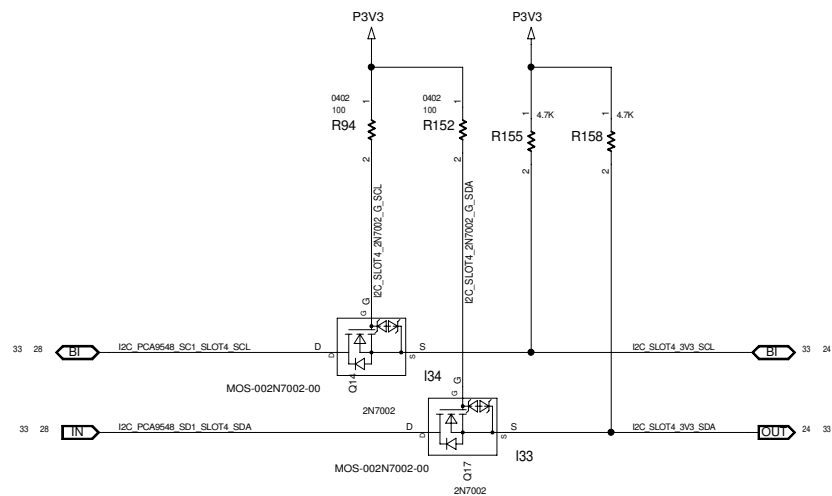
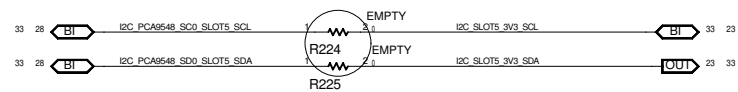
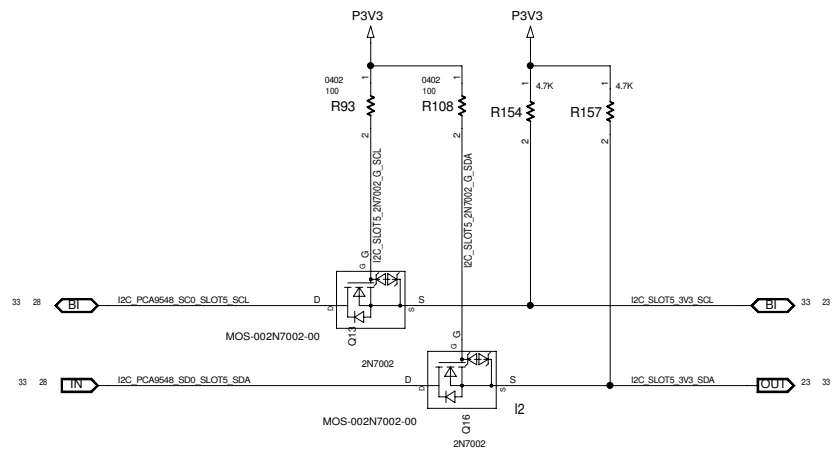
The schematic diagram shows a 2N7002 MOSFET circuit. A P3V3 power supply is connected to a 4.7K resistor R3. The other end of R3 is connected to the gate of MOSFET I109 (2N7002). The source of I109 is connected to ground. The drain of I109 is connected to the gate of MOSFET I106 (2N7002). The source of I106 is connected to ground. The drain of I106 is connected to a 4.7K resistor R4. The other end of R4 is connected to the output OUT, which is connected to a 29-pin connector. The circuit is powered by P3V3 and ground.

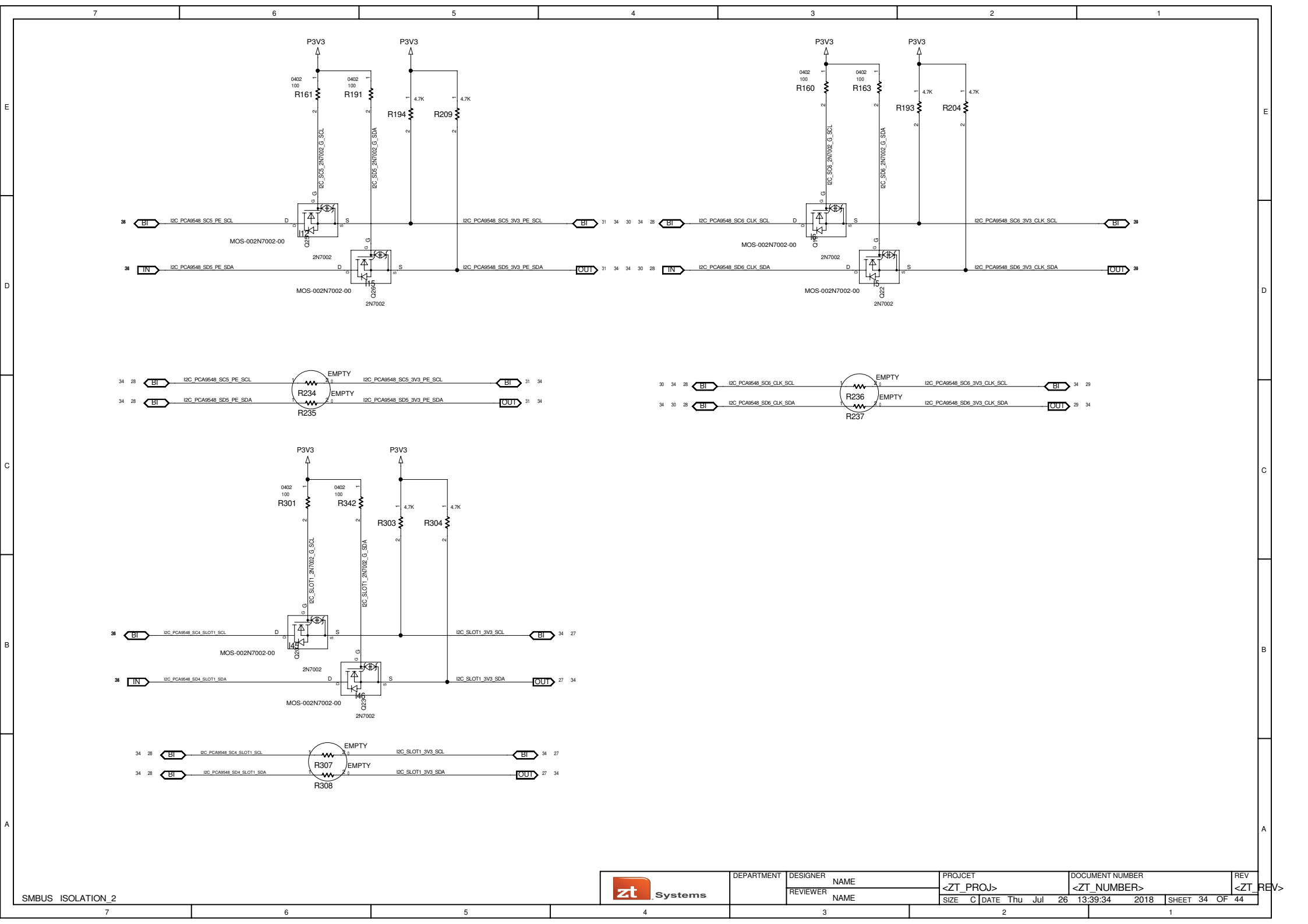


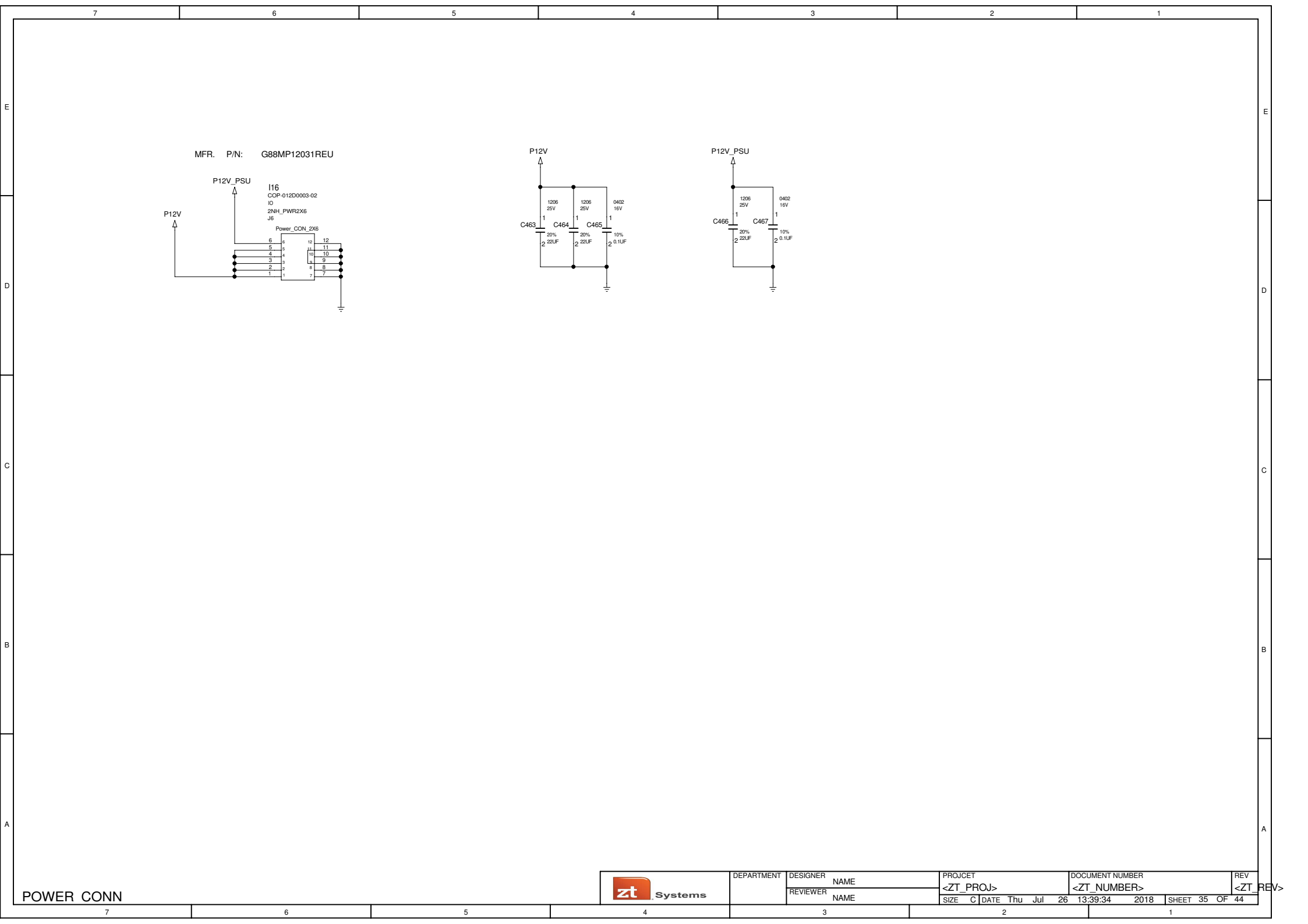




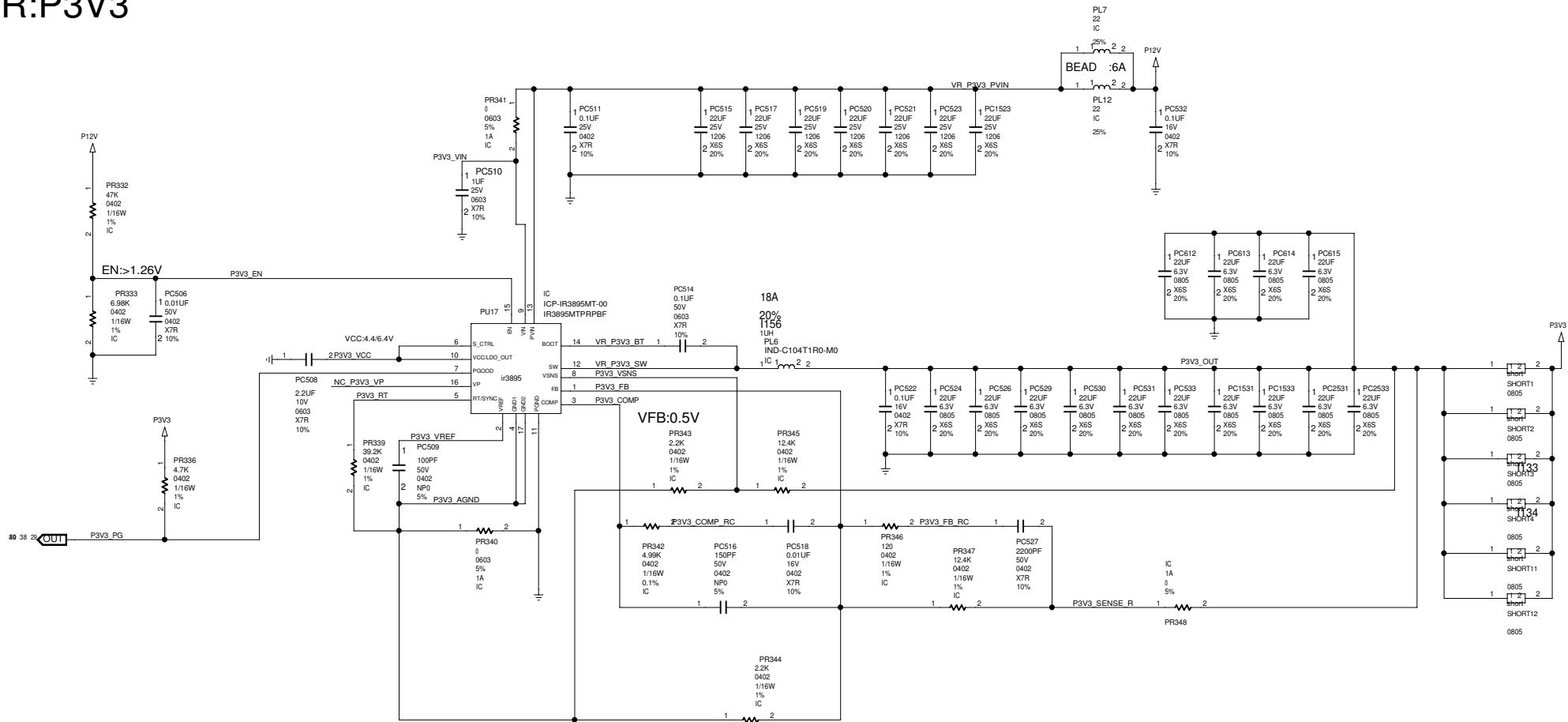








VR:P3V3



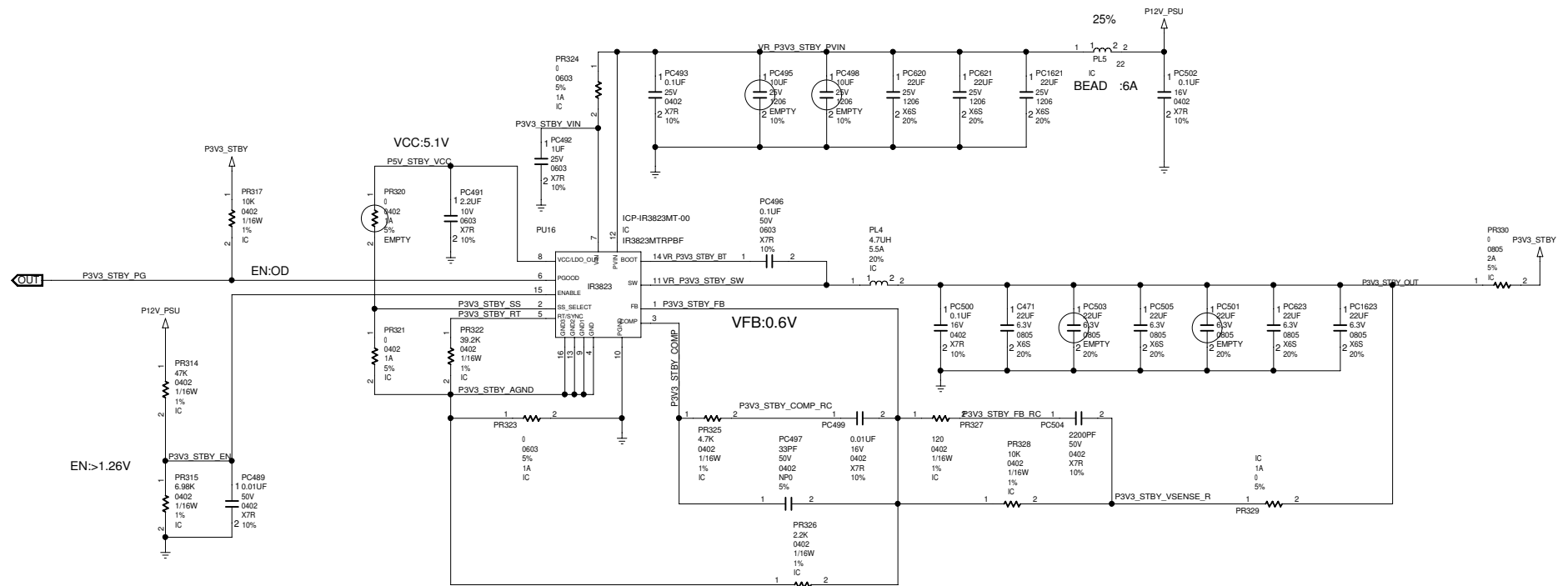
P12V TO P3V3 (AC:±5%)
TDC :12A
IMAX :12A
OCP :MIN=14.4A
FSW :605KHZ
SOLUTION :IR3895 (16A POL)

P3V3



DEPARTMENT	DESIGNER NAME	PROJECT	DOCUMENT NUMBER	REV
	REVIEWER NAME	<ZT_PROJ>	<ZT_NUMBER>	<ZT_REV>
SIZE	C	DATE	Thu Jul 26 2018	SHEET 36 OF 44

VR:P3V3_STBY
(NON-POP)



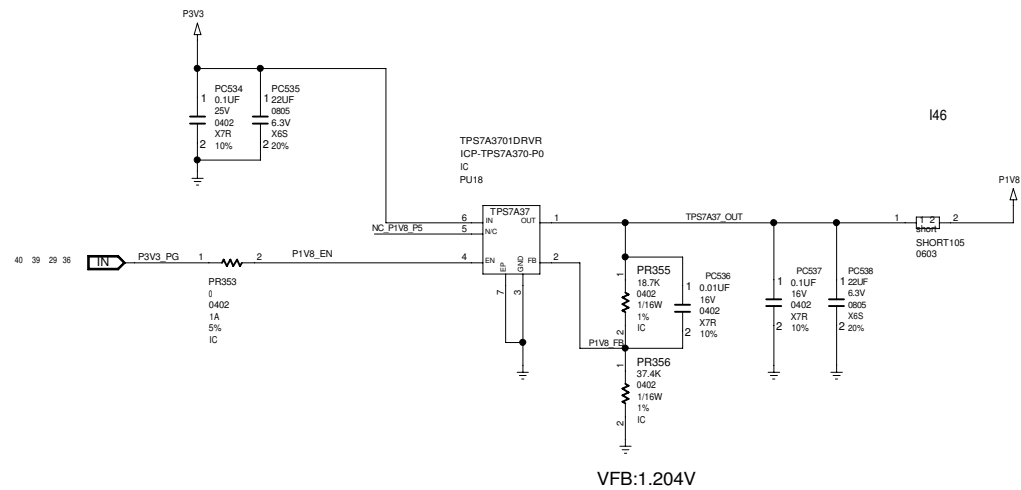
P12V_PSU TO P3V3_STBY (AC: +/-5%)
TDC :1.5A
IMAX :1.5A
OCP :MIN=1.8A
FSW :600KHZ
SOLUTION :IR3823 (3A POL)

P3V3_STBY



DEPARTMENT	DESIGNER	NAME	PROJECT					DOCUMENT NUMBER					REV
	REVIEWER		<ZT_PROJ>					<ZT_NUMBER>					<ZT
		NAME	SIZE	C	DATE	Thu	Jul	26	13:39:25	2018	SHEET	37	OF

VR:P1V8



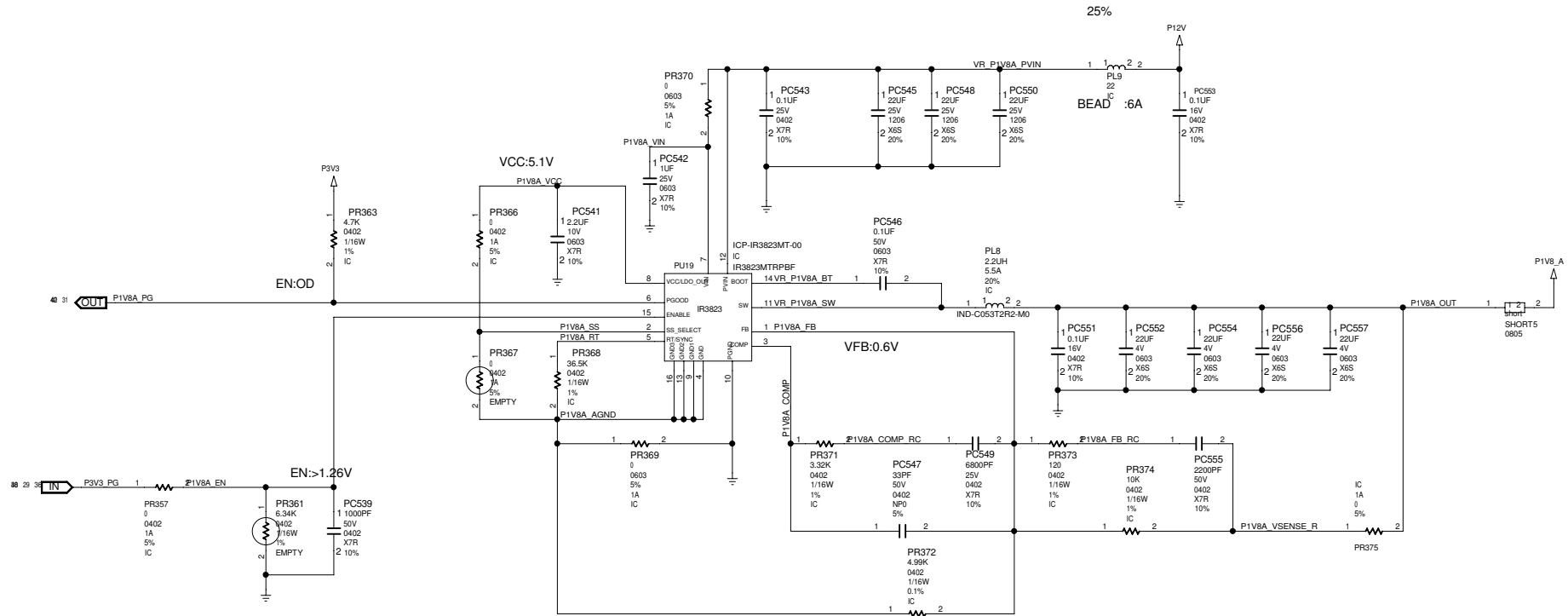
P3V3 TO P1V8 (AC:±5%)
TDC :0.1A
IMAX :0.1A
OCP :MIN=0.12A
SOLUTION :TPS7A37 (LDO)

P1V8



DEPARTMENT	DESIGNER NAME	PROJECT	DOCUMENT NUMBER	REV
	REVIEWER NAME	<ZT_PROJ>	<ZT_NUMBER>	<ZT_REV>
SIZE	C	DATE	Thu Jul 26 13:39:35 2018	SHEET 38 OF 44

VR:P1V8_A

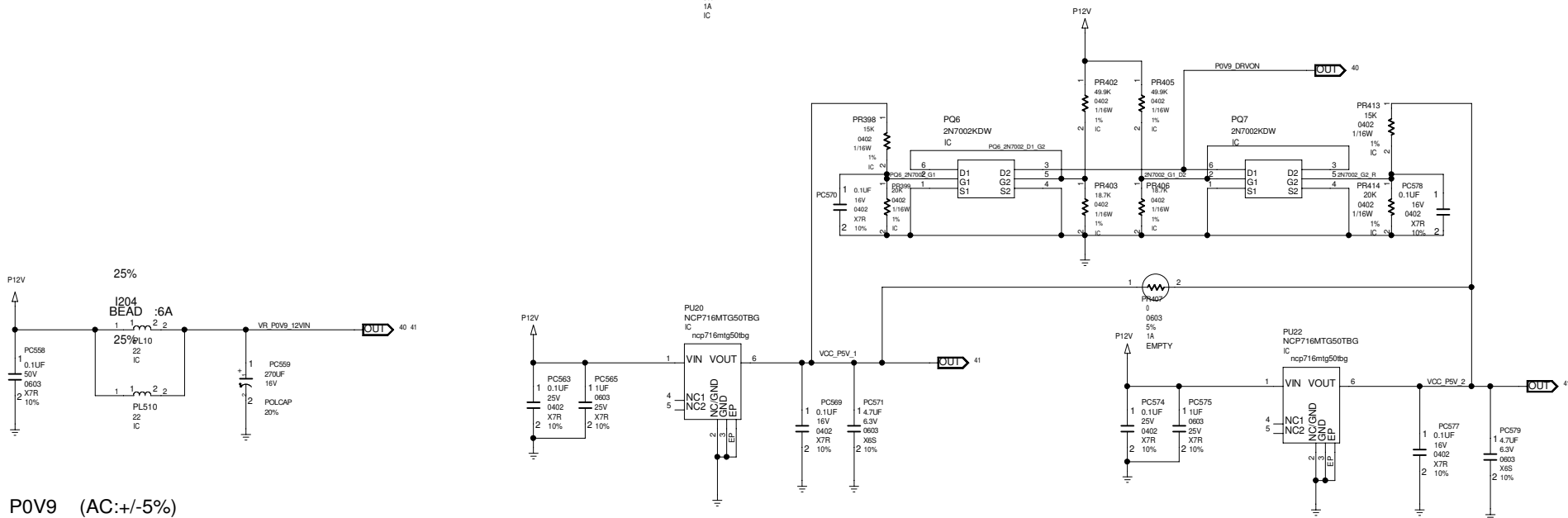
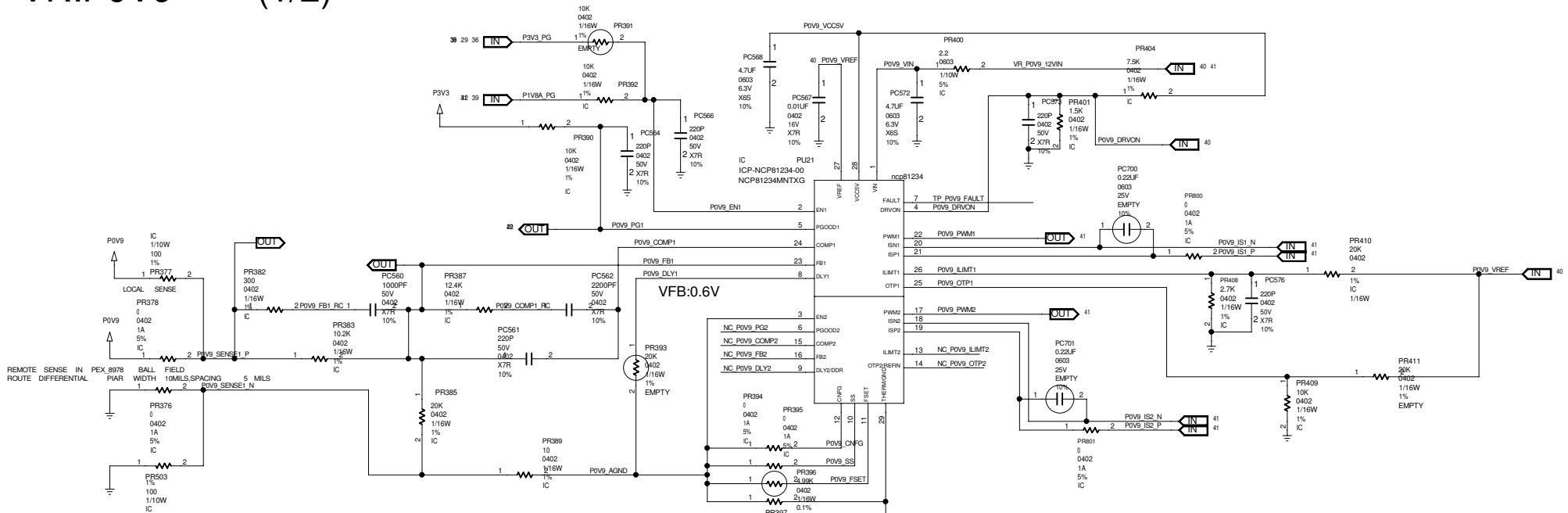


P12V TO P1V8_A (AC:±5%)
TDC :2.3A
IMAX :2.3A
OCP :MIN=2.8A
FSW :648KHZ
SOLUTION :IR3823 (3A POL)



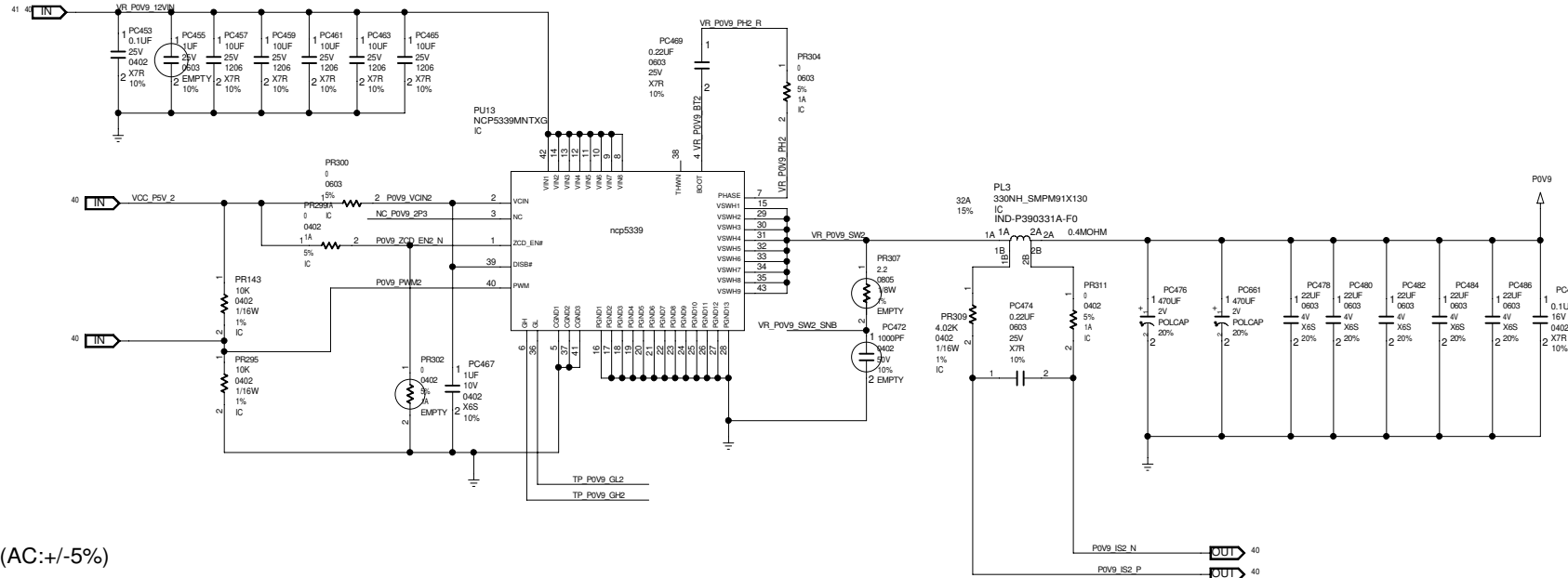
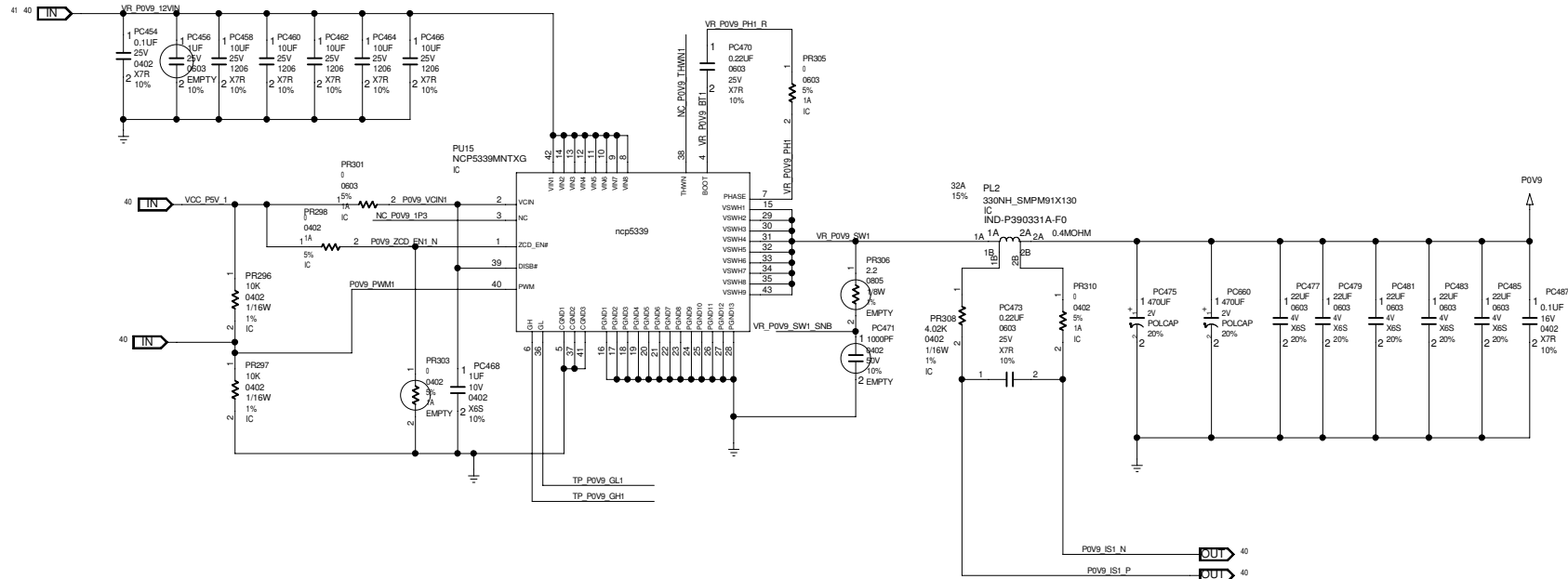
DEPARTMENT	DESIGNER NAME	PROJECT	DOCUMENT NUMBER	REV
	REVIEWER NAME	<ZT_PROJ>	<ZT_NUMBER>	<ZT_REV>
SIZE	C	DATE	Thu Jul 26 13:39:24 2018	SHEET 39 OF 44

VR:P0V9 (1/2)



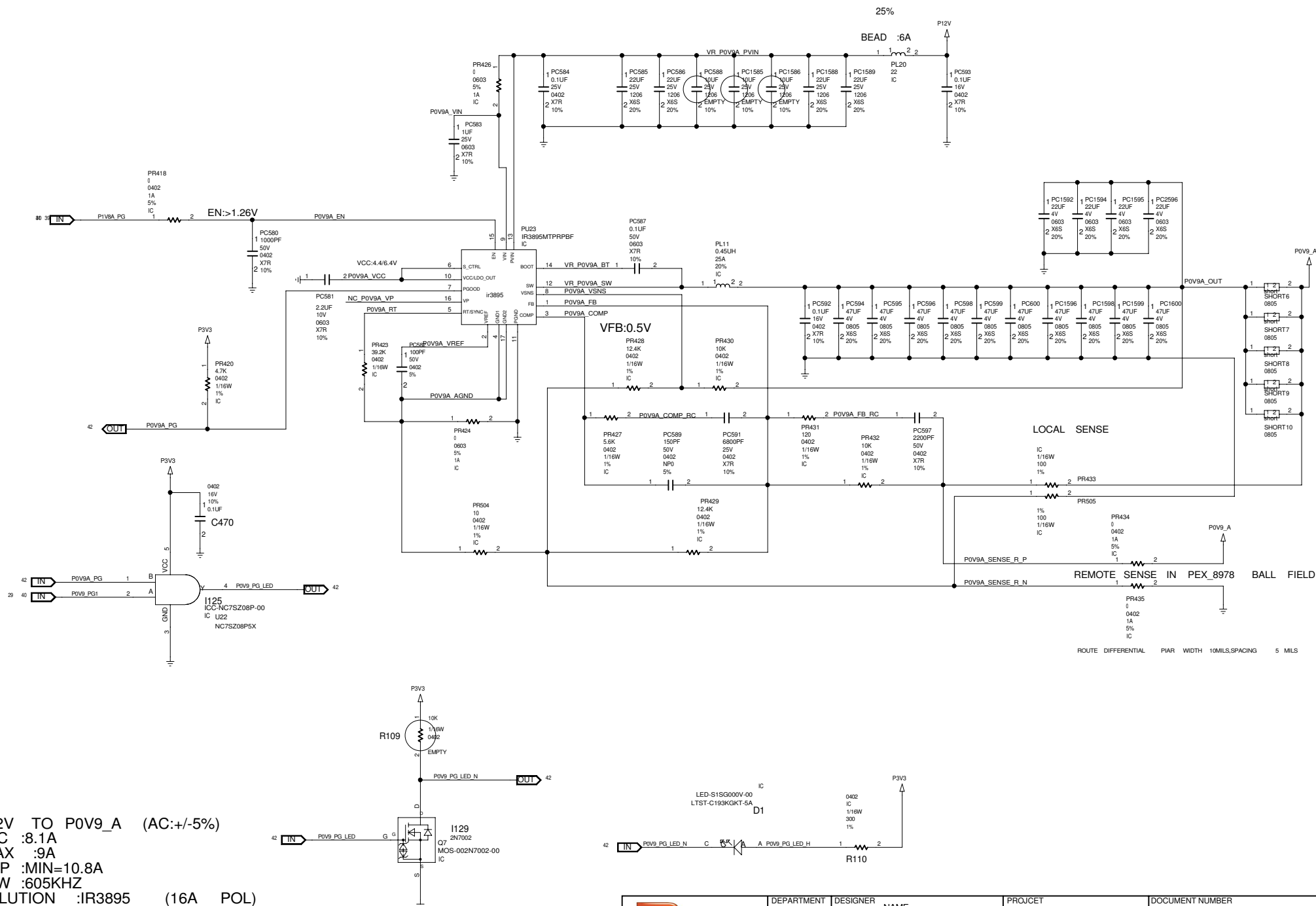
P12V TO P0V9 (AC:+/-5%)
TDC :32.4A
IMAX :36A
OCP :MIN=43.2A
FSW :400KHZ
SOLUTION :NCP81234 +NCP5339
P0V9 1/2

VR:P0V9 (2/2)



P12V TO P0V9 (AC:+/-5%)
TDC :32.4A
IMAX :36A
OCP :MIN=43.2A
FSW :400KHZ
SOLUTION :NCP81234 +NCP5339
P0V9 2/2

VR:P0V9_A



P12V TO P0V9_A (AC:±5%)
TDC :8.1A
IMAX :9A
OCP :MIN=10.8A
FSW :605KHZ
SOLUTION :IR3895 (16A POL)

P0V9 A

