

MOXLIE RISER 3 & 5

<4 SLOT>

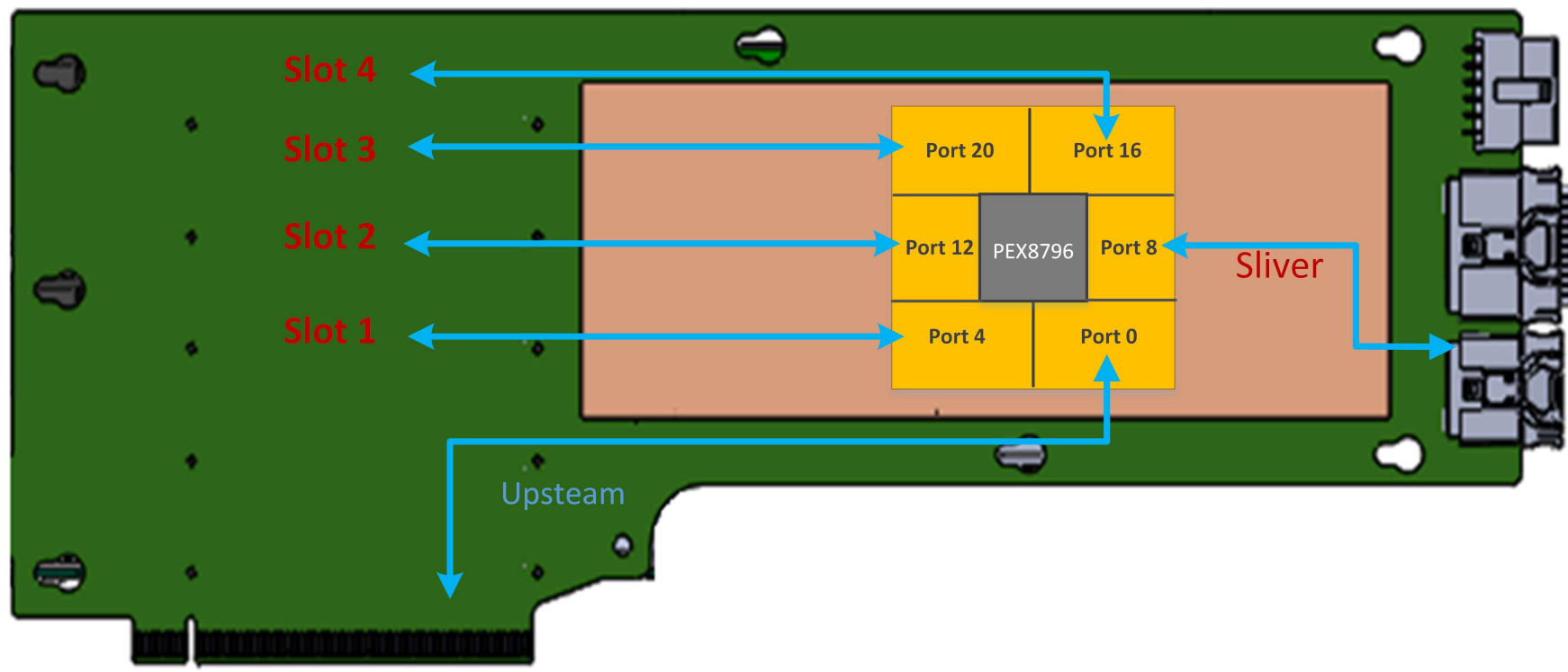
STAGE: PVT
VERSION: 3.12
DATE: 2018.10.25



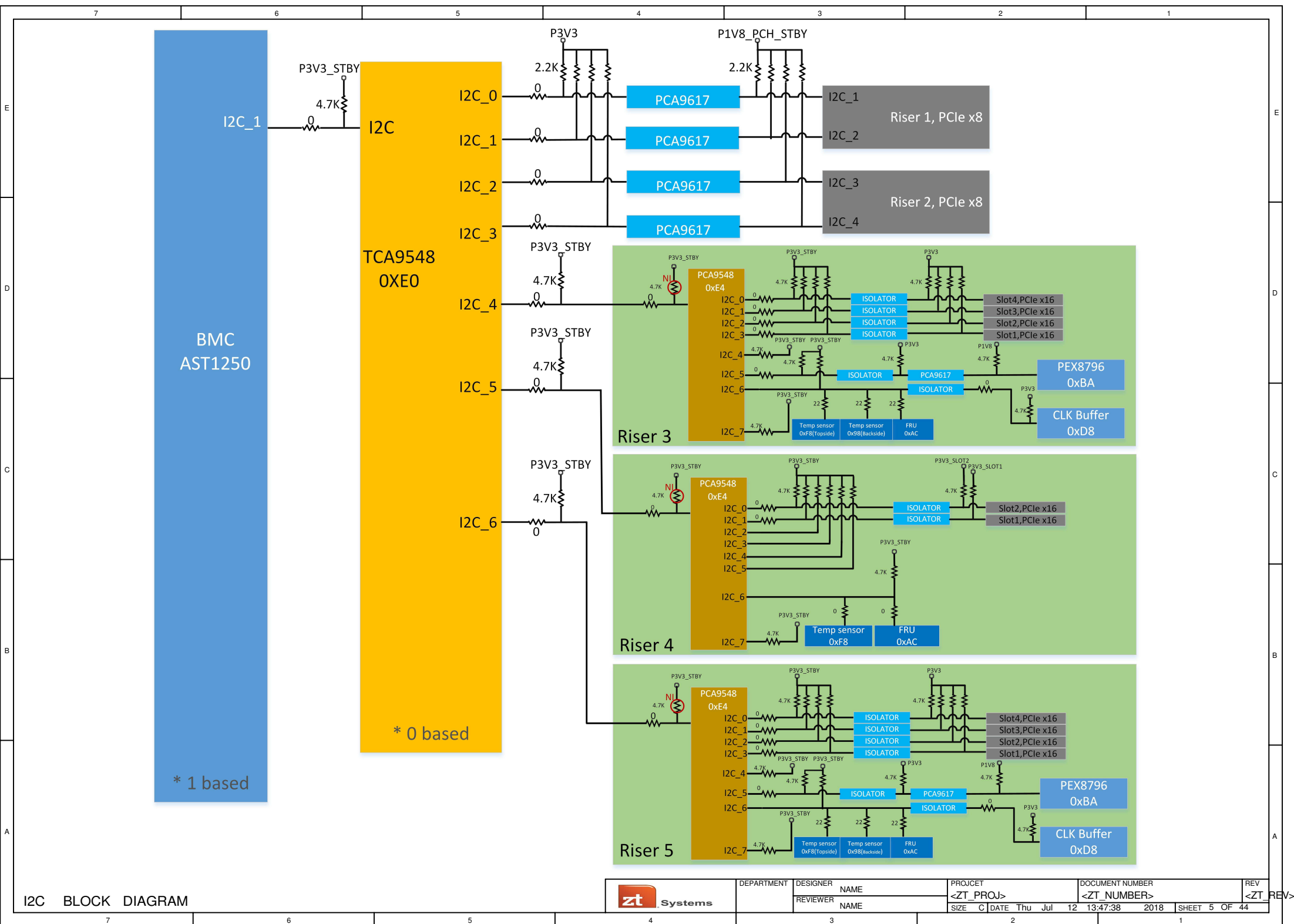
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	REVIEWER	NAME	<ZT_PROJ>		<ZT_NUMBER>		<ZT_REV>
			SIZE	C	DATE	Thu Oct 25 10:06:45 2018	SHEET 1 OF 44

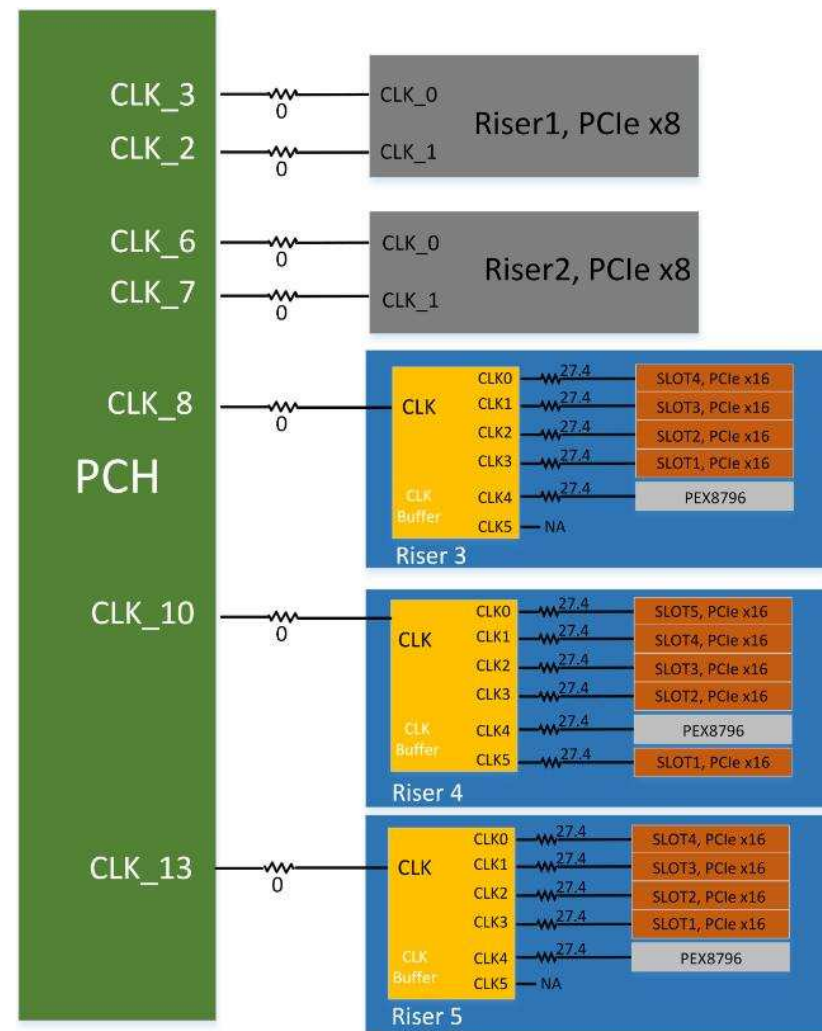
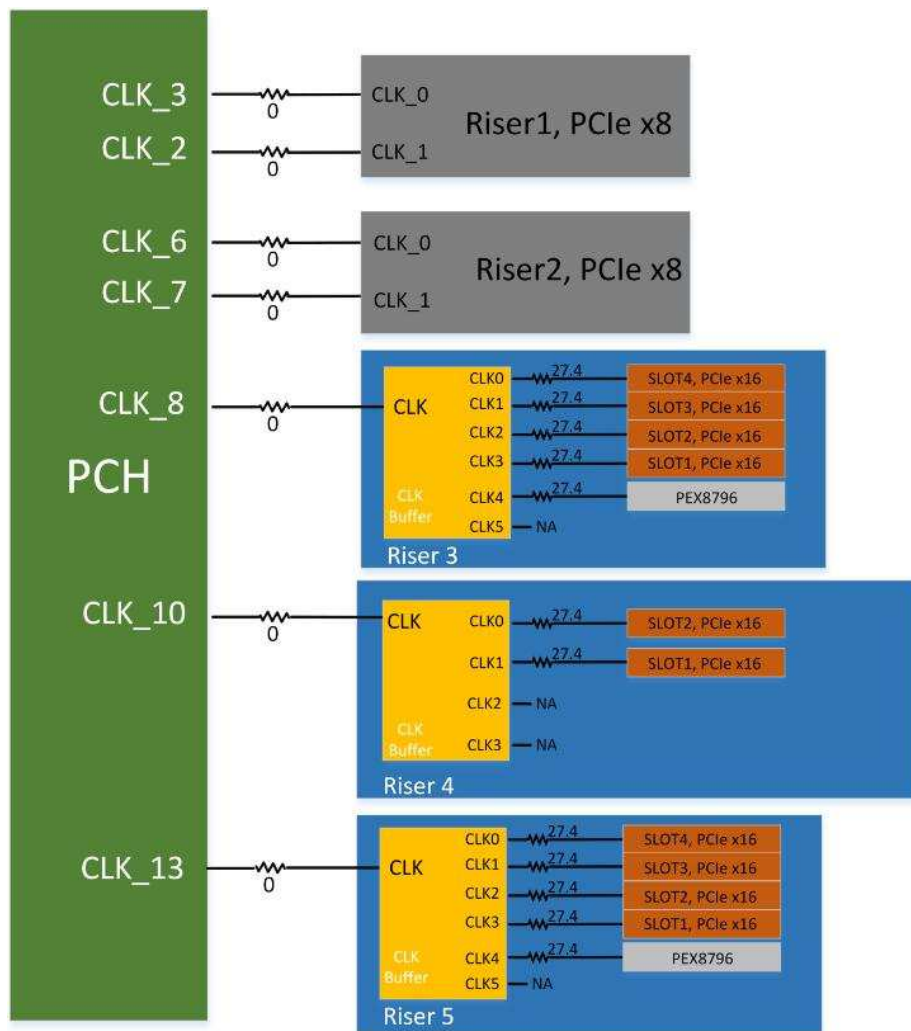
Dielectric and Copper Properties									
Layer		Copper		Dielectric Material			Layer		
Name	Description	Type	Weight	Type	Type	Er	Df	Design Thickness (mil)	Actual Thickness (mil)
Top_SM	Top Soldermask	Soldermask			Soldermask	3.5	0.030	0.50	
L1top	Signal_L1top	Signal	0.5 oz. plated	STD				1.90	
PP_L1top_L2	Prepreg	PP			Material 1	3.6	0.009	2.70	
L2	GND_L2	GND	1.0 oz.	RTF				0.65	
Core_L2_L3	Core	Core			Material 2	3.6	0.009	3.00	
L3	Signal_L3	Signal	1.0 oz.	RTF				0.65	
PP_L3_L4	Prepreg	PP			Material x	3.6	0.009	5.50	
L4	GND_L4	GND	1.0 oz.	RTF				0.65	
Core_L4_L5	Core	Core			Material y	3.6	0.009	3.00	
L5	Signal_L5	Signal	1.0 oz.	RTF				0.65	
PP_L5_L6	Prepreg	PP			Material y	3.6	0.009	9.50	
L6	PWR_L6	PWR	1.0 oz.	RTF				1.30	
Core_L6_L7	Core	Core			Material 2	3.8	0.009	4.00	
L7	PWR_L7	PWR	1.0 oz.	RTF				1.30	
PP_L7_L8	Prepreg	PP			Material y	3.6	0.009	9.50	
L8	Signal_L8	Signal	1.0 oz.	RTF				0.65	
Core_L8_L9	Core	Core			Material y	3.6	0.009	3.00	
L9	GND_L9	GND	1.0 oz.	RTF				0.65	
PP_L9_L10	Prepreg	PP			Material x	3.6	0.009	5.50	
L10	Signal_L10	Signal	1.0 oz.	RTF				0.65	
Core_L10_L11	Core	Core			Material 2	3.6	0.009	3.00	
L11	GND_L11	GND	1.0 oz.	RTF				0.65	
PP_L11_L12bot	Prepreg	PP			Material 1	3.6	0.009	2.70	
L12bot	Signal_L12bot	Signal	0.5 oz. plated	STD				1.90	
Bot_SM	Bot Soldermask	Soldermask			Soldermask	3.5	0.030	0.50	
with soldermask, total thickness:								64.0	0.0
without soldermask, total thickness:								63.0	0.0





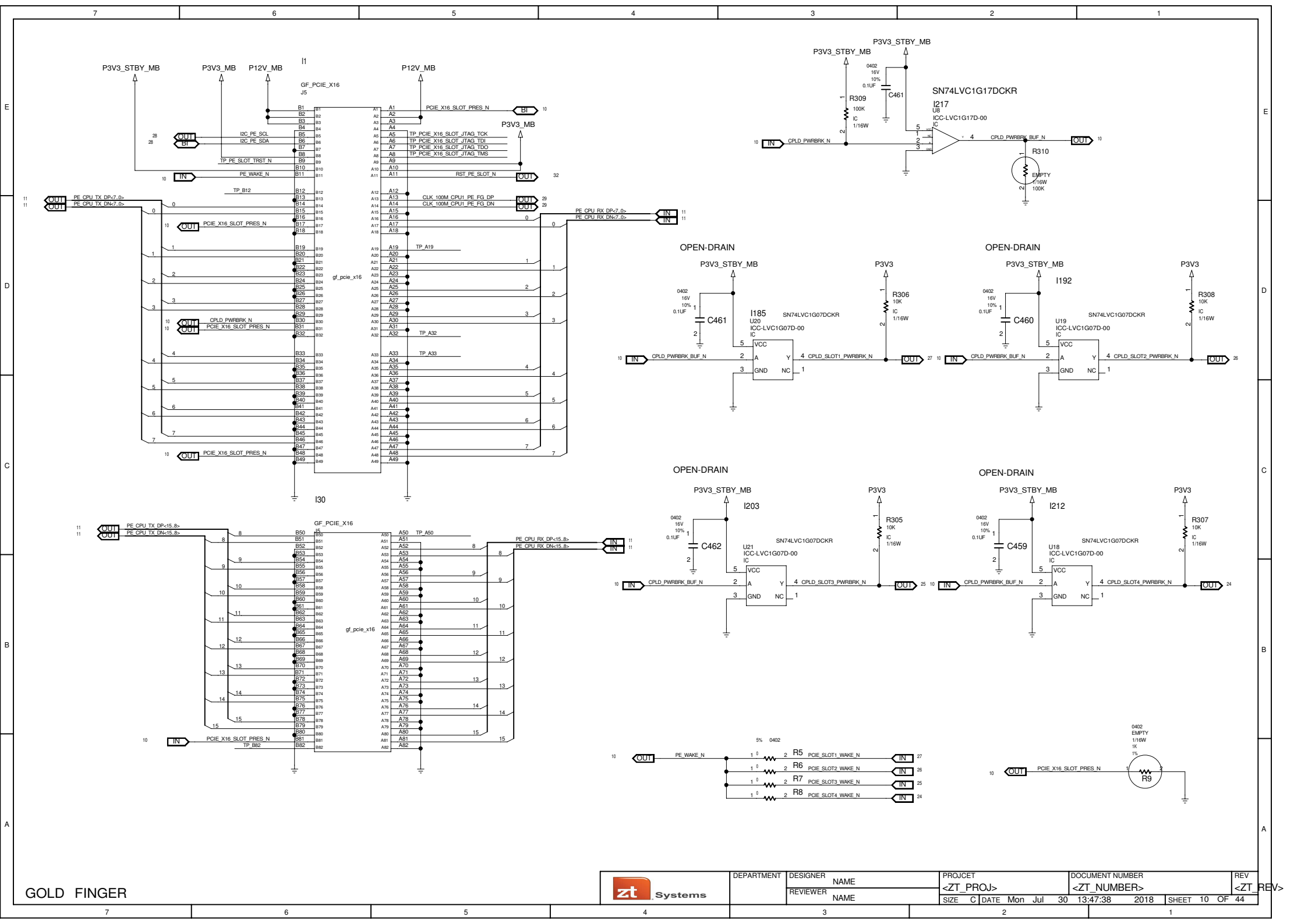
PEX8796	PORTS	SLOTS	NUMBER
	PORT 0	UPSTREAM	
	PORT 4	SLOT 1	
	PORT 8	SLIVER	CONNECTOR(P2P)
	PORT 12	SLOT 2	
	PORT 16	SLOT 4	
	PORT 20	SLOT 3	





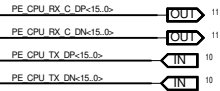
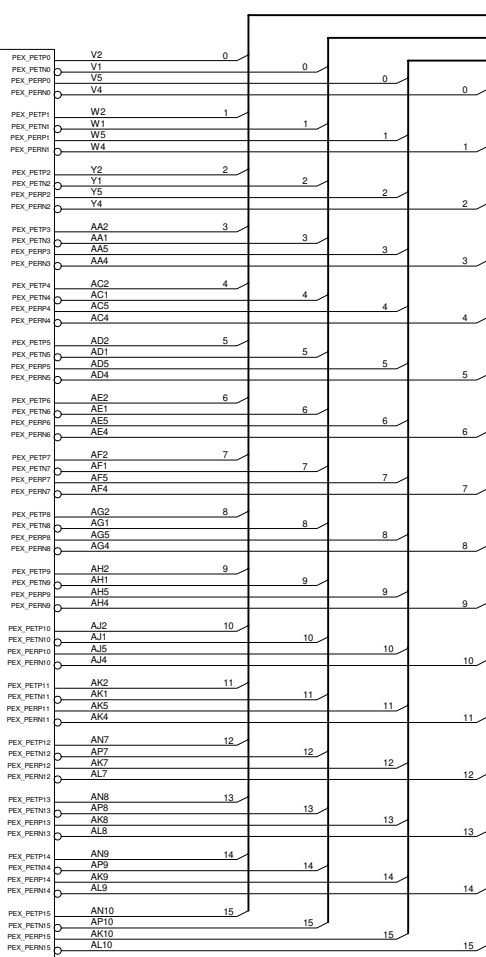
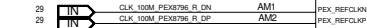
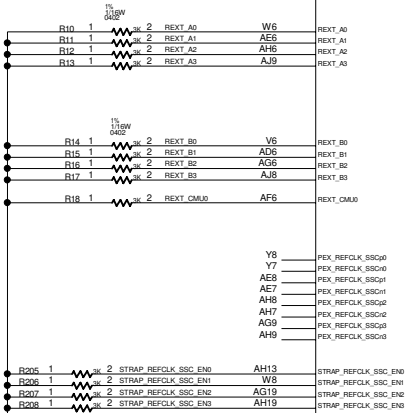
CLOCK BLOCK DIAGRAM



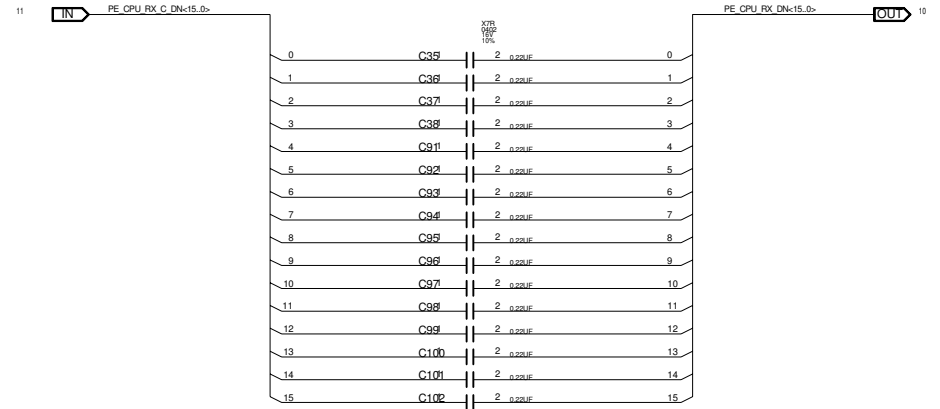
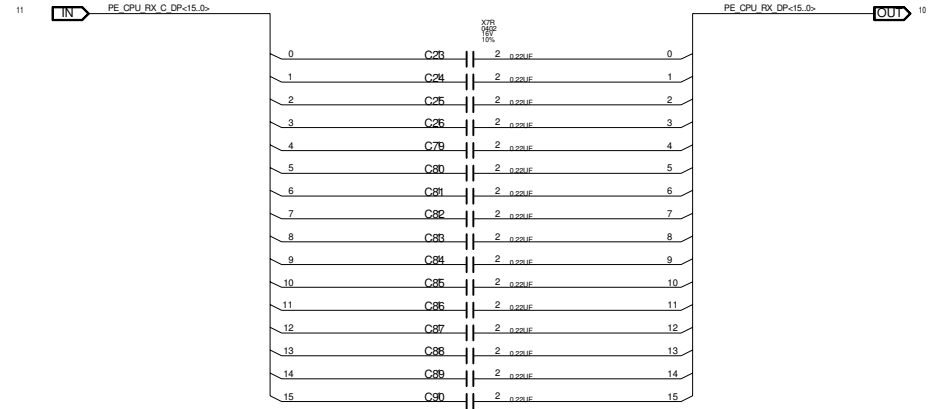


PEX8796 PORT 0(0~15)

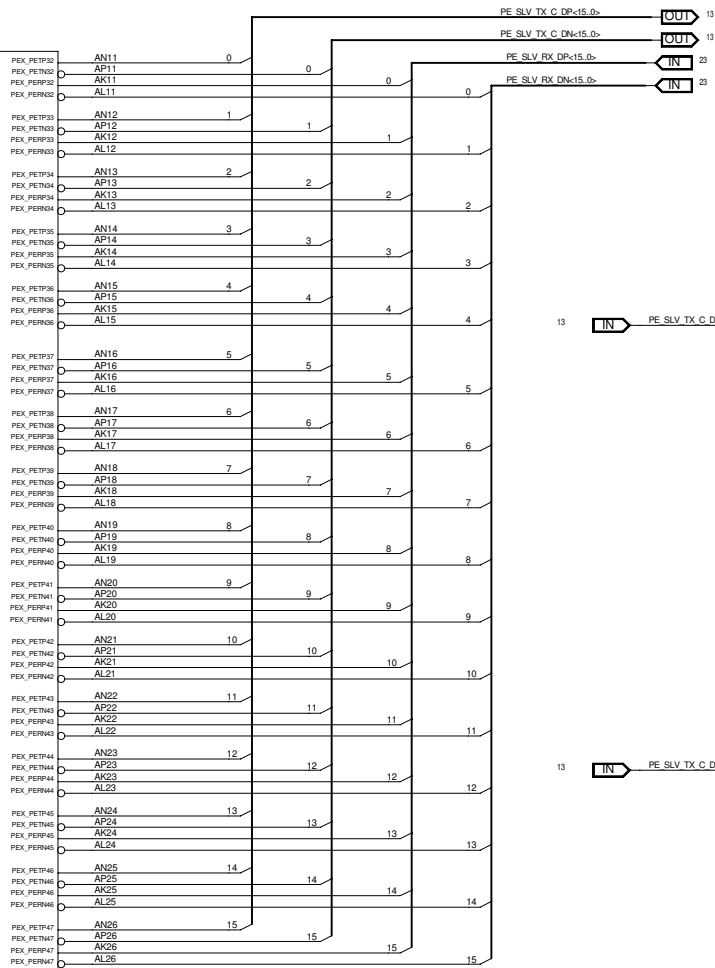
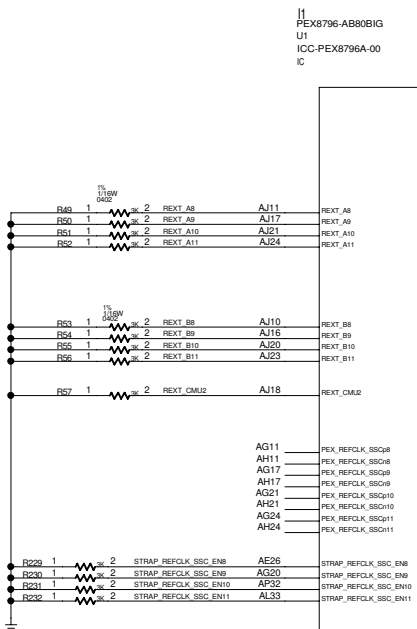
I1
PEX8796-AB80BIG
U1
ICC-PEX8796A-00
IC



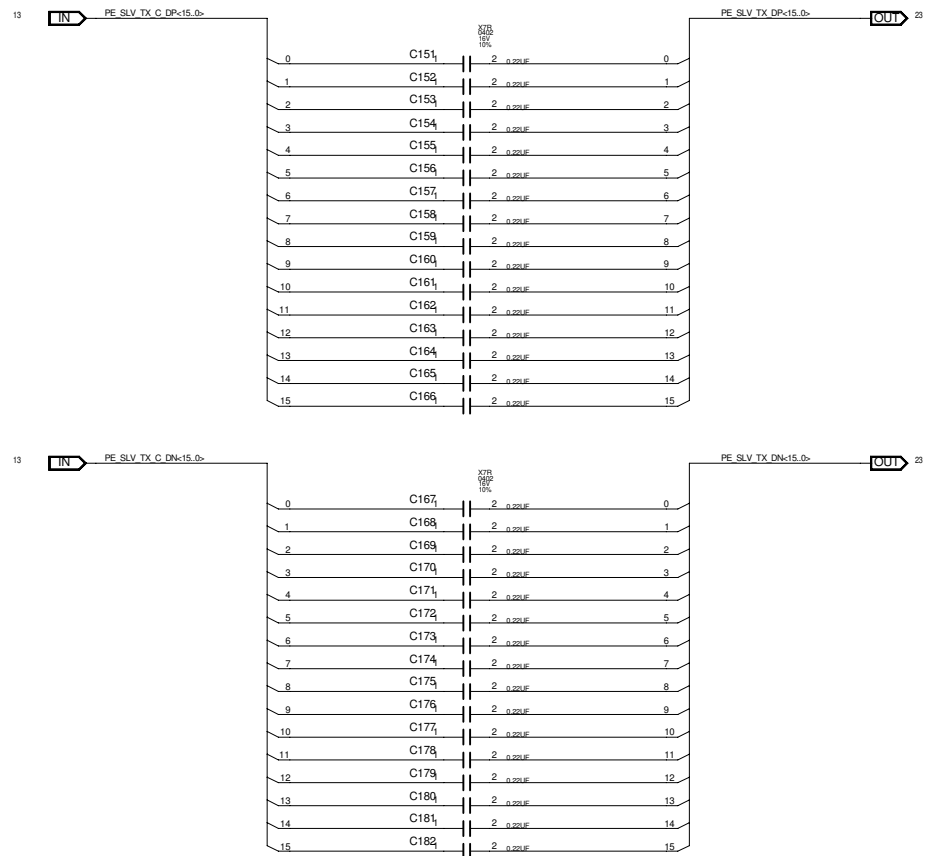
UPSTREAM





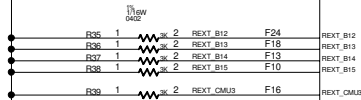
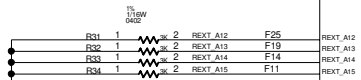


SLIVER CONN(J7 & J8)



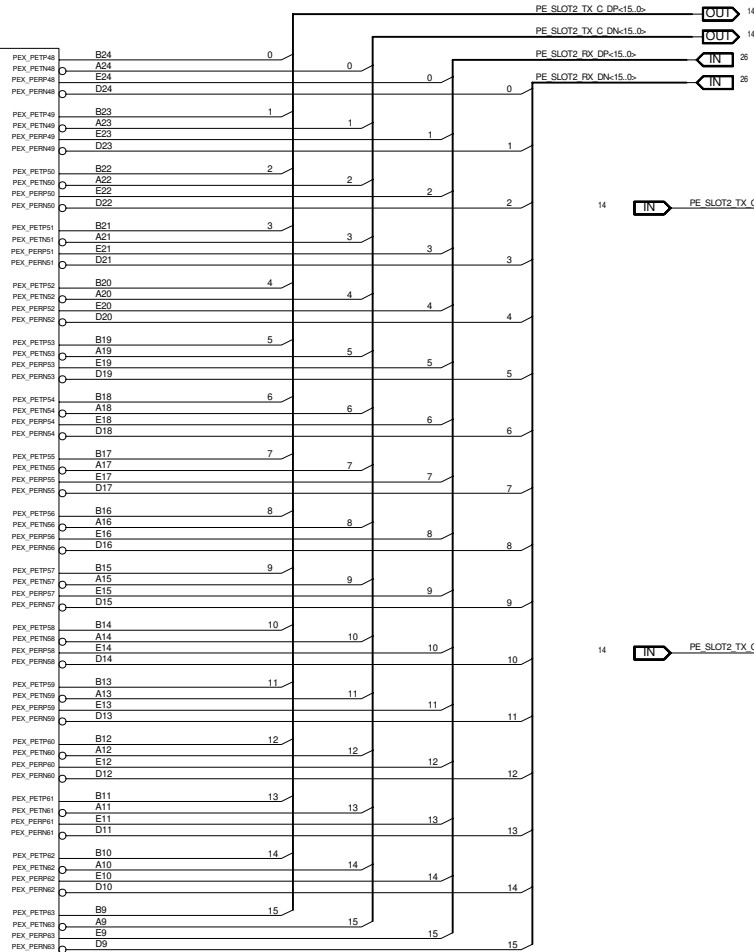
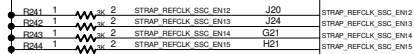
PEX8796 PORT 12(48~63)

I1
PEX8796-AB80BIG
U1
ICC-PEX8796A-00
IC

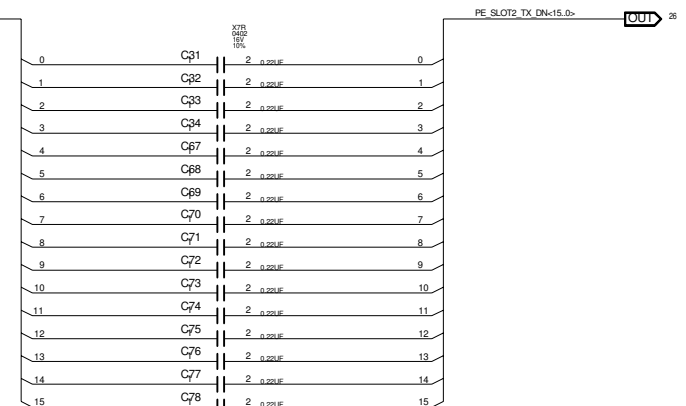
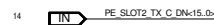
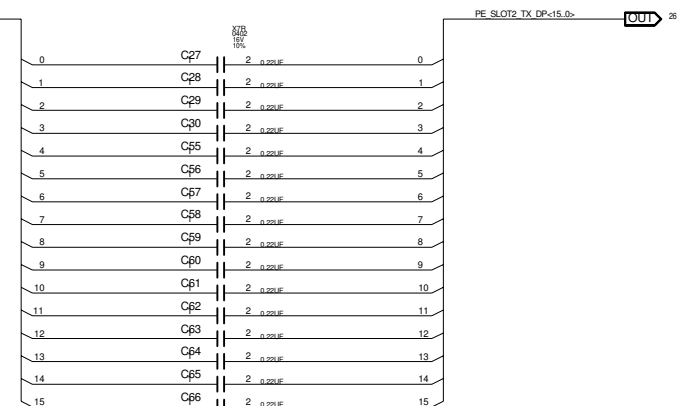
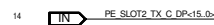
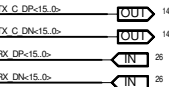


H22
G22
H18
G18
H14
G14
H11
G11

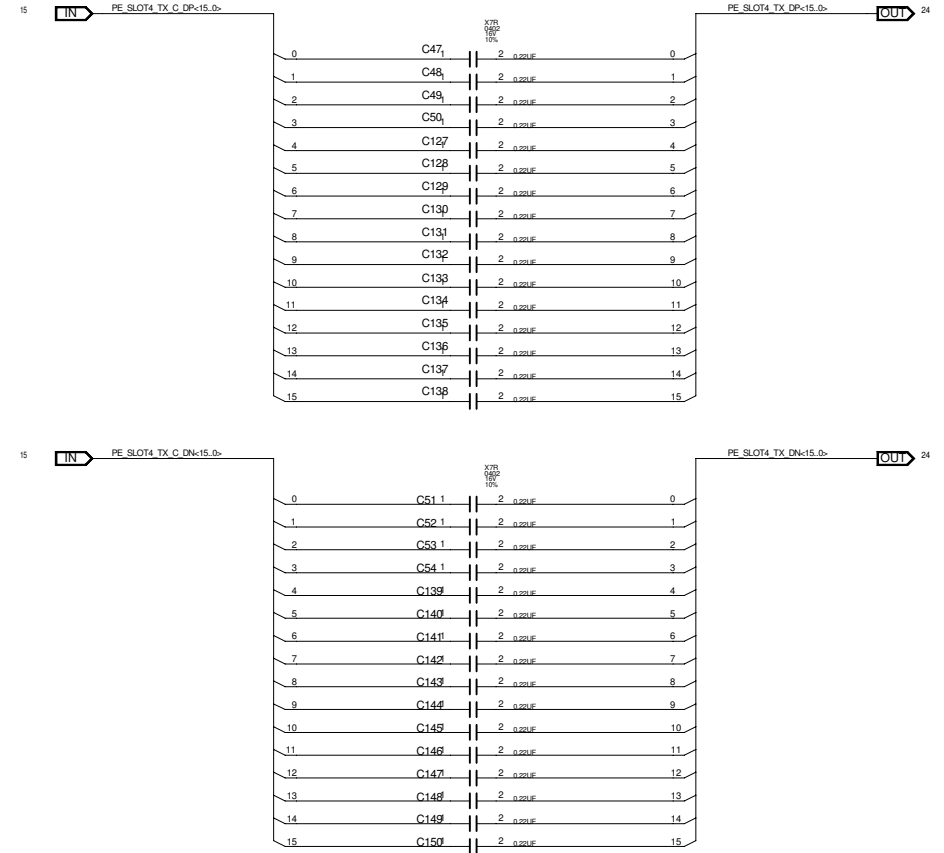
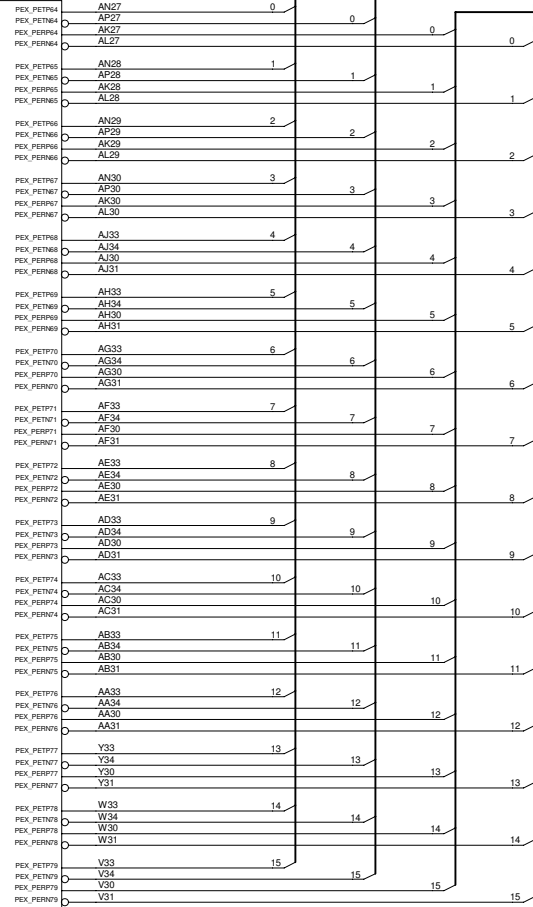
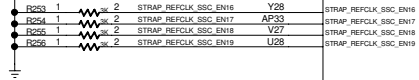
PEX_REFCLK_SSQn12
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PEX_REFCLK_SSQn14
PEX_REFCLK_SSQn15



PCIE SLOT2(J2)

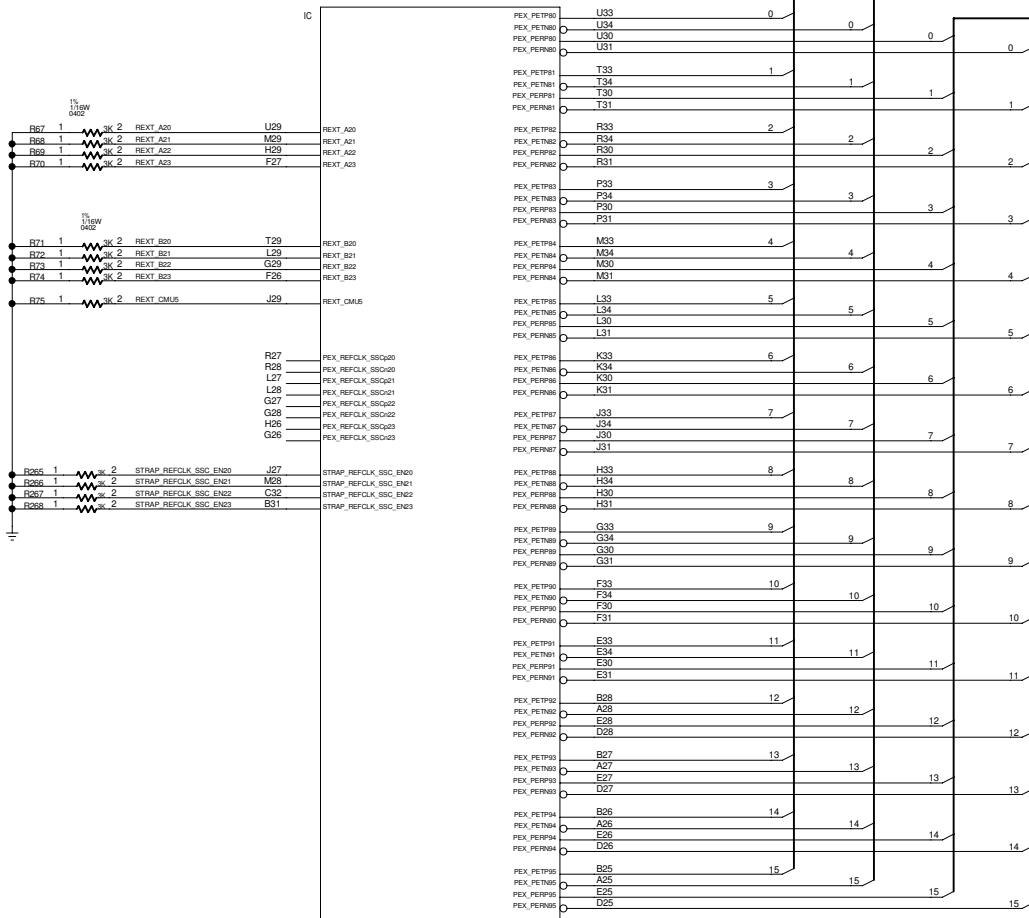


STRAP_REFCLK_SSC_EN16
STRAP_REFCLK_SSC_EN17
STRAP_REFCLK_SSC_EN18
STRAP_REFCLK_SSC_EN19

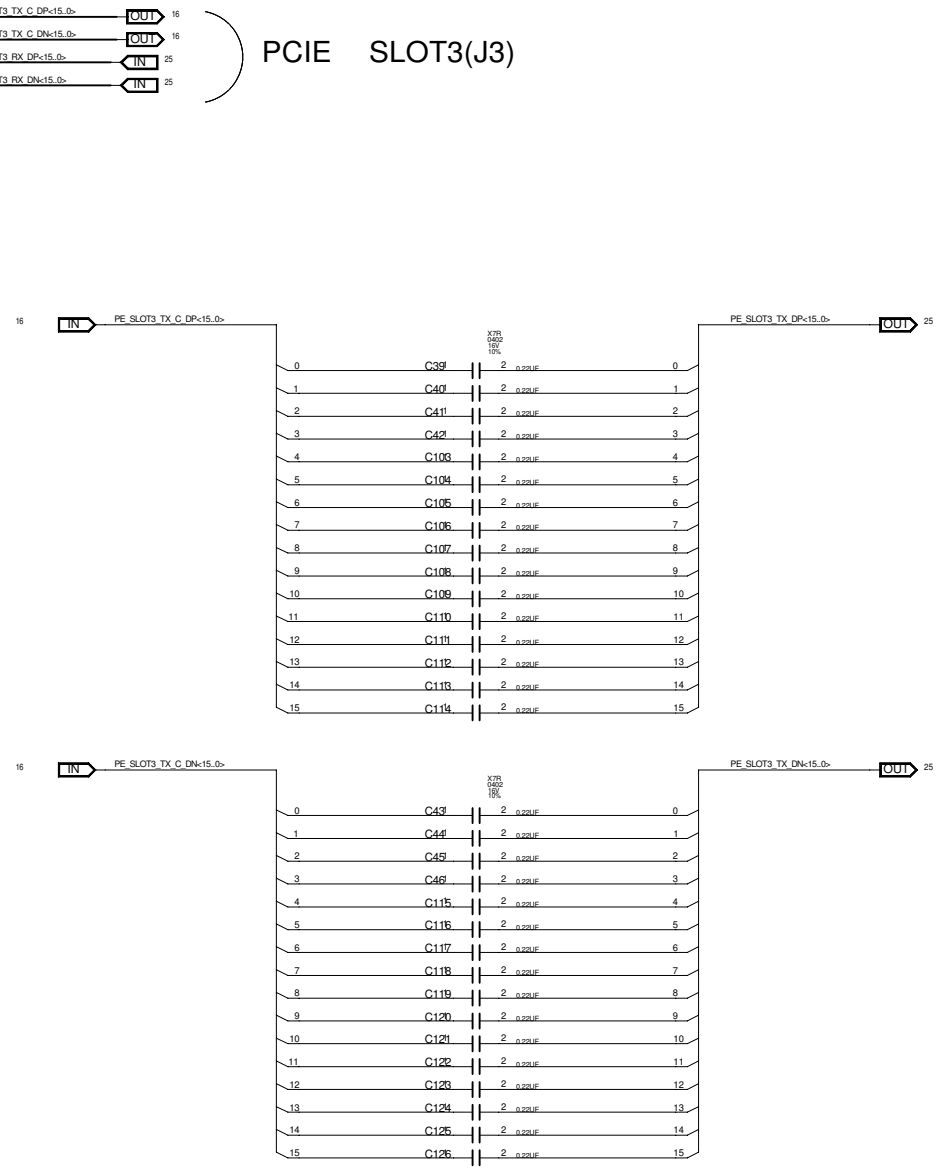


PEX8796 PORT 20(80~95)

I184
PEX8796-AB80BIG
U1
ICC-PEX8796A-00

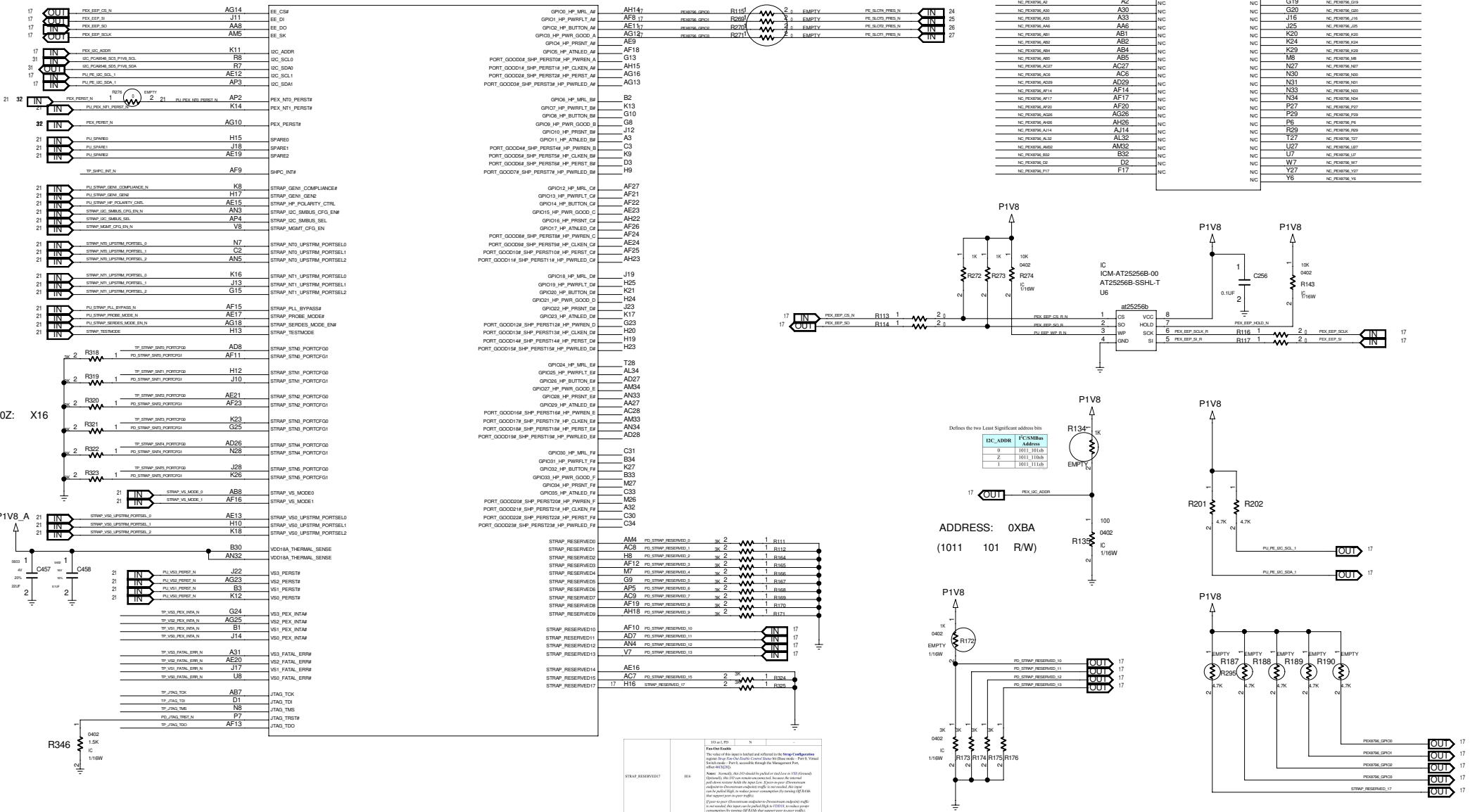


PCIE SLOT3(J3)

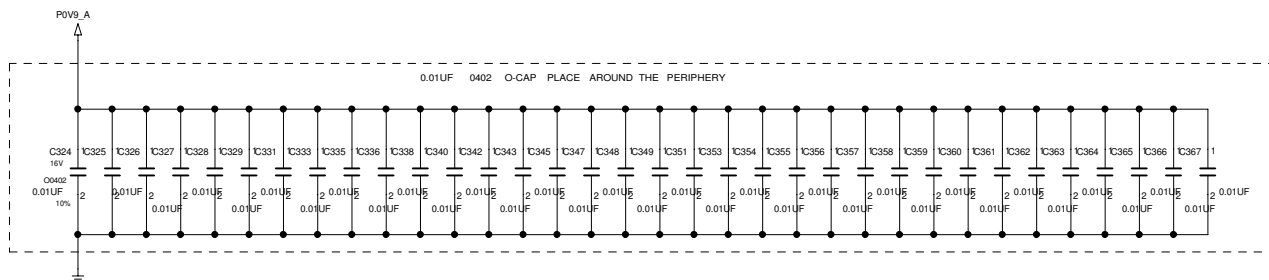
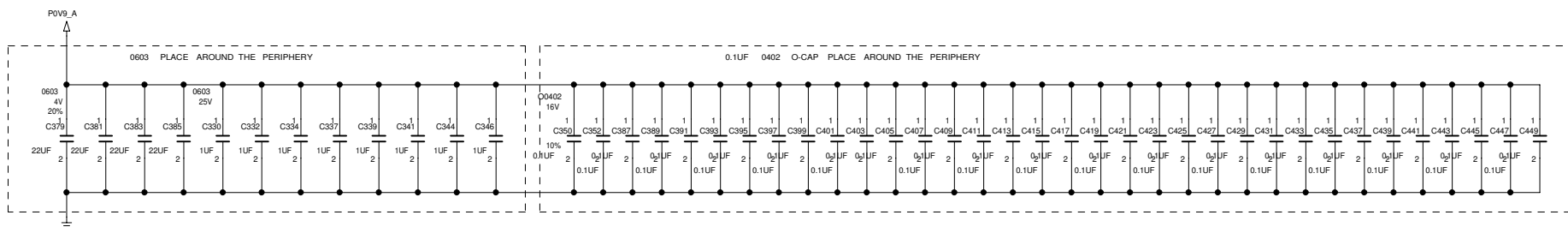
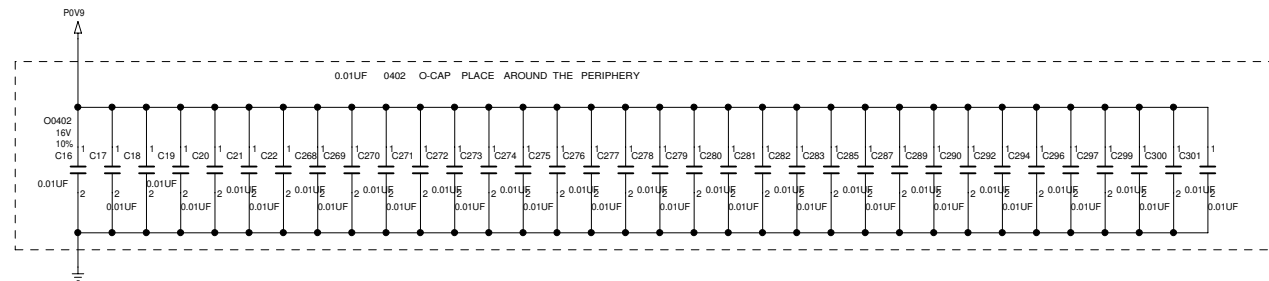
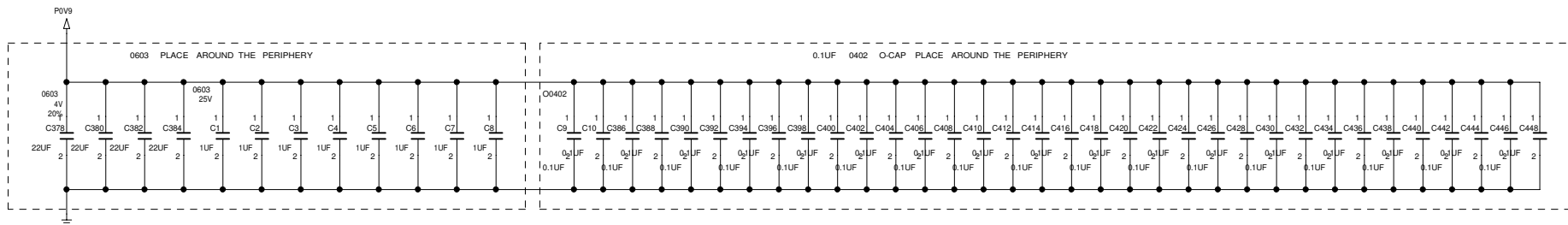


U1
ICC-PEX8796A-00
IC

U1
I132
ICC-PEX8796A-00
IC







PEX_NT_PERST_N:
0= WRITING 0 CLEARS THE RESET CONDITION
1= CAUSES RESET

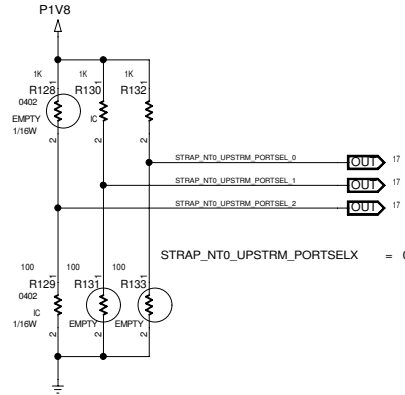
SPARE2	SPARE1	SPARE0	I/O, PU	No	—
AEI19	J18	H15	Spares (3 Balls)		
<i>Reserved for future use</i>					
<i>Note: Normally, these I/O should be pulled High to VDD1/8. Optionally, these I/O can remain unconnected, because the internal pull-up resistor holds the input High.</i>					

STRAP_GEN1_GEN2 Input State	Offset 78h[3:0]	Offset 98h[3:0]	Offset 46Ch[12:11]
0 = Gen 1 (2.5 GT/s)	1	1	10b
Z = Gen 2 (5.0 GT/s)	2	2	01b
1 = Gen 3 (8.0 GT/s)	3	3	11b

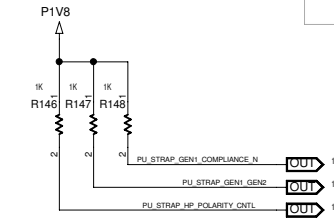
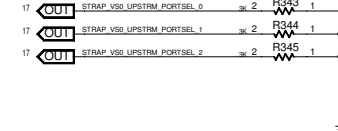
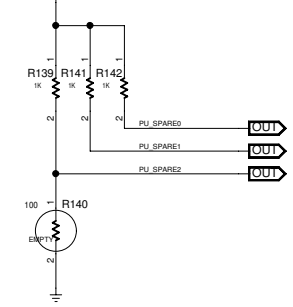
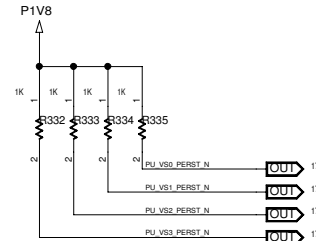
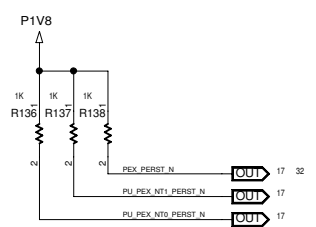
STRAP_GEN1_COMPLIANCE#

K8

IO as I, PU	No	—
Compatibility Enable for Non-Compliant Gen 1 Endpoints		
When STRAP_GEN1_COMPLIANCE# is Low and the Link training sequence fails during either the LTSSM Palling or Configuration state, the next time the LTSSM enters the <i>Owner</i> state, TX Ordered-Sets advertise only the Gen 1 data rate, and no Autonomous Change support.		
When STRAP_GEN1_COMPLIANCE# is High, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the Gen 3 data rate and Autonomous Change.		
The value of this input is latched and reflected in the Strap Configuration register Gen 1 Compatible/Disable-Slower Set (Blue mode - Port 6; Virtual Switch mode - Port 0, accessible through the Management Port, offset 46Ch[0]).		
<i>Note: This feature should be enabled only if a non-compliant Gen 1 device will not linkup if these Data Rate Identifier bits are Set.</i>		
<i>Normally, this I/O should be pulled High to VDD1/8. Optionally, this input can remain unconnected, because the internal pull-up resistor holds the input High.</i>		

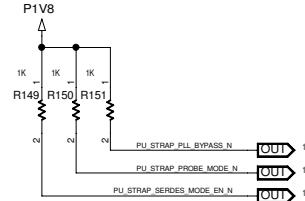


STRAP_NTO_UPSTRM_PORTSELX = 011 (PORT 8)



STRAP_I2C_SMBUS_SEL	Offsets 2C8h[0, 8]	Offsets 46Ch[6, 7]
0	0, 1	1, -
Z	1, 0	0, 0
1	1, 1	0, 1

0 = Enables I²C Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus
Z = Enables SMBus with Address Resolution Protocol (ARP), on the I2C_SCL0 and I2C_SDA0 2-wire bus
1 = Enables SMBus without ARP, on the I2C_SCL0 and I2C_SDA0 2-wire bus

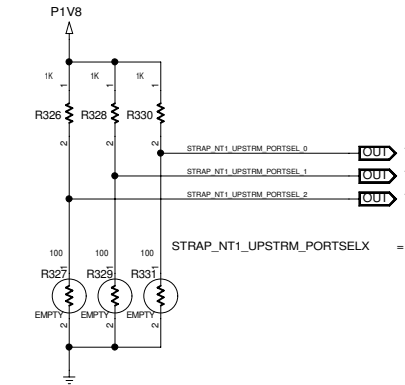


Input State	Offset 46Ch[27:24] Value	TESTMODE Default Functionality
0	0h	0 PORT_GOOD# + GPIOx input
Z	1h	1 SHP_PERST# + GPIOx input
1	2h	2 Parallel Hot Plug I/O (default) ³

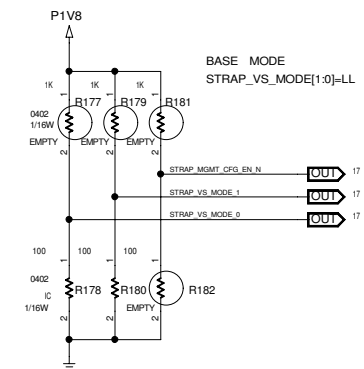
STRAP_I2C_SMBUS_CFG_EN#:
L = ENABLE I2C FOR INITIAL DEVICE CONFIGURATION
H = DISABLE I2C FOR INITIAL DEVICE CONFIGURATION

STRAP_I2C_SMBUS_SEL:
0 = ENABLE I2C SLAVE PROTOCOL ON I2C_SCL0/SDA0
Z = ENABLE SMBUS WITH ADDRESS RESOLUTION PROTOCOL(ARP) ON I2C_SCL0/SDA0
1 = ENABLE SMBUS WITHOUT ARP ON I2C_SCL0/SDA0

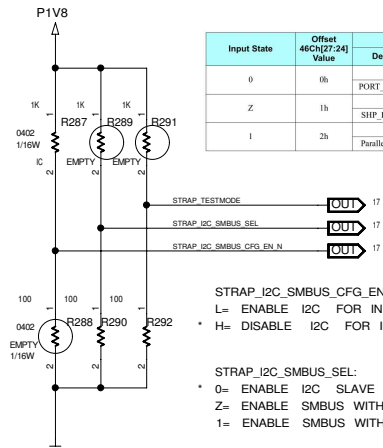
STRAP_PLL_BYPASS#	AF15	I, PU	No	—
<i>Factory Test Only</i> Must be pulled or tied High to VDD1/8.				
STRAP_PROBE_MODE#	AEI7	I, PU	No	—
<i>Factory Test Only</i> Must be pulled or tied High to VDD1/8.				
STRAP_SERDES_MODE_EN#	AG18	I, PU	No	—
<i>Factory Test Only</i> Must be pulled or tied High to VDD1/8.				



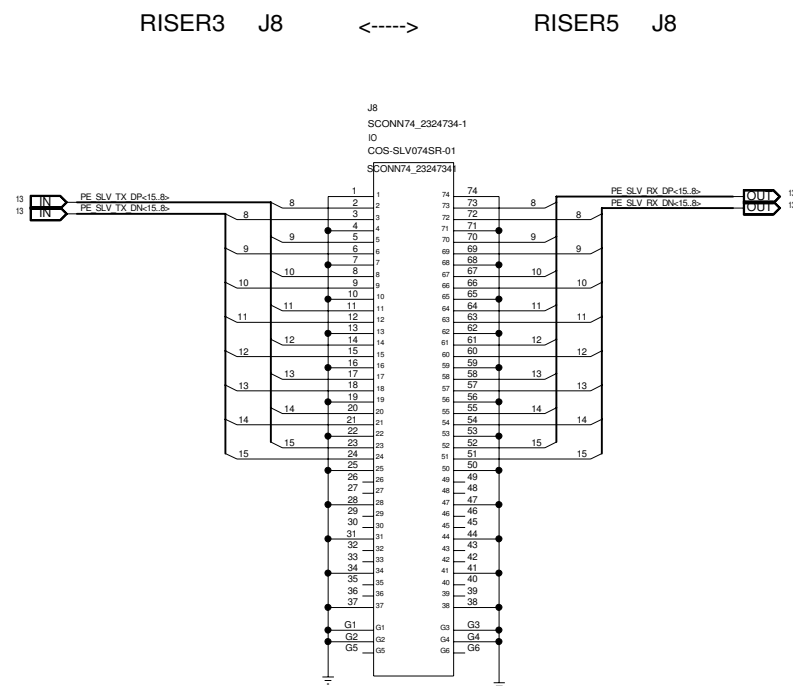
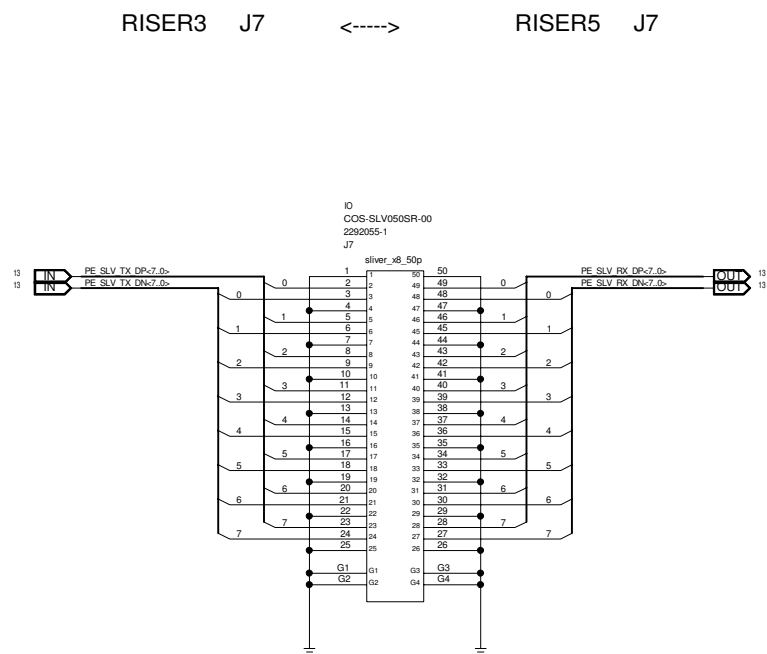
STRAP_NT1_UPSTRM_PORTSELX = 111 (NT1 DISABLE)

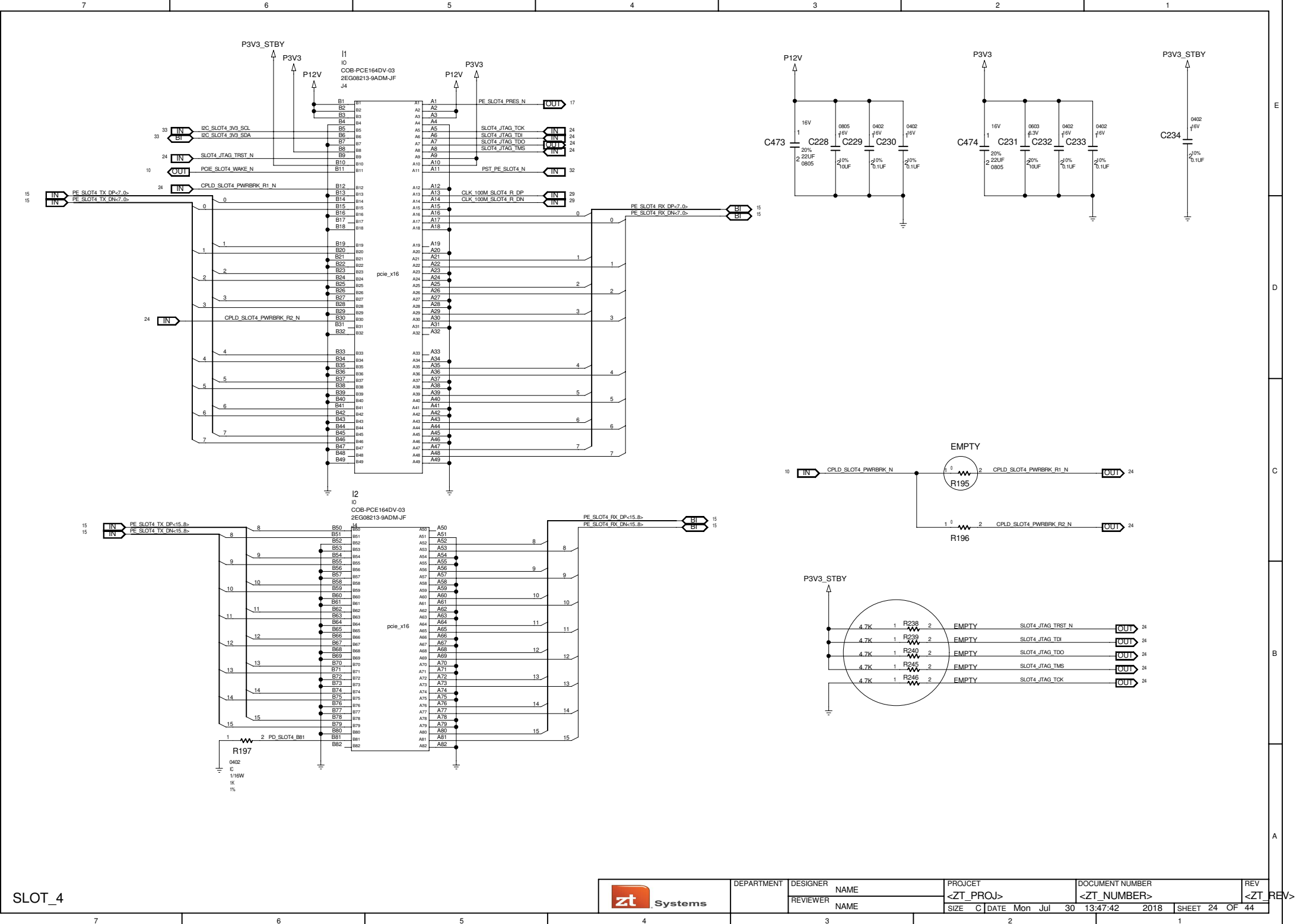


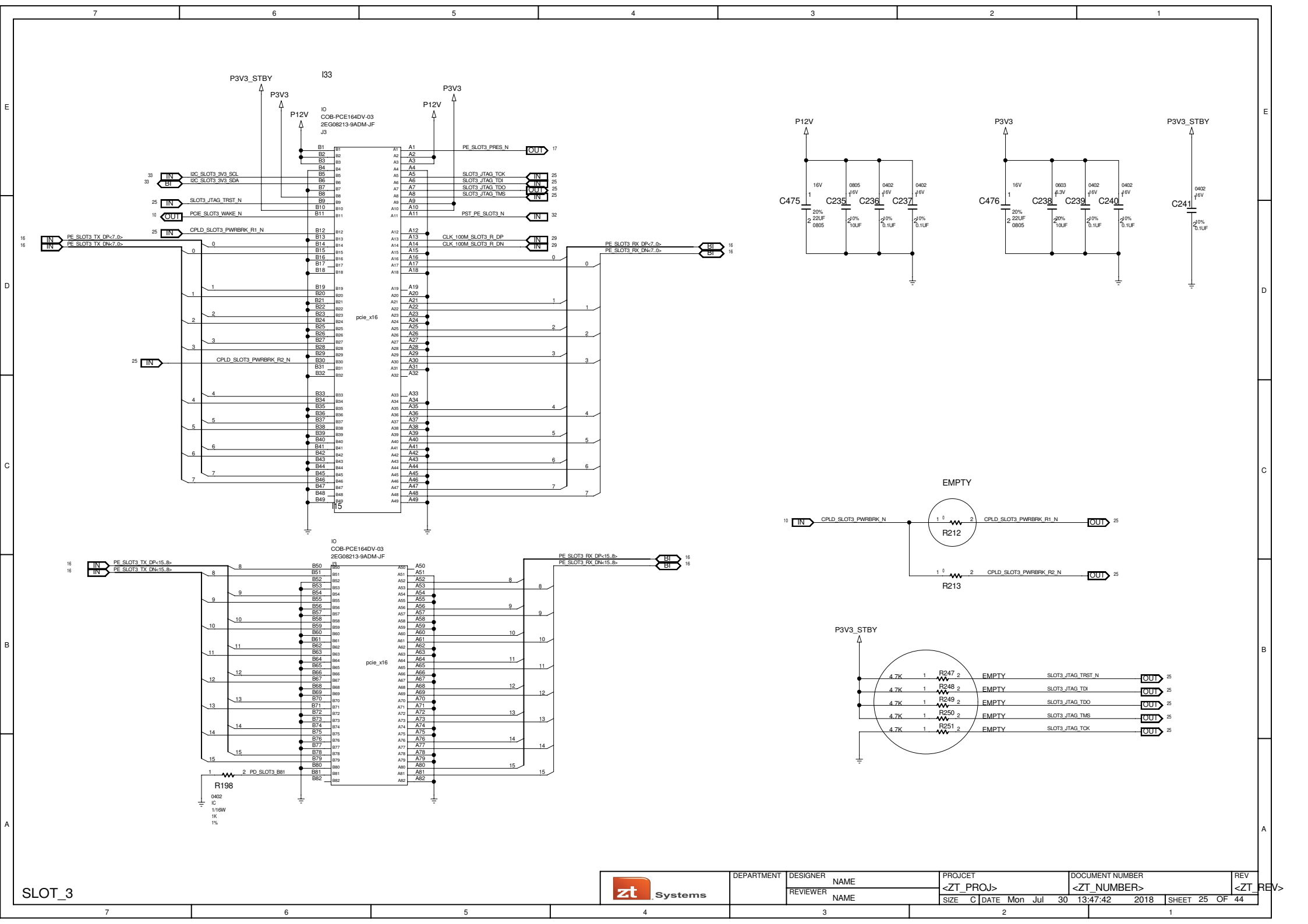
BASE MODE- THIS INPUT IS DON'T CARE
) SINGLE SWITCH(DEFAULT, NO VIRTUAL SWITCHES)

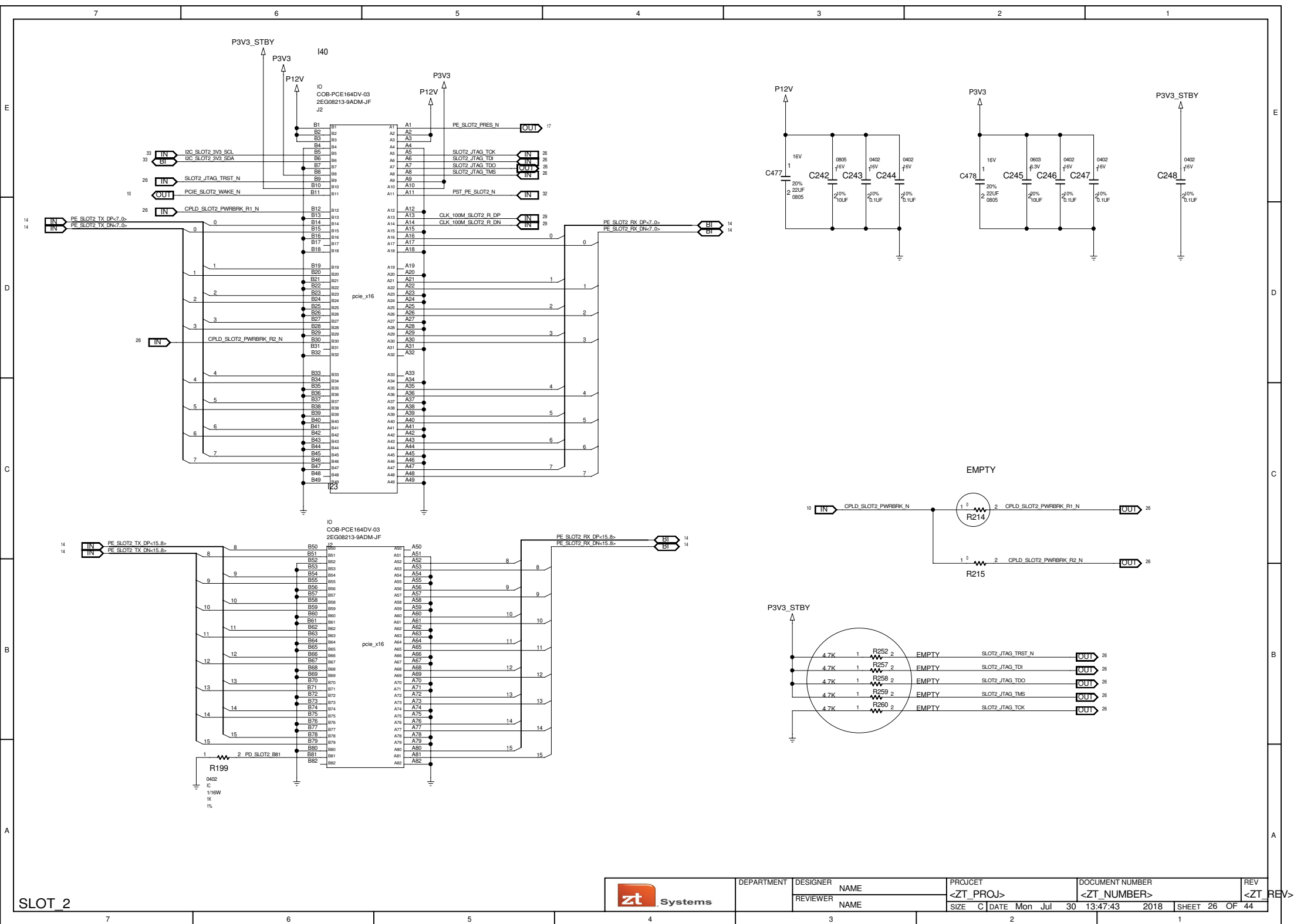


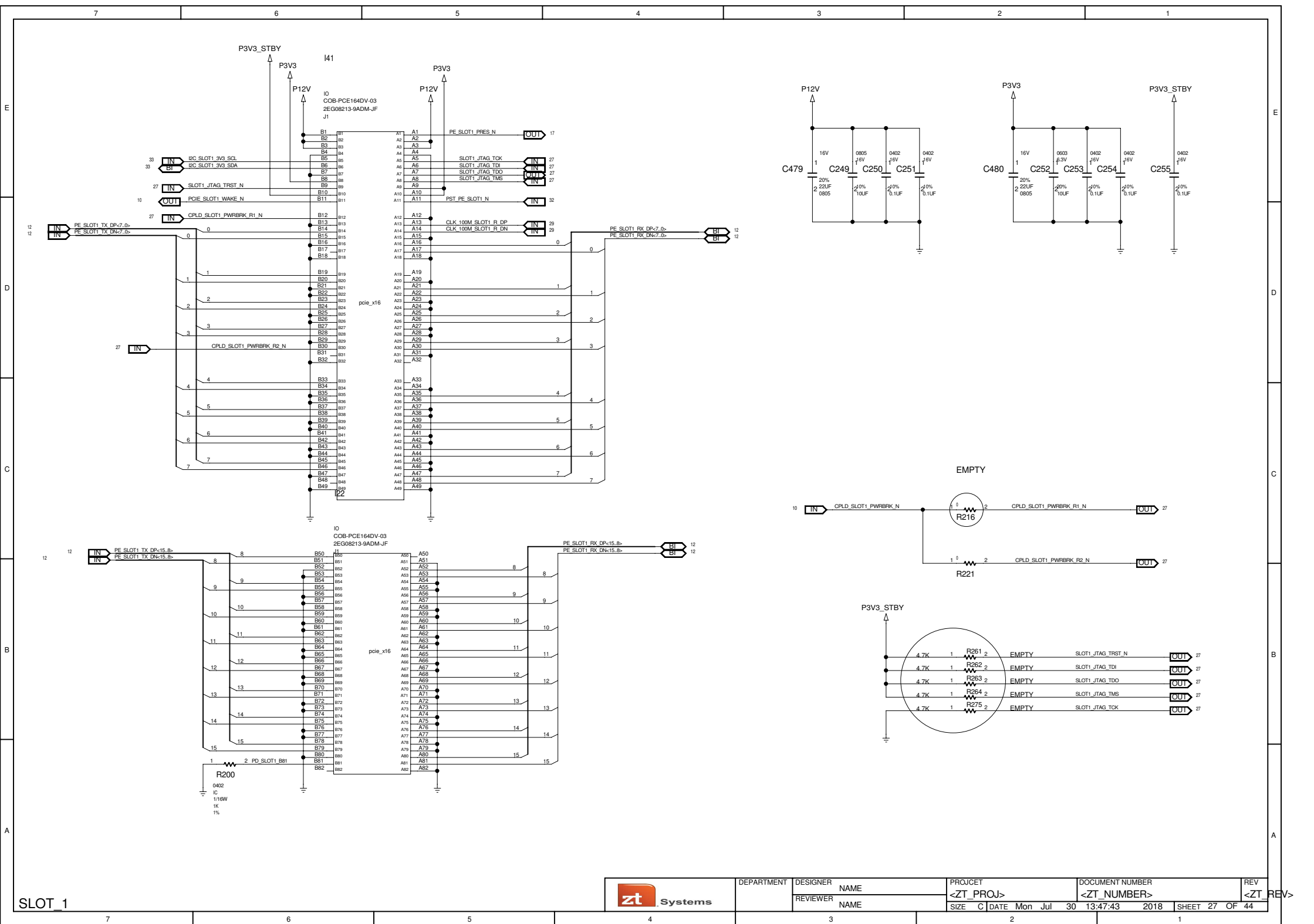
7							6							5							4							3							2							1																											
E																																										E																											
D																																										D																											
C																																										C																											
B																																										B																											
A																																										A																											
UNTITLED																																			DEPARTMENT							DESIGNER NAME							PROJECT							DOCUMENT NUMBER							REV						
																																										REVIEWER NAME							<ZT_PROJ>							<ZT_NUMBER>							<ZT_REV>						
7							6							5							4							3							2							1																											
SIZE							C							DATE							Tue Jan 09 11:45:46 2018							SHEET 22 OF 44																																									

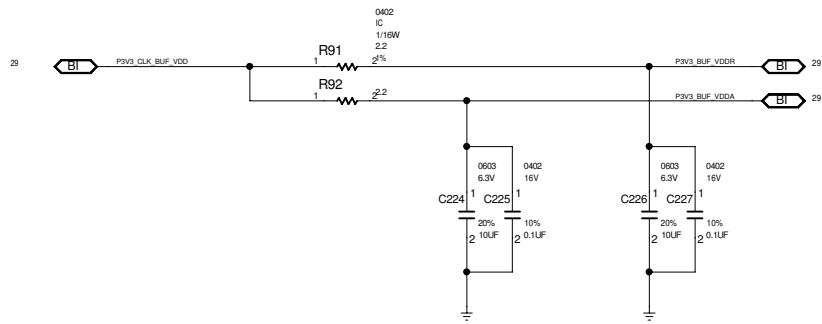








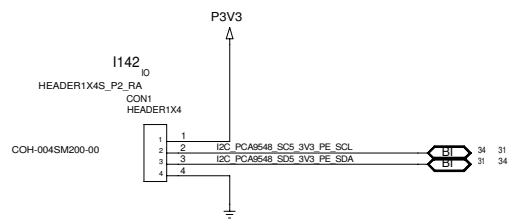
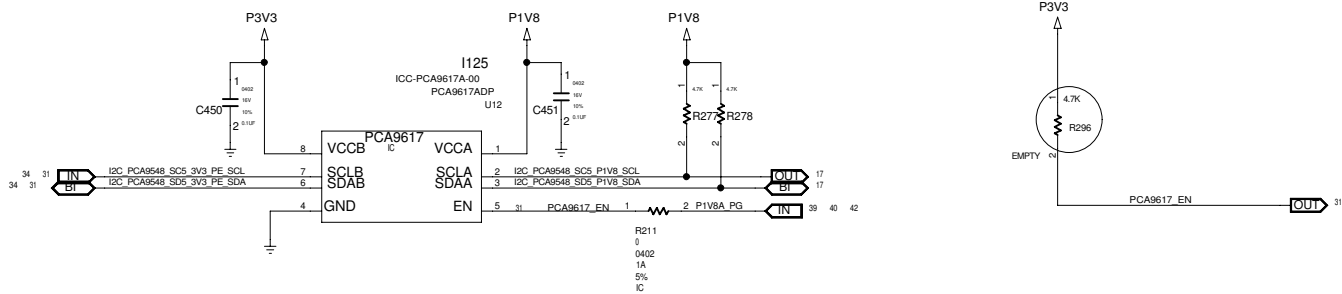


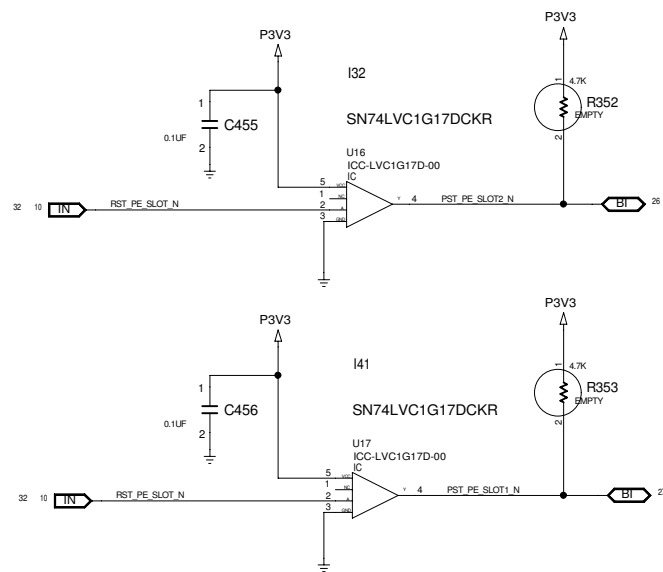
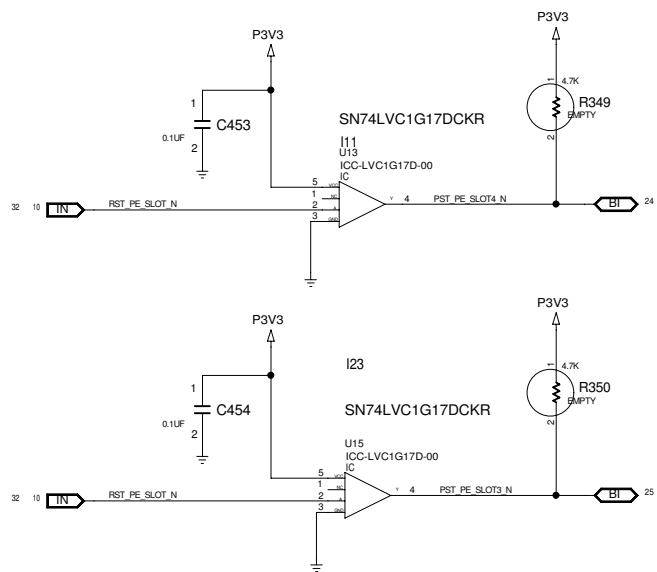
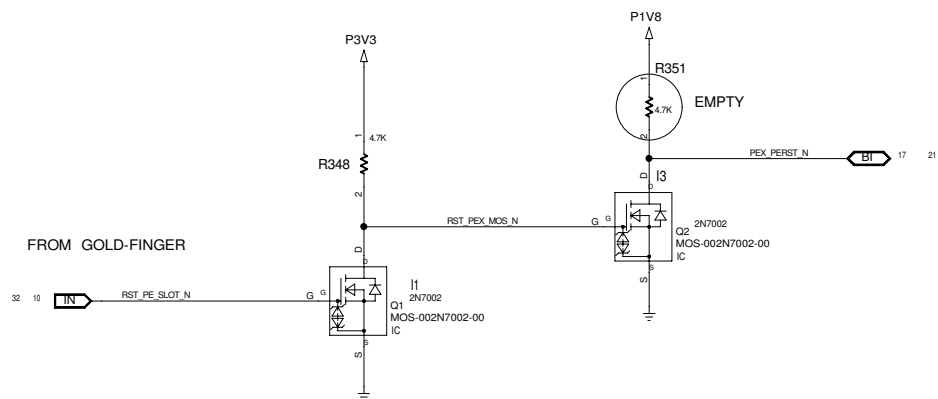


HiBW BypM LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode



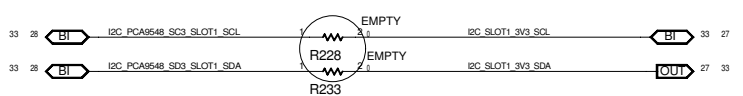
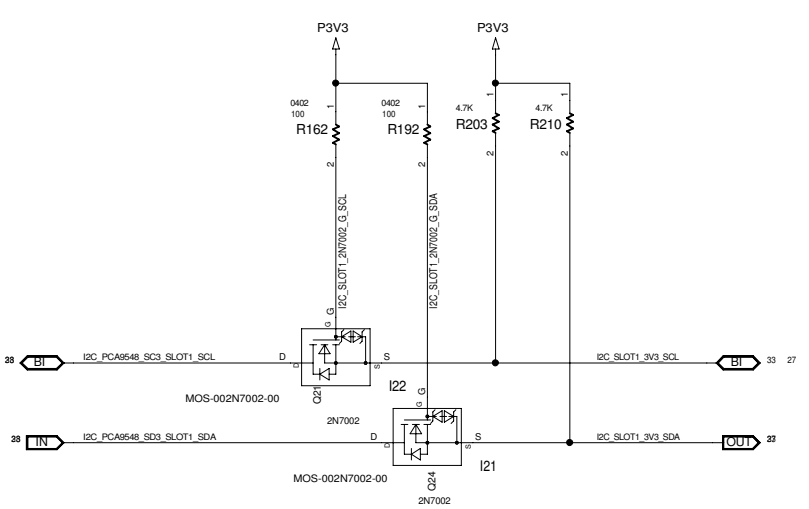
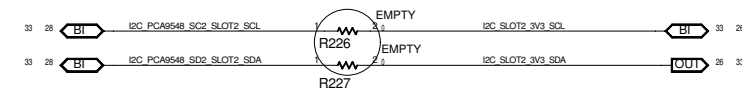
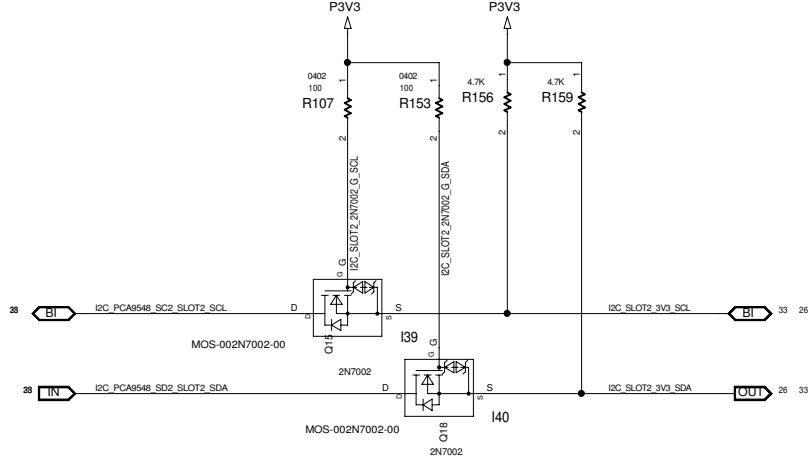
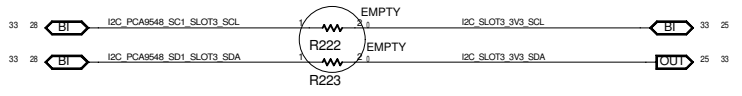
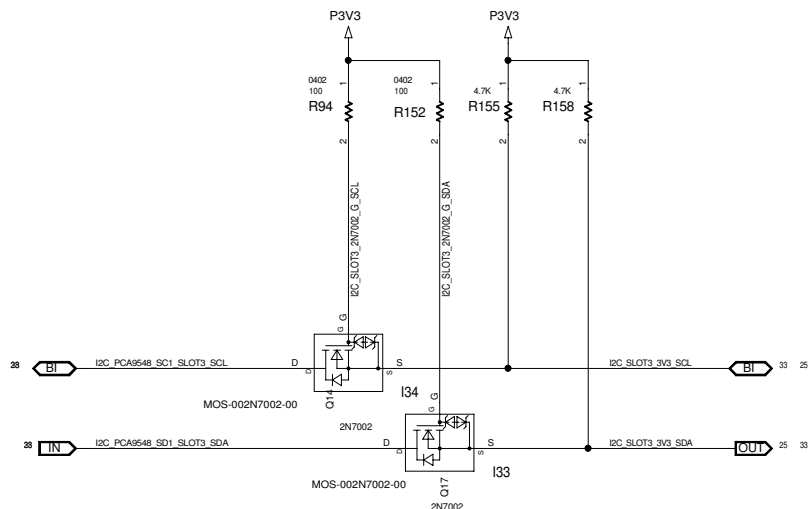
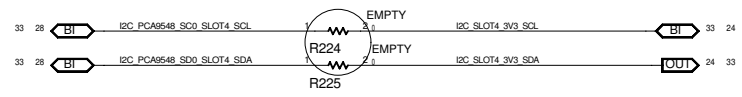
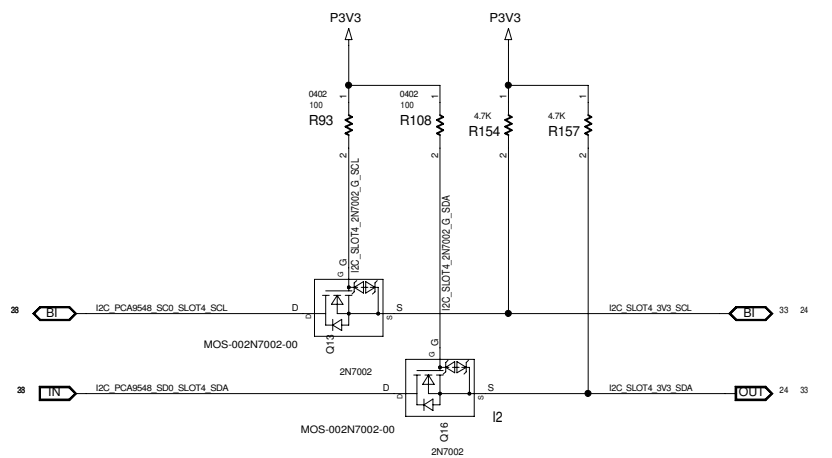


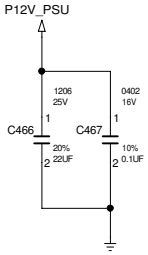
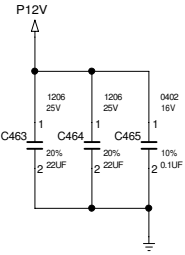
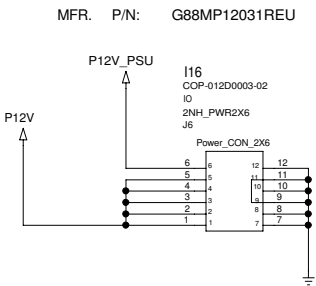


RESET BUFFER

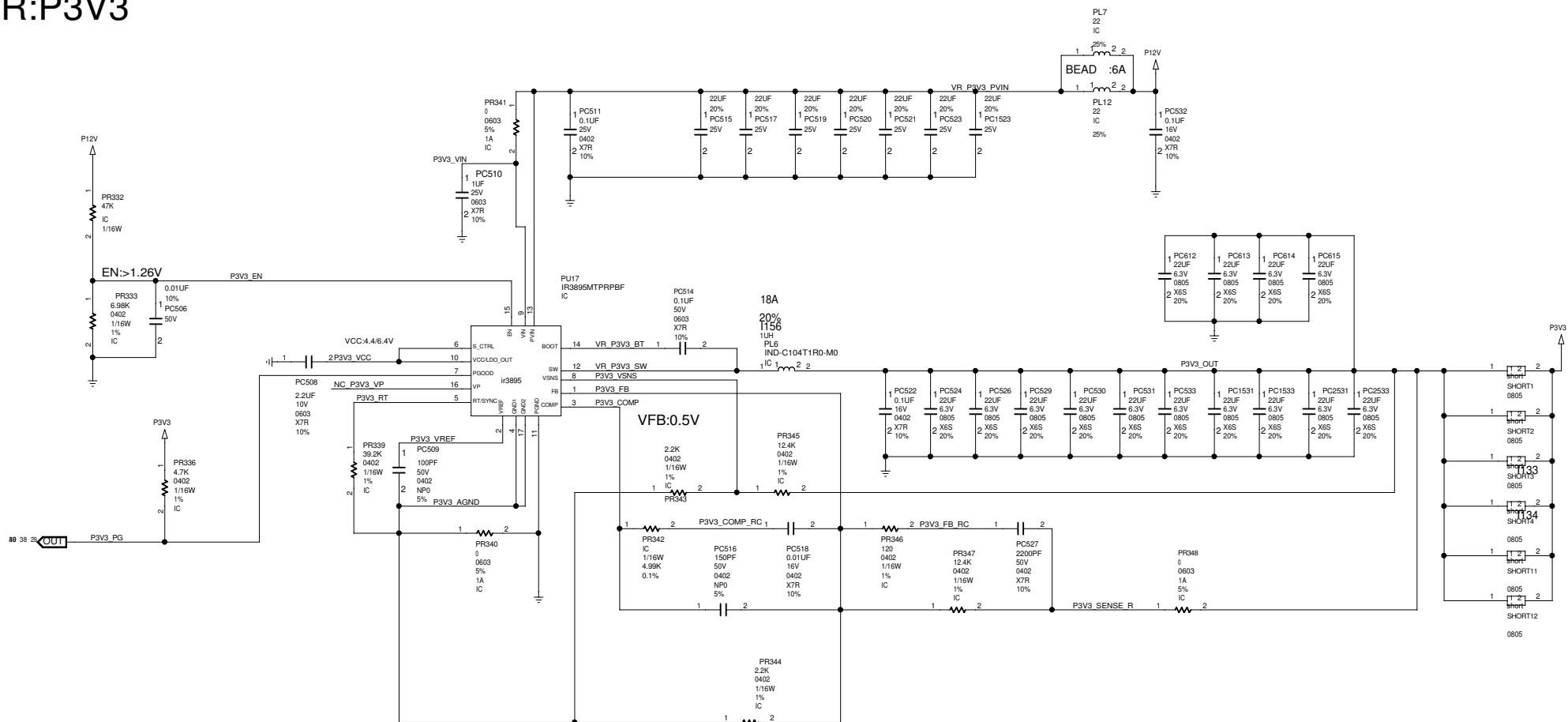


DEPARTMENT	DESIGNER NAME	PROJECT	DOCUMENT NUMBER	REV
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VR:P3V3



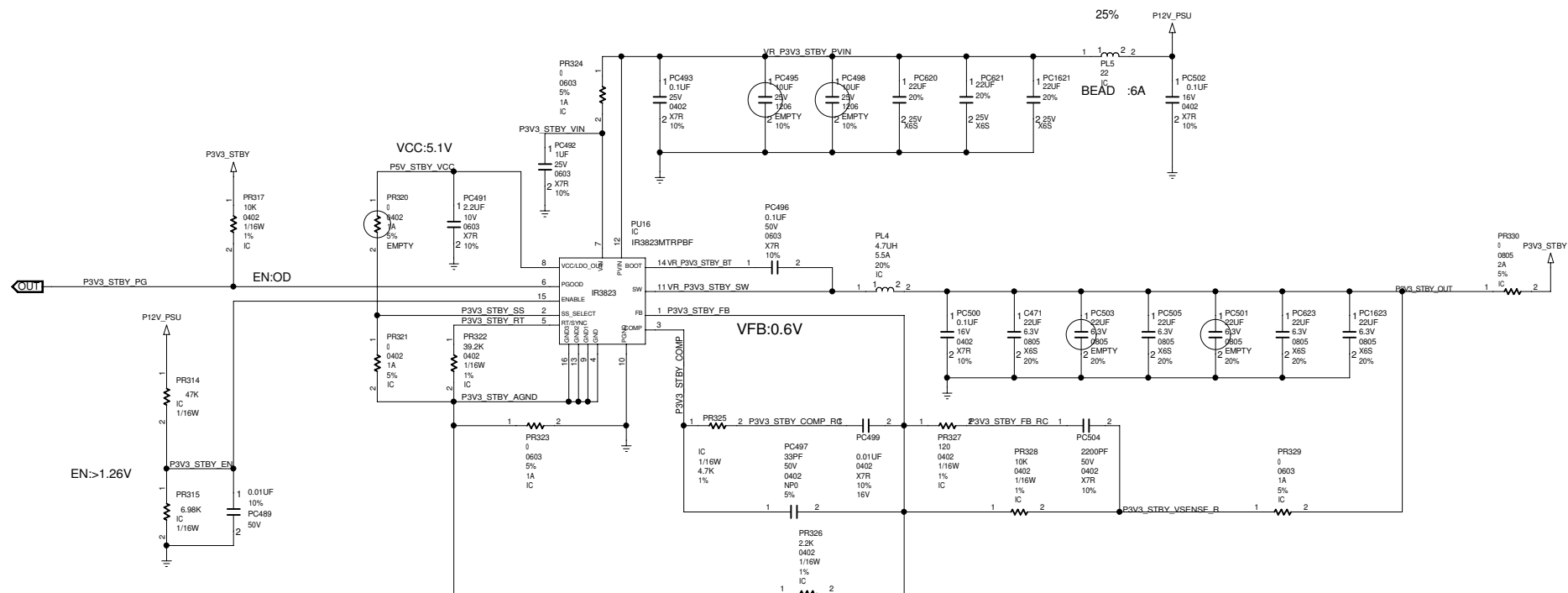
P12V TO P3V3 (AC:±5%)
TDC :12A
IMAX :12A
OCP :MIN=14.4A
FSW :605KHZ
SOLUTION :IR3895 (16A POL)

P3V3



DEPARTMENT	DESIGNER	NAME	PROJCT	DOCUMENT NUMBER	REV
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VR:P3V3_STBY



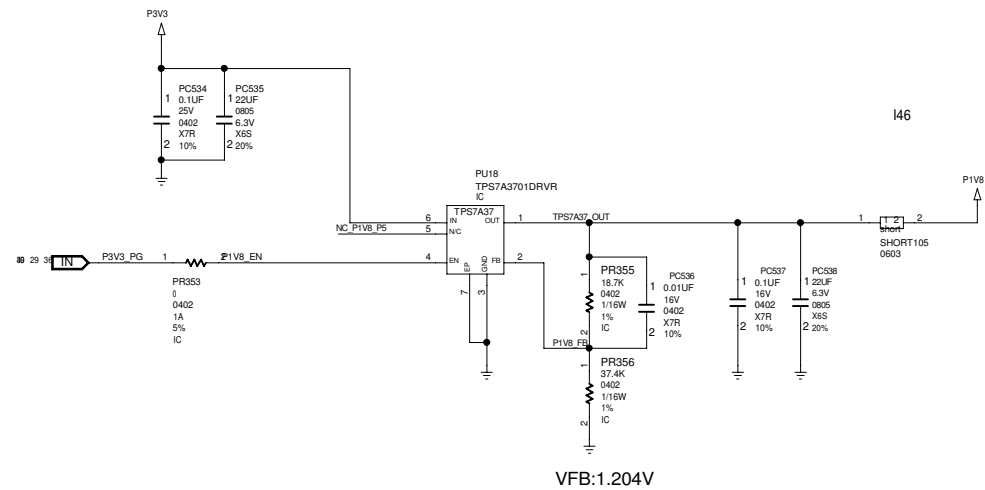
P12V_PSU TO P3V3_STBY (AC:+/-5%)
TDC :1.5A
IMAX :1.5A
OCP :MIN=1.8A
FSW :600KHZ
SOLUTION :IR3823 (3A POL)

P3V3_STBY



DEPARTMENT	DESIGNER	PROJECT				DOCUMENT NUMBER				REV			
	NAME	<ZT_PROJ>				<ZT_NUMBER>				<ZT_REV>			
	REVIEWER	SIZE	C	DATE	Fri	Dec	07	10:28:28	2018	SHEET	37	OF	44
	NAME												

VR:P1V8



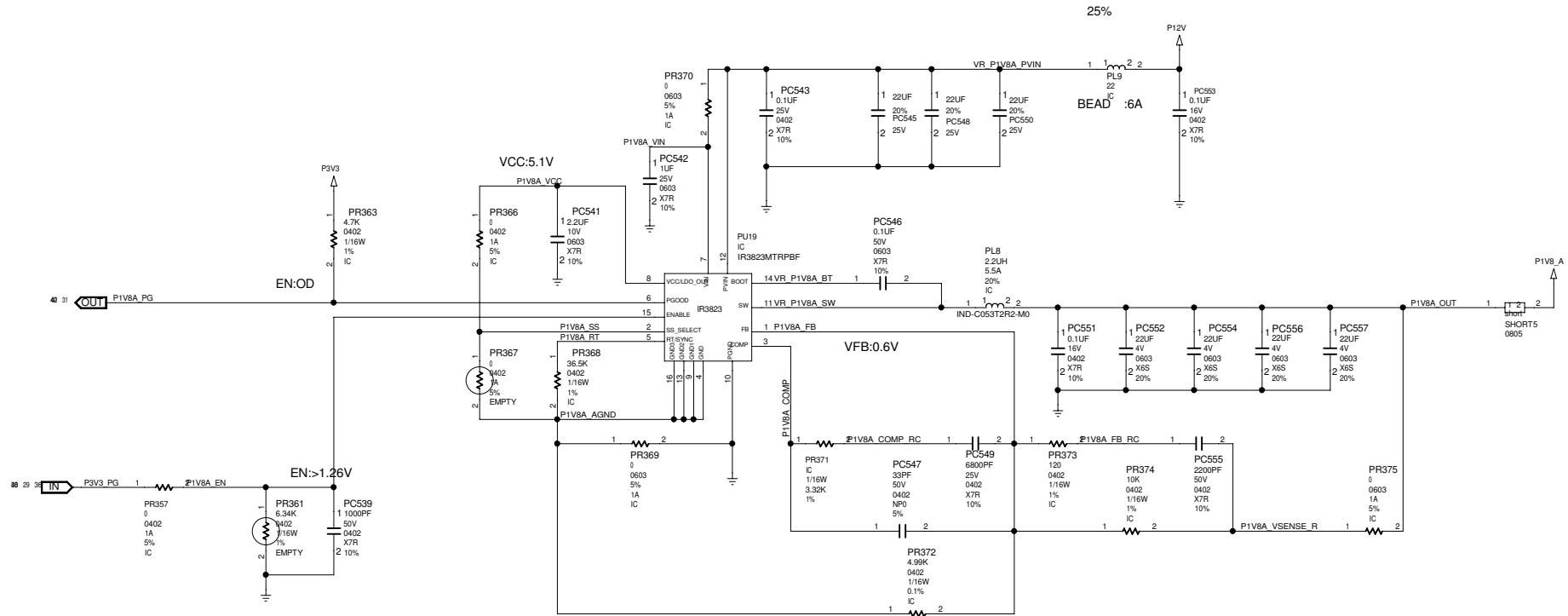
P3V3 TO P1V8 (AC:±5%)
TDC :0.1A
IMAX :0.1A
OCP :MIN=0.12A
SOLUTION :TPS7A37 (LDO)

P1V8



DEPARTMENT	DESIGNER NAME	PROJECT	DOCUMENT NUMBER	REV
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VR:P1V8_A

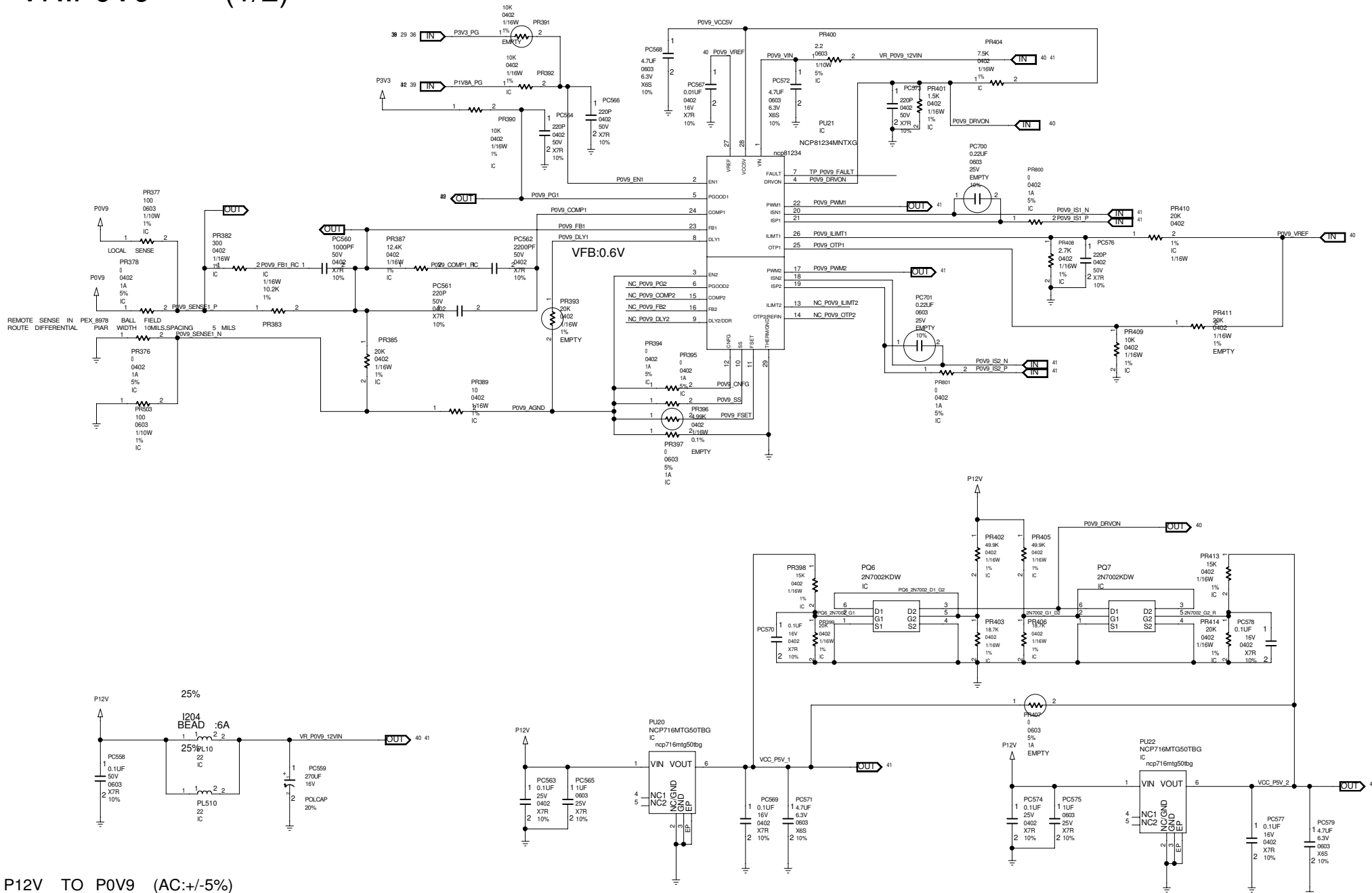


P12V TO P1V8_A (AC:±5%)
 TDC :2.3A
 IMAX :2.3A
 OCP :MIN=3.6A (FIXED BY VR CHIP)
 FSW :648KHZ
 SOLUTION :IR3823 (3A POL)



DEPARTMENT	DESIGNER NAME	PROJECT	DOCUMENT NUMBER	REV
	REVIEWER NAME	<ZT_PROJ>	<ZT_NUMBER>	<ZT_REV>
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VR:P0V9 (1/2)

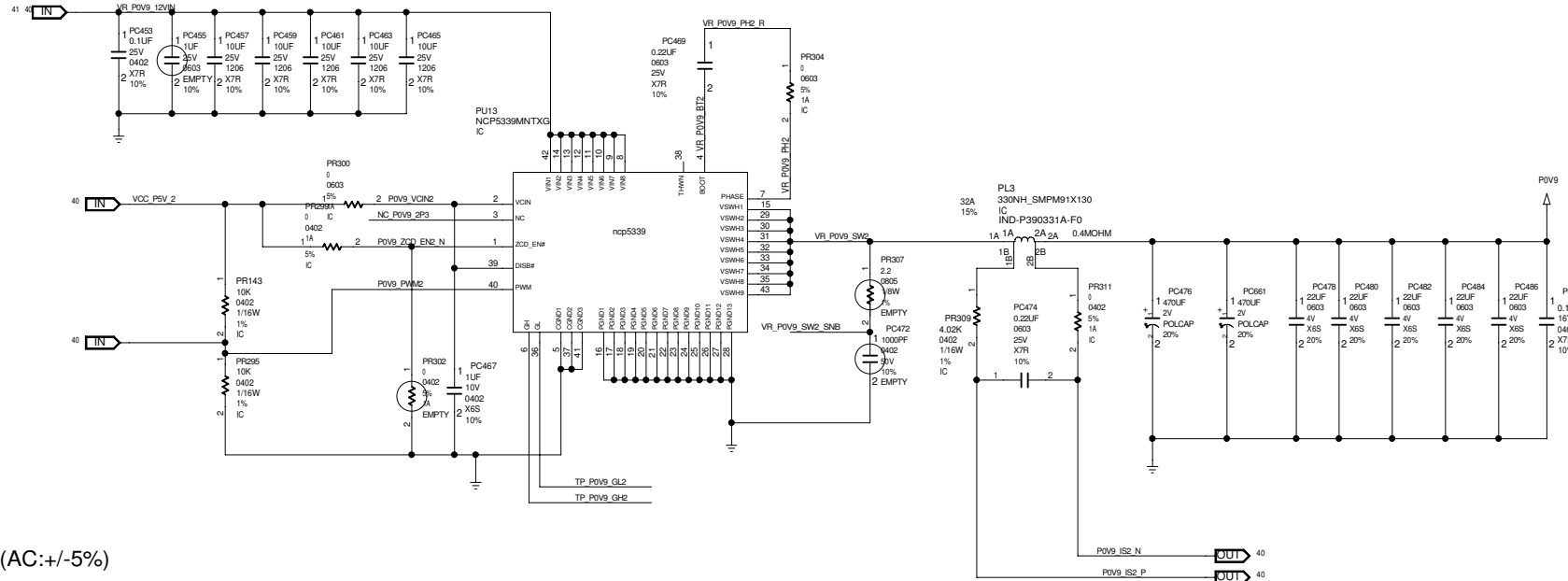
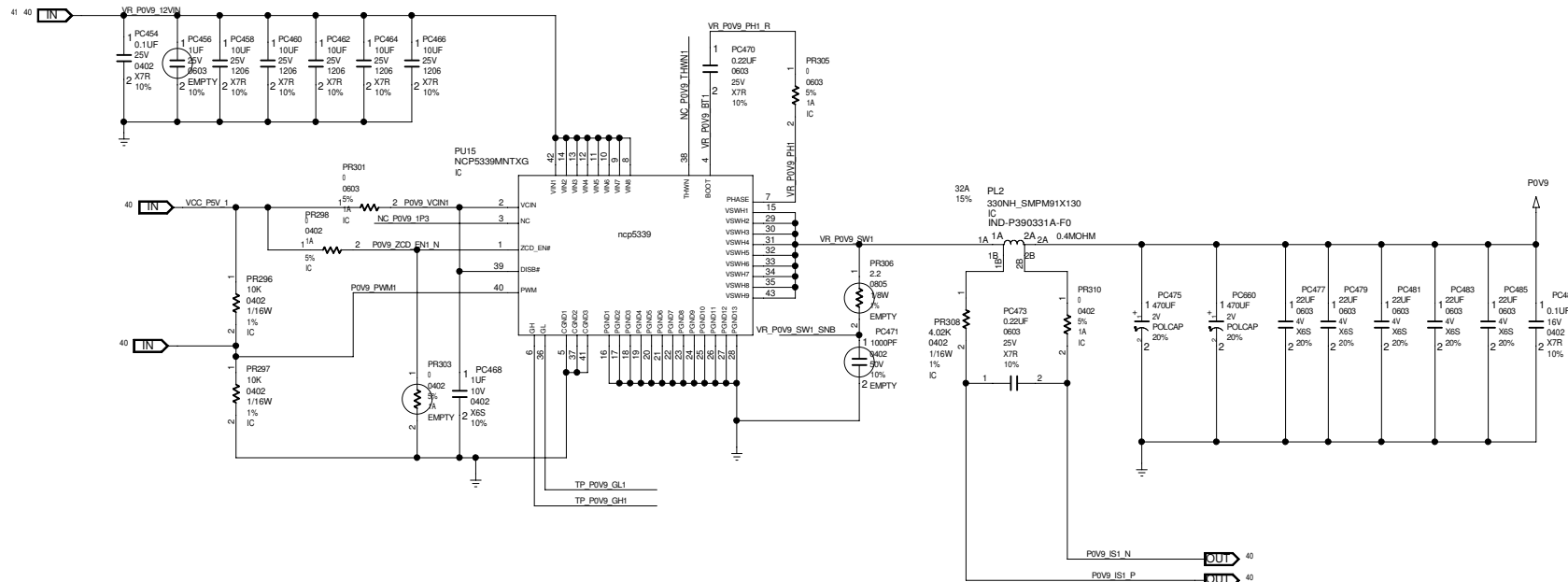


P12V TO P0V9 (AC:±5%)
TDC :32.4A
IMAX :36A
OCP :MIN=43.2A
FSW :400KHZ
SOLUTION :NCP81234 +NCP5339
POV9 1/2



DEPARTMENT	DESIGNER NAME	PROJECT	DOCUMENT NUMBER	REV
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VR:P0V9 (2/2)

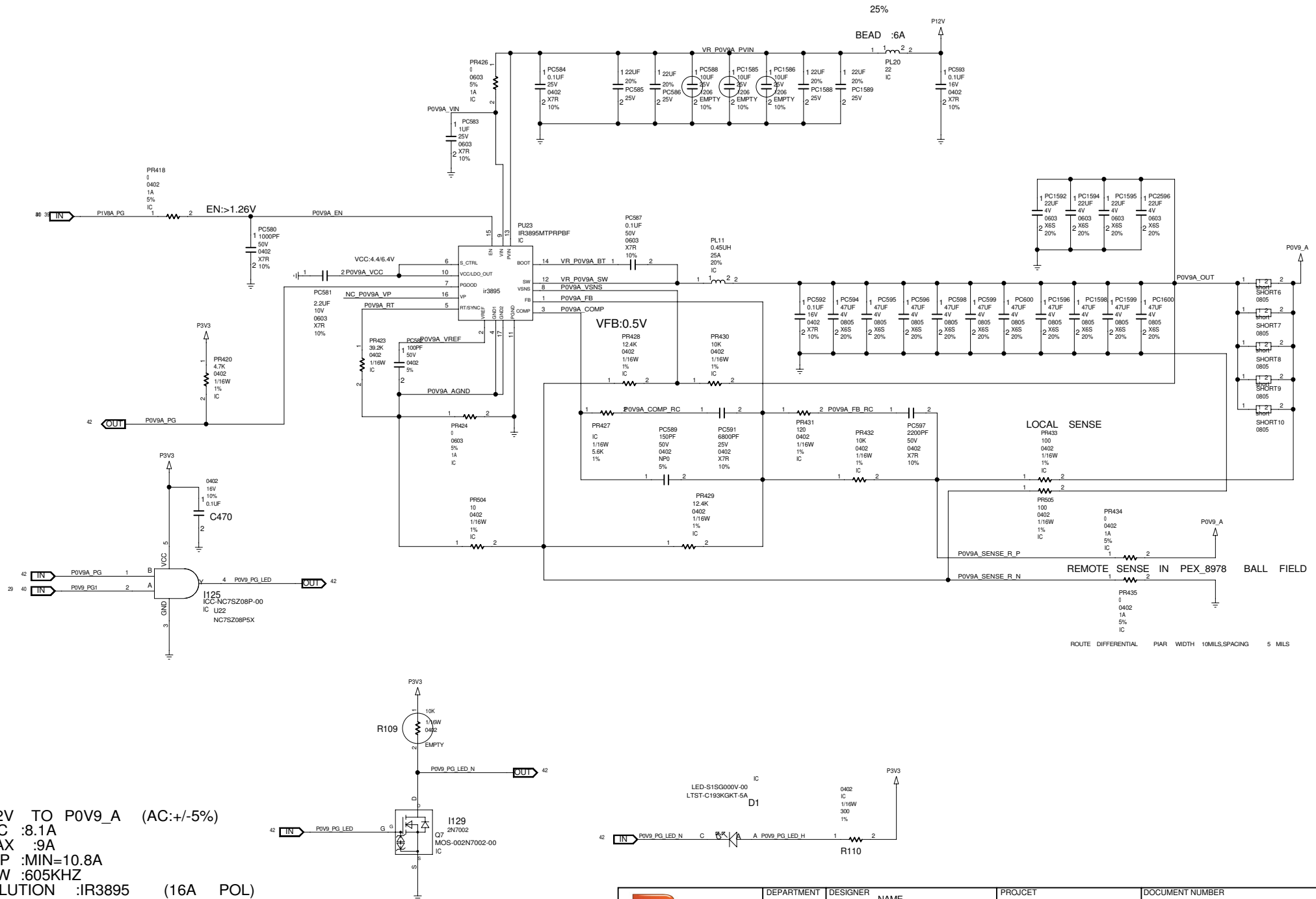


P12V TO P0V9 (AC:±5%)
TDC :32.4A
IMAX :36A
OCP :MIN=43.2A
FSW :400KHZ
SOLUTION :NCP81234 +NCP5339
P0V9 2/2



DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
	REVIEWER	NAME	<ZT_PROJ>	<ZT_NUMBER>	<ZT_REV>
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VR:P0V9_A



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P12V TO P0V9_A (AC: +/-5%)
TDC :8.1A
IMAX :9A
OCP :MIN=10.8A
FSW :605KHZ
SOLUTION :IR3895 (16A POL)
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P0V9_A

