



OPEN
Compute Project

Advanced Programmable Switch

BF2556X-1T

Hardware Design Specification

V.02



Contents

1. Overview	5
1.1. Purpose	5
1.2. Functional Introduction.....	5
1.3. Physical Overview Front Panel.....	5
2. Product Overview	6
2.1. Features	6
2.2. Key Components.....	7
2.3. System Block Diagram.....	8
2.4. I2C Bus	8
2.5. System Reset.....	10
2.6. Interrupt.....	12
2.7. Power Tree	14
2.8. Power up Sequence.....	15
2.9. Clock Tree	15
2.10. SyncE and 1588	16
3. BMC Sub-system	18
3.1. BMC Sub-system Block Diagram	18
3.2. Hardware Strap Configuration.....	19
3.3. UART Connection.....	22
3.4. FAN Control.....	22
4. MDC/MDIO	25
4.1. Functional Block Diagram	25
4.2. MIIM.....	25
4.3. Network Interface	26
5. LED.....	35
5.1. System LED	35
5.2. Management Port LED.....	36
5.3. PSU LED	37
5.4. FAN LED	38
5.5. SFP28/QSFP28 Port LED.....	38

6.	CLPD	40
6.1.	Registers Mapping Table	40
6.2.	CPLD Upgrading	40
7.	Power Consumption and Monitor	41
8.	System Cooling	43
8.1.	FAN module	43
9.	PSU Sub-System	45
9.1.	Feature	45
9.2.	Dimension	46
9.3.	Output Connector	46
9.3.1.	Power supply connector	46
9.3.2.	CPU to Main board connector	47
9.3.3.	Main to daughter board connector	49
10.	Mechanical	51
10.1.	Dimension	51
10.2.	Feature	51
11.	Environment and Regulatory	52

Revision History

Rev.	Date	Revision Description
V0.1	2018/8/7	Initial release
V0.2	2018/11/8	I2C and CPLD spec update
V0.3	2019/1/10	Update panel, block diagram, SyncE, 1588

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1. Overview

1.1. Purpose

This hardware functional specification document provides the accurate information that must be known and followed up for all steps of hardware and software development on. Once this document is finalized or released, all features, functions, interface connections, port mapping, register contents, circuit implementation, etc. specified in this hardware functional specification should be followed up tightly in subsequent development phases. Schematic and all test plans are based upon this hardware functional specification.

1.2. Functional Introduction

This document describes the technical specifications of the 48x25G and 8x100G Top of Rack/Leaf switch. The model which support 16 ports 1G/10G/25G, 32 ports 10G/25G, and 8 ports 10G/25G /40G/50G/100G.

The model supports 8 port QSFP28 ports that each can operate at 4x10G or 4x25G with QSFP28-4xSFP28 break out cables, 2x50G with QSFP28-2xQSFP28 break out cables, 40G with standard QSFP+ optics/DAC cables, and 100G with QSFP28 optics/DAC cables.

And the model support Sync-E and IEEE 1588 function.

1.3. Physical Overview Front Panel

Front Panel



Figure 1. Front Panel Drawing

Rear Panel



Figure 2. Rear Panel Drawing

2. Product Overview

2.1. Features

The system uses Barefoot BFN-T10-032D-020 (Tofino 2.0T) Switch Chip which can support 20 x 100GE ports.

Major features are:

- 2.0 Tbps bandwidth
- One Barefoot BFN-T10-032D-020(Tofino 2.0T) Switch ASIC
 - Ethernet support 80x25G SERDES ports
 - Management SERDES support four ports 10G-KR
 - PCIe Gen 3 x 4 lanes
- Eight Marvell 98PX1024
 - Single chip support 4x25G SERDES
- Network Interface
 - 48 x 25G SFP28 and 8 x 100G QSFP28
 - SFP28 port1~16 can configure into 1G/10G/25G.
 - SFP28 port17~48 can configure into 10G/25G.
 - Each QSFP28 port can configure into 1x100G, 2x50G, 4x25G, 1x40G or 4x10G Mode.
- CPU Module: Optional Module design for flexibility
 - Intel® Xeon® Processors D1527 (BDXDE)
- BMC: Base Board Management Controller
 - BMC is a specialized service processor that monitors the physical state of a system.
 - ASPEED AST2520
- Management Port:
 - 3x RJ45 10/100/1000Mbps OOBM(Out Of Band Management) port
 - 1xConsole RJ45
 - 1xUSB 3.0
- FAN Tray:
 - Four 40mmx56mm Fan-tray
 - Supporting 3+1 redundancy
 - Support front to back and back to front air direction.
- PSU:
 - 1+1 redundant PSU

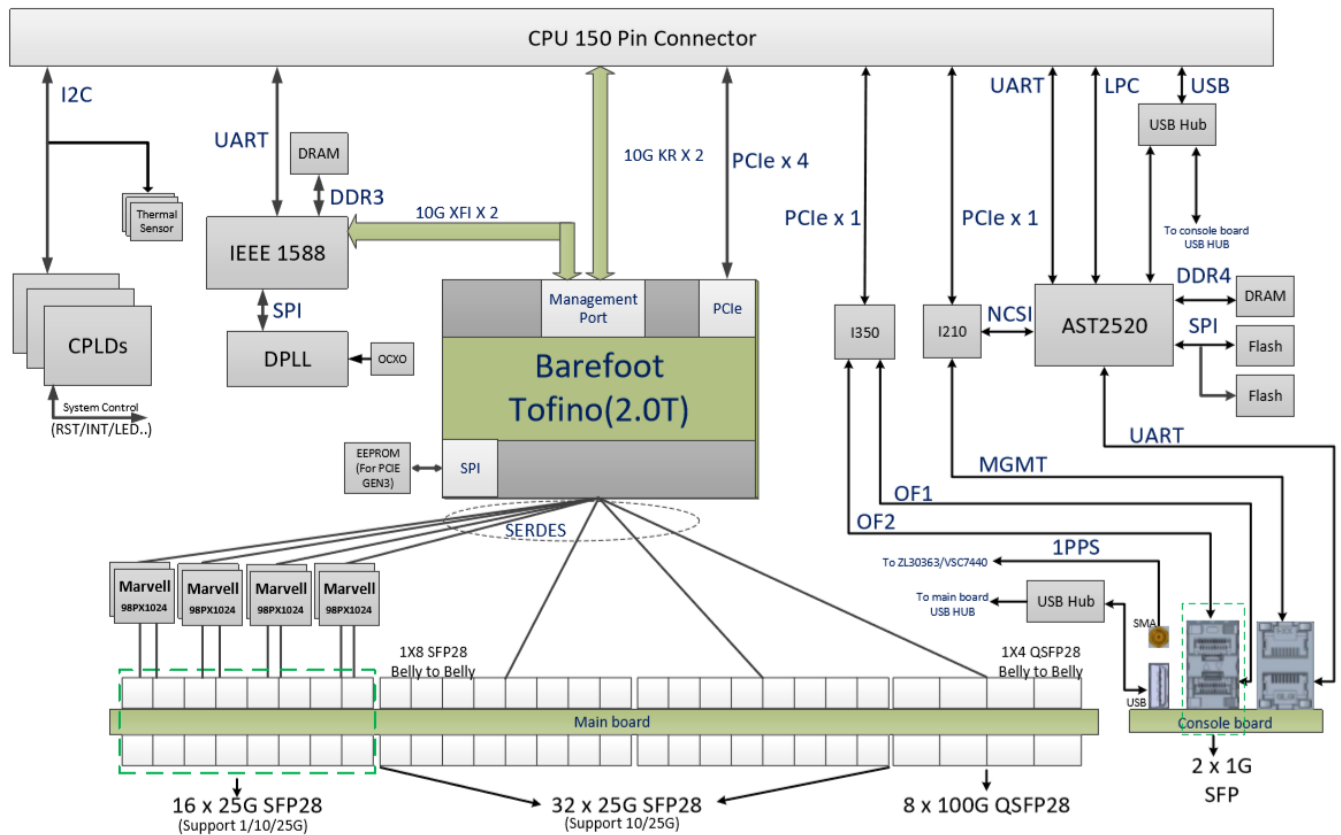
- Each PSU will be supporting 850W power to system.
- 12V standby power for system management chips.
- Support DC power supply

2.2. Key Components

	MFG PN	Quantity
CPU	Intel BDXDE	1
Flash (BIOS)	16MB NOR FLASH	2
Memory (CPU)	16G DDR4 MODULE	2
Storage	128GB MLC SSD	1
MAC	Tofino 2.0T	1
PIPE	98PX1024	8
BMC	AST2520A2-GP	1
Memory (BMC)	512Mbyte DDR4 on board	1
BMC Flash	32MB NOR FLASH	2
OOBM NIC	WGI210AT/ WGI350AT	2
System CPLD	Lattice LCMX03LF-2100C	1
Port CPLD	Lattice LCMX03L/LF-4300	2
FAN	GFC0412DS-SM06XMP	4
PSU	DPS-850AB-4 Q (850W AC PSU)	2

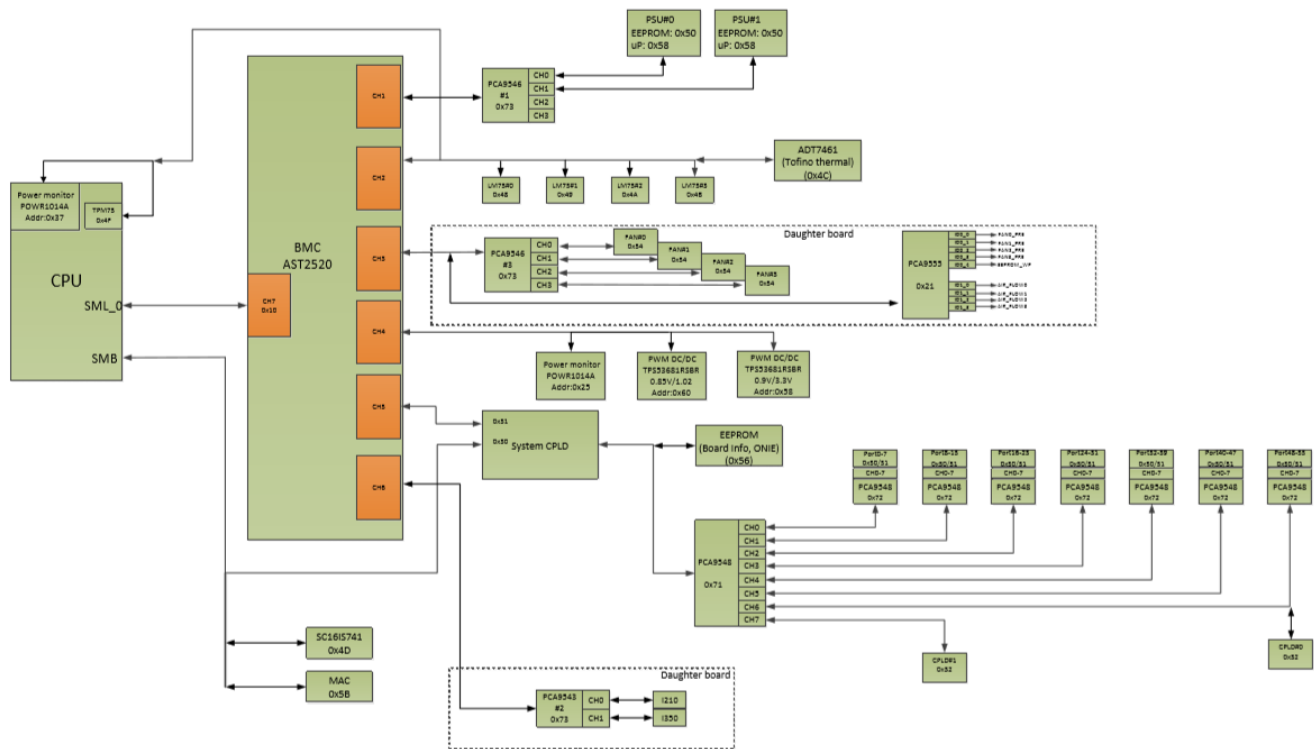
2.3. System Block Diagram

Block Diagram



2.4. I2C Bus

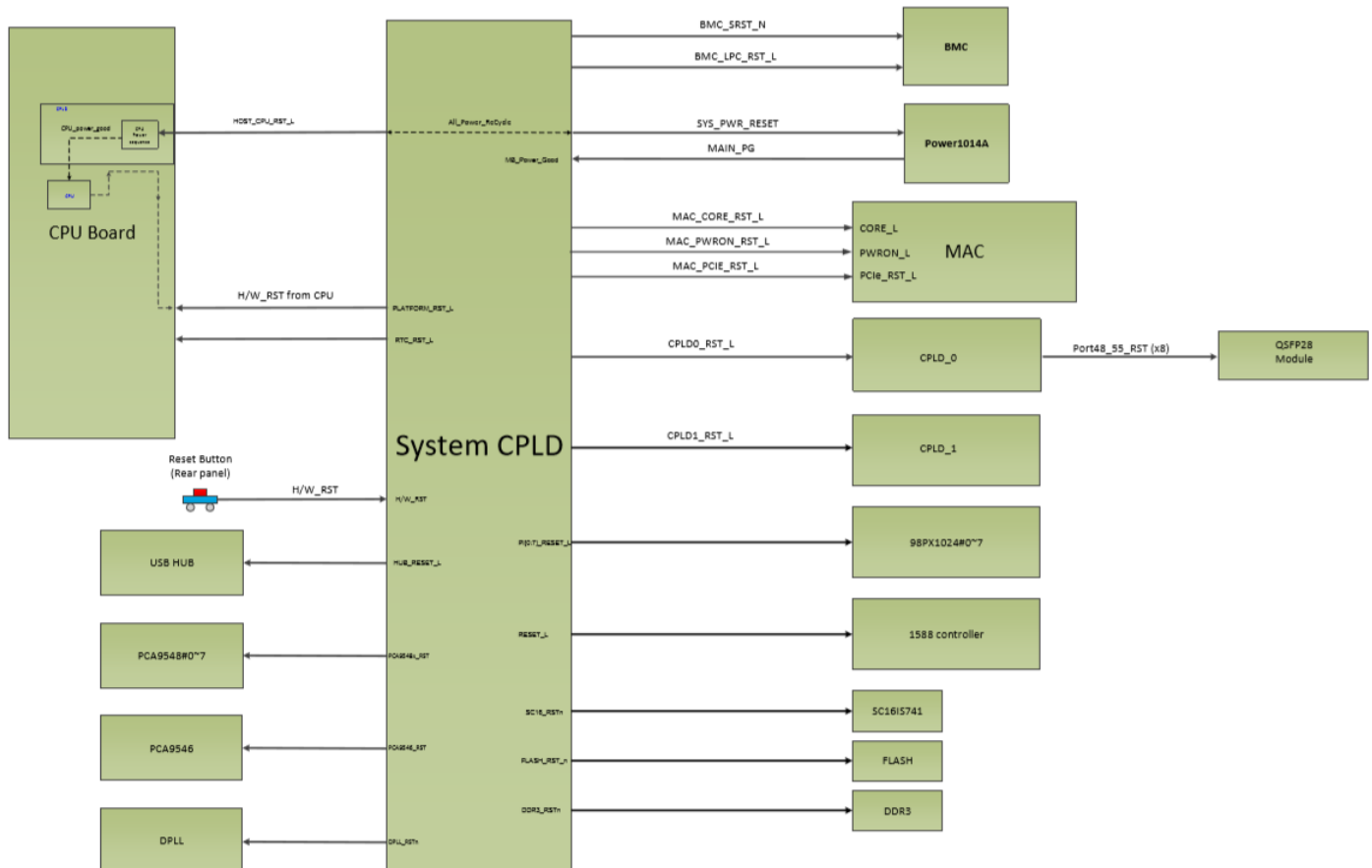
BMC I2C Bus is used for access PSU, thermal sensor, DC VRs, CPLDs, Optical module, DAC etc. System CPLD and port CPLDs can be access by either BMC or Host CPU. There is I2C arbitration handled by system CPLD and default I2C bus is set to BMC. If Host CPU want to access I2C bus, need to set I2C arbitration bit to high (in system CPLD spec address offset 0x0f bit0).



I2C BUS	Component	Adr.	Note
PSU	PSU0(uP)	0x58	PCA9546(0x73)□CH0
	PSU0 (EEPROM)	0x50	
	PSU1(uP)	0x58	PCA9546(0x73)□CH1
	PSU1 (EEPROM)	0x50	
I2C BUS	Component	Adr.	Note
FAN Tray	Need BMC set GPIOA4 to High		
	FAN Tray 0	0x54	PCA9546(0x73)□CH0
	FAN Tray 1	0x54	PCA9546(0x73)□CH1
	FAN Tray 2	0x54	PCA9546(0x73)□CH2
	FAN Tray 3	0x54	PCA9546(0x73)□CH3
I2C BUS	Component	Adr.	Note
CPLD	System CPLD	0X30 0X31	0X30 for Host CPU 0X31 for BMC
	CPLD0	0x32	PCA9548(0x71)□CH6
	CPLD1	0x32	PCA9548(0x71)□CH7
I2C BUS	Component	Adr.	Note
Temp Sensor	LM75	0x48	On main board
	LM75	0x49	On main board
	LM75	0x4A	On main board
	LM75	0X4B	On main board
	LM75	0X4F	On CPU board
	ADT7461	0X4C	For MAC
I2C BUS	Component	Adr.	Note
PWM Voltage Regulator	TPS53681	0X60	Control MAC_0V85 and PIPE 1.02V
	TPS53681	0X58	Control MAC_0V9 and 3.3V

2.5. System Reset

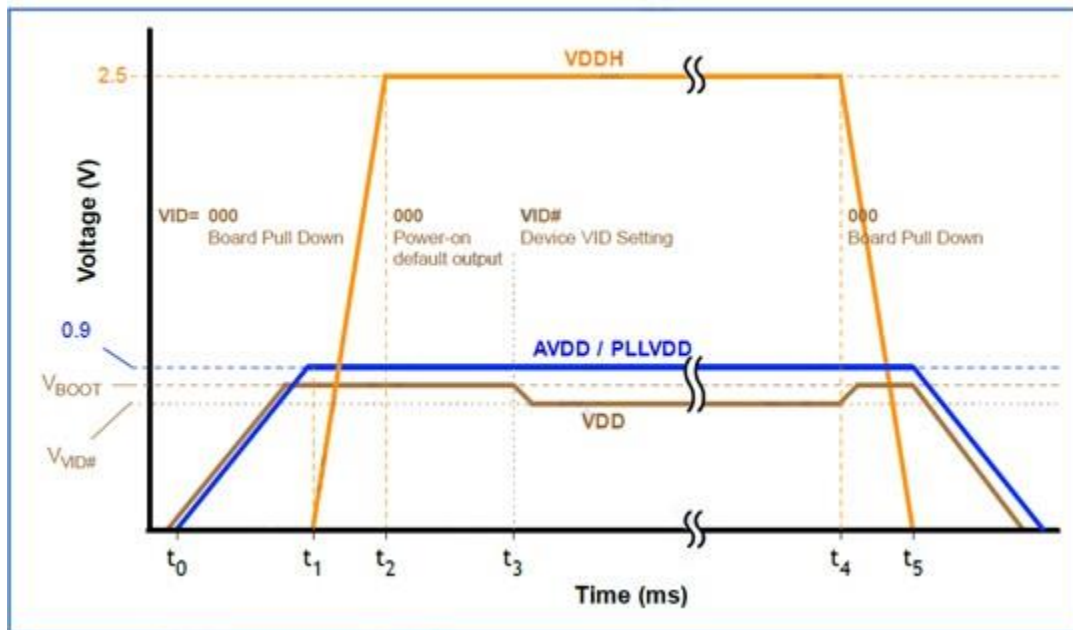
Once the system power up which System CPLD will generate the power on reset (POR) to all device directly. The POR timing is controlled by system CPLD to meet the reset timing requirement of each device.



MAC Tofino

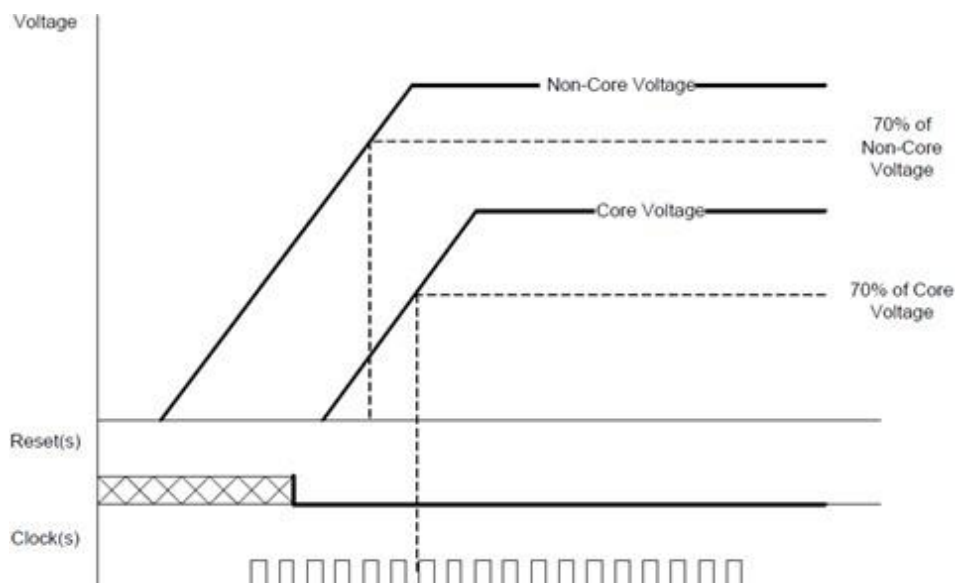
The following illustrated Power up and Reset timing.

The 10k Device requires VDD and AVDD/PLLVDV⁷ supplies be powered on together first (see t_0 in the figure below). Immediately after VDD and AVDD are stable, power-on the CMOS IO supply VDDH (see t_1).



PIPE 98PX1024

- The Non-Core voltages (I/O and Analog) must reach 70% of their voltage level before the Core voltages reach 70% of their voltage level.
The order of the power up sequence between the Non-Core voltages is unimportant as long as the Non-Core voltages power up before the Core voltages reach 70% of their voltage level. See [Figure 2, Power Up Sequence Example](#).
- The reset signal(s) must be asserted before the Core voltages reach 70% of their voltage level, see [Figure 2](#).
- The reference clock(s) inputs must toggle with their respective voltage levels before the Core voltages reach 70% of their voltage level, see [Figure 2](#).



1588 controller

During power on and off, V_{DD_A} , V_{DD_HS} , and V_{DD_VS} must never be more than 300 mV above V_{DD} .

V_{DD_HS} and V_{DD_VS} must be powered, even if the associated interface is not used. These power supplies must not remain at ground or left floating.

A maximum delay of 100 ms from V_{DD_IODDR} to V_{DD} is recommended. There is no requirement from V_{DD} to V_{DD_IODDR} .

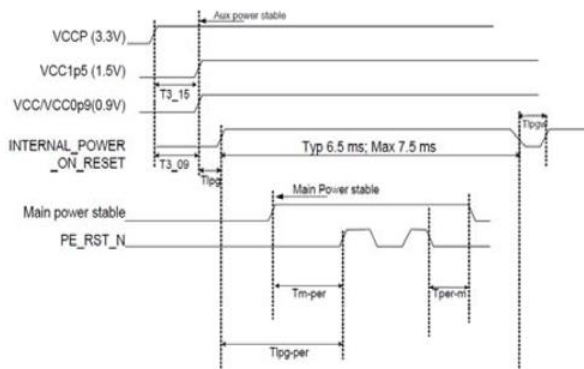
The V_{DD_IODDR} supply can remain at ground or left floating if not used. If V_{DD_IODDR} is grounded, DDR_Vref must also be grounded.

There are no sequencing requirements for V_{DD_IO} .

BMC AST2520

Power on reset SRST# will reset full chip (including DRAM and JTAG) except partial PCIE/VGA/2D functions. It must be asserted at least 1 ms after all powers ready (reference power-up sequence).

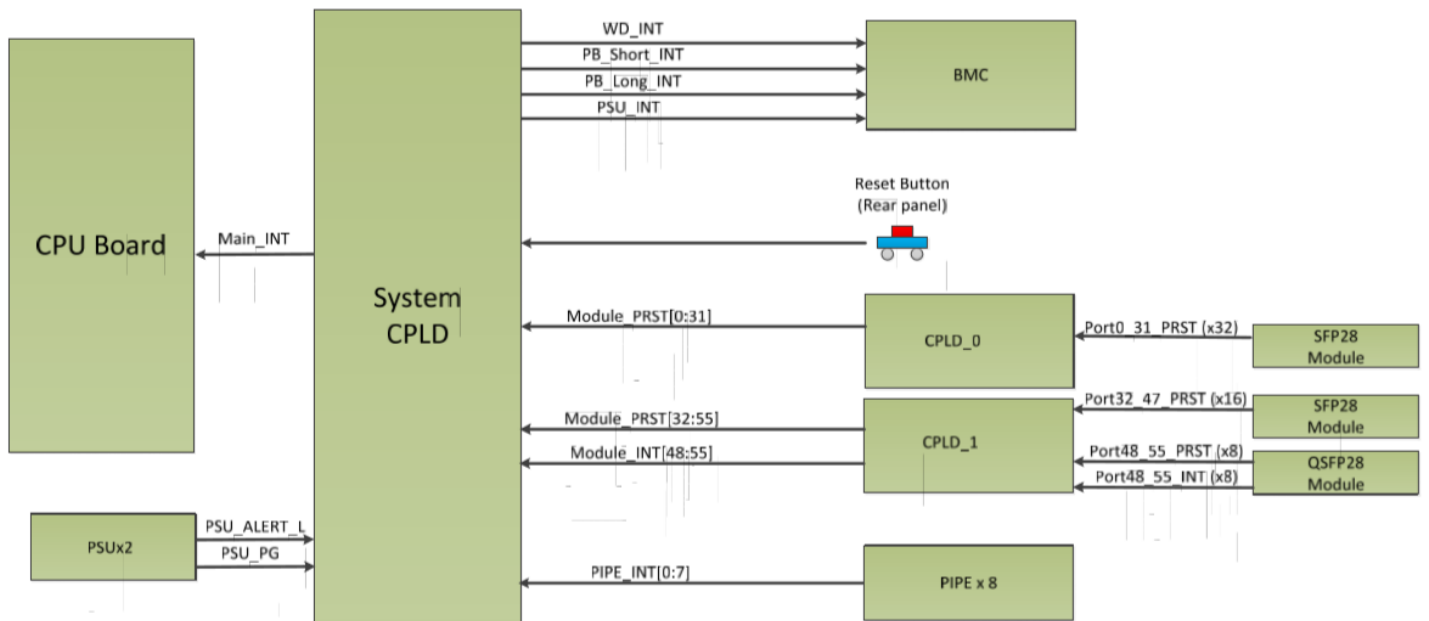
OOBM NIC I210/I350



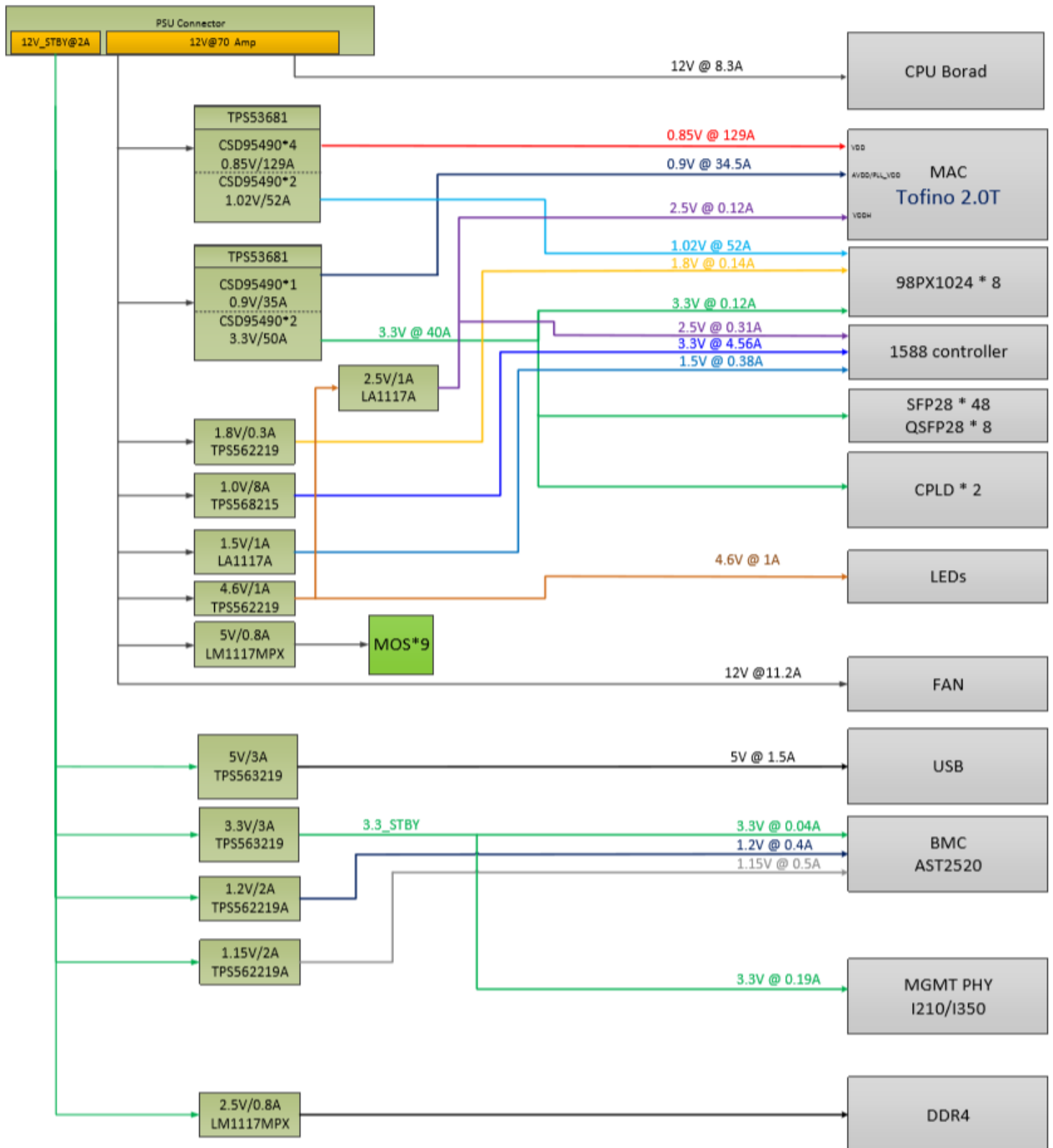
Symbol	Parameter	Min	Max	Units
T3_09	VCC3P3 (3.3V) power supply stable to VCC0P9 (0.9V) power supply stable	1 ²	20	ms
T3_15	VCC3P3 (3.3V) power supply stable to VCC1P5 (1.5V) power supply stable	1 ²	20	ms
Tm-per	3.3V power supply to PE_RST_N de-assertion ¹	100		ms
Tlpg	Power Supplies Stable to LAN_PWR_GOOD assertion	0		ms
Tlpg-per	LAN_PWR_GOOD assertion to PE_RST_N de-assertion ¹	100		ms
Tper-m	PE_RST_N off before 3.3V power supply down	0		ms
Tlpgw	LAN_PWR_GOOD de-assertion time ²	1		ms

2.6. Interrupt

The block diagram illustrates the interrupt mechanism as shown on below. The System CPLD is used for recording the interrupt status. Once interrupts occurred, Host CPU / BMC needs to access the interrupt status registers of CPLDs or device itself.

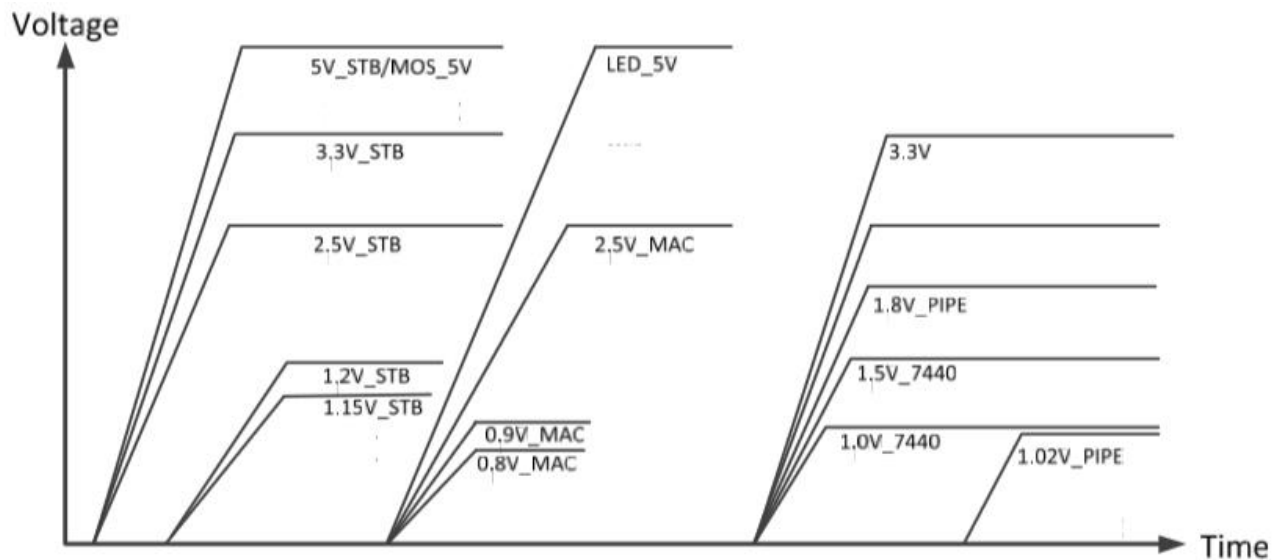


2.7. Power Tree

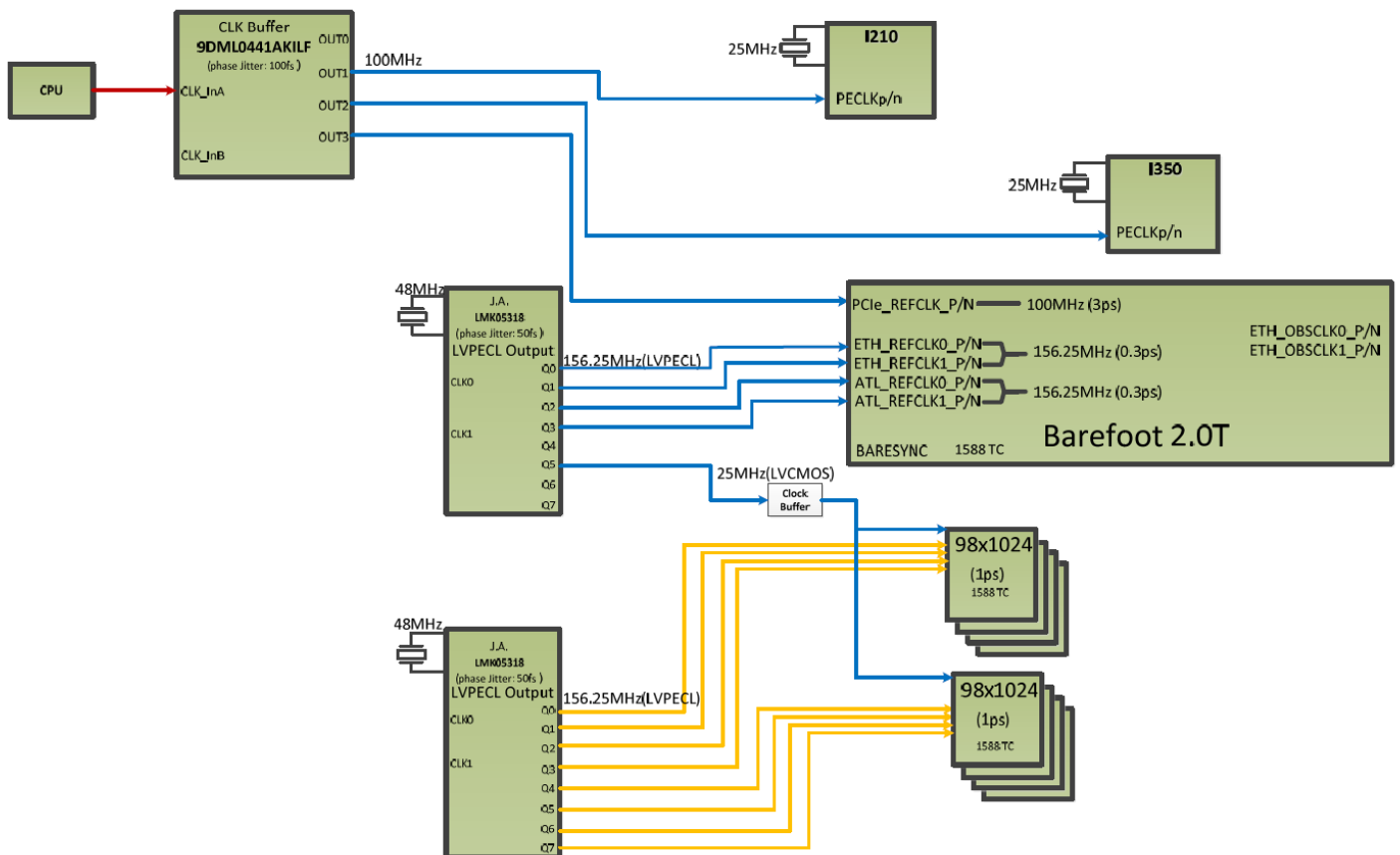


2.8. Power up Sequence

The stand-by 3.3V power will be brought up firstly by PSU 12V_STB, then enable 1.2V_STB, 1.15V_STB, 0.9V_STB rails. For system all other DC rails will handled by Power1014A according to requirement below figure.



2.9. Clock Tree



2.10. SyncE and 1588

SyncE and 1588 support.

Recovery clock is dynamic change if port is link in different speed, please refer to below information: Barefoot: recovery clock 25G is 80.56640MHz and 10G is 64.453125MHz

The frequency for **tx_clk** and **rx_clk** is 644.53125MHz in 25GbE mode and 515.625MHz in 10GbE mode. These are line rates divide by 40 and 20 respectively. The output divider in the ETH_OBSCLK pad can be used to reduce the clock frequency. The divider settings are 1, 2, 3, and 8.

The following procedure brings out the recovered clock from Port 8, lane 0 to ETH_OBSCLK0.

```
wr 0x0211_FD20 0x0000_0004 // Select lane 0 rx_clk and select SerDes output
wr 0x0004_0004 0x0000_001F // Divide output by 2, select chain 0 for ETH_OBSCLK0
```

Marvell:

1G is 25MHz

10G is 32.226525MHz

25G is 40.283203125MHz



Interface	SERDES Speed (Gbps)	Recovered Clock Frequency Without a Division Factor	Recommended Division Factor	Recovered Clock Frequency With a Division Factor
SGMII	1.25	125 MHz	5	25 MHz
SGMII @ 2.5G	3.125	312.5 MHz	8	39.0625 MHz
5G	5.15625	257.8125 MHz	16	16.11328125 MHz
10G	10.3125	515.625 MHz	16	32.2265625 MHz
20G	10.3125	515.625 MHz	16	32.2265625 MHz
40G	10.3125	515.625 MHz	16	32.2265625 MHz
12G/24G/48G	12.1875	609.375 MHz	16	38.0859375 MHz
25G	25.78125	644.53125 MHz	16	40.283203125 MHz
50G	25.78125	644.53125 MHz	16	40.283203125 MHz
100G	25.78125	644.53125 MHz	16	40.283203125 MHz
110G	27.5	687.5 MHz	16	42.96875 MHz
110G	28.125	703.125 MHz	16	43.9453125 MHz
XAUI		156.25 MHz	5	31.25 MHz
RXAUI		312.5 MHz	8	39.0625 MHz
QSGMII		250 MHz	8	31.25 MHz
20G DR-XAUI		312.5 MHz	8	39.0625 MHz

CPU Sub-system

Please refer to below attached file.



Broadwell_CPU_B
oard_HWS.pdf

3. BMC Sub-system

AST2520 is a BMC chip with internal 800MHz ARM11 CPU by ASPEED. It's a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable platforms.

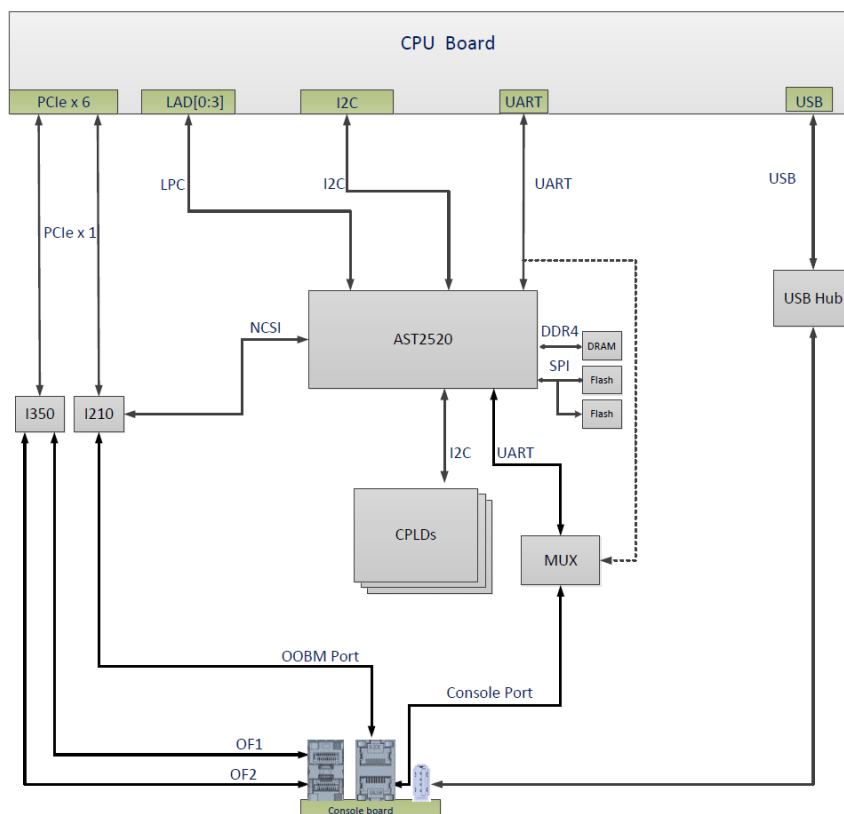
The sensors of a BMC measure internal physical variables such as temperature, power-supply

voltage, FAN speed, communication functions. If any of these variables happens to stray outside

specified limits, the administrator is notified. That person can then take corrective action by remote

control. The monitor device can power cycle or reboot as necessary.

3.1. BMC Sub-system Block Diagram



3.2. Hardware Strap Configuration

Offset: 0x1E6E2070				Hardware Strap Table			
Bit/ Pin	R/ W	Description				Default Value	
31 FWSPIMOSI	RW	Enable SPI Flash Strap Auto Fetch Mode 0: Disable. 1: Enable.				1	
30 FWSPICK	RW	Enable GPIO Strap Mode 0: Disable. 1: Enable.				1	
29 TXD5	RW	Select UART Debug port 0: Select UART1 as BMC console port. 1: Select UART5 as BMC console port. This bit is used to select the UART port for user debugging. It is not the BMC console function.				1	
28	RW	Reserved				1	
27 GPIOZ7	RW	Enable fast reset mode for ARM ICE debugger 0: Long reset mode, normal operation (default) 1: Fast reset mode, for ICE debugger connection Enable fast reset mode to enable ICE debugger can stop ARM at starting address				0	
26 RTCK	RW	Enable eSPI flash mode 0: eSPI respond with no flash attached 1: eSPI respond with flash attached This bit is valid only when eSPI is enabled.				0	
25 FWSPIMISO	RW	Enable eSPI mode 0: LPC mode 1: eSPI mode				0	
24 RGMII2TXD3	RW	Select DDR4 SDRAM 0: DDR3 SDRAM 1: DDR4 SDRAM				1	
23 RGMII2TXD2	RW	RW Select 25 MHz reference clock input mode 0: CLKIN is 24 MHz and USBCKI not used 1: CLKIN is 25 MHz and USBCKI = 24/48 MHz (determined by bit[18])				0	
22 RGMII2TXD1	RW	Enable GPIOE pass-through mode 0: Disable, pass through can be enabled by SCU8C[15:12]. 1: Enable pass-through at power on. Pass-through pins set: GPIOE0 → GPIOE1 GPIOE2 → GPIOE3 GPIOE4 → GPIOE5 GPIOE6 → GPIOE7				0	
21 RGMII2TXD0	RW	Enable GPIOD pass-through mode 0: Disable, pass through can be enabled by SCU8C[11:8]. 1: Enable pass-through at power on. Pass-through pins set: GPIOD0 → GPIOD1 GPIOD2 → GPIOD3 GPIOD4 → GPIOD5 GPIOD6 → GPIOD7				0	
20 GPIOZ6	RW	Disable LPC to decode SuperIO 0x2E/0x4E address 0: Enable address decoding (default) 1: Disable address decoding				0	
19 RGMII1TXD3	RW	Enable ACPI function 0: Disable ACPI. 1: Enable ACPI.				0	

18 GPIOZ5	RW	Select USBCKI input frequency 0: 24 MHz. 1: 48 MH	0
17GPIOZ4	RW	Enable BMC 2nd boot watchdog timer 0: Disable1: Enable BMC 2nd boot watchdog timer start counting at power up.The watchdog timer was located at WDT2. After watchdog timeout, it willreset BMC and restart booting from the 2nd boot flash at CS1#. CS1# mustbe the same flash type as CS0# and could be the same firmware as CS0#.	1
16 RGMII1TXD2	RW	SuperIO configuration address selection 0: Decode 0x2E. 1: Decode 0x4E.	1
15 GPIO57	RW	VGA Class Code selection 0: Select the Class Code for video device. 1: Select the Class Code for VGA device.	1
14	RW	Select dedicated LPC reset input 0: LPC reset is shared with PCIe reset pin. 1: LPC reset is located at pin number G22, shared with GPIOAC7.	1
13:12 RGMII1TXD1 RGMII1TXD0	RW	SPI mode selection 00: Disable SPI interface. 01: Enable SPI Master 10: RSVD, enable SPI Master and SPI Slave to AHB Bridge (debug mode) 11: Enable SPI Pass-through	11
11:09	RW	AXI/AHB clock frequency ratio selection 000: undefined 001: Select AXI:AHB = 2:1 010: Select AXI:AHB = 3:1 011: Select AXI:AHB = 4:1 100: Select AXI:AHB = 5:1 101: Select AXI:AHB = 6:1 110: Select AXI:AHB = 7:1 111: Select AXI:AHB = 8:1 HCLK freq = H-PLL / 2 / (ratio of AXI-AHB)	001
8	RW	Reserved	0
7 RGMII2TXCTL	RW	Define MAC#2 interface 0: RMII/NCSI. 1: RGMII.	0
6 RGMII1TXCTL	RW	Define MAC#1 interface 0: RMII/NCSI. 1: RGMII.	0
5 GPIO56	RW	Enable dedicated VGA BIOS ROM 0: No VGA BISO ROM, VGA BIOS is merged in the system BIOS (default) 1: Enable dedicated VGA BIOS ROM	0
4	RW	Reserved	0

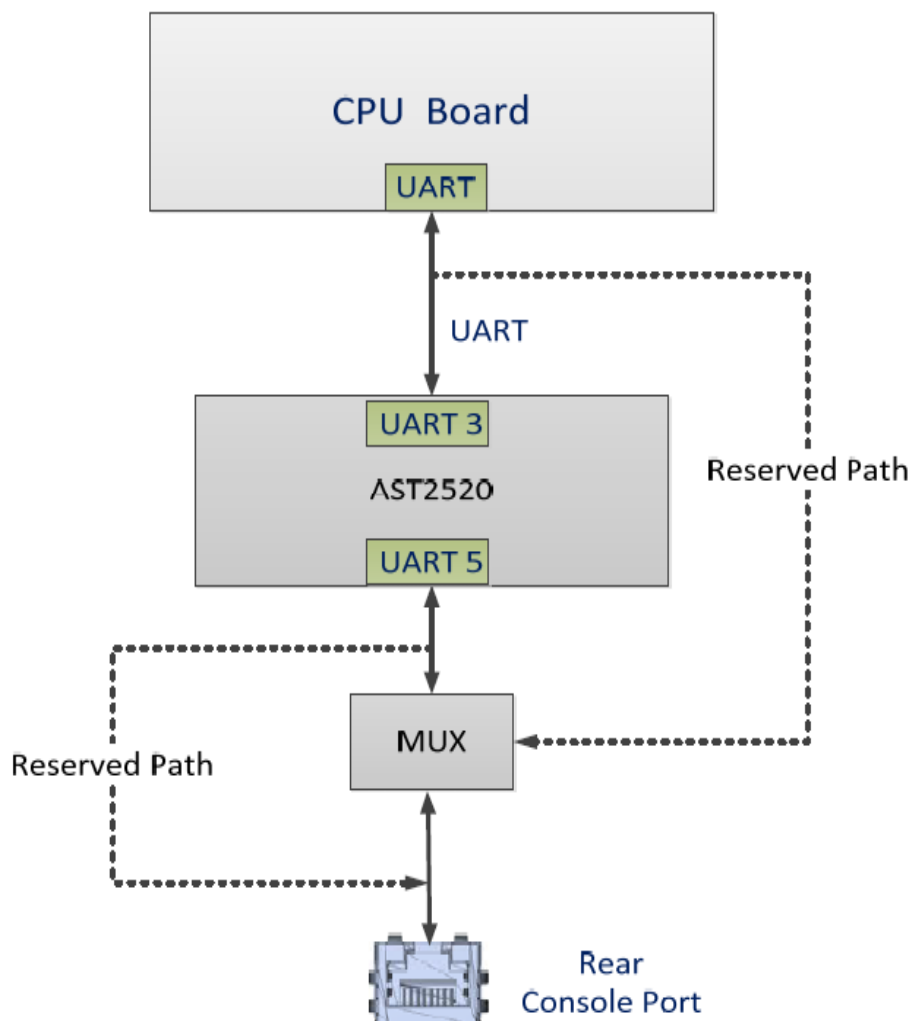
3:2 GPIO54	RW	VGA memory size selection 00: Select 8 MB VGA memory 01: Select 16 MB VGA memory (default) 10: Select 32 MB VGA memory 11: Select 64 MB VGA memory Defined the VGA memory size that will share with SOC memory. The minimum memory size required for the VGA high resolution mode shows as below: 1280x1024x16bpp = 8MB 1600x1200x16bpp = 8MB 1680x1050x16bpp = 8MB 1920x1080x16bpp = 8MB 1920x1200x16bpp = 8MB 1280x1024x32bpp = 8MB 1600x1200x32bpp = 8MB 1680x1050x32bpp = 8MB 1920x1080x32bpp = 16MB 1920x1200x32bpp = 16MB	01
1	RW	Reserved	1
0 FWSPIC50	RW	Disable CPU boot 0: Enable boot 1: Disable CPU operation, when no firmware exist	0

3.3. UART Connection

AST2500 includes 5 UART controllers and 6 UART IO interfaces, 5 with full flow control pins and 1 with Tx/Rx only for BMC console output. The 5 UART controllers can be directed to any one

of the 6 UART IO interfaces.

The rear console port can be switched either from BMC or CPU.



3.4. FAN Control

BMC AST2520 supporting 4 PWM outputs for fan speed control as well as 8 tachometer input for fan speed measurement.

AST2520	FAN TACH		
	Channel	Pin Name	FAN number
	TACH0	FAN_TACH0	FAN1_Front
	TACH1	FAN_TACH1	FAN2_Front
	TACH2	FAN_TACH2	FAN3_Front
	TACH3	FAN_TACH3	FAN4_Front
	TACH4	FAN_TACH0_1	FAN1_Rear
	TACH5	FAN_TACH1_1	FAN2_Rear
	TACH6	FAN_TACH2_1	FAN3_Rear
	TACH7	FAN_TACH3_1	FAN4_Rear
	FAN PWM		
	Channel	Pin Name	FAN number
	PWM0	FAN_PWM0	FAN1
	PWM1	FAN_PWM1	FAN2
	PWM2	FAN_PWM2	FAN3
	PWM3	FAN_PWM3	FAN4

AST2520	FAN LED truth table					
	Channel	Pin Name	LED color		Default	Note
	GPIOC0	FAN0_LED	0	Yellow	1	Detect FAN present to set LED color 0 : No FAN tray or Faulty 1: FAN tray present and good
			1	Green	1	
	GPIOC1	FAN1_LED	0	Yellow	1	
			1	Green	1	
	GPIOC2	FAN2_LED	0	Yellow	1	
			1	Green	1	
	GPIOC3	FAN3_LED	0	Yellow	1	
			1	Green	1	

PWM Controller

- Support 4 PWM outputs
- Support both low-frequency and high-frequency (e.g. 25KHz and 50KHz) PWM for fan speed control
- Duty cycle from 0 to 100% with 1/256 resolution incremental
- Support low-frequency PWM pulse stretching for fan speed measurements

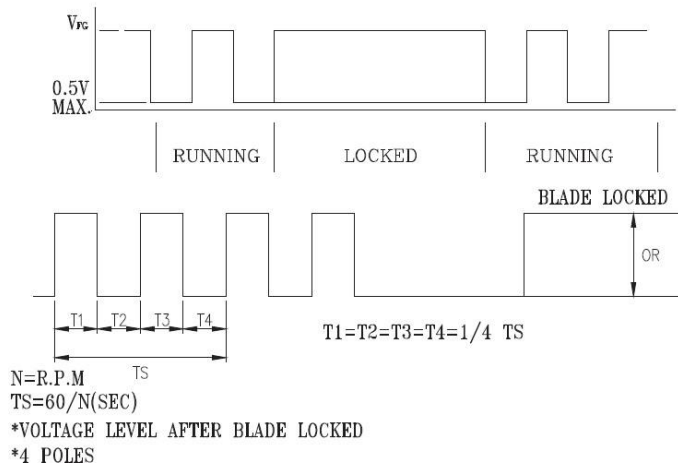
PWM Controller

- Support 8 tachometer inputs
- Measurement schemes: rising edge, falling edge or both edges
- Support interrupt trigger when over fan speed limitation setting

$$\text{RPM} = (24000000 * 60) / (2 * \text{TachoValue} * \text{TachoClkDivision})$$

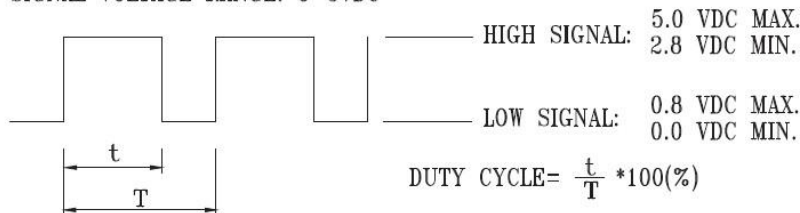
FAN RPM and PWM control show as below:

3. FREQUENCY GENERATOR WAVEFORM:



11. PWM CONTROL SIGNAL:

SIGNAL VOLTAGE RANGE: 0~5VDC



- THE PREFERRED OPERATING POINT FOR THE FAN IS 25KHZ.
- AT 100% DUTY CYCLE, THE ROTOR WILL SPIN AT MAXIMUM SPEED.
- AT 0% DUTY CYCLE, THE ROTOR WILL BE STOPPED.
- WITH CONTROL SIGNAL LEAD DISCONNECTED, THE FAN WILL SPIN AT MAXIMUM SPEED.

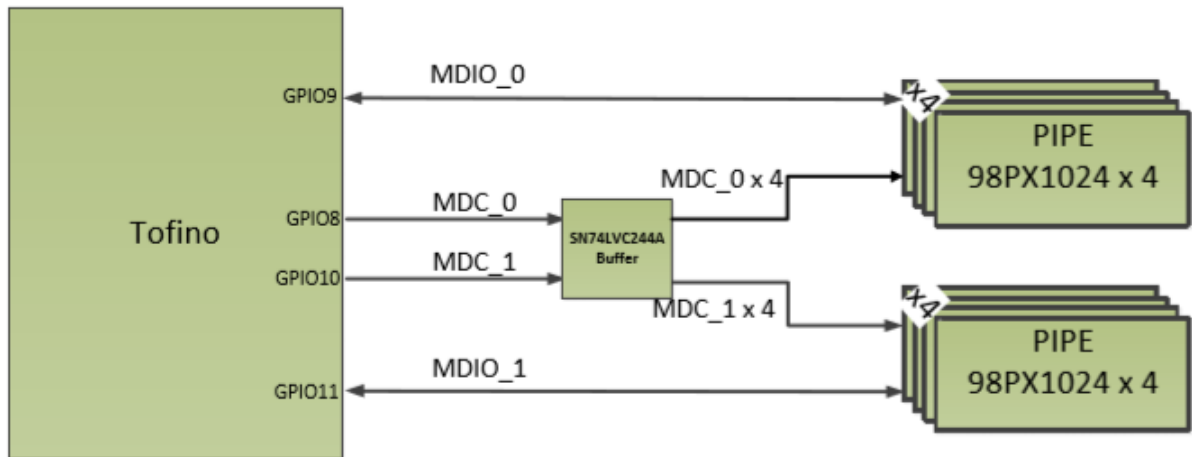
12. SPEED VS PWM CONTROL SIGNAL:

(AT RATED 12V & PWM FREQUENCY=25KHZ)

DUTY CYCLE (%)	SPEED R.P.M. (REF.)		CURRENT (A) TYP.
	FRONT	REAR	
100	23000±8%	20500±8%	2.27
10	1500±500	1500±500	0.06
0	0	0	0.04

4. MDC/MDIO

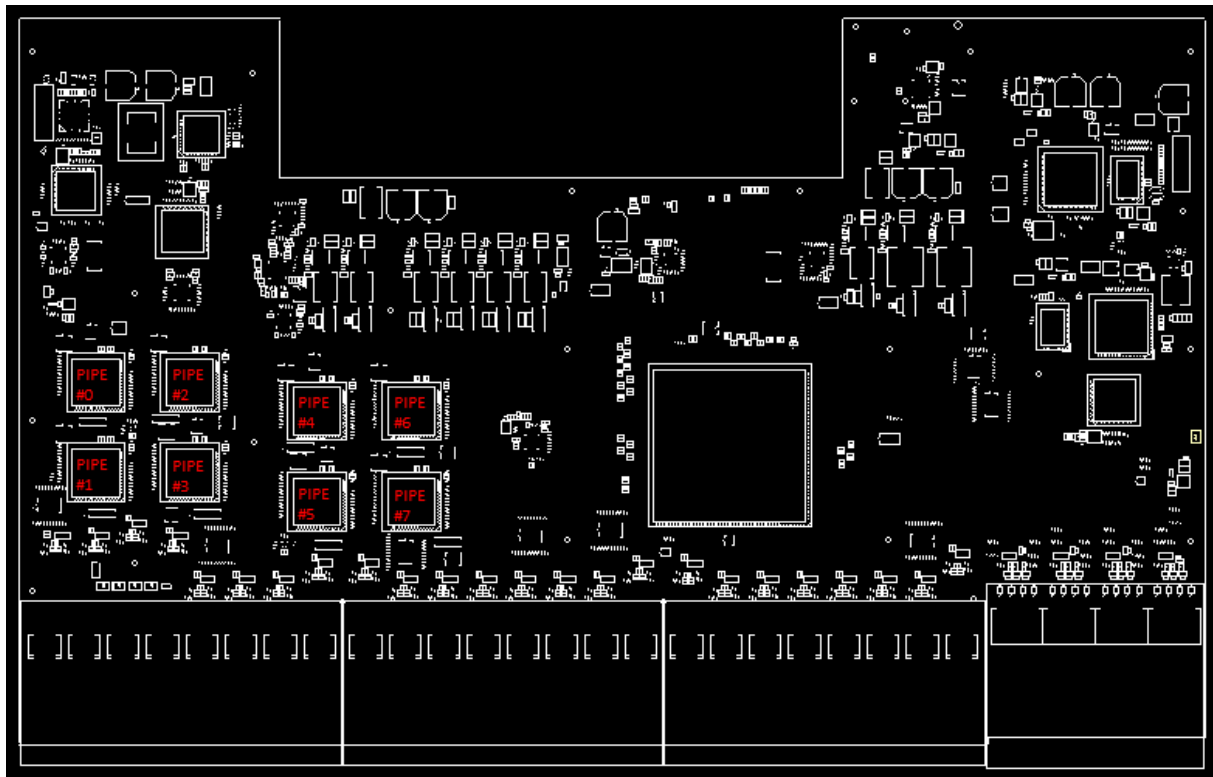
4.1. Functional Block Diagram



4.2. MIIM

The MAC (Tofino) ASIC supports the IEEE802.3u standard MIIM interface to access all PIPEs in the system. The MIIM interface of both MAC and PIPE (98PX1024) will be configured to Clause 22.

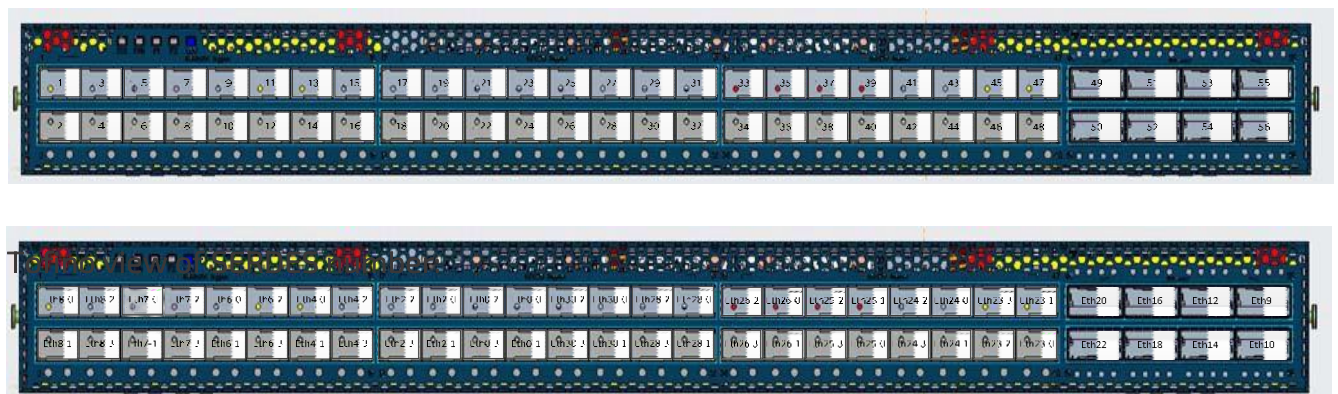
MAC Device	MDC/MDIO	PHY Device	PHY Address					PHY ID
			A4	A3	A2	A1	A0	
Tofino	GPIO8/9	98PX1024#0	0	0	0	0	0	0x2
		98PX1024#1	0	0	0	0	1	0x2
		98PX1024#2	0	0	0	1	0	0x2
		98PX1024#3	0	0	0	1	1	0x2
	GPIO10/11	98PX1024#4	0	0	1	0	0	0x2
		98PX1024#5	0	0	1	0	1	0x2
		98PX1024#6	0	0	1	1	0	0x2
		98PX1024#7	0	0	1	1	1	0x2



4.3. Network Interface

There is no P/N or Lane swap in all SERDES connection. Port1 to Port16 support 1G/10G/25G network speed and use Marvell PIPE 98PX1024 to handle speed change. Port17 to Port48 support 10G/25G and Port49 to Port56 can support up to 100G.

Physical view of front port number:



Detail information as below table:

MAC Tofino			PIPE 98PX102 4				Front Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
	RX Lane	ETH8_RD0P	LANE12_TX_P	PHY #0	000	LANE14_TX_P	1
		ETH8_RD0N	LANE12_TX_N			LANE14_TX_N	
		ETH8_RD1P	LANE13_TX_P			LANE15_TX_P	2
		ETH8_RD1N	LANE13_TX_N			LANE15_TX_N	
	TX Lane	ETH8_TD0P	LANE12_RX_P			LANE14_RX_P	1
		ETH8_TD0N	LANE12_RX_N			LANE14_RX_N	
		ETH8_TD1P	LANE13_RX_P			LANE15_RX_P	2
		ETH8_TD1N	LANE13_RX_N			LANE15_RX_N	
	RX Lane	ETH8_RD2P	LANE12_TX_P	PHY #1	001	LANE14_TX_P	3
		ETH8_RD2N	LANE12_TX_N			LANE14_TX_N	
		ETH8_RD3P	LANE13_TX_P			LANE15_TX_P	4
		ETH8_RD3N	LANE13_TX_N			LANE15_TX_N	
	TX Lane	ETH8_TD2P	LANE12_RX_P			LANE14_RX_P	3
		ETH8_TD2N	LANE12_RX_N			LANE14_RX_N	
		ETH8_TD3P	LANE13_RX_P			LANE15_RX_P	4
		ETH8_TD3N	LANE13_RX_N			LANE15_RX_N	
	RX Lane	ETH7_RD0P	LANE12_TX_P	PHY #2	010	LANE14_TX_P	5
		ETH7_RD0N	LANE12_TX_N			LANE14_TX_N	
		ETH7_RD1P	LANE13_TX_P			LANE15_TX_P	6
		ETH7_RD1N	LANE13_TX_N			LANE15_TX_N	
	TX Lane	ETH7_TD0P	LANE12_RX_P			LANE14_RX_P	5
		ETH7_TD0N	LANE12_RX_N			LANE14_RX_N	
		ETH7_TD1P	LANE13_RX_P			LANE15_RX_P	6
		ETH7_TD1N	LANE13_RX_N			LANE15_RX_N	
	RX Lane	ETH7_RD2P	LANE12_TX_P	PHY #3	011	LANE14_TX_P	7
		ETH7_RD2N	LANE12_TX_N			LANE14_TX_N	
		ETH7_RD3P	LANE13_TX_P			LANE15_TX_P	8
		ETH7_RD3N	LANE13_TX_N			LANE15_TX_N	
	TX Lane	ETH7_TD2P	LANE12_RX_P			LANE14_RX_P	7
		ETH7_TD2N	LANE12_RX_N			LANE14_RX_N	
		ETH7_TD3P	LANE13_RX_P			LANE15_RX_P	8
		ETH7_TD3N	LANE13_RX_N			LANE15_RX_N	
	RX Lane	ETH6_RD0P	LANE12_TX_P	PHY #4	100	LANE14_TX_P	9
		ETH6_RD0N	LANE12_TX_N			LANE14_TX_N	
		ETH6_RD1P	LANE13_TX_P			LANE15_TX_P	10
		ETH6_RD1N	LANE13_TX_N			LANE15_TX_N	
	TX Lane	ETH6_TD0P	LANE12_RX_P			LANE14_RX_P	9
		ETH6_TD0N	LANE12_RX_N			LANE14_RX_N	
		ETH6_TD1P	LANE13_RX_P			LANE15_RX_P	10
		ETH6_TD1N	LANE13_RX_N			LANE15_RX_N	
	RX Lane	ETH6_RD2P	LANE12_TX_P	PHY #5	101	LANE14_TX_P	11
		ETH6_RD2N	LANE12_TX_N			LANE14_TX_N	
		ETH6_RD3P	LANE13_TX_P			LANE15_TX_P	12
		ETH6_RD3N	LANE13_TX_N			LANE15_TX_N	
	TX Lane	ETH6_TD2P	LANE12_RX_P			LANE14_RX_P	11
		ETH6_TD2N	LANE12_RX_N			LANE14_RX_N	
		ETH6_TD3P	LANE13_RX_P			LANE15_RX_P	12
		ETH6_TD3N	LANE13_RX_N			LANE15_RX_N	

MAC Tofino			PIPE 98PX102 4				Front Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
	RX Lane	ETH6_TD3N	LANE13_RX_N	PHY #6	110	LANE15_RX_N	13
		ETH4_RD0P	LANE12_TX_P			LANE14_TX_P	
		ETH4_RD0N	LANE12_TX_N			LANE14_TX_N	14
		ETH4_RD1P	LANE13_TX_P			LANE15_TX_P	
	TX Lane	ETH4_RD1N	LANE13_TX_N			LANE15_TX_N	13
		ETH4_TD0P	LANE12_RX_P			LANE14_RX_P	
		ETH4_TD0N	LANE12_RX_N			LANE14_RX_N	14
		ETH4_TD1P	LANE13_RX_P			LANE15_RX_P	
	RX Lane	ETH4_TD1N	LANE13_RX_N	PHY #7	111	LANE15_RX_N	15
		ETH4_RD2P	LANE12_TX_P			LANE14_TX_P	
		ETH4_RD2N	LANE12_TX_N			LANE14_TX_N	16
		ETH4_RD3P	LANE13_TX_P			LANE15_TX_P	
	TX Lane	ETH4_RD3N	LANE13_TX_N			LANE15_TX_N	15
		ETH4_TD2P	LANE12_RX_P			LANE14_RX_P	
		ETH4_TD2N	LANE12_RX_N			LANE14_RX_N	16
		ETH4_TD3P	LANE13_RX_P			LANE15_RX_P	
	RX Lane	ETH4_TD3N	LANE13_RX_N			LANE15_RX_N	19
		ETH2_RD0P		NA	NA		
		ETH2_RD0N					20
		ETH2_RD1P					
	TX Lane	ETH2_RD1N					17
		ETH2_RD2P					
		ETH2_RD2N					18
		ETH2_RD3P					
		ETH2_RD3N					19
	RX Lane	ETH2_TD0P		NA	NA		
		ETH2_TD0N					20
		ETH2_TD1P					
		ETH2_TD1N					17
		ETH2_TD2P					
		ETH2_TD2N					18
		ETH2_TD3P					
		ETH2_TD3N					23
	TX Lane	ETH0_RD0P		NA	NA		
		ETH0_RD0N					24
		ETH0_RD1P					
		ETH0_RD1N					21
		ETH0_RD2P					
		ETH0_RD2N					22
		ETH0_RD3P					
		ETH0_RD3N					23
	TX Lane	ETH0_TD0P		NA	NA		
		ETH0_TD0N					24
		ETH0_TD1P					
		ETH0_TD1N					21
		ETH0_TD2P					
		ETH0_TD2N					

		ETH0_TD3P				22
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MAC Tofino			PIPE 98PX102 4				Front Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
		ETH0_TD3N					
	RX Lane	ETH30_RD0P		NA	NA		27
		ETH30_RD0N					
		ETH30_RD1P					28
		ETH30_RD1N					
		ETH30_RD2P					25
		ETH30_RD2N					
		ETH30_RD3P					26
		ETH30_RD3N					
	TX Lane	ETH30_TD0P		NA	NA		27
		ETH30_TD0N					
		ETH30_TD1P					28
		ETH30_TD1N					
		ETH30_TD2P					25
		ETH30_TD2N					
		ETH30_TD3P					26
		ETH30_TD3N					
	RX Lane	ETH28_RD0P		NA	NA		31
		ETH28_RD0N					
		ETH28_RD1P					32
		ETH28_RD1N					
		ETH28_RD2P					29
		ETH28_RD2N					
		ETH28_RD3P					30
		ETH28_RD3N					
	TX Lane	ETH28_TD0P		NA	NA		31
		ETH28_TD0N					
		ETH28_TD1P					32
		ETH28_TD1N					
		ETH28_TD2P					29
		ETH28_TD2N					
		ETH28_TD3P					30
		ETH28_TD3N					
	RX Lane	ETH26_RD0P		NA	NA		35
		ETH26_RD0N					
		ETH26_RD1P					36
		ETH26_RD1N					
		ETH26_RD2P					33
		ETH26_RD2N					
		ETH26_RD3P					34
		ETH26_RD3N					
	TX Lane	ETH26_TD0P		NA	NA		35
		ETH26_TD0N					
		ETH26_TD1P					36
		ETH26_TD1N					
		ETH26_TD2P					33
		ETH26_TD2N					
		ETH26_TD3P					34
		ETH26_TD3N					

MAC Tofino			PIPE 98PX102 4				Front Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
	RX Lane	ETH26_TD3N					
		ETH25_RD0P		NA	NA		40
		ETH25_RD0N					
		ETH25_RD1P					39
		ETH25_RD1N					
		ETH25_RD2P					37
		ETH25_RD2N					
		ETH25_RD3P					38
		ETH25_RD3N					
	TX Lane	ETH25_TD0P		NA	NA		40
		ETH25_TD0N					
		ETH25_TD1P					39
		ETH25_TD1N					
		ETH25_TD2P					37
		ETH25_TD2N					
		ETH25_TD3P					38
		ETH25_TD3N					
	RX Lane	ETH24_RD0P		NA	NA		43
		ETH24_RD0N					
		ETH24_RD1P					44
		ETH24_RD1N					
		ETH24_RD2P					41
		ETH24_RD2N					
		ETH24_RD3P					42
		ETH24_RD3N					
	TX Lane	ETH24_TD0P		NA	NA		43
		ETH24_TD0N					
		ETH24_TD1P					44
		ETH24_TD1N					
		ETH24_TD2P					41
		ETH24_TD2N					
		ETH24_TD3P					42
		ETH24_TD3N					
	RX Lane	ETH23_RD0P		NA	NA		48
		ETH23_RD0N					
		ETH23_RD1P					47
		ETH23_RD1N					
		ETH23_RD2P					46
		ETH23_RD2N					
		ETH23_RD3P					45
		ETH23_RD3N					
	TX Lane	ETH23_TD0P		NA	NA		48
		ETH23_TD0N					
		ETH23_TD1P					47
		ETH23_TD1N					
		ETH23_TD2P					46
		ETH23_TD2N					
		ETH23_TD3P					45
		ETH23_TD3N					

MAC Tofino			PIPE 98PX102 4				Front Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
		ETH23_TD3N					
	RX Lane	ETH20_RD0P		NA	NA		48
		ETH20_RD0N					
		ETH20_RD1P					
		ETH20_RD1N					
		ETH20_RD2P					
		ETH20_RD2N					
		ETH20_RD3P					
		ETH20_RD3N					
	TX Lane	ETH20_TD0P		NA	NA		48
		ETH20_TD0N					
		ETH20_TD1P					
		ETH20_TD1N					
		ETH20_TD2P					
		ETH20_TD2N					
		ETH20_TD3P					
		ETH20_TD3N					
	RX Lane	ETH22_RD0P		NA	NA		49
		ETH22_RD0N					
		ETH22_RD1P					
		ETH22_RD1N					
		ETH22_RD2P					
		ETH22_RD2N					
		ETH22_RD3P					
		ETH22_RD3N					
	TX Lane	ETH22_TD0P		NA	NA		49
		ETH22_TD0N					
		ETH22_TD1P					
		ETH22_TD1N					
		ETH22_TD2P					
		ETH22_TD2N					
		ETH22_TD3P					
		ETH22_TD3N					
	RX Lane	ETH16_RD0P		NA	NA		50
		ETH16_RD0N					
		ETH16_RD1P					
		ETH16_RD1N					
		ETH16_RD2P					
		ETH16_RD2N					
		ETH16_RD3P					
		ETH16_RD3N					
	TX Lane	ETH16_TD0P		NA	NA		50
		ETH16_TD0N					
		ETH16_TD1P					
		ETH16_TD1N					
		ETH16_TD2P					
		ETH16_TD2N					
		ETH16_TD3P					

MAC Tofino			PIPE 98PX102 4				Front Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
	RX Lane	ETH16_TD3N		NA	NA		51
		ETH18_RD0P					
		ETH18_RD0N					
		ETH18_RD1P					
		ETH18_RD1N					
		ETH18_RD2P					
		ETH18_RD2N					
		ETH18_RD3P					
		ETH18_RD3N					
	TX Lane	ETH18_TD0P		NA	NA		51
		ETH18_TD0N					
		ETH18_TD1P					
		ETH18_TD1N					
		ETH18_TD2P					
		ETH18_TD2N					
		ETH18_TD3P					
		ETH18_TD3N					
	RX Lane	ETH12_RD0P		NA	NA		52
		ETH12_RD0N					
		ETH12_RD1P					
		ETH12_RD1N					
		ETH12_RD2P					
		ETH12_RD2N					
		ETH12_RD3P					
		ETH12_RD3N					
	TX Lane	ETH12_TD0P		NA	NA		52
		ETH12_TD0N					
		ETH12_TD1P					
		ETH12_TD1N					
		ETH12_TD2P					
		ETH12_TD2N					
		ETH12_TD3P					
		ETH12_TD3N					
	RX Lane	ETH14_RD0P		NA	NA		53
		ETH14_RD0N					
		ETH14_RD1P					
		ETH14_RD1N					
		ETH14_RD2P					
		ETH14_RD2N					
		ETH14_RD3P					
		ETH14_RD3N					
	TX Lane	ETH14_TD0P		NA	NA		53
		ETH14_TD0N					
		ETH14_TD1P					
		ETH14_TD1N					
		ETH14_TD2P					
		ETH14_TD2N					
		ETH14_TD3P					
		ETH14_TD3N					

MAC Tofino			PIPE 98PX102 4				Fron t Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
		ETH14_TD3N					
	RX Lane	ETH9_RD0P		NA	NA		54
		ETH9_RD0N					
		ETH9_RD1P					
		ETH9_RD1N					
		ETH9_RD2P					
		ETH9_RD2N					
		ETH9_RD3P					
		ETH9_RD3N					
		TX Lane	ETH9_TD0P				
	ETH9_TD0N						
	ETH9_TD1P						
	ETH9_TD1N						
	ETH9_TD2P						
	ETH9_TD2N						
	ETH9_TD3P						
	ETH9_TD3N						
	RX Lane	ETH10_RD0P		NA	NA		55
		ETH10_RD0N					
		ETH10_RD1P					
		ETH10_RD1N					
		ETH10_RD2P					
		ETH10_RD2N					
		ETH10_RD3P					
		ETH10_RD3N					
	TX Lane	ETH10_TD0P		NA	NA		55
		ETH10_TD0N					
		ETH10_TD1P					
		ETH10_TD1N					
		ETH10_TD2P					
		ETH10_TD2N					
		ETH10_TD3P					
		ETH10_TD3N					
Tofino MGMT			CPU and 1588 controller				
	RX Lane	ETH32_RD0P			CPU		LAN0
		ETH32_RD0N			CPU		LAN0
		ETH32_RD1P			CPU		LAN1
		ETH32_RD1N			CPU		LAN1
		ETH32_RD2P			1588 controller		Port9
		ETH32_RD2N			1588 controller		Port9
		ETH32_RD3P			1588 controller		Port10
		ETH32_RD3N			1588 controller		Port10
	TX Lane	ETH32_TD0P			CPU		LAN0
		ETH32_TD0N			CPU		LAN0
		ETH32_TD1P			CPU		LAN1
		ETH32_TD1N			CPU		LAN1
		ETH32_TD2P			1588 controller		Port9
		ETH32_TD2N			1588 controller		Port9

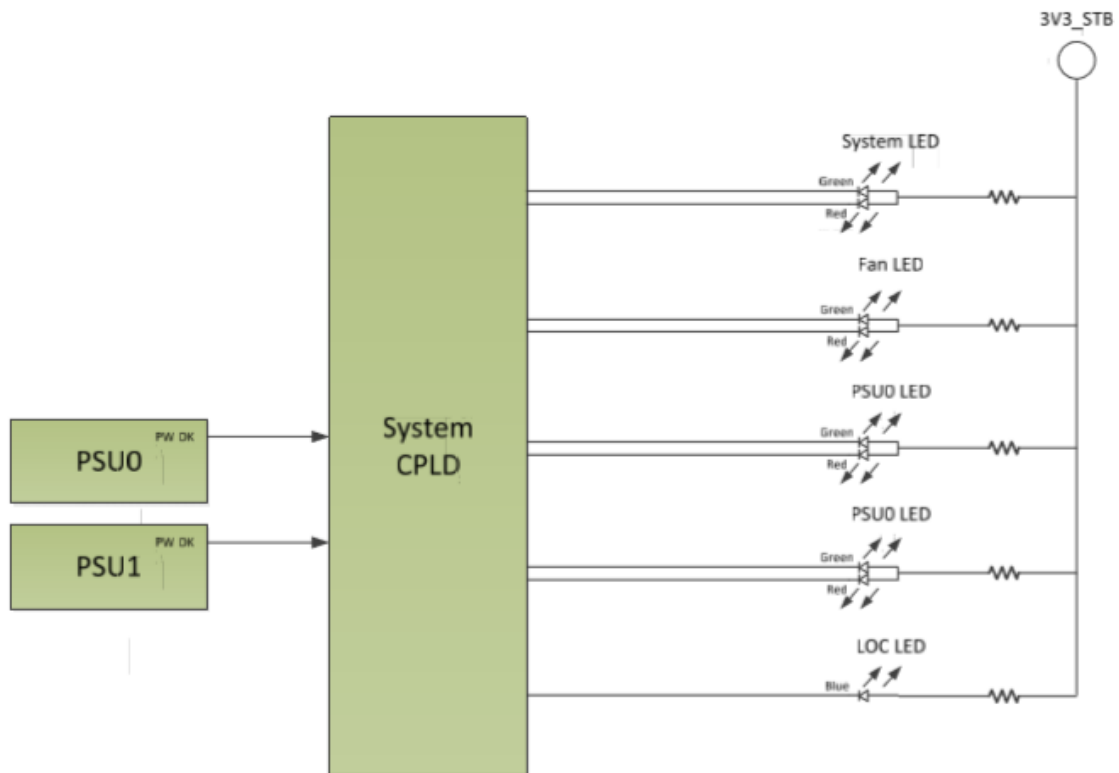
MAC Tofino			PIPE 98PX102 4				Front Port
		Lane	Host	PHY No.	PHY ADDR[2:0]	Line side	
		ETH32_TD3P			1588 controller		Port1 0
		ETH32_TD3N			1588 controller		Port1 0

5. LED

5.1. System LED

All these system LEDs are located at front panel and control by system CPLD.

	Description
System LED	Solid Green – System normal operation Blinking Green – System booting Solid Red – System Fault
PSU LED	Solid Green – PSU operating normally Solid Red – PSU Fault Off – No PSU installed
FAN LED	Solid Green – FAN operating normally Solid Red – FAN Fault Off – No FAN installed
LOC LED	Blue – indicate machine location



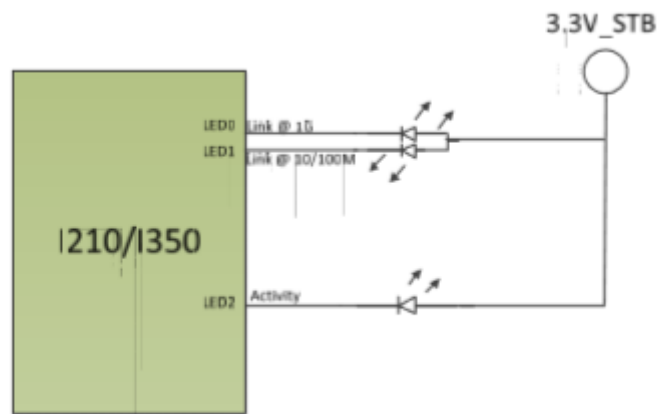
PSU LED True Table			
Power OK	LED Green	LED Red	Note
x	Off	Off	LED off, PSU is not plugged in
High	On	Off	LED Green on, PSU works fine
Low	Off	On	LED Red on, PSU Fault

5.2. Management Port LED

The I210/I350 implements three output drivers intended for driving external LED circuits. Each of the three LED outputs can be individually configured to select the particular event, state, or activity, which is indicated on that output. In addition, each LED can be individually configured for output polarity as well as for blinking versus a non-blinking (steady-state) indication.

MGMT port(I210)	Description
Link LED	OFF – No link is established on the port. Solid Green – Link at 1000Mbps Solid Yellow – Link at 10/100Mbps
Activity LED	OFF – No link is established on the port. Blinking Green – Activity, transmitting or receiving packet

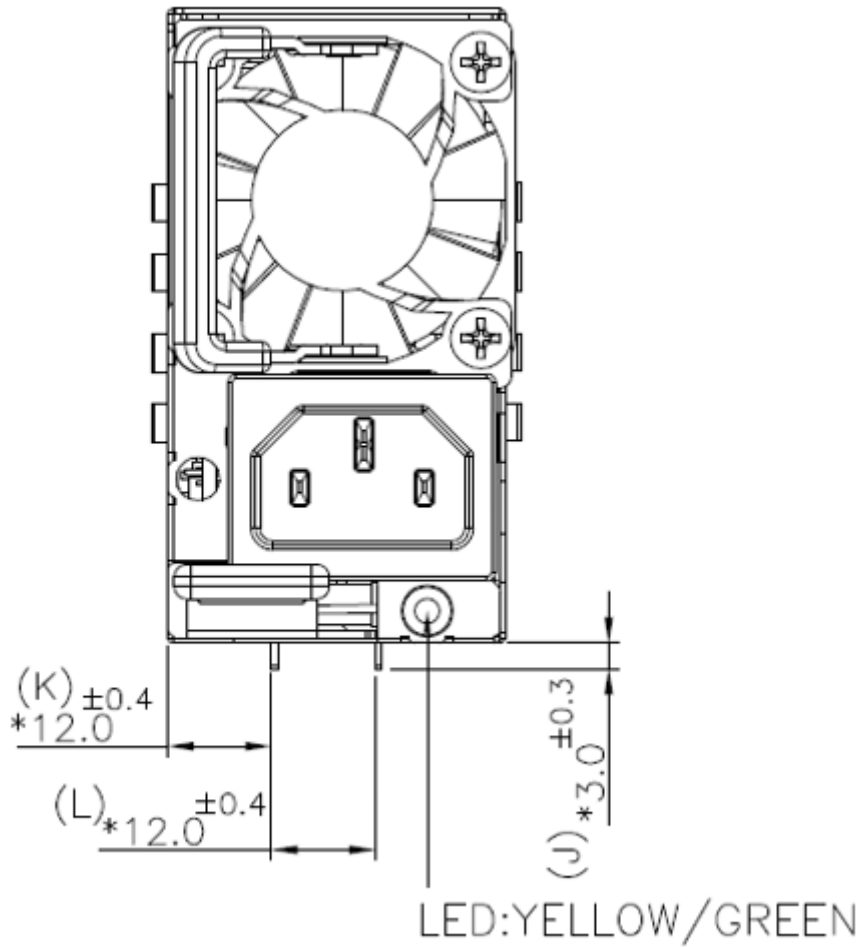
CTRL1/2 port(I350)	Description
Link LED	OFF – No link is established on the port. Solid Green – Link at 1000Mbps
Activity LED	OFF – No link is established on the port. Blinking Green – Activity, transmitting or receiving packet



5.3. PSU LED

The power supply uses one bi-color LED which are Amber and Green to illustrate status as below

LED	Statement	Description
Green	Solid on	Operating normally ; PSU output is good
	Blinking	AC power present /Only +12VSB on (12V Off) or PSU in smart on state
	Off	AC power lost: All power supplies
Amber	Solid on	1. AC power lost: The others PSU in parallel AC power are on 2. PSU critical event occurred cause main power shunt-down: OCP/OCP/FAN Failed
	Blinking (1Hz)	PSU warning: Where the PSU continue operating at high temp/high power, etc.
	Blinking (2Hz)	Power supply FW upgrading



5.4. FAN LED

The fan tray uses one bi-color LED which is green and red to illustrate status as below

	Description
FAN Status LED	Solid Green – Normal operation Solid Yellow–Fan fault

5.5. SFP28/QSFP28 Port LED

Each port supports RGB-color LED to indicate port and lanes status as following table.

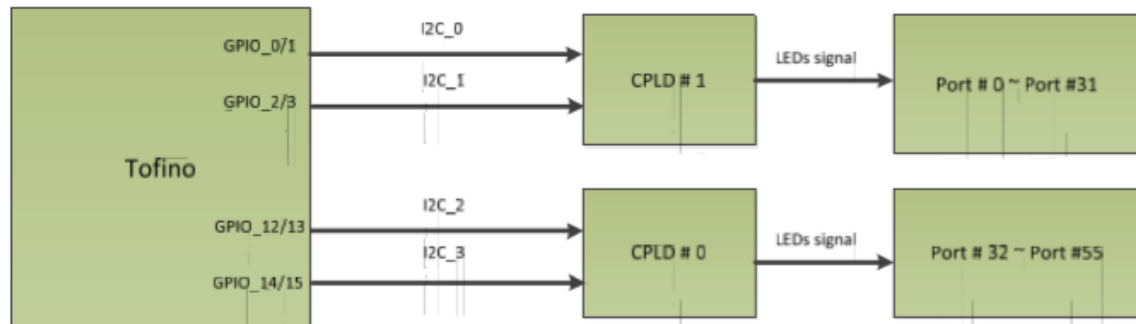
	Description	
LED	100G	Solid Green – Linked at 100G
		Blinking Green – Activity at 100G
	50G	Solid White – Linked at 50G
		Blinking White – Activity at 50G
	40G	Solid Amber – Linked at 40G
		Blinking Amber – Activity at 40G
	25G	Solid Blue – Linked at 25G
		Blinking Blue – Activity at 25G
	10G	Solid Purple – Linked at 10G
		Blinking Purple – Activity at 10G
	1G	Solid Purple – Linked at 1G
		Blinking Purple – Activity at 1G

Following format and table shows the LED mapping of bit stream. Each port has 5-bit stream as defined on below table. Software should configure the MAC internal LED controller to generate serial stream to light port LED through CPLDs.

LED status			LED				LED PWM(CPLD control)		
			R	G	B	Color	R	G	B
0	0	OFF	0	0	0	OFF	0	0	0
0	1	ON	0	0	1	Blue	0	0	255
1	0	Fast blinking	0	1	0	Green	0	255	0
1	1	Slow blinking	0	1	1	Cyan	0	255	255
			1	0	0	Red	255	0	0
			1	0	1	Purple	255	0	255
			1	1	0	Amber	255	191	0
			1	1	1	White	255	255	255

Port LED lighting implementation

Below diagram shows how port LED to be implemented by system.



Tofino use GPIO as I2C master to write LED data to CPLD.

6. CLPD

There is one System CPLD and two Port CPLDs in system, which are Lattice LCMX03-2100 for system CPLD and LCMX03-4300 for port CPLD. □ The system CPLD function which includes reset, interrupt, and system LED. □ The port CPLD function which includes module information (interrupt, present, control signals), port LEDs.

6.1. Registers Mapping Table

The mapping table of SYSCPLD and Port CPLD used in system as attached file.



SYS CPLD SPEC.pdf



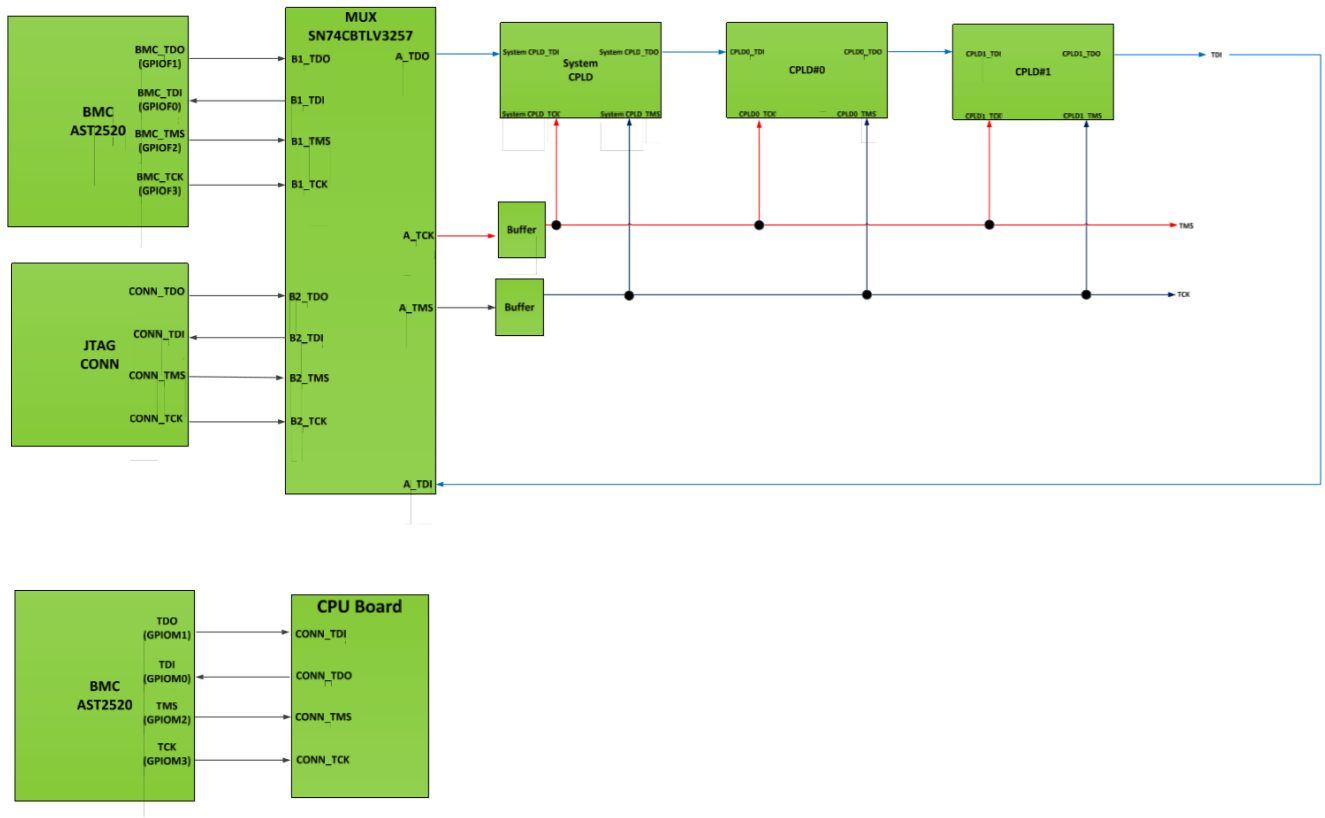
Port LED CPLD0.pdf



Port LED CPLD1.pdf

6.2. CPLD Upgrading

SYSCPLD, Port CPLD and CPU CPLD can be online upgraded by BMC. Use the following GPIO to emulate CPLD JTAG signals to upgrade CPLD.



7. Power Consumption and Monitor

Power consumption table as below:

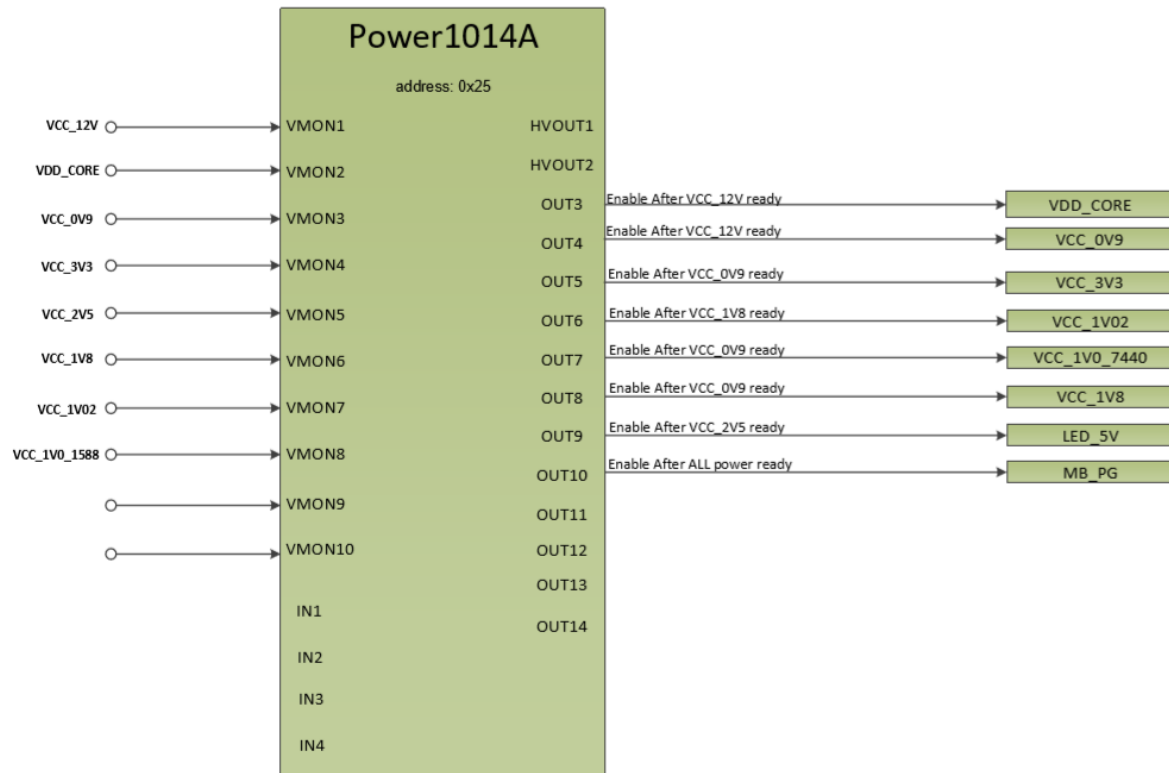
Power monitor use Lattice POWR1014A and BMC can use I2C (addr:0x25) to read voltage status.

Power Domain	Channel	Power Rail	Voltage	Criteria
Main Power	VMON1	VCC_12V	4.86V(12V derived by resistor)	+/-5%
	VMON2	VDD_CORE	0.85V(default)	Refer to MAC VID
	VMON3	VCC_0V9	0.9V	+/-3%
	VMON4	VCC_3V3	3.3V	+/-5%
	VMON5	VCC_2V5	2.5V	+/-5%
	VMON6	VCC_1V8	1.8V	+/-5%
	VMON7	VCC_1V02	1.02V	+/-2%
	VMON8	VCC_1V0_1588	1.0V	+/-5%
	VMON9	VCC_1V5	1.5V	+/-5%
	VMON10	Reserved		

MAC VID and limitation are shown as below table. BMC need to read MAC VID during system boot up and send voltage change to DC/DC (address: 0x60).

VID[2:0]	Min voltage(mV)	Normal voltage(mV)	Max voltage(mV)
000	820	850	875
001	790	820	845
010	740	770	795
011	840	870	895
100	715	745	775
101	815	845	870

Power Consumption Estimation Table																
Voltage(V)	12V	5V	3.3V	2.5V	1.8V	1.5V	1.2V	1.15V	1.0V	1.02V	0.9V	VDD_CORE	Unit Power	Quantity	Unility(%)	Total(W)
Device	12	5	3.3	2.5	1.8	1.5	1.2	1.15	1	1.02	0.9	0.85				
CPU board	8334												100.008	1		100.008
Tofino 2.0T				120							34550	129760	141.691	1		157.4344
98PX1024			120		140					6470			7.2474	8		64.42133
AST2520			39				385	510					1.1772	1		1.308
DDR4				20			133						0.2096	1		0.232889
I210			190										0.627	2		1.393333
I350			848										2.7984	1		3.109333
CPLD			600										1.98	3		6.6
LEDs			20										0.066	85		6.233333
MISC			3300										10.89	1		12.1
USB		1000											5	1		5.555556
FAN	2800												33.6	4		134.4
GBIC_25G			455										1.5015	48		80.08
GBIC_100G			1515										4.9995	8		44.44
Total by DC rails		1	42.987	0.14	1.12	0	0.518	0.51	0	51.76	34.55	129.76				
Voltage Toleration(%)		5%	5%	5%	5%	3%	5%	5%	5%	2%	3%	2%				617.3162



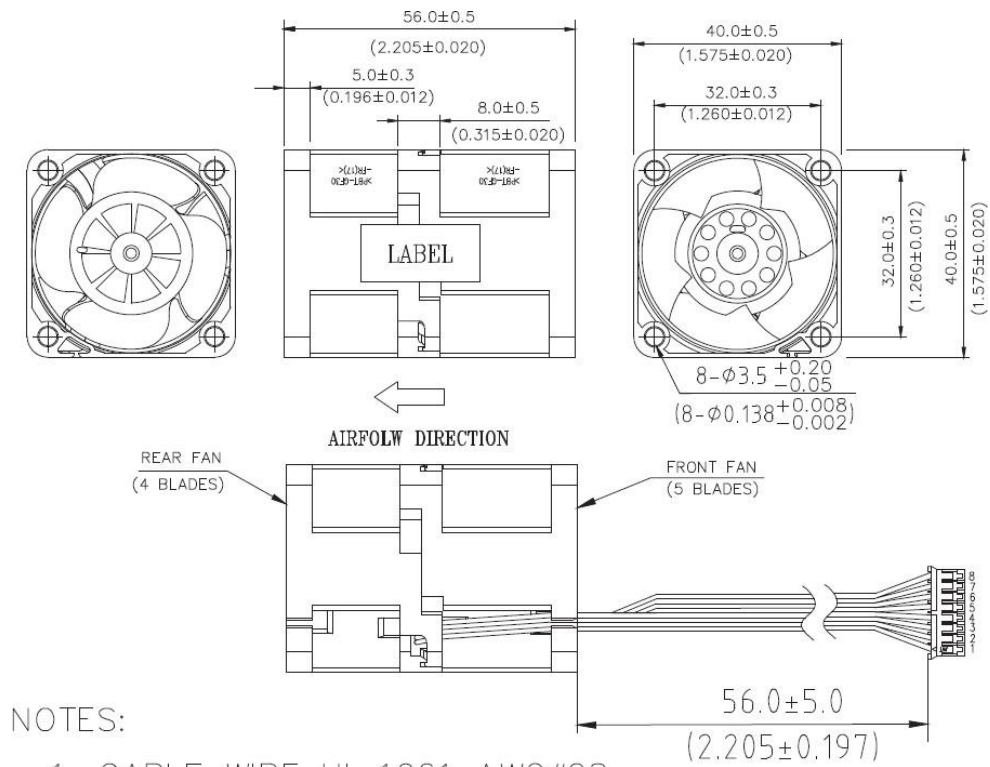
Power monitor address: 0x25

8. System Cooling

This model support 3+1 redundancy FAN module and support front to back/back to front air direction.

8.1. FAN module

FAN dimension as below:



SPEED VS PWM CONTROL SIGNAL: (AT RATED 12V & PWM FREQUENCY=25KHZ)

DUTY CYCLE (%)	SPEED R.P.M. (REF.)		CURRENT (A) TYP. TOTAL
	FRONT	REAR	
100	23000±8%	20500±8%	2.27
10	1500±500	1500±500	0.06
0	0	0	0.04

9. PSU Sub-System

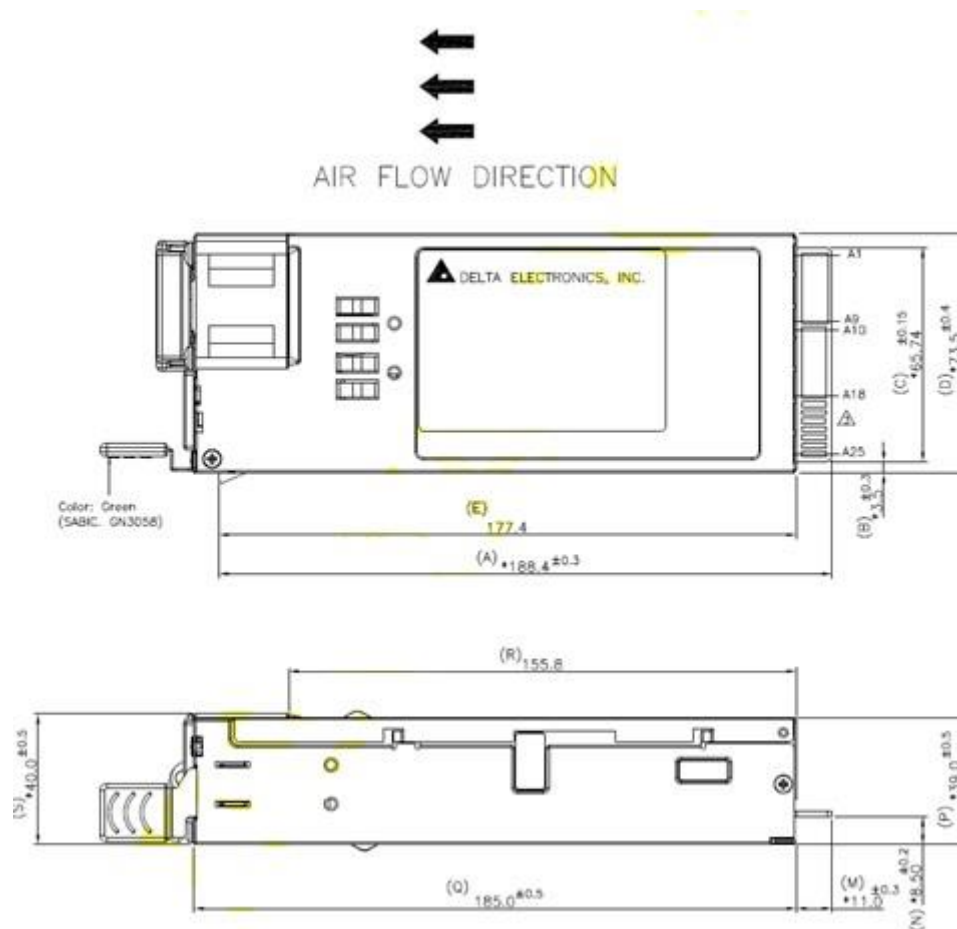
This model will support 1+1 redundancy power supply. Each PSU can provide 850W power to the system.

9.1. Feature

The model will support the following PSU solution:

- ☐ AC Input: DPS-850AB-4 Q
- ☐ DC Input: DPS-800AB

9.2. Dimension



9.3. Output Connector

9.3.1. Power supply connector

The power supply uses a card edge output for power and signals.

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	SDA	B19	A0
A20	SCL	B20	A1
A21	PSON#	B21	+12VSB
A22	SMBAAlert#	B22	Smart_On
A23	RS-	B23	+12VLS
A24	RS+	B24	N/C
A25	PWOK	B25	N/C

Note: B24 and B25 are optional signals for Present_N# and PS_KILL respectively.

9.3.2. CPU to Main board connector

	Pin			Pin	
JTAG	2	GND	GND	1	PCIe*8
	4	TMS	PCIe_TX_0P	3	
	6	TDI	PCIe_TX_0N	5	
	8	GND	GND	7	
	10	TDO	PCIe_TX_1P	9	
	12	TCK	PCIe_TX_1N	11	
UART*1	14	GND	GND	13	
	16	UART_RXD	PCIe_TX_2P	15	
	18	UART_TXD	PCIe_TX_2N	17	
LPC/eSPI	20	GND	GND	19	
	22	LPC_LAD[3]	PCIe_TX_3P	21	
	24	LPC_LAD[2]	PCIe_TX_3N	23	
	26	GND	GND	25	
	28	LPC_LAD[1]	PCIe_TX_4P	27	

	30	LPC_LAD[0]	PCle_TX_4N	29	
	32	GND	GND	31	
	34	LPC_CLK (eSPI_CLK)	PCle_TX_5P	33	
	36	LPC_SERIRQ# (eSPI_Alert#)	PCle_TX_5N	35	
	38	GND	GND	37	
	40	LPC_FRAME# (eSPI_CS#)	PCle_TX_6P	39	
	42	Reserved (eSPI_Reset#)	PCle_TX_6N	41	
PCle*1	44	GND	GND	43	
	46	PCle_RX_8P(Gen1 only)	PCle_TX_7P	45	
	48	PCle_RX_8N(Gen1 only)	PCle_TX_7N	47	
	50	GND	GND	49	
	52	PCle_TX_8P(Gen1 only)	PCle_RX_0P	51	
	54	PCle_TX_8N(Gen1 only)	PCle_RX_0N	53	
UART1	56	GND	GND	55	
	58	UART_TXD1	PCle_RX_1P	57	
	60	UART_RXD1	PCle_RX_1N	59	
System	62	GND	GND	61	
	64	CPU_SHUTDOWN#	PCle_RX_2P	63	
1588	66	1PPS_IN	PCle_RX_2N	65	
I2C*3	68	GND	GND	67	
	70	I2C_SDA_0(reserved)	PCle_RX_3P	69	
	72	I2C_SCK_0(reserved)	PCle_RX_3N	71	
	74	GND	GND	73	
	76	I2C_SDA_1	PCle_RX_4P	75	
	78	I2C_SCK_1	PCle_RX_4N	77	
	80	GND	GND	79	
	82	I2C_SDA_2(from MB)	PCle_RX_5P	81	
	84	I2C_SCK_2(from MB)	PCle_RX_5N	83	
System	86	GND	GND	85	
	88	IPMI_Alert#	PCle_RX_6P	87	
	90	PECL_Power(1.05V)	PCle_RX_6N	89	
	92	PECL	GND	91	
	94	MB_PG	PCle_RX_7P	93	
	96	CPU_ALERT#	PCle_RX_7N	95	
	98	MB_INT#	GND	97	
	100	CPU_POWER_RST#	PCle_CLK_P	99	
					PCle_CLK

	102	MB_RST#	PCIe_CLK_N	101	
USB 3.0	104	GND	GND	103	KR*4
	106	USB_EN	10G_KR_TX_3P	105	
	108	USB_OC#	10G_KR_TX_3N	107	
	110	GND	GND	109	
	112	USB_SSRX_P	10G_KR_TX_2P	111	
	114	USB_SSRX_N	10G_KR_TX_2N	113	
	116	GND	GND	115	
	118	USB_SSTX_P	10G_KR_TX_0P	117	
	120	USB_SSTX_N	10G_KR_TX_0N	119	
	122	GND	GND	121	
	124	USB_D_P	10G_KR_TX_1P	123	
	126	USB_D_N	10G_KR_TX_1N	125	
System	128	GND	GND	127	
	130	RTC_RESET#	10G_KR_RX_3P	129	
3V3_STBY	132	P3V3_STBY	10G_KR_RX_3N	131	
12V_PWR	134	GND	GND	133	
	136	12V	10G_KR_RX_2P	135	
	138	12V	10G_KR_RX_2N	137	
	140	12V	GND	139	
	142	12V	10G_KR_RX_0P	141	
	144	12V	10G_KR_RX_0N	143	
	146	12V	GND	145	
	148	12V	10G_KR_RX_1P	147	
	150	12V	10G_KR_RX_1N	149	

9.3.3. Main to daughter board connector

Pin			Pin
2	BMC_FAN_SDA	NIC_I2C_SDA	1
4	BMC_FAN_SCL	NIC_I2C_SCL	3
6	GND	GND	5
8	PCIE_I350_CLK_P	PCIE_I210_CLK_P	7
10	PCIE_I350_CLK_N	PCIE_I210_CLK_N	9
12	GND	GND	11
14	I350_PE_TX_P	I210_PE_TX_P	13
16	I350_PE_TX_N	I210_PE_TX_N	15



18	GND	GND	17
20	CPU_I350_PCIE_RXP	CPU_I210_PCIE_RXP	19

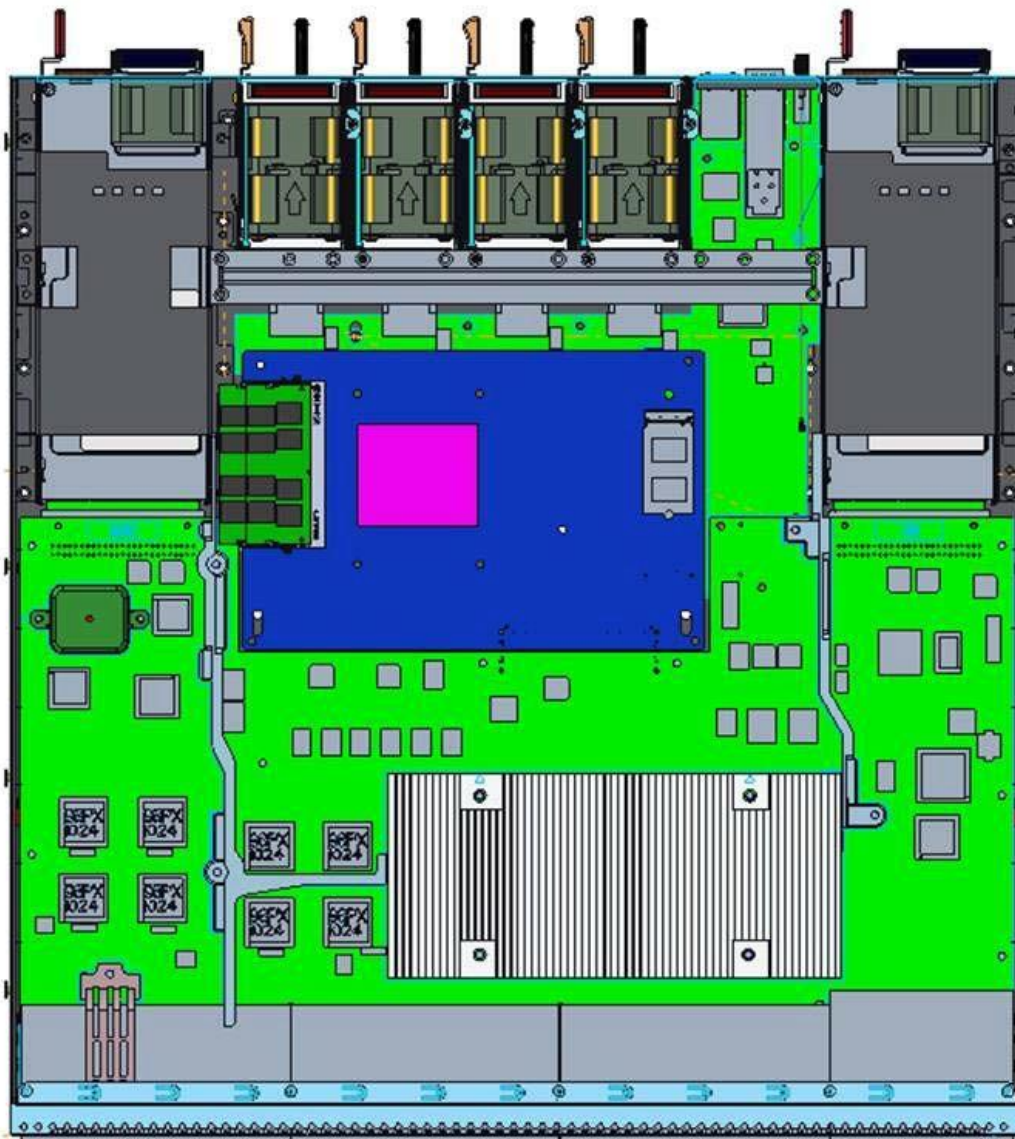
22	CPU_I350_PCIE_RXN	CPU_I210_PCIE_RXN	21
24	GND	GND	23
26	BMC_TXD0	BMC_RXD0	25
28	BMC_TXD1	BMC_RXD1	27
30	GND	GND	29
32	REAR_USB_SSRXP	NCSI_REF_CLK	31
34	REAR_USB_SSRXN	GND	33
36	GND	NCSI_TX_EN	35
38	REAR_USB_SSTXP	NCSI_CR5_DV	37
40	REAR_USB_SSTXN	HUB1_RESET_L	39
42	GND	NIC_ALRT_L	41
44	REAR_USB_DP	NIC_RST_N	43
46	REAR_USB_DM	I210_DEV_OFF_N	45
48	GND	I350_DEV_OFF_N	47
50	FAN_TACH0	HW_BOTTOM_RST_L	49
52	FAN_TACH0_1	FAN_I2C_RST	51
54	FAN_TACH1	FAN_INTn	53
56	FAN_TACH1_1	FAN0_LED	55
58	FAN_TACH2	FAN1_LED	57
60	FAN_TACH2_1	FAN2_LED	59
62	FAN_TACH3	FAN3_LED	61
64	FAN_TACH3_1	VCC_12V	63
66	FAN_PWM0	VCC_12V	65
68	FAN_PWM1	VCC_12V	67
70	FAN_PWM2	VCC_12V	69
72	FAN_PWM3	VCC_12V	71
74	RS232_TXD	VCC_12V	73
76	RS232_RXD	VCC_12V	75
78	GND	12V_STB	77
80	1PPS	12V_STB	79

10. Mechanical

10.1. Dimension

W x D x H: 438.5 x 460 x 43.5 mm, 1RU design

10.2. Feature



11. Environment and Regulatory

- Operation Temperature: 0 ~ 40°C
- Storage Temperature: -20 ~ 70°C
- Operation Humidity: 10 ~ 90%RH
- Storage Humidity: 5 ~ 95%RH
- Altitude: 6000ft

□ Safety:

- EN60950-1
- UL/CSA 60950-1
- IEC 60950-1

□ Emissions:

- AS/NZS CISPR 22: Class A, ICES-003, Issue Class A
- EN 55022: Class A, VCCI Class A,
- FCC CFR 47 Part 15, Subpart B Class A

□ Immunity:

- □ EN 300 386
- □ EN 55024
- □ EN 61000-3-2
- □ EN 61000-3-3
- □ EN 61000-4-2
- □ EN 61000-4-3
- □ EN 61000-4-5
- □ EN 61000-4-6
- □ EN 61000-4-8
- □ EN 61000-4-11

□ EU RoHS Compliant